XS1-L2 124QFN Datasheet

Version 1.5

XMOS

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1 Description

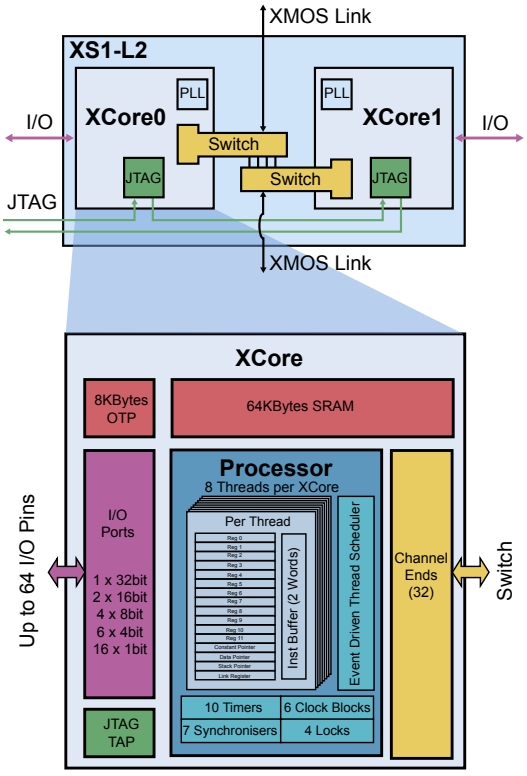
The XS1-L2 is a member of the XS1-L family of XMOS devices. The XS1-L family blends a powerful programmable fabric based on multi-threaded processors with a high-level programming language design flow. XMOS chips are general-purpose programmable devices that can be used in a wide range of applications and systems.

The XS1-L2 device is based on the XMOS XCore™. Each XCore contains a 32-bit processor, SRAM memory, I/O ports for communicating with external components and channels for communicating with other devices.

OTP memory is provided for application boot code and security keys, with a secure mode that disables debug and prevents read-back of memory contents.

High performance switches supports low latency and deterministic communication between the threads in different XCores.

The XMOS architecture is unique in its direct support for concurrent processing (multi-threading), event handling, communication and timed I/O operations.



XS1-L2 Package Features

Two XCores providing up to 1000MIPS and 16 concurrent, deterministic real-time tasks
84 user I/O pins, dynamically configurable as input, output or bi-directional

XCore Resources (per core)

Threads	8
Channel Ends	32
Timers	10
Clock Blocks	6 (includes the reference clock)
XMOS Links	2 (5bit or 2bit)
Thread Synchronisers	7
Hardware Locks	4
SRAM	64KBytes
OTP Memory	8KBytes

2 Signal Descriptions

This section describes the external signal pins of the XS1-L2 in the 124 QFN package.

The following I/O type conventions are used in this document:

I/O Type convention	
I	Input
O	Permanent Output
IO	Bidirectional
OT	Tristatable Output
PU	Pull Up
PD	Pull Down
ST	Schmitt Trigger

2.1 XCore Signals

The XS1-L2 124QFN device provides 84 XCore signals that can be used for generic I/O ports or XMOS Links.

2.1.1 XCore signals as I/O ports

The following table shows the IO ports available on each XCore processor. See Section 2.2 Port Pin Table for further information on the availability of I/O ports in the 124QFN package.

Port Width	**1-bit**	**4-bit**	**8-bit**	**16-bit**
Number of ports	16 [A:P]	6 [A:F]	4 [A:D]	2 [A:B]

Note that the top 4 bits of P8D and P16B are not available on Core 1.

2.1.2 XCore signals as XMOS Links

XMOS Links are bidirectional and may operate in either 5bit/direction or 2bit/direction mode. See Section 2.2 Port Pin Table for further information.

XMOS Links per Core	**Total XMOS Links per L2 Device**
2 [A:B]	4

2.1.3 Precedence

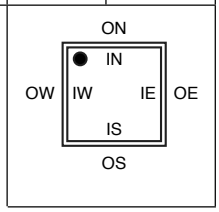
Ports and XMOS Links are connected to pins on the XS1-L2 by the program running on the device. The ports and links are multiplexed and follow a defined precedence if they overlap on the same core:

- If an XMOS Link is enabled, the link has access to the pins; the pins of the underlying ports are disabled.
- If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled.

Ports always operate at their specified width, even if they share pins with another port.

2.2 Port Pin Table

Signal	Pin ID		XMOS LINKS		PORTS				Note	RING	
	Core 0	Core 1	5bit	2bit	1b	4b	8b	16b		Core 0	Core 1
X*n*D0	A15	A39			P1A0				1	OW	OE
X*n*D1	A16	A40	XLA4out		P1B0				1	OW	OE
X*n*D2	A5	A41	XLA3out			P4A0	P8A0	P16A0	2	OW	OE
X*n*D3	A6	A42	XLA2out			P4A1	P8A1	P16A1	2	OW	OE
X*n*D4	A7	A43	XLA1out	XLA1out		P4B0	P8A2	P16A2	2	OW	OE
X*n*D5	A8	A44	XLA0out	XLA0out		P4B1	P8A3	P16A3	2	OW	OE
X*n*D6	A9	A45	XLA0in	XLA0in		P4B2	P8A4	P16A4	2	OW	OE
X*n*D7	A10	A46	XLA1in	XLA1in		P4B3	P8A5	P16A5	2	OW	OE
X*n*D8	A11	A47	XLA2in			P4A2	P8A6	P16A6	2	OW	OE
X*n*D9	A12	A48	XLA3in			P4A3	P8A7	P16A7	2	OW	OE
X*n*D10	A13	A49	XLA4in		P1C0				1	OW	OE
X*n*D11	A14	A50			P1D0				1	OW	OE
X*n*D12	A55	A21			P1E0				2	ON	OS
X*n*D13	A57	A23	XLB4out		P1F0				2	ON	OS
X*n*D14	A58	A24	XLB3out			P4C0	P8B0	P16A8	2	ON	OS
X*n*D15	A59	A25	XLB2out			P4C1	P8B1	P16A9	2	ON	OS
X*n*D16	A60	A26	XLB1out	XLB1out		P4D0	P8B2	P16A10	2	ON	OS
X*n*D17	A61	A27	XLB0out	XLB0out		P4D1	P8B3	P16A11	2	ON	OS
X*n*D18	A63	A29	XLB0in	XLB0in		P4D2	P8B4	P16A12	2	ON	OS
X*n*D19	A64	A30	XLB1in	XLB1in		P4D3	P8B5	P16A13	2	ON	OS
X*n*D20	A65	A31	XLB2in			P4C2	P8B6	P16A14	2	ON	OS
X*n*D21	A66	A32	XLB3in			P4C3	P8B7	P16A15	2	ON	OS
X*n*D22	A56	A22	XLB4in		P1G0				2	ON	OS
X*n*D23	A62	A28			P1H0				2	ON	OS
X*n*D24	A54	A20			P1I0					ON	OS
X*n*D25	A67	A33			P1J0					ON	OS
X*n*D26	B38	B16				P4E0	P8C0	P16B0	2	IE	IS
X*n*D27	B39	B17				P4E1	P8C1	P16B1	2	IE	IS
X*n*D28	B40	B18				P4F0	P8C2	P16B2	2	IE	IS
X*n*D29	B41	B19				P4F1	P8C3	P16B3	2	IE	IS
X*n*D30	B44	B20				P4F2	P8C4	P16B4	2	IN	IS
X*n*D31	B45	B21				P4F3	P8C5	P16B5	2	IN	IS
X*n*D32	B46	B22				P4E2	P8C6	P16B6	2	IN	IS
X*n*D33	B47	B23				P4E3	P8C7	P16B7	2	IN	IS
X*n*D34	A4	B24			P1K0					OW	IS
X*n*D35	A3	B25			P1L0					OW	IS
X*n*D36	B48	B26			P1M0		P8D0	P16B8		IN	IS
X*n*D37	B49	B27			P1N0		P8D1	P16B9	2	IN	IS
X*n*D38	B50	B30			P1O0		P8D2	P16B10	2	IN	IE
X*n*D39	B51	B31			P1P0		P8D3	P16B11	2	IN	IE
X*n*D40	B52	N/A					P8D4	P16B12	2	IN	N/A
X*n*D41	B53						P8D5	P16B13	2	IN	
X*n*D42	B54						P8D6	P16B14	2	IN	
X*n*D43	B55						P8D7	P16B15	2	IN	



[1] SPI signals must be attached to specific pins—see Section 3.3
[2] ULPI signals must be attached to specific pins. In addition some ports are not available when ULPI is enabled—see Section 8.1

2.3 System Service Pin Table

Pin ID	Signal
B7	CLK
B37	DEBUG
B33	MODE0
B34	MODE1
B35	MODE2
B36	MODE3
A35	MODE4
B32	OTP_VDDIO

Pin ID	Signal
A37	PLL_AGND
A38	PLL_AVDD
B8	RST_N
B10	TCK
B12	TDI
B9	TDO
B11	TMS
B13	TRST_N

2.4 Core Power and Ground Pin Table

Pin ID	Signal
A19	VDD
A34	VDD
A53	VDD
A68	VDD
B15	VDD
B28	VDD
B43	VDD
B56	VDD

Pin ID	Signal
PADDLE	GND
A1	GND
A18	GND
A52	GND

2.5 XCore I/O Power Table

Pin ID	Signal
A2	VDDIO
A17	VDDIO
A36	VDDIO
A51	VDDIO

Pin ID	Signal
B1	VDDIO
B14	VDDIO
B29	VDDIO
B42	VDDIO

2.6 PCU Signals Table

Pin ID	Signal
B5	PCU_VDD
B4	PCU_VDDIO
B6	PCU_CLK

Pin ID	Signal
B2	PCU_WAKE
B3	PCU_GATE

2.7 XMOS Link Pin Table

See Section 2.2 Port Pin Table

3 System Services

System Services are required to support correct device behavior. These signals control clocking, reset and boot behavior of the device.

3.1 Clock control signals

These signals control the PLL of the XS1-L2

Signal	Pin ID	I/O	Description
PLL_AVDD	A38	pwr	Analog power supply for the PLL
PLL_AGND	A37	pwr	Analog ground for the PLL
CLK	B7	I, PD, ST	Reference clock input for the PLL

Functional description

PLL_AVDD The on-chip PLL requires a very clean AVDD power supply. It is recommended that this supply node be separated from the other, noisier, supplies on the board. The supply should be decoupled close to the respective IC package pin. Nominally 1.0V.

PLL_AGND Analog ground for the PLL. Connect directly to board ground.

CLK Reference clock signal for the on-chip PLL. This signal is used as a reference by the PLL in generating all on chip clocks.

3.2 Miscellaneous control signals

Signal	Pin ID	I/O	Description
MODE[3:0]	B36, B35, B34, B33	I, PU, ST	Sets boot mode
MODE[4]	A35	I, PU, ST	Controls slave core boot from SPI
DEBUG	B37	IO, PU	Multi-device debug
RST_N	B8	I, PU, ST	Asynchronous system reset

Functional description

MODE[4:0] These pins determine the boot source and PLL boot mode of the master and slave devices. Bits [4:2] control the boot source according to the following table:

MODE4	MODE3	MODE2	Boot Mode
X	0	0	None - Both cores wait to be booted (via JTAG)
X	0	1	Reserved
0	1	0	Master core boots from XMOS Link B, slave core boots from internal link via master core
0	1	1	Master core boots from SPI, slave core boots from internal link via master core
1	1	0	Reserved
1	1	1	Both cores boot from SPI independantly

Bits [1:0] control the PLL boot mode according to the following table:

MODE1	MODE0	PLL Multiplier Ratio	PLL reference clk	Boot Frequency
0	0	30.75	4.22 to 13 MHz	130 to 399.75 MHz
0	1	4	21.66 to 100 MHz	86.66 to 400 MHz
1	0	8.3333	10.4 to 48 MHz	86.66 to 400 MHz
1	1	20	4.33 to 20 MHz	86.66 to 400 MHz

NOTE: If secure boot from OTP is enabled by programming the OTP, the boot mode indicated on the MODE[4:2] pins is ignored. For further details on booting XCores see the XS1-L System Specification.

MODE[4] Tie low for normal use. If this pin is asserted high, the second core may be booted from an SPI flash device.

DEBUG This pin is used to synchronize the debugging of multiple XS1 devices. This pin can operate in both output and input mode. In output mode and when configured to do so, DEBUG is driven low by the device when one or more internal XCore processors hit a debug break point. Prior to this point the pin will be tri-stated. In input mode and when configured to do so, driving this pin low will put all internal CPUs into debug mode. Software can set the behavior of each internal XCore based on this pin. This pin should have an external pull up of 4K7 ohms.

RST_N Active low asynchronous-assertion reset signal. This pin must be driven low for at least 100ns to reset the entire device. Following a reset the PLL re-establishes lock after which the XCores boot up according to the boot mode (see MODE).

3.3 SPI Interface

To boot the master core on the XS1-L2 device from an SPI interface, the SPI device must be connected as follows:

Signal	Pin ID	Pin I/O	Function	Description
X0D0	A15	I	MISO	Data - Master In Slave Out
X0D1	A16	O	SS	Slave Select
X0D10	A13	O	SCLK	Clock
X0D11	A14	O	MOSI	Data - Master out Slave In

To boot the both cores independently from an SPI device, use the same pins defined above and set MODE[4]=1.

3.4 Power Control Unit

The XS1-L2 power control unit (PCU) provides control signals to isolate the core voltage of the device and reapply it under a controlled condition known as *sleep mode*. The device recovers into functional mode under the control of an external PCU_WAKE signal or an internal timer.

Signal	Pin ID	I/O	Description
PCU_VDD	B5	pwr	PCU core power supply
PCU_VDDIO	B4	pwr	PCU IO power supply
PCU_WAKE	B2	I, PD, ST	PCU wake up signal
PCU_GATE	B3	OT	PCU output to FET gate
PCU_CLK	B6	I, PD, ST	PCU clock signal

Functional description

PCU_VDD The PCU core power. Connect to the permanent 1V0 core supply.

PCU_VDDIO The PCU must operate exclusively from the PCU_VDDIO as core voltage cannot be guaranteed. In standard power mode PCU_VDDIO should be connected to the 3V3 VDDIO supply.

PCU_WAKE PCU input to asynchronously wake up the device (i.e. turn the MOSFET on). In standard power mode PCU_WAKE should be left unconnected.

PCU_GATE PCU output connected to gate of VDD_CORE switching MOSFET. During sleep state, PCU_GATE is driven low. In standard power mode PCU_GATE should be left unconnected.

PCU_CLK Clock source for PCU. If the device is used in standard power mode PCU_CLK should be tied to the main system clock input. If the device is to be used in low power mode, PCU_CLK must be tied to a low power oscillator so that the power control unit remains clocked while in sleep mode.

3.5 One Time Programmable Memory

Signal	Pin ID	I/O	Description
OTP_VDDIO	B32	pwr	OTP Power Supply

Functional description

OTP_VDDIO OTP Power Supply. Must be 3V3. This supply must be at its nominal level before the core supply is enabled.

3.6 JTAG Operation

The XS1-L2 device contains a standard 5 pin JTAG interface, which allows the following functionality:

- Boundary scan testing for verifying printed circuit board connectivity.
- In-circuit source level debugging of the XCores.
- Programming of the One Time Programmable (OTP) ROM.

The JTAG interface on the XS1-L2 consists of the following signals:

Signal	Pin ID	I/O	Description
TCK	B10	I, PU, ST	Test clock
TMS	B11	I, PU, ST	Test mode select
TRST_N	B13	I, PU, ST	Test reset (active low)
TDI	B12	I, PU, ST	Test data in
TDO	B9	OT, PD	Test data out

The TRST_N pin must be driven low for at least 100ns after the power supplies are stable to reset the JTAG circuitry. If JTAG debug is not required, the TRST_N pin can be tied low to hold the JTAG port in reset.

The XS1-L2 JTAG structure is conceptually composed of two XS1-L1 JTAG structures connected together. The XS1-L2 device can therefore be looked at externally as two L1 devices connected in a chain as shown in the JTAG chain structure diagram.

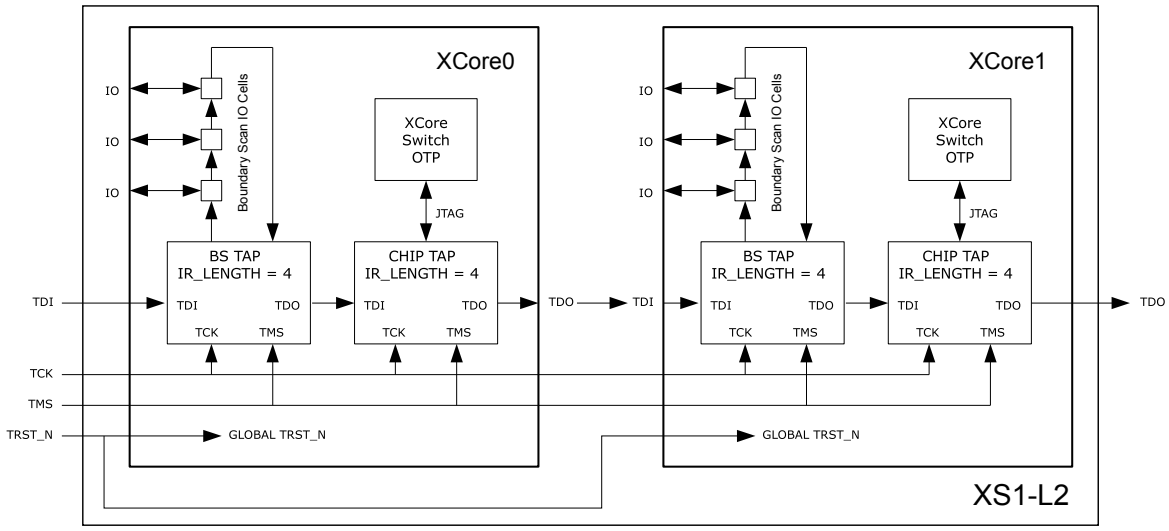
Each XS1-L1 structure contains multiple TAP controllers, each enabling different functionality. For the XS1-L1, directly after reset, two TAP controllers are present in the JTAG chain - the boundary scan TAP (BS TAP) and the chip TAP (CHIP TAP). This means for the L2 there will be four TAP controllers present in total.

The boundary scan TAP is a standard 1149.1 compliant TAP and can be used for boundary scan of the I/O pins of the device. The chip TAP allows access into the

XCore, Switch and OTP for such actions as loading code and debugging. Both TAPs have an instruction register length of 4. From reset, the chip TAP is in BYPASS so simply presents an extra 1-bit into the scan chain when shifting data.

If access to the XCore/Switch/OTP is required, the ChipTAP sets internal multiplexers which optionally add in additional TAPs into the JTAG chain for each of the Switch, XCore and OTP. The XCore TAP allows register read/write commands to be made for program loading/debug.

A diagram of the JTAG chain structure is shown below:



3.6.1 Device identification register

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified as follows:

Bit31																												Bit0
Version				Part Number														Manufacturer Identity										1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	1
0				0				0				0				2		6				3				3			

3.6.2 Usercode register

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified as follows:

Bit31																												Bit0
OTP User ID										Unused				Silicon Revision														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0				0				0				2				8		0				0				0			

The OTP User ID is read from the OTP and can be programmed as a means of identifying versions of OTP programmed devices. Unprogrammed devices have these bits set to zero.

4 DC and Switching Characteristics

4.1 Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD(IO)	I/O DC supply voltage	3	3.3	3.6	V	
VDD(CORE)	Core DC supply voltage	0.95	1.0	1.05	V	
AVDD(PLL)	PLL analogue supply	0.95	1.0	1.05	V	
Cl	XCore I/O load capacitance			25	pF	
Ta	Operating temperature range (Commercial)	0		70	°C	
	Operating temperature range (Industrial)	-40		85	°C	
Tj	Junction temperature			125	° C	
Tstg	Storage temperature	-65		150	° C	

4.2 DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2		3.6	V	1,6
V(IL)	Input low voltage	-0.3		0.7	V	1,6
V(OH)	Output high voltage	2.7			V	2,3,6
V(OL)	Output low voltage			0.6	V	2,4,6
R(PU)	Pull-up resistance		35k		Ohms	5,6
R(PD)	Pull-down resistance		35k		Ohms	5,6

Notes:

1. All pins except power supply pins.
2. P1A, P1D, P1E, P1H, P1I, P1J, P1K and P1L are nominal 8mA drivers, the remainder of the general purpose I/O are 4mA.
3. Measured with 4mA drivers sourcing 4mA, 8mA drivers sourcing 8mA.
4. Measured with 4mA drivers sinking 4mA, 8mA drivers sinking 8mA.
5. Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry.
6. Preliminary figures.

4.3 ESD Stress Voltage

ESD Model	ESD Stress Voltage	Notes
HBM	± 2.0 KV	
MM	± 200 V	

4.4 Reset Timing

XS1 devices include an internal counter which ensures the PLL has had time to lock before the rest of the device is brought out of reset. An active low pulse on RST_N clears this counter. Counting begins when RST_N is de-asserted.

Parameters	MIN	TYP	MAX	UNITS	Notes
Reset pulse width	100			ns	
Initialisation time	10		150	us	1

Notes:

1. The time taken to start booting after RST_N has gone high.

4.5 Power Supply

Power is applied to the device through the VDDIO and VDD pins. Several pins of each type are provided to minimize the effect of inductance within the package. All supply pins must be connected. Each supply should be decoupled close to the chip by several 100nF low inductance (for example, ceramic) capacitors between VDDIO and GND, and VDD and GND.

Input voltages must not exceed specification with respect to VDDIO, VDD and GND, even during power up and power down ramping. Permanent damage can occur if the operation exceeds these ranges.

4.5.1 Power Supply Sequencing

To ensure correct device operation, the VDDIO and OTP_VDDIO supplies should be present before the VDD supply. Specifically, the VDDIO and OTP_VDDIO supplies should rise to their nominal operating range with VDD held at 0V. The VDD supply should then rise to its nominal operating range with a rise time of less than 10ms.

4.5.2 Power Consumption

Core power consumption

The power consumption of the XS1-L2 is highly application dependant. The following figures should be used for budgetary purposes only:

Commercial and Industrial Qualification						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
I(DDCQ)	Quiescent VDD(core) current		28		mA	1
PD	Core Power dissipation		450		μW/MIPS	2, 3, 4

Notes:

1. Assumes typical core and I/O voltages, with no switching activity.
2. Assumes typical core and I/O voltages, with nominal activity.
3. Assumes 1MHz = 1 MIPS.
4. PD(TYP) value is the usage power consumption under typical operating conditions.

Core power consumption example

Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
IDD	Active VDD(core) current		320		mA	1

Notes:

1. Measurement conditions: VDD = 1.0V, VDDIO = 3.3V, 25°C, 400MHz, Both XCores at average resource usage.

PLL current consumption

Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
I(ADDPLL)	PLL_AVDD current			14	mA	1

Notes:

1. PLL_AVDD = 1.0V

For a more detailed analysis see Estimating Power Consumption For XS1-L Devices.

4.6 Clock

XS1-L devices use an input clock frequency, supplied by the user on the CLK pin, to drive the PLL and obtain the system clock. The nominal frequency of the clock for all XS1 family components is 20MHz but other clock frequencies can be used by reprogramming the internal PLL through use of the MODE pins or by application

software. For further details on configuring the clock see the XS1-L Clock Frequency Control Application Note.

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
	Frequency	4.22	20	100	MHz	
	Slew Rate	0.1			V/ns	
	Long Term Jitter (pk-pk)			2	%	CLK period

CLK pin clock edges must be monotonic and remain within the specified voltage and time limits. CLK should be stable before RST_N is taken high.

A set of system clock dividers are applied to the system clock frequency allowing specific clock frequencies to be derived for each XCore, the switch and the reference clock.

Speed Grade 4						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
	System Clock Frequency			400	MHz	

Speed Grade 5						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
	System Clock Frequency			500	MHz	

4.7 Memory

4.7.1 Internal static memory

The XS1-L2 has a total of 128KBytes (64KBytes per core) of fast internal static memory for high rates of data throughput. Each internal memory access consumes one core clock cycle. There is no dedicated external memory interface, although memory can be expanded through appropriate use of the ports.

4.7.2 Internal one-time programmable memory

The XS1-L2 has a total of 16KBytes of one-time programmable memory (8KBytes per core). This can be programmed using the JTAG interface or through external pins.

4.8 Port Timing

4.8.1 XCore I/O AC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOINVALID)	XCore I/O Minimum Output Data Invalid window which can be achieved using Port/ClkBlk combination	9			ns	
T(XOVALID)	XCore I/O Minimum Input Data Valid window to allow safe acquisition of data using Port/ClkBlk combination	8			ns	
T(XIFMAX)	Maximum XCore I/O toggle frequency which can be safely acquired and used as a clock source using a ClkBlk			60	MHz	

The Input Valid window parameter relates to the capability of the XS1-L family devices to capture data input to the chip with respect to an external clock source. This parameter can be calculated as the sum of the input setup time and input hold time with regard to the external clock as measured at the L2 device pins. The output invalid window specifies the time for which an output will be invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the L2 provides functionality to delay the incoming clock with respect to the incoming data.

For further details on these parameters and on interfacing to higher speed synchronous interfaces see XS1 Port I/O Timing Application Note.

4.9 Link Interface Performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blink)	2b link bandwidth			95	Mbit/s	1
B(5blink)	5b link bandwidth			244	Mbit/s	1

Notes:

1. Assumes 32 Byte packet, 7.5ns symbol time.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

4.10 JTAG Timing

All JTAG operations are synchronous to TCK apart from the global asynchronous reset TRST_N.

Parameters	MIN	TYP	MAX	UNITS	Notes
TCK frequency (debug)			18	MHz	
TCK frequency (boundary scan)			10	MHz	
T_{SETUP}	5			ns	1
T_{HOLD}	5			ns	1
$T_{CLOCK\ to\ OUT}$			15	ns	2

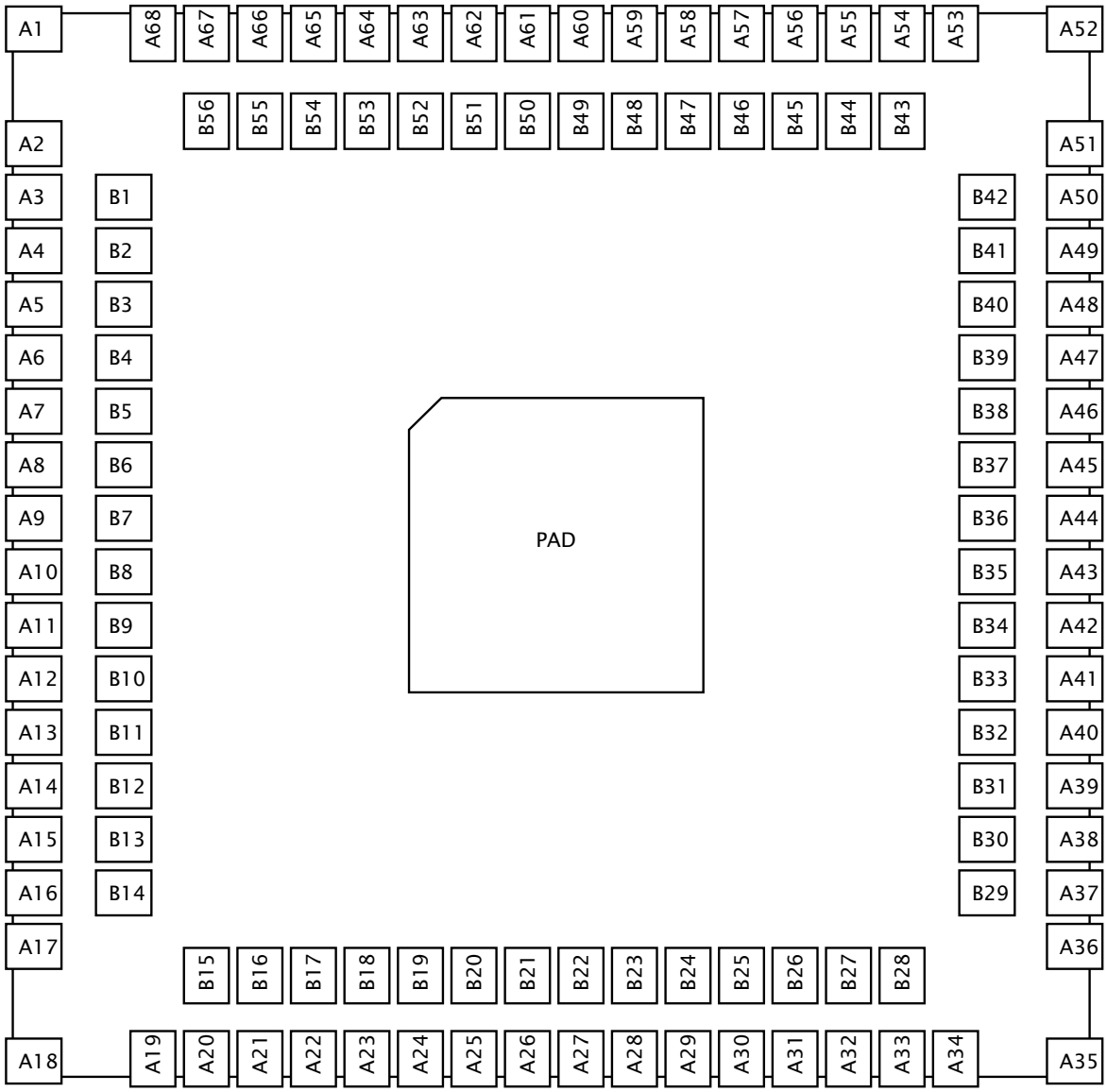
Notes:

1. Timing applies to TMS and TDI inputs
2. Timing applies to TDO output from negative edge of TCK

5 Package Details

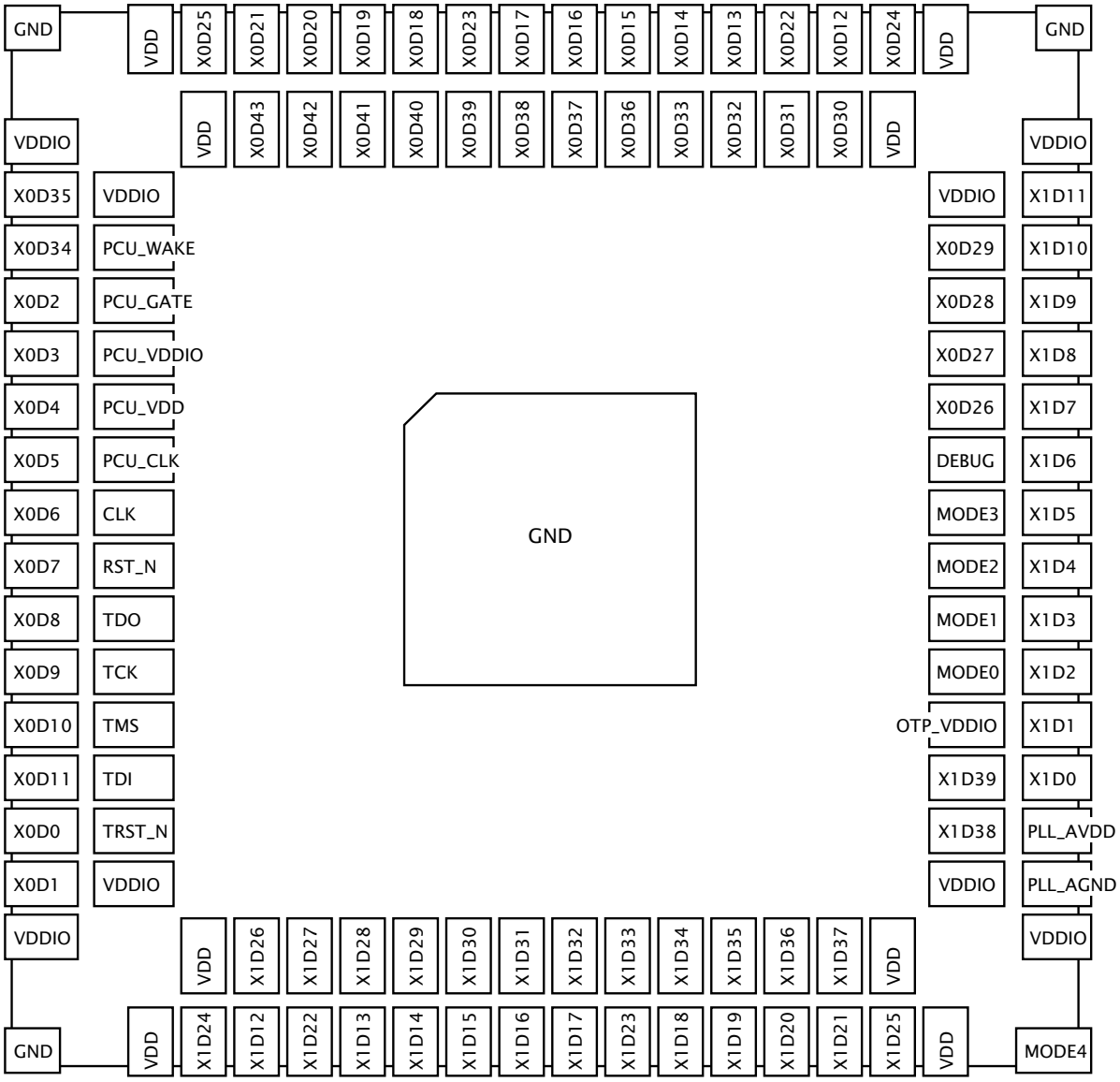
5.1 Package Pin Layout

The following diagram shows the pin name and location for the 124 QFN package (top view).

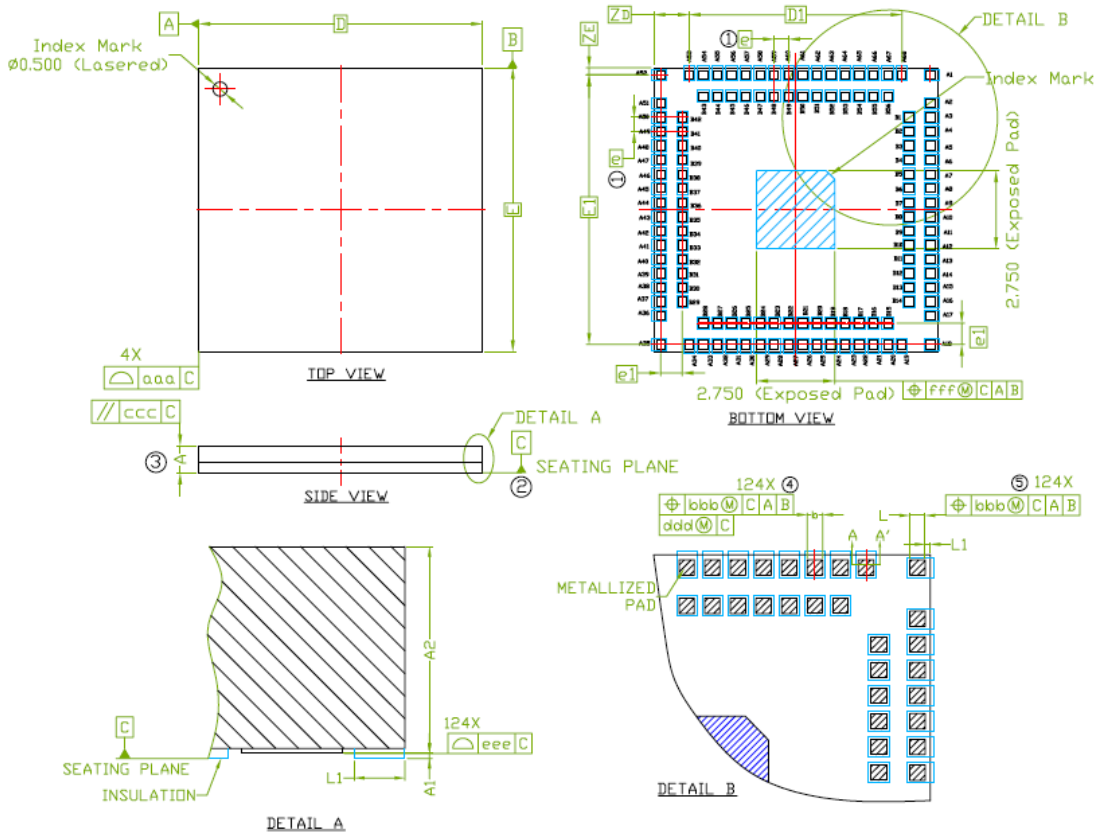


5.2 Package Signal Layout

The following diagram shows the signal name and location for the 124 QFN package (top view).



5.3 Package Mechanical Details

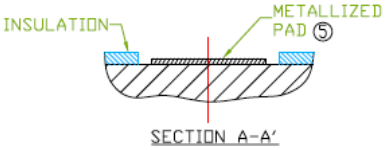


DIMENSIONAL REFERENCES

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.99	1.05	1.11
A1	–	–	0.05
A2	–	–	1.06
b	0.25	0.30	0.35
D	10.00 BSC		
E	10.00 BSC		
D1	7.50 BSC		
E1	9.50 BSC		
e	0.50 BSC		
e1	0.75 BSC		
L	0.25	0.30	0.35
L1	0.10 BSC		
ZD	1.25 BSC		
ZE	0.25 BSC		

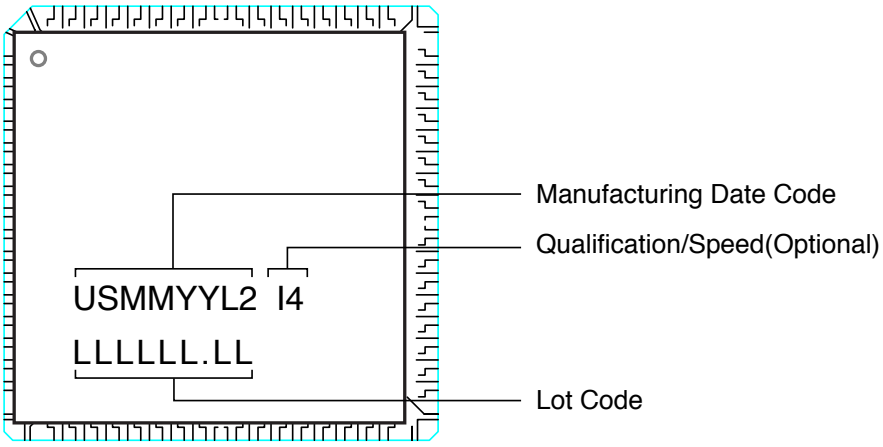
DIMENSIONAL REFERENCES

Ref	TOLERANCE OF FROM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.08
eee	0.08
fff	0.10



Note:
① 'eT' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
② DATUM 'C' IS THE MOUNTING SURFACE, WITH WHICH THE PACKAGE IS IN CONTACT.
③ DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
④ DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
⑤ METALLIZED PADS ARE Cu PAD WITH IT'S EXPOSED SURFACE PLATED WITH Ni & Au.

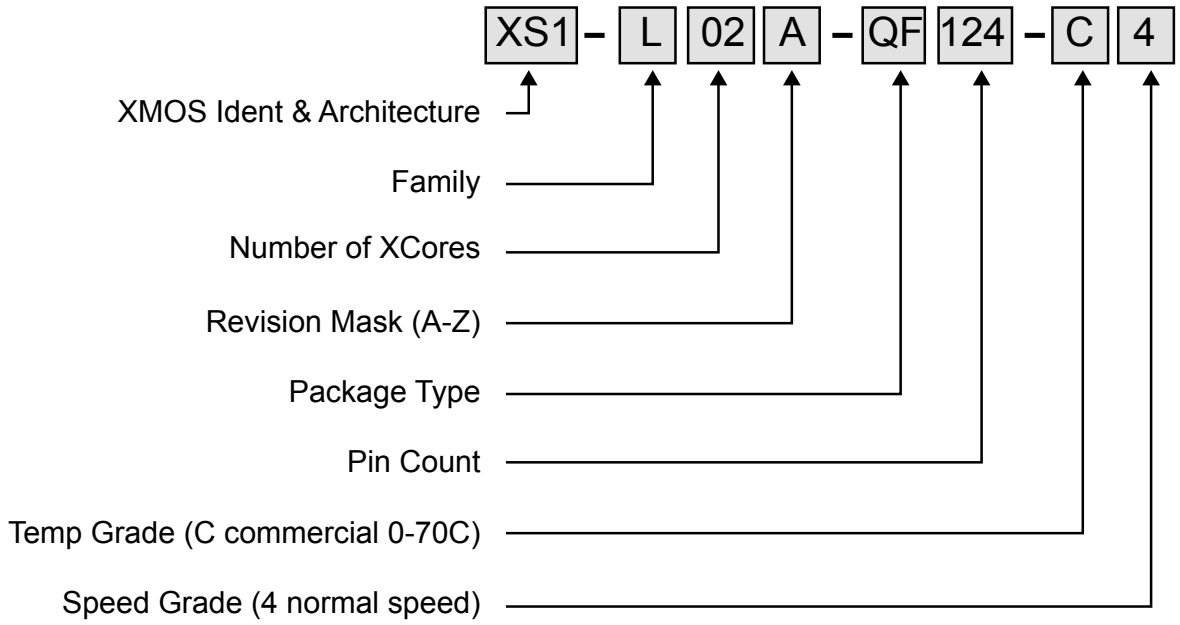
5.4 Package Marking Details



Manufacture Date Code	Part Number
USMMYYL2	XS1-L02A-QF124-C4
USMMYYL2 C5	XS1-L02A-QF124-C5
USMMYYL2 I4	XS1-L02A-QF124-I4
USMMYYL2 I5	XS1-L02A-QF124-I5

6 Ordering information

Part numbering and ordering information.



6.1 Orderable part numbers

Part Number	Speed	Package	Qualification
XS1-L02A-QF124-C4	800MIPS	124 pin QFN 0.5mm pitch	Commercial 0° C to +70° C
XS1-L02A-QF124-C5	800MIPS	124 pin QFN 0.5mm pitch	Commercial 0° C to +70° C
XS1-L02A-QF124-I4	1000MIPS	124 pin QFN 0.5mm pitch	Industrial -40° C to +85° C
XS1-L02A-QF124-I5	1000MIPS	124 pin QFN 0.5mm pitch	Industrial -40° C to +85° C

7 Device Configuration

Example schematic diagrams detailing minimal system configurations may be found at: http://xmos.com/support/silicon

8 Addendum

8.1 USB ULPI Mode

When using the XS1-L2 with ULPI, the ULPI signals must only be connected to the following pins on one core:

Pin Name	Pin ID		ULPI Signal	Description
	Core 0	Core 1		
X*n*D12	A55	A21	ULPI_STP	Stop data
X*n*D13	A57	A23	ULPI_NXT	Next data
X*n*D14:X*n*D21	A58, A59, A60, A61, A63, A64, A65, A66	A24, A25, A26, A27, A29, A30, A31, A32	ULPI_DATA[0:7]	Data
X*n*D22	A56	A22	ULPI_DIR	Data direction
X*n*D23	A62	A28	ULPI_CLK	Interface clock

Some ports on the selected core are not available for use by user software while the ULPI is enabled—see the XS1-L Hardware Design Checklist for further details.

9 Related Documents

Information about XMOS technology is primarily available from the XMOS web site; please see http://xmos.com/documentation for the latest documents or click on one of the links below to find out more information.

Document title	Document reference
The XMOS XS1 Architecture	xs1_en
Programming XC on XMOS Devices	xc_en
XS1-L System Specification	xsysteml
XMOS Tools User Guide	xtools_en
XS1 Assembly Language Manual	xas_en
XMOS XS1 32-Bit Application Binary Interface	abi_en
XS1-L Clock Frequency Control Application Note	xs1l_clk
XS1 Port I/O Timing Application Note	xs1_port_timing
XS1-L Link Performance and Design Guidelines	xs1l_links
Estimating Power Consumption For XS1-L Devices	xs1l_power
XS1-L Active Power Conservation	xs1laec
XS1-L Hardware Design Checklist	xs1lcheck

10 Document History

Date	Release	Comment
2009-12-18	1v0	First release
2010-01-07	1v1	Section 3.2, NOTE updated "... the boot mode indicated on the MODE[3:2] pins is ignored." Added Package marking section. Added ring position to pin table.
2010-01-19	1.2	Added Precedence section. Added PCU details. Added SPI boot details.
2010-03-15	1.3	Added Power Supply Sequencing section. Enumerated all Mode[4:0] pin options Aligned with L1-64 and L1-128 datasheets v2.0. Changed from 'Preliminary' to 'Release'.
2010-05-20	1.4	Added USB ULPI Mode section. Added Industrial part numbers and characteristics. Added 500MHz part.
2010-06-16	1.5	Corrected Mode 4—pin A35 in Errata, in line with all other MODE 4 references in document. Corrected A23—Pin XnD13 Core 1 USB ULPI Mode section

11 Errata

To guarantee a logic low is seen on the following pins, the driving circuit should present an impedance of less than 100 ohms to ground.

Pin ID	Signal
A35	MODE4
B8	RST_N
B37	DEBUG
B36, B35, B34, B33	MODE[3:0]
B13	TRST_N
B11	TMS
B10	TCK
B12	TDI
B55	X0D43

Usually this is not a problem for CMOS drivers driving single inputs, however, if one or more of these inputs are placed in parallel, additional logic buffers may be required to guarantee correct operation.

For static inputs tied high or low, the relevant input pin should be tied directly to GND or VDDIO.

Disclaimer