XS1-L1 64LQFP Datasheet

Version 2.1

XMOS

Publication Date: 2010/05/20

1 Description

XS1-L1 Description

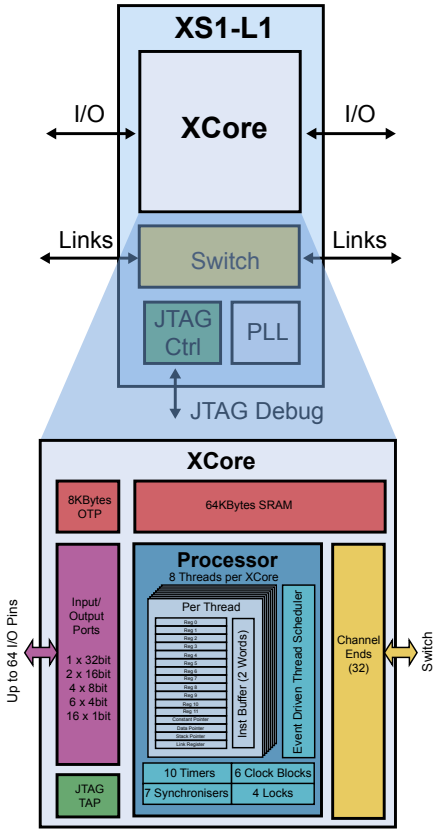
The XS1-L1 is a member of the XS1-L family of XMOS devices. The XS1-L family blends a powerful programmable fabric based on multi-threaded processors with a high-level programming language design flow. XMOS chips are general-purpose programmable devices that can be used in a wide range of applications and systems.

The XS1-L1 device is based on the XMOS XCore™. Each XCore contains a 32-bit processor, SRAM memory, I/O ports for communicating with external components and channels for communicating with other devices.

One Time Programmable (OTP) memory is provided for application boot code and security keys, with a secure mode that disables debug and prevents read-back of memory contents.

A high performance switch supports low latency and deterministic communication between the threads in different XCores.

The XMOS architecture is unique in its direct support for concurrent processing (multi-threading), event handling, communication and timed I/O operations.



XS1-L1 64LQFP Package Features

One XCore providing 400/500MIPS and eight concurrent, deterministic real-time tasks
36 user I/O pins, dynamically configurable as input, output or bi-directional

XCore Resources

Threads	8
Channel Ends	32
Timers	10
Clock Blocks	6 (includes the reference clock)
XMOS Links	2 (5bit or 2bit)
Thread Synchronisers	7
Hardware Locks	4
SRAM	64KBytes
OTP Memory	8KBytes

2 Signal Descriptions

This section describes the external signal pins of the XS1-L1 in the 64 LQFP package.

The following I/O type conventions are used in this document:

I/O type convention	
I	Input
O	Permanent Output
IO	Bidirectional
OT	Tristatable Output
PU	Pull Up
PD	Pull Down
ST	Schmitt Trigger

2.1 XCore Signals

The XS1-L1 64 LQFP device provides 36 XCore signals that can be used for generic I/O ports or for XMOS Links.

2.1.1 XCore signals as I/O ports

The following table shows the I/O ports available on the XCore processor. Each port is bidirectional. See Section 2.2 Port Pin Table for details on the I/O ports in the 64 LQFP device.

Port Width	**1-bit**	**4-bit**	**8-bit**	**16-bit**
Number of ports	16 [A:P]	5 [A:E]	2 [A:B]	1 [A]

2.1.2 XCore signals as XMOS Links

XMOS Links are bidirectional and may operate in either 5bit/direction or 2bit/direction mode. See Section 2.2 Port Pin Table for further information.

Interface type	**5bit fast**	**2bit serial**
Number of XMOS links	2 [A:B]	2 [A:B]

2.1.3 Precedence

Ports and XMOS Links are connected to pins on the XS1-L1 by the program running on the device. The ports and links are multiplexed and follow a defined precedence if they overlap on the same core:

- If an XMOS Link is enabled, the link has access to the pins; the pins of the underlying ports are disabled.
- If a port is enabled, it overrules ports with higher widths that share the same pins. The pins on the wider port that are not shared remain available for use when the narrower port is enabled.

Ports always operate at their specified width, even if they share pins with another port.

2.2 Port Pin Table

Package		XMOS Links		Ports				Notes
Pin Name	Pin ID	5bit	2bit	1b	4b	8b	16b	
X0D0	16			P1A0				1
X0D1	15	X0LA4out		P1B0				1
X0D2	14	X0LA3out			P4A0	P8A0	P16A0	2
X0D3	12	X0LA2out			P4A1	P8A1	P16A1	2
X0D4	11	X0LA1out	X0LA1out		P4B0	P8A2	P16A2	2
X0D5	10	X0LA0out	X0LA0out		P4B1	P8A3	P16A3	2
X0D6	7	X0LA0in	X0LA0in		P4B2	P8A4	P16A4	2
X0D7	5	X0LA1in	X0LA1in		P4B3	P8A5	P16A5	2
X0D8	3	X0LA2in			P4A2	P8A6	P16A6	2
X0D9	2	X0LA3in			P4A3	P8A7	P16A7	2
X0D10	1	X0LA4in		P1C0				1
X0D11	64			P1D0				1
X0D12	63			P1E0				2
X0D13	62	X0LB4out		P1F0				2
X0D14	59	X0LB3out			P4C0	P8B0	P16A8	2
X0D15	58	X0LB2out			P4C1	P8B1	P16A9	2
X0D16	57	X0LB1out	X0LB1out		P4D0	P8B2	P16A10	2
X0D17	56	X0LB0out	X0LB0out		P4D1	P8B3	P16A11	2
X0D18	55	X0LB0in	X0LB0in		P4D2	P8B4	P16A12	2
X0D19	54	X0LB1in	X0LB1in		P4D3	P8B5	P16A13	2
X0D20	51	X0LB2in			P4C2	P8B6	P16A14	2
X0D21	50	X0LB3in			P4C3	P8B7	P16A15	2
X0D22	49	X0LB4in		P1G0				2
X0D23	48			P1H0				2
X0D24	47			P1I0				
X0D25	46			P1J0				
X0D26	45				P4E0	P8C0	P16B0	2
X0D27	44				P4E1	P8C1	P16B1	2
X0D32	36				P4E2	P8C6	P16B6	2
X0D33	35				P4E3	P8C7	P16B7	2
X0D34	34			P1K0				
X0D35	33			P1L0				
X0D36	42			P1M0		P8D0	P16B8	
X0D37	41			P1N0		P8D1	P16B9	2
X0D38	39			P1O0		P8D2	P16B10	2
X0D39	38			P1P0		P8D3	P16B11	2

[1] SPI signals must be attached to specific pins—see Section 3.3

[2] ULPI signals must be attached to specific pins. In addition some ports are not available when ULPI is enabled—see Section 8.1

2.3 System Service Pins

Pin ID	Signal
9	CLK
17	DEBUG
22	MODE0
23	MODE1
24	MODE2
25	MODE3

Pin ID	Signal
19	PLL_AGND
20	PLL_AVDD
8	RST_N
29	TCK
30	TDI
31	TDO
27	TMS
26	TRST_N

2.4 Core Power and Ground Pins

Pin ID	Signal
4	VDD
13	VDD
21	VDD
28	VDD
37	VDD
43	VDD
52	VDD
61	VDD

Pin ID	Signal
PADDLE	GND

2.5 XCore I/O Power Pins

Pin ID	Signal
6	VDDIO
18	VDDIO
32	VDDIO

Pin ID	Signal
40	VDDIO
53	VDDIO
60	VDDIO

2.6 XMOS Link Pins

See Section 2.2 Port Pin Table

3 System Services

System Services are required to support correct device behavior. These signals control clocking, reset and boot behavior of the device.

3.1 Clock control signals

These signals control the on-chip PLL of the XS1-L1

Signal	Pin ID	I/O	Description
PLL_AVDD	20	pwr	Analog power supply for the PLL
PLL_AGND	19	pwr	Analog ground for the PLL
CLK	9	I, PD, ST	Reference clock input for the PLL

Functional description

PLL_AVDD The PLL requires a very clean AVDD power supply. It is recommended that this supply node be separated from the other, noisier, supplies on the board. The supply should be decoupled close to the respective IC package pin. Nominally 1.0V.

PLL_AGND Analog ground for the PLL. Connect directly to board ground.

CLK Reference clock input for the PLL. This signal is used as a reference by the PLL in generating all on chip clocks.

3.2 Miscellaneous control signals

Signal	Pin ID	I/O	Description
MODE[3:0]	25, 24, 23, 22	I, PU, ST	Sets boot mode
DEBUG	17	IO, PU	Multi-device debug
RST_N	8	I, PU, ST	Asynchronous system reset

Functional description

MODE[3:0] These pins determine the boot source and PLL boot mode of the device. Bits [3:2] control the boot source according to the following table:

MODE3	MODE2	Boot Source
0	0	None - Device will wait to be booted (via JTAG)
0	1	Reserved
1	0	XMOS Link B
1	1	SPI

Bits [1:0] control the PLL boot mode according to the following table:

MODE1	MODE0	PLL Multiplier Ratio	PLL reference clk	Boot Frequency
0	0	30.75	4.22 to 13 MHz	130 to 399.75 MHz
0	1	4	21.66 to 100 MHz	86.66 to 400 MHz
1	0	8.3333	10.4 to 48 MHz	86.66 to 400 MHz
1	1	20	4.33 to 20 MHz	86.66 to 400 MHz

NOTE: If secure boot from OTP is enabled by programming the OTP, the boot source specified on the MODE[3:2] pins is ignored. For further details on booting XCores see the XS1-L System Specification.

DEBUG This pin is used to synchronize the debugging of multiple XS1 devices. This pin can operate in both output and input mode. In output mode and when configured to do so, DEBUG is driven low by the device when the XCore processor hits a debug break point. Prior to this point the pin will be tri-stated. In input mode and when configured to do so, driving this pin low will put the XCore into debug mode. Software can set the behavior of the XCore based on this pin. This pin should have an external pull up of 4K7 ohms.

RST_N Active low asynchronous-assertion global reset signal. At power-up, this pin must be activated for at least 5us after the power supplies are stable to ensure reliable booting. Following a reset the PLL re-establishes lock after which the device boots up according to the boot mode (see MODE).

3.3 SPI Interface

When booting the XS1-L1 device from a SPI interface, the SPI device must be connected to the XS1-L1 as follows:

Pin Name	Pin ID	SPI Signal	Description
X0D0	16	MISO	Data - Master In Slave Out
X0D1	15	SS	Slave Select
X0D10	1	SCLK	Clock
X0D11	64	MOSI	Data - Master Out Slave In

3.4 JTAG Operation

The XS1-L1 device contains a standard 5 pin JTAG interface, which allows the following functionality:

- Boundary scan testing for verifying printed circuit board connectivity.
- In-circuit source level debugging of the XCore.
- Programming of the One Time Programmable (OTP) ROM.

The JTAG interface on the XS1-L1 consists of the following signals:

Signal	Pin ID	I/O	Description
TCK	29	I, PU, ST	Test clock
TMS	27	I, PU, ST	Test mode select
TRST_N	26	I, PU, ST	Test reset (active low)
TDI	30	I, PU, ST	Test data in
TDO	31	OT, PD	Test data out

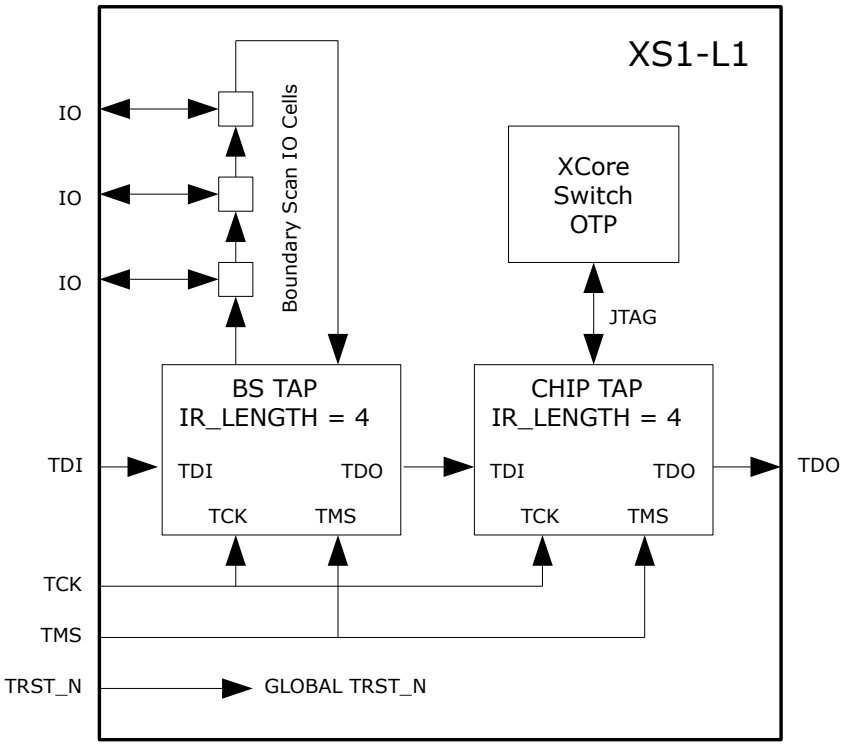
The TRST_N pin must be driven low for at least 100ns after the power supplies are stable to reset the JTAG circuitry. If JTAG debug is not required, the TRST_N pin can be tied low with a 1k resistor to hold the JTAG port in reset.

Each XS1-L device contains multiple TAP controllers, each enabling different functionality. Directly after reset, two TAP controllers are present in the JTAG chain - the boundary scan TAP (BS TAP) and the chip TAP (CHIP TAP).

The boundary scan TAP is a standard 1149.1 compliant TAP and can be used for boundary scan of the I/O pins of the device. The chip TAP allows access into the XCore, Switch and OTP for such actions as loading code and debugging. Both TAPs have an instruction register length of 4. From reset, the chip TAP is in BYPASS so simply presents an extra 1-bit into the scan chain when shifting data.

If access to the XCore/Switch/OTP is required, the ChipTAP sets internal multiplexers which optionally add in additional TAPs into the JTAG chain for each of the Switch, XCore and OTP. The XCore TAP allows register read/write commands to be made for program loading/debug.

A diagram of the JTAG chain structure is shown below:



3.4.1 Device identification register

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified as follows:

Bit31																												Bit0
Version				Part Number														Manufacturer Identity										1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	1	1
0				0				0				0				2				6				3				3	

3.4.2 Usercode register

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified as follows:

Bit31																												Bit0
OTP User ID										Unused				Silicon Revision														
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0				0				0				2				8				0				0				0	

The OTP User ID is read from the OTP and can be programmed as a means of identifying versions of OTP programmed devices. Unprogrammed devices have these bits set to zero.

4 DC and Switching Characteristics

4.1 Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
VDD(IO)	I/O DC supply voltage	3.0	3.3	3.6	V	
VDD(CORE)	Core DC supply voltage	0.95	1.0	1.05	V	
AVDD(PLL)	PLL analogue supply	0.95	1.0	1.05	V	
Cl	XCore I/O load capacitance			25	pF	
Ta	Operating temperature range (Commercial)	0		70	°C	
	Operating temperature range (Industrial)	-40		85	°C	
Tj	Junction temperature			125	°C	
Tstg	Storage temperature	-65		150	°C	

4.2 DC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
V(IH)	Input high voltage	2		3.6	V	1,6
V(IL)	Input low voltage	-0.3		0.7	V	1,6
V(OH)	Output high voltage	2.7			V	2,3,6
V(OL)	Output low voltage			0.6	V	2,4,6
R(PU)	Pull-up resistance		35K		Ohms	5,6
R(PD)	Pull-down resistance		35K		Ohms	5,6

Notes:

1. All pins except power supply pins.
2. P1A, P1D, P1E, P1H, P1I, P1J, P1K and P1L are nominal 8mA drivers, the remainder of the general purpose I/O are 4mA.
3. Measured with 4mA drivers sourcing 4mA, 8mA drivers sourcing 8mA.
4. Measured with 4mA drivers sinking 4mA, 8mA drivers sinking 8mA.
5. Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry.
6. Preliminary figures.

4.3 ESD Stress Voltage

ESD Model	ESD Stress Voltage	Notes
HBM	± 2.0 KV	
MM	± 200 V	

4.4 Reset Timing

Parameters	MIN	TYP	MAX	UNITS	Notes
Reset pulse width	100			ns	
Initialisation time			150	us	1

Notes:

1. This parameter shows the time taken to start booting after RST_N has gone high.

4.5 Power Supply

Power is applied to the device through the VDDIO and VDD pins. Several pins of each type are provided to minimize the effect of inductance within the package. All supply pins must be connected. Each supply should be decoupled close to the chip by several 100nF low inductance (for example, ceramic) capacitors between VDDIO and GND, and VDD and GND.

Input voltages must not exceed specification with respect to VDDIO, VDD and GND, even during power up and power down ramping. Permanent damage can occur if the operation exceeds these ranges.

4.5.1 Power Supply Sequencing

To ensure correct device operation, the VDDIO supply should be present before the VDD supply. Specifically, the VDDIO supply should rise to its nominal operating range with VDD held at 0V. The VDD supply should then rise to its nominal operating range with a rise time of less than 10ms.

4.5.2 Power Consumption

Core power consumption

The power consumption of the XS1-L1 is highly application dependant. The following figures should be used for budgetary purposes only:

Commercial and Industrial Qualification						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
I(DDCQ)	Quiescent VDD(core) current		14		mA	1
PD	Core Power dissipation		450		μW/MIPS	2, 3, 4

Notes:

1. Assumes typical core and I/O voltages, with no switching activity.
2. Assumes typical core and I/O voltages, with nominal activity.
3. Assumes 1MHz = 1 MIPS.
4. PD(TYP) value is the usage power consumption under typical operating conditions.

Core power consumption example

Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
IDD	Active VDD(core) current		160		mA	1

Notes:

1. Measurement conditions: VDD = 1.0V, VDDIO = 3.3V, 25°C, 400MHz, average device resource usage.

PLL current consumption

Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
I(ADDPLL)	PLL_AVDD current			7	mA	1

Notes:

1. PLL_AVDD = 1.0V

For a more detailed analysis see Estimating Power Consumption For XS1-L Devices.

4.6 Clock

XS1-L devices use an input clock frequency, supplied by the user on the CLK pin, to drive the PLL and obtain the system clock. The nominal frequency of the clock for all XS1 family components is 20MHz but other clock frequencies can be used by reprogramming the internal PLL through use of the MODE pins or by application software. For further details on configuring the clock see the XS1-L Clock Frequency Control Application Note.

Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
	Frequency	4.22	20	100	MHz	
	Slew Rate	0.1			V/ns	
	Long Term Jitter (pk-pk)			2	%	CLK period

CLK pin clock edges must be monotonic and remain within the specified voltage and time limits. CLK should be stable before RST_N is taken high.

A set of system clock dividers are applied to the system clock frequency allowing specific clock frequencies to be derived for the XCore, the switch and the reference clock.

Speed Grade 4						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
	System Clock Frequency			400	MHz	1

Speed Grade 5						
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**UNITS**	**Notes**
	System Clock Frequency			500	MHz	1

Notes:

1. Assumes typical core and I/O voltages, with nominal activity.

4.7 Memory

4.7.1 Internal static memory

The XS1-L1 has a total of 64KBytes of fast internal static memory for high rates of data throughput. Each internal memory access consumes one core clock cycle. There is no dedicated external memory interface, although memory can be expanded through appropriate use of the ports.

4.7.2 Internal one-time programmable memory

The XS1-L1 has a total of 8KBytes of one-time programmable memory. This can be programmed using the JTAG interface or by application software.

4.8 Port Timing

4.8.1 XCore I/O AC Characteristics

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
T(XOINVALID)	XCore I/O Minimum Output Data Invalid window which can be achieved using Port/ClkBlk combination	9			ns	
T(XOVALID)	XCore I/O Minimum Input Data Valid window to allow safe acquisition of data using Port/ClkBlk combination	8			ns	
T(XIFMAX)	Maximum XCore I/O toggle frequency which can be safely acquired and used as a clock source using a ClkBlk			60	MHz	

The Input Valid window parameter relates to the capability of the XS1-L1 family devices to capture data input to the chip with respect to an external clock source. This parameter can be calculated as the sum of the input setup time and input hold time with regard to the external clock as measured at the L1 device pins. The output invalid window specifies the time for which an output will be invalid with respect to the external clock. Note that these parameters are specified as a window rather than absolute numbers since the L1 provides functionality to delay the incoming clock with respect to the incoming data.

For further details on these parameters and on interfacing to higher speed synchronous interfaces see XS1 Port I/O Timing Application Note.

4.9 Link Interface Performance

Symbol	Parameter	MIN	TYP	MAX	UNITS	Notes
B(2blink)	2b link bandwidth			95	Mbit/s	1
B(5blink)	5b link bandwidth			244	Mbit/s	1

Notes:

1. Assumes 32 Byte packet, 7.5ns symbol time.

The asynchronous nature of links means that the relative phasing of CLK clocks is not important in a multi-clock system, providing each meets the required stability criteria.

4.10 JTAG Timing

All JTAG operations are synchronous to TCK apart from the global asynchronous reset TRST_N.

Parameters	MIN	TYP	MAX	UNITS	Notes
TCK frequency (debug)			18	MHz	
TCK frequency (boundary scan)			10	MHz	
T_{SETUP}	5			ns	1
T_{HOLD}	5			ns	1
$T_{CLOCK\ to\ OUT}$			15	ns	2

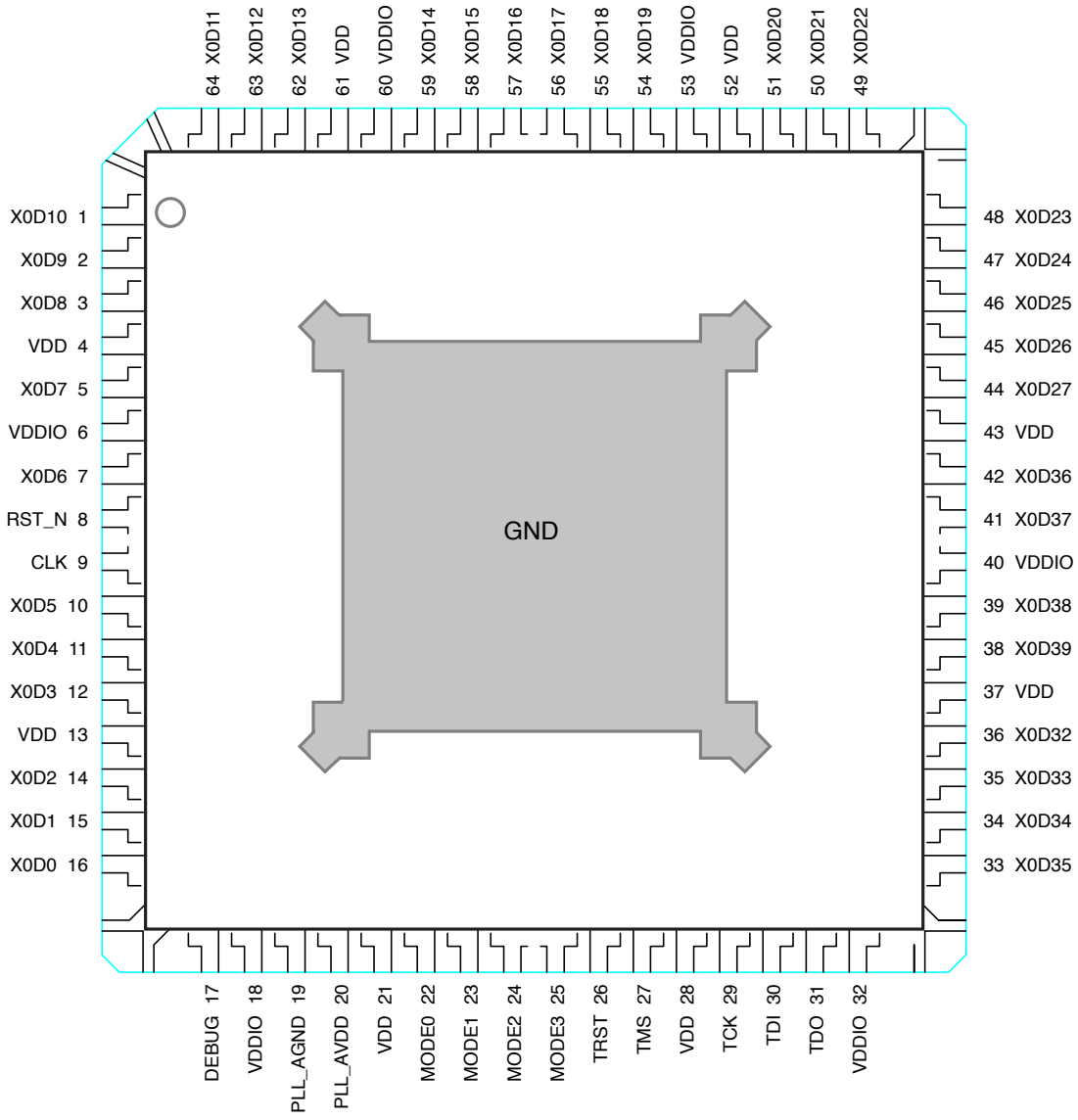
Notes:

1. Timing applies to TMS and TDI inputs
2. Timing applies to TDO output from negative edge of TCK

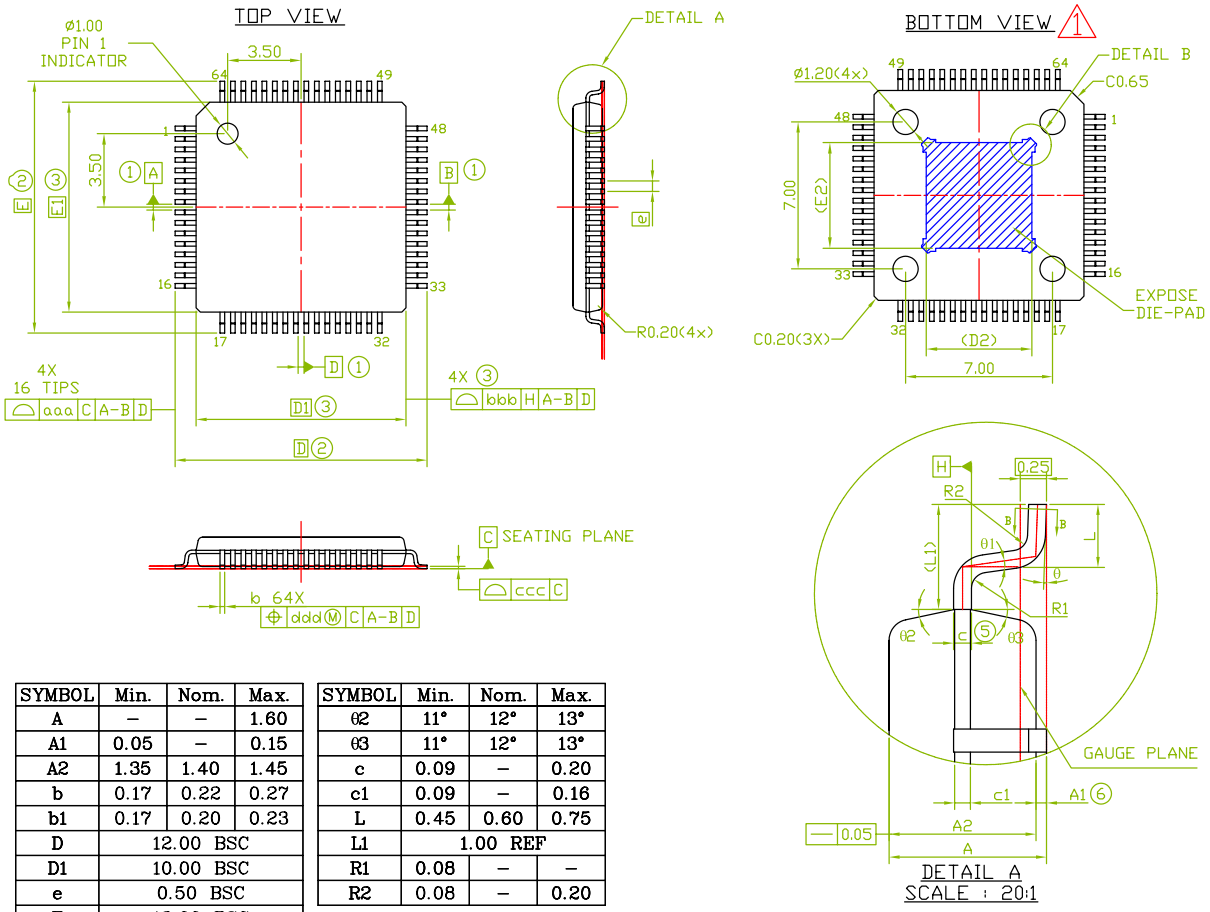
5 Package Details

5.1 Package Pin Layout

The following diagram shows the pin names and locations for the 64 LQFP package.



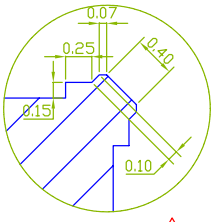
5.2 Package Mechanical Details



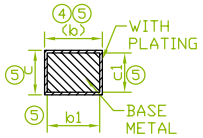
SYMBOL	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
D	12.00 BSC		
D1	10.00 BSC		
e	0.50 BSC		
E	12.00 BSC		
E1	10.00 BSC		
θ	0°	3.5°	7°
θ1	0°	–	–

SYMBOL	Min.	Nom.	Max.
θ2	11°	12°	13°
θ3	11°	12°	13°
c	0.09	–	0.20
c1	0.09	–	0.16
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	–	–
R2	0.08	–	0.20

REF	TOLERANCES OF FORM AND POSITION
aaa	0.20
bbb	0.20
ccc	0.08
ddd	0.08



DETAIL B
SCALE : 20:1

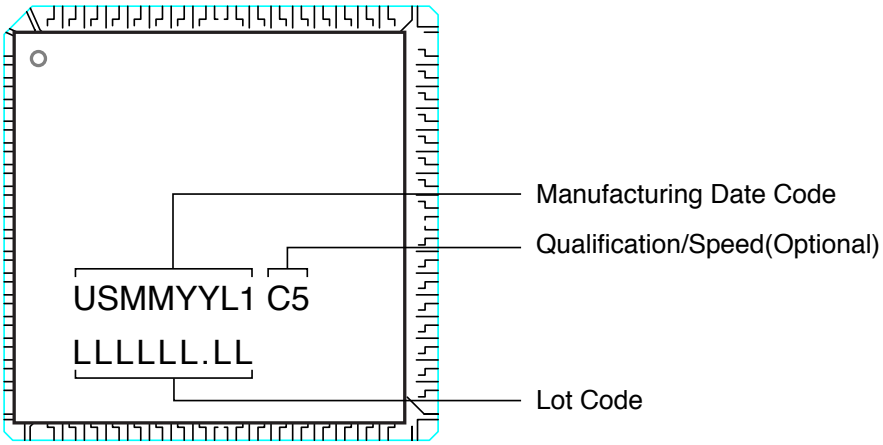


SECTION B-B
SCALE : 50:1

NOTE :
① DATUM A-B AND D TO DETERMINE AT DATUM PLANE H.
② TO BE DETERMINED AT SEATING DATUM PLANE C.
③ DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
④ DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07mm FOR 0.4mm AND 0.5mm PITCH PACKAGE.
⑤ THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
⑥ A1 IS THE DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7 PACKAGE DIMENSIONS REFERENCE TO JEDEC MS-026 Rev.D, except D2 and E2

LF Ref#	Symbol	Min	Nom	Max
L-16-09006	D2	4.93	5.03	5.13
	E2	4.93	5.03	5.13

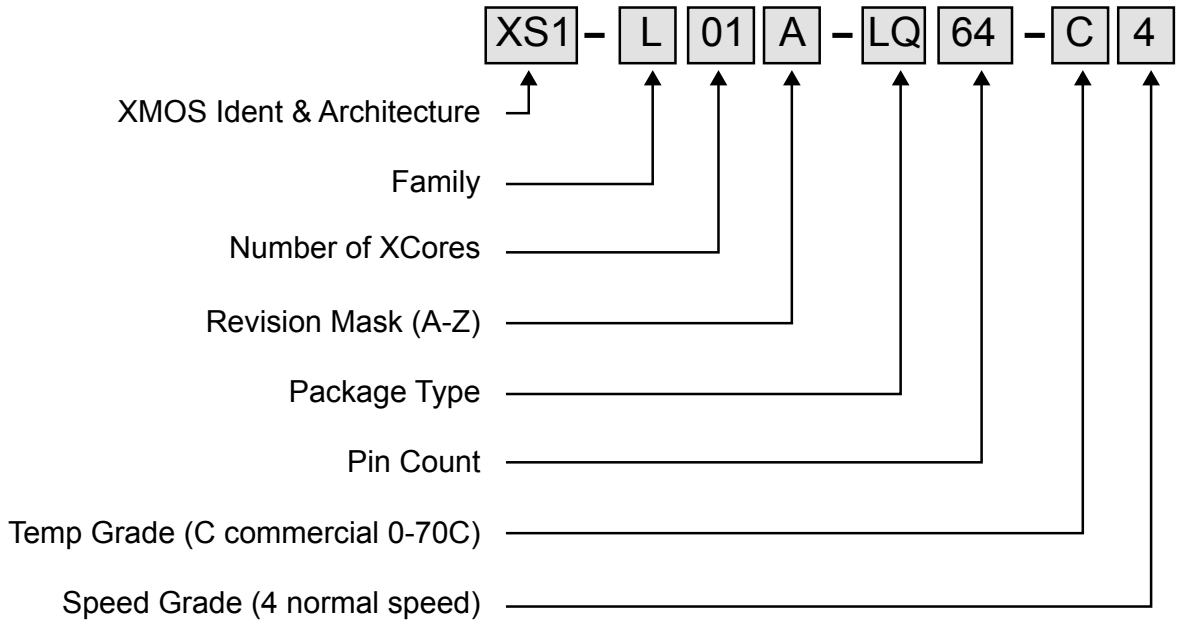
5.3 Package Marking Details



Manufacture Date Code	Part Number
USMMYYL1	XS1-L01A-LQ64-C4
USMMYYL1 C5	XS1-L01A-LQ64-C5
USMMYYL1 I4	XS1-L01A-LQ64-I4
USMMYYL1 I5	XS1-L01A-LQ64-I5

6 Ordering information

Part numbering and ordering information



6.1 Orderable part numbers

Part Number	Speed	Package	Qualification
XS1-L01A-LQ64-C4	400MIPS	64 pin LQFP 0.5mm pitch	Commercial 0° C to +70° C
XS1-L01A-LQ64-C5	500MIPS	64 pin LQFP 0.5mm pitch	Commercial 0° C to +70° C
XS1-L01A-LQ64-I4	400MIPS	64 pin LQFP 0.5mm pitch	Industrial -40° C to +85° C
XS1-L01A-LQ64-I5	500MIPS	64 pin LQFP 0.5mm pitch	Industrial -40° C to +85° C

7 Device Configuration

Example schematic diagrams detailing minimal system configurations may be found at: http://xmos.com/support/silicon

8 Addendum

8.1 USB ULPI Mode

When using the XS1-L1 with ULPI, the ULPI signals must only be connected to the following pins:

Pin Name	Pin ID	ULPI Signal	Description
X0D12	63	ULPI_STP	Stop data
X0D13	62	ULPI_NXT	Next data
X0D14:X0D21	59, 58, 57, 56, 55, 54, 51, 50	ULPI_DATA[0:7]	Data
X0D22	49	ULPI_DIR	Data direction
X0D23	48	ULPI_CLK	Interface clock

Some ports on the core are not available for use by user software while the ULPI is enabled—see the XS1-L Hardware Design Checklist for further details.

9 Related Documents

Information about XMOS technology is primarily available from the XMOS web site; please see http://xmos.com/documentation for the latest documents or click on one of the links below to find out more information.

Document title	Document reference
The XMOS XS1 Architecture	xs1_en
Programming XC on XMOS Devices	xc_en
XS1-L System Specification	xsysteml
XMOS Tools User Guide	xtools_en
XS1 Assembly Language Manual	xas_en
XMOS XS1 32-Bit Application Binary Interface	abi_en
XS1-L Clock Frequency Control Application Note	xs1l_clk
XS1 Port I/O Timing Application Note	xs1_port_timing
XS1-L Link Performance and Design Guidelines	xs1l_links
Estimating Power Consumption For XS1-L Devices	xs1l_power
XS1-L Active Power Conservation	xs1laec
XS1-L Hardware Design Checklist	xs1lcheck

10 Document History

Date	Release	Comment
2010-01-15	1.6	Added Package Marking section Added Industrial and Commercial Qualification values Added 500MHz part Section 3.2, NOTE updated "... the boot mode indicated on the MODE[3:2] pins is ignored." Corrected document title to XS1-L1 64LQFP Datasheet. Added SPI pin details. Added Precedence section. Revised format
2010-02-15	2.0	Added JTAG information Added power sequencing requirement Added power consumption details
2010-05-20	2.1	Added USB ULPI Mode section

11 Errata

To guarantee a logic low is seen on the following pins, the driving circuit should present an impedance of less than 100 ohms to ground.

Pin ID	Signal
8	RST_N
17	DEBUG
25, 24, 23, 22	MODE[3:0]
26	TRST_N
27	TMS
29	TCK
30	TDI

Usually this is not a problem for CMOS drivers driving single inputs, however, if one or more of these inputs are placed in parallel, additional logic buffers may be required to guarantee correct operation.

For static inputs tied high or low, the relevant input pin should be tied directly to GND or VDDIO.

Disclaimer