**Communications and Advanced
Consumer Technologies Group**

MC68SEC000

Freescale Semiconductor, Inc.

Product Brief
MC68SEC000 Microprocessor

INTRODUCTION

The MC68SEC000 is a cost-effective static embedded processor engineered for low-power applications. In addition to providing the substantial cost and performance benefits of the MC68EC000, the low-power mode of the MC68SEC000 provides significant advantages in power consumption and power management. The typical current consumption of the MC68SEC000 is only 0.5µA in static standby mode and 15.0mA in normal 3.3V operation. The MC68SEC000 operates in either 3.3V or 5.0V systems. The remarkably low power consumption, small footprint packages, and static implementation are combined in the MC68SEC000 for low-power applications such as personal digital assistants, portable measuring equipment, electronic games, and battery-operated hand-held consumer products.

The HCMOS MC68SEC000 static architecture is a direct replacement for the MC68EC000, which offers the lowest cost entry point to 32-bit processing. The internal 32-bit architecture provides fast and efficient processing that satisfies the requirements of sophisticated applications based on high-level languages. In addition to being pin-for-pin compatible with the MC68EC000, the MC68SEC000 is object-code compatible with any member of the M68000 Family. Complete code compatibility lets system designers reduce time to market because they can rely on existing M68000 Family code and a broad base of established development tools.

The MC68SEC000 will be available in two small footprint packages: the 64 lead plastic Quad Flat Pack and the 64 lead Thin Quad Flat Pack. The Thin Quad Flat Pack provides a very small package footprint (10.0mm x 10.0mm), making it an ideal choice for portable applications.

The primary features of the MC68SEC000 embedded processor include the following:

- Direct Replacement for the MC68EC000

    — Pin-for-pin compatibility with the MC68EC000 in the plastic QFP package
    — Vast selection of existing third-party development tools for the MC68EC000 support the MC68SEC000
    — Software written for the MC68EC000 will run unchanged on the MC68SEC000

- Power Management

    — Low power HCMOS technology
    — Static design allows for stopping the processor clock
    — 3.3V or 5V operation
    — Typical 0.5µA current consumption at 3.3V in sleep mode

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- Architecture

    — Eight 32-bit address registers
    — Eight 32-bit data registers
    — 16-Mbyte linear addressing range
    — 56 powerful instruction types
    — Operations on five main data types
    — Memory-mapped I/O
    — 14 addressing modes

- Software Strength

    — Fully upward object-code compatible with other M68000 Family products
    — M68000 architecture allows effective assembly code with a C compiler

- Available Packages

    — 64-pin plastic Quad Flat Pack (QFP)
    — 64-pin Thin Quad Flat Pack (TQFP)

- Speed

    — 10/16/20 MHz

- Upgrade

    — Fully upward code-compatible with higher performance 680x0 and 68300 Family members
    — ColdFire^{TM} code-compatible with minor modifications

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OVERVIEW

Figure 1 is a block diagram of the MC68SEC000 embedded processor. This processor provides a 24-bit address bus and a statically selectable 8- or 16-bit data bus, sixteen 32-bit registers, and seven interrupt levels.
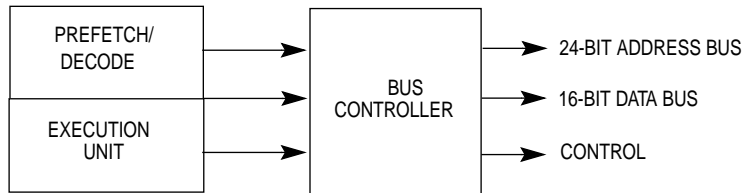
Figure 1. Block Diagram of MC68SEC000

HARDWARE/SOFTWARE COMPATIBILITY

The MC68SEC000 embedded processor is hardware compatible with the MC68EC000, object-code compatible with the MC68EC000, and upward compatible with all members of the M68000 Family.   Object-code compatibility with the M68000 enables code written for the MC68SEC000 to be migrated without modification to any member of the M68000 Family.

LOW-POWER MODE

The MC68SEC000 provides static low-power operation. While in low-power mode, power consumption is reduced to its quiescent value while maintaining the internal state of the processor. The recommended method for placing the MC68SEC000 into low-power mode is described in *Addendum to M68000 8-/16-/32-Bit Microprocessor Users Manual,* M68000 UMAD/AD*.*

SIGNAL DESCRIPTION

Figure 2 shows the functional signal groups for the MC68SEC000. These groups are briefly described in the following paragraphs.
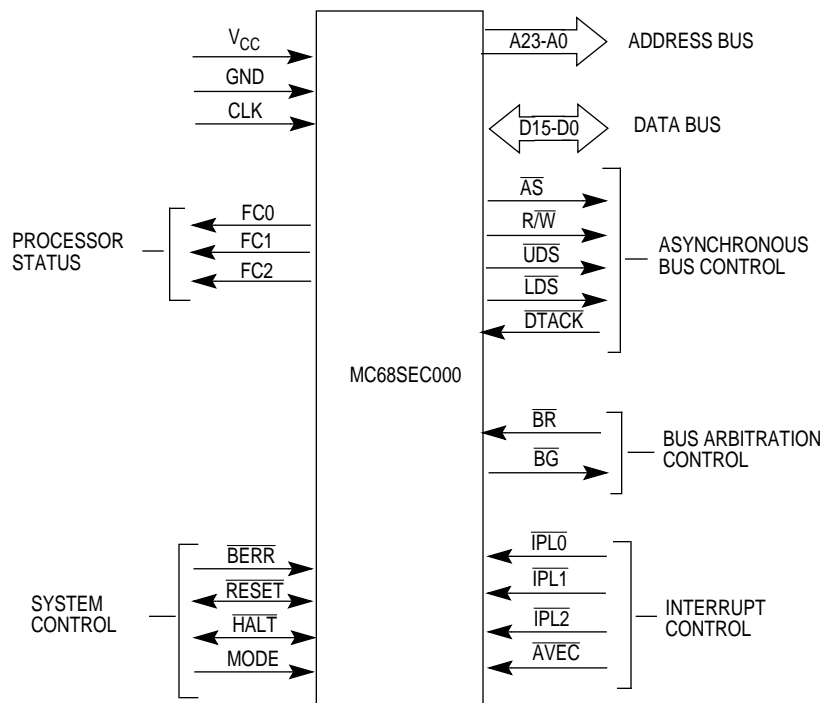
Figure 2. Functional Signal Groups

Address Bus (A23-A0)

This 24-bit, unidirectional, three-state bus can address 16 Mbytes of data. It provides the address for bus operation during all cycles except interrupt cycles. During interrupt cycles, A3, A2, and A1 reflect the level of the interrupt being serviced, while A23-A4 and A0 are set to a logic high.

Data Bus (D15-D0)

This 16-bit, bidirectional, three-state bus is the general-purpose data path. Using the mode pin, you can statically select either 8- or 16-bit modes for data transfer.

Asynchronous Bus Control

Asynchronous data transfers are handled using the following control signals: address strobe ($\overline{AS}$), read/write (R/$\overline{W}$), upper and lower data strobes ($\overline{UDS}$, $\overline{LDS}$), and data transfer acknowledge ($\overline{DTACK}$). The address strobe signal indicates there is a valid address on the address bus. Read/write defines the data bus transfer as a read or write cycle. The data strobes control the flow of data on the data bus and the data transfer acknowledge indicates that the data transfer is complete.

Bus Arbitration Control

In multiple bus master systems, the bus arbitration circuit determines which device will be the bus master. The bus request ($\overline{BR}$) indicates that an external device requires bus mastership. A bus grant ($\overline{BG}$) indicates to all other potential bus master devices that the controller will release bus control at the end of the current bus cycle.

Interrupt Control

The MC68SEC000 provides seven levels of interrupts. The interrupt priority level ($\overline{\text{IPL2}}$, $\overline{\text{IPL1}}$, $\overline{\text{IPL0}}$) inputs determine the priority level. Level 7 is nonmaskable and is the highest priority interrupt. Automatic vectoring, based on IPL inputs, is available with the autovector ($\overline{\text{AVEC}}$) input.

System Control

The system control inputs include the $\overline{\text{RESET}}$, $\overline{\text{HALT}}$, $\overline{\text{BERR}}$, and MODE signals. These signals can reset or halt the controller, indicate to the controller that a bus error has occurred, and select from 8- or 16-bit operating mode.

Processor Status (FC2, FC1, FC0)

These active-high, three-state function code outputs indicate the mode (user or supervisor) and the address space currently being accessed. The function code outputs are valid whenever $\overline{\text{AS}}$ is active.

PACKAGE DIAGRAM

The following package diagram applies to both the plastic QFP and TQFP packages of the MC68SEC000.
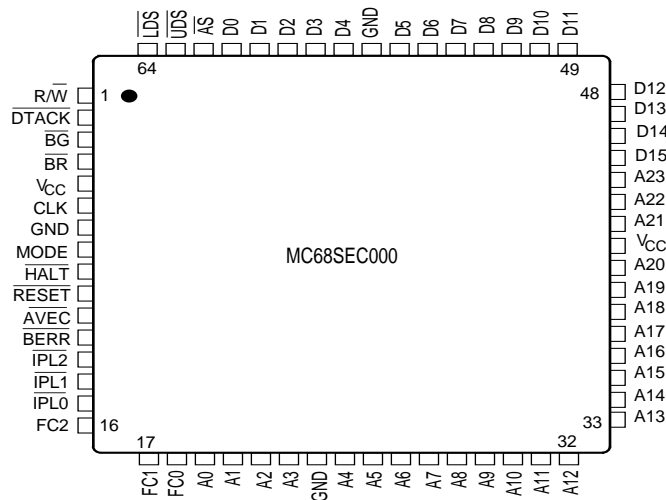
64 LEAD QFP and TQFP

Figure 3. MC68SEC000 Package Diagram

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ORDERING INFORMATION

The following table contains the ordering information for the MC68SEC000.

MC68SEC000 Ordering Information

PACKAGE	BODY SIZE	LEAD SPACING	SPEED	VOLTAGE	SUFFIX	TEMPERATURE RANGE
QFP	14.0 mm X 14.0mm	0.8mm			FU	0C to +70C
			10/16/20 MHz	3.3V or 5.0V	CFU	-40C to +85C
TQFP	10.0mm x 10.0mm	0.5mm			PB	0C to +70C
					CPB	-40C to +85C

DEVELOPER TOOLS

All of the existing third-party developer tools widely available for the MC68EC000 will directly support the MC68SEC000. You can find detailed descriptions of these tools in the *High Performance Embedded Systems Source Catalog* (Revision 4).

DOCUMENTATION

The documents listed in the following table contain detailed information that pertain to the MC68SEC000 processor. These documents can be obtained from the Literature Distribution Centers at the addresses listed on the last page of this document.

MC68SEC000 DOCUMENTATION

MC68SEC000 DOCUMENTATION	DOCUMENT NUMBER	AVAILABILITY
M68000 Family Programmer's Reference Manual	M68000PM/AD	Now
M68000 User's Manual Revision 8	M68000UM/AD	Now
Addendum to M68000 8-/16-/32- Bit Microprocessor Users Manual Revision 8	M68000UMAD/AD	Now
High Performance Embedded Systems Source Catalog Revision 4	BR729/D Rev. 4	Now

Literature Distribution Centers:
USA/EUROPE: Motorola Literature Distribution; P.O. Box 20912, Arizona 85036.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong.

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