CMOS Z-BUS® SCC SERIAL COMMUNICATION CONTROLLER

Z80C30

Product Brief

PB005702-0608

FEATURES

- Z85C30 Optimized for Non-Multiplexed Bus Microprocessors. Z80C30 Optimized for Multiplexed Bus Microprocessors.
- Pin Compatible to NMOS Versions
- Two Independent, 0 to 4.1 Mbit/Second, Full-Duplex Channels, Each with a Separate Crystal Oscillator, BaudRate Generator, and Digital Phase-Locked Loop (DPLL) for Clock Recovery.
- Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.
- Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits Per Character, Programmable Clock Factor, Break Detection and Generation; Parity, Overrun, and Framing Error Detection.
- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT Preset to either 1s or 0s.
- SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop.
- Software Interrupt Acknowledge Feature (not with NMOS)
- Local Loopback and Auto Echo Modes
- Supports T1 Digital Trunk
- Enhanced DMA Support (not with NMOS)
  - 10 x 19-Bit Status FIFO
  - 14-Bit Byte Counter
- Speeds:
  - Z85C30 -8.5, 10, 16.384 MHz
  - Z80C30 -8, 10 MHz

Other Features for Z85C30 only:

- New programmable WR7' (write register 7 prime) to enable new features.
- Improvements to support SDLC mode of synchronous communication:
  - Improve functionality to ease sending back-to-back frames.
  - Automatic SDLC opening Flag transmission*
  - Automatic Tx Underrun/EOM Latch reset in SDLC mode*
  - Automatic /RTS deactivation*
  - TxD pin forced "H" in SDLC NRZI mode after closing flag*
  - Complete CRC reception*
  - Improved response to Abort sequence in status FIFO
  - Automatic Tx CRC generator preset/reset
  - Extended read for write registers*
  - Write data set-up timing improvement
- Improved AC timing
  - Three to 3.6 PCLK access recovery time
  - Programmable /DTR//REQ timing*
  - Write data to falling edge of /WR set-up time requirement is now eliminated.
  - Reduced /INT timing
- Other features include:
  - Extended read function to read back the written value to the write registers. *
  - Latching RR0 during read

– RR0, bit D7 and RR10, bit D6 now has reset default value.

Some of the features listed above are available by default, and some of them (features with "*") are disabled on default to maintain compatibility with the existing SCC design, and "program to enable" through WR7' (write register 7 prime).

GENERAL DESCRIPTION

The Zilog Serial Communications Controller, Z80C30 SCC, is a pin and software compatible CMOS member of the SCC family introduced by Zilog in 1981. It is a dual channel, multi-protocol data communications peripheral that easily interfaces to CPU's with multiplexed address/data buses. The advanced CMOS process offers lower-power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allows the SCC to be configuredto satisfy a wide variety of serial communications applications. The many on-chip features such as baud rate generators, digital phase locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features including a 10x19-bit status FIFO and 14-bit byte counter were added to support high speed SDLC transfers using DMA controllers.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drives, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The daisy-chain interrupt hierarchy is also supported as is standard for Zilog peripheral components.

Note: *All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only).*

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

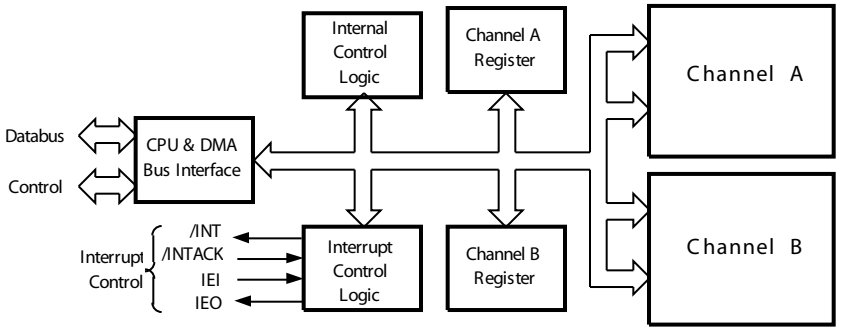

Figure 1. Z80C30 Functional Block Diagram

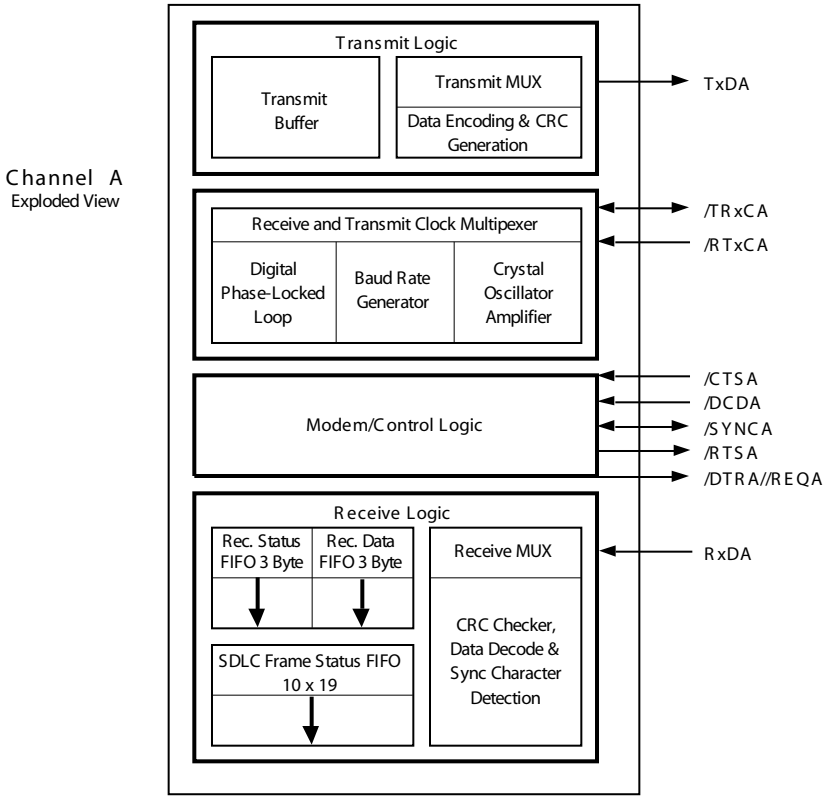

Figure 2. Channel A Exploded View

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