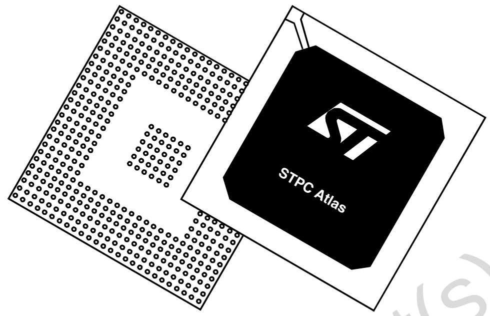
STPC® ATLAS

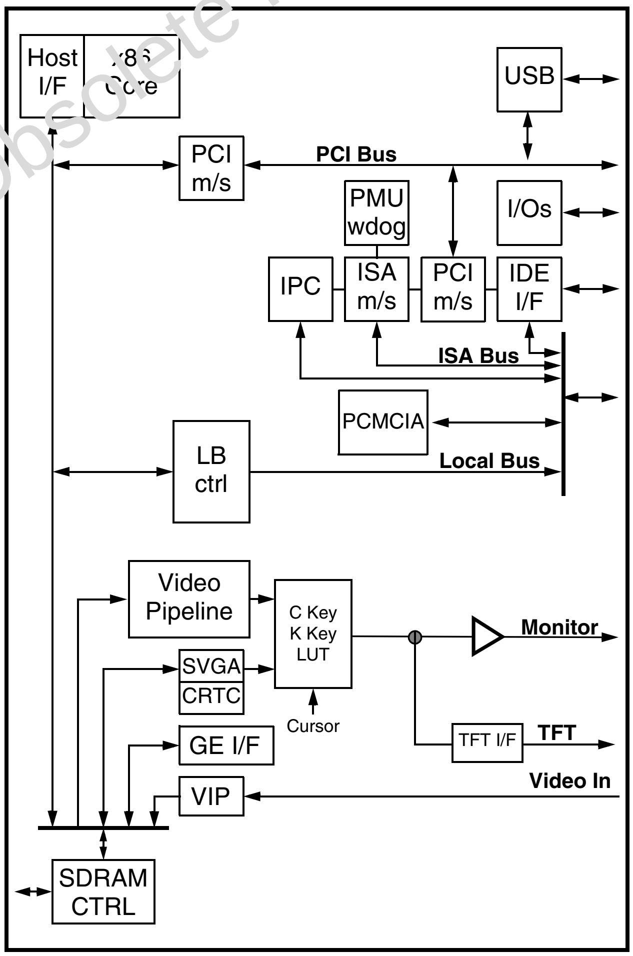
X86 CORE PC COMPATIBLE SYSTEM-ON-CHIP FOR TERMINALS

- POWERFUL x86 PROCESSOR
- 64-BIT SDRAM UMA CONTROLLER
- GRAPHICS CONTROLLER
  - VGA & SVGA CRT CONTROLLER
  - 135MHz RAMDAC
  - ENHANCED 2D GRAPHICS ENGINE
- VIDEO INPUT PORT
- VIDEO PIPELINE
  - UP-SCALER
  - VIDEO COLOUR SPACE CONVERTER
  - CHROMA & COLOUR KEY SUPPORT
- TFT DISPLAY CONTROLLER
- PCI 2.1 MASTER / SLAVE / ARBITER
- ISA MASTER / SLAVE CONTROLLER
- 16-BIT LOCAL BUS INTERFACE
- PCMCIA INTERFACE CONTROLLER
- EIDE CONTROLLER
- 2 USB HOST HUB INTERFACES
- I/O FEATURES
  - PC/AT+ KEYBOARD CONTROLLER
  - PS/2 MOUSE CONTROLLER
  - 2 SERIAL PORTS
  - 1 PARALLEL PORT
  - 16 GENERAL PURPOSE I/Os
  - I²C INTERFACE
- INTEGRATED PERIPHERAL CONTROLLER
  - DMA CONTROLLER
  - INTERRUPT CONTROLLER
  - TIMER / COUNTERS
- POWER MANAGEMENT UNIT
- WATCHDOG
- JTAG IEEE1149.1



PBGA516

Logic Diagram



Rev. 3

DESCRIPTION

The STPC Atlas integrates a standard 5th generation x86 core along with a powerful UMA graphics/video chipset, support logic including PCI, ISA, Local Bus, USB, EIDE controllers and combines them with standard I/O interfaces to provide a single PC compatible subsystem on a single device, suitable for all kinds of terminal and industrial appliances.

- **X86 Processor core**
- Fully static 32-bit 5-stage pipeline, x86 processor fully PC compatible.
- Can access up to 4GB of external memory.
- 8Kbyte unified instruction and data cache with write back and write through capability.
- Parallel processing integral floating point unit, with automatic power down.
- Runs up to 133 MHz (X2).
- Fully static design for dynamic clock control.
- Low power and system management modes.
- Optimized design for 2.5V operation.

- **SDRAM Controller**
- 64-bit data bus.
- Up to 90MHz SDRAM clock speed.
- Integrated system memory, graphic frame memory and video frame memory.
- Supports 8MB up to 128 MB system memory.
- Supports 16-Mbit, 64-Mbit and 128-Mbit SDRAMs.
- Supports 8, 16, 32, 64, and 128 MB DIMMs.
- Supports buffered, non buffered, and registered DIMMs
- 4-line write buffers for CPU to DRAM and PCI to DRAM cycles.
- 4-line read prefetch buffers for PCI masters.
- Programmable latency
- Programmable timing for SDRAM parameters.
- Supports -8, -10, -12, -13, -15 memory parts
- Supports memory hole between 1MB and 8MB for PCI/ISA busses.
- 32-bit access, Autoprecharge & Power-down are not supported.

- **Enhanced 2D Graphics Controller**
- Supports pixel depths of 8, 16, 24 and 32 bit.
- Full BitBLT implementation for all 256 raster operations defined for Windows.
- Supports 4 transparent BLT modes - Bitmap Transparency, Pattern Transparency, Source Transparency and Destination Transparency.
- Hardware clipping
- Fast line draw engine with anti-aliasing.
- Supports 4-bit alpha blended font for anti-aliased text display.
- Complete double buffered registers for pipelined operation.
- 64-bit wide pipelined architecture running at 90 MHz. Hardware clipping

- **CRT Controller**
- Integrated 135MHz triple RAMDAC allowing for 1280 x 1024 x 75Hz display.
- 8-, 16-, 24-bit pixels.
- Interlaced or non-interlaced output.

- **Video Input port**
- Accepts video inputs in CCIR 601/656 mode.
- Optional 2:1 decimator
- Stores captured video in off setting area of the onboard frame buffer.
- HSYNC and B/T generation or lock onto external video timing source.

- **Video Pipeline**
- Two-tap interpolative horizontal filter.
- Two-tap interpolative vertical filter.
- Color space conversion (RGB to YUV and YUV to RGB).
- Programmable window size.
- Chroma and color keying for integrated video overlay.

- **TFT Interface**
- Programmable panel size up to 1024 by 1024 pixels.
- Support for VGA and SVGA active matrix TFT flat panels with 9, 12, 18-bit interface (1 pixel per clock).
- Support for XGA and SXGA active matrix TFT flat panels with 2 x 9-bit interface (2 pixels per clock).
- Programmable image positionning.
- Programmable blank space insertion in text mode.
- Programmable horizontal and vertical image expansion in graphic mode.
- One fully programmable PWM (Pulse Width Modulator) signals to adjust the flat panel brightness and contrast.
- Supports **PanelLink**™ high speed serial transmitter externally for high resolution panel interface.

- **PCI Controller**
- Compatible with PCI 2.1 specification.
- Integrated PCI arbitration interface. Up to 3 masters can connect directly. External logic allows for greater than 3 masters.
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- PCI clock is 1/2, 1/3 or 1/4 Host bus clock.

- **ISA master/slave**
- Generates the ISA clock from either 14.318MHz oscillator clock or PCI clock
- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back to back I/O cycles.
- Fast Gate A20 and Fast reset.
- Supports the single ROM that C, D, or E. blocks shares with F block BIOS ROM.
- Supports flash ROM.
- Supports ISA hidden refresh.
- Buffered DMA & ISA master cycles to reduce bandwidth utilization of the PCI and Host bus.

- **Local Bus interface**
- Multiplexed with ISA/DMA interface.
- Low latency asynchronous bus
- 16-bit data bus with word steering capability.
- Programmable timing (Host clock granularity)
- 4 Programmable Flash Chip Select.
- 8 Programmable I/O Chip Select.
- I/O device timing (setup & recovery time) programmable
- Supports 32-bit Flash burst.
- 2-level hardware key protection for Flash boot block protection.
- Supports 2 banks of 32MB flash devices with boot block shadowed to 0x000F0000.
- Reallocatable Memory space Windows

- **EIDE Interface**
- Supports PIO
- Transfer Rates to 22 MBytes/sec
- Supports up to 4 IDE devices
- Concurrent channel operation (PIO modes) - 4 x 32-Bit Buffer FIFOs per channel
- Support for PIO mode 3 & 4.
- Individual drive timing for all four IDE devices
- Supports both legacy & native IDE modes
- Supports hard drives larger than 528MB
- Support for CD-ROM and tape peripherals
- Backward compatibility with IDE (ATA-1).

- **Integrated Peripheral Controller**
- 2X8237/AT compatible 7-channel DMA controller.
- 2X8259/AT compatible interrupt Controller. 16 interrupt inputs - ISA and PCI.
- Three 8254 compatible Timer/Counters.
- Co-processor error support logic.
- Supports external RTC (Not in Local Bus Mode).

- **PCMCIA interface**
- Support one PCMCIA 68-pin standard PC Card Socket.
- Power Management support.
- Support PCMCIA/ATA specifications.
- Support I/O PC Card with pulse-mode interrupts.

- **USB Interface**
- USB 1.1 compatible.
- Open HCI 1.0 compliant.
- User configurable RootHub.
- Support for both LowSpeed and HighSpeed USB devices.
- No bi-directionnal or Tri-state busses.
- No level sensitive latches.
- System Management Interrupt pin support
- Hooks for legacy device support.

- **Keyboard interface**
- Fully PC/AT+ compatible

- **Mouse interface**
- Fully PS/2 compatible

- **Serial interface**
- 16550 compatible
- Programmable word length, stop bits, parity.
- 16-bit programmable baud rate generator.
- Interrupt generator.
- Loop-back mode.
- 8-bit scratch register.
- Two 16-bit FIFOs.
- Two DMA handshake lines.

Parallel port
- All IEEE Standard 1284 protocols supported: Compatibility, Nibble, Byte, EPP, and ECP modes.
- 16 bytes FIFO for ECP.

- **Power Management**
- Four power saving modes: On, Doze, Standby, Suspend.
- Programmable system activity detector
- Supports Intel & Cyrix SMM and APM.
- Supports STOPCLK.
- Supports IO trap & restart.
- Independent peripheral time-out timer to monitor hard disk, serial & parallel port.
- 128K SM_RAM address space from 0xA0000 to 0xB0000

- **JTAG**
- Boundary Scan compatible IEEE1149.1.
- Scan Chain control.
- Bypass register compatible IEEE1149.1.
- ID register compatible IEEE1149.1.
- RAM BIST control.

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1 GENERAL DESCRIPTION

At the heart of the STPC Atlas is an advanced processor block that includes a powerful x86 processor core along with a 64-bit SDRAM controller, advanced 64-bit accelerated graphics and video controller, a high speed PCI bus controller and industry standard PC chip set functions (Interrupt controller, DMA Controller, Interval timer and ISA bus).

The STPC Atlas has in addition, a TFT output, a Video Input, an EIDE controller, a Local Bus interface, PCMCIA and super I/O features including USB host hub.

1.1. ARCHITECTURE

The STPC Atlas makes use of a tightly coupled Unified Memory Architecture (UMA), where the same memory array is used for CPU main memory and graphics frame-buffer. This means a reduction in total system memory for system performances that are equal to that of a comparable frame buffer and system memory based system, and generally much better, due to the higher memory bandwidth allowed by attaching the graphics engine directly to the 64-bit processor host interface running at the speed of the processor bus rather than the traditional PCI bus.

The 64-bit wide memory array provides the system with an 800MB/s peak bandwidth. This allows for higher resolution screens and greater color depth. The processor bus runs at 133 MHz, further increasing “standard” bandwidth by at least a factor of two.

The ‘standard’ PC chipset functions (DMA, interrupt controller, timers, power management logic) are integrated together with the x86 processor core; additional low bandwidth functions such as communication ports are accessed by the STPC Atlas via an internal ISA bus.

The PCI bus is the main data communication link to the STPC Atlas chip. The STPC Atlas translates appropriate host bus I/O and Memory cycles onto the PCI bus. It also supports the generation of Configuration cycles on the PCI bus. The STPC Atlas, as a PCI bus agent (host bridge class), is compatible with PCI specification 2.1. The chip-set also implements the PCI mandatory header registers in Type 0 PCI configuration space for easy porting of PCI aware system BIOS. The device contains a PCI arbitration function for three external PCI devices.

Figure 1-1 describes this architecture.

1.2. GRAPHICS FEATURES

Graphics functions are controlled through the on-chip SVGA controller and the monitor display is produced through the 2D graphics display engine.

This Graphics Engine is tuned to work with the host CPU to provide a balanced graphics system with a low silicon area cost. It performs limited graphics drawing operations which include hardware acceleration of text, bitblts, transparent blts and fills. The results of these operations change the contents of the on-screen or off-screen frame buffer areas of SDRAM memory. The frame buffer can occupy a space up to 4 Mbytes anywhere in the physical main memory.

The maximum graphics resolution supported is 1280 x 1024 in 16 Million colours at 75 Hz refresh rate and is VGA and SVGA compatible. Horizontal timing fields are VGA compatible while the vertical fields are extended by one bit to accommodate above display resolution.

To generate the TFT output, the STPC Atlas extracts the digital video stream before the RAMDAC and reformats it to the TFT format. The height and width of the flat panel are programmable.

1.3. INTERFACES

An industry standard EIDE (ATA 2) controller is built in to the STPC Atlas and connected internally via the PCI bus.

The STPC Atlas integrates two USB ports. Universal Serial Bus (USB) is a general purpose communications interface for connecting peripherals to a PC. The USB Open Host Controller Interface (Open HCI) Specification, revision 1.1, supports speeds of up to 12 MB/s. USB is royalty free and is likely to replace low-speed legacy serial, parallel, keyboard, mouse and floppy drive interfaces. USB Revision 1.1 is fully supported under Microsoft Windows 98 and Windows 2000.

The STPC Atlas PCMCIA controller has been specifically designed to provide the interface with PCMCIA cards which contain additional memory or I/O

The power management control facilities include socket power control, insertion/removal capability, power saving with Windows inactivity, NCS controlled Chip Power Down, together with further controls for 3.3V suspend with Modem Ring Resume Detection.

The STPC Atlas implements a multi-function parallel port. The standard PC/AT compatible logical address assignments for LPT1, LPT2 and LPT3 are supported. It can be configured for any of the following three modes and supports the IEEE Standard 1284 parallel interface protocol standards, as follows:
- Compatibility Mode (Forward channel, standard)
- Nibble Mode (Reverse channel, PC compatible)
- Byte Mode (Reverse channel, PS/2 compatible)

The General Purpose Input/Output (GPIO) interface provides a 16-bit I/O facility, using 16 dedicated device pins. It is organised using two blocks of 8-bit Registers, one for lines 0 to 7, the other for lines 8 to 15.
Each GPIO port can be configured as an input or an output simply by programming the associated port direction control register. All GPIO ports are configured as inputs at reset, which also latches the input levels into the Strap Registers. The input states of the ports are thus recorded automatically at reset, and this can be used as a strap register anywhere in the system.

1.4. FEATURE MULTIPLEXING

The STPC Atlas BGA package has 516 balls. This however is not sufficient for all of the integrated functions available; some features therefore share the same balls and cannot thus be used at the same time. The STPC Atlas configuration is done by ‘strap options’. This is a set of pull-up or pull-down resistors on the memory data bus, checked on reset, which auto-configure the STPC Atlas.

There 3 multiplexed functions are the external ISA bus, the Local Bus and the PCMCIA interface.

1.5. POWER MANAGEMENT

The STPC Atlas core is compliant with the Advanced Power Management (APM) specification to provide a standard method by which the BIOS can control the power used by personal computers. The Power Management Unit (PMU) module controls the power consumption, providing a comprehensive set of features that controls the power usage and supports compliance with the United States Environmental Protection Agency's Energy Star Computer Program. The PMU provides the following hardware structures to assist the software in managing the system power consumption:

- System Activity Detection.

- 3 power-down timers detecting system inactivity:
  - Doze timer (short durations).
  - Stand-by timer (medium durations).
  - Suspend timer (long durations).

- House-keeping activity detection.

- House-keeping timer to cope with short bursts of house-keeping activity while dozing or in stand-by state.

- Peripheral activity detection.

- Peripheral timer detecting peripheral inactivity

- SUSP# modulation to adjust the system performance in various power down states of the system including full power-on state.

- Power control outputs to disable power from different planes of the board.

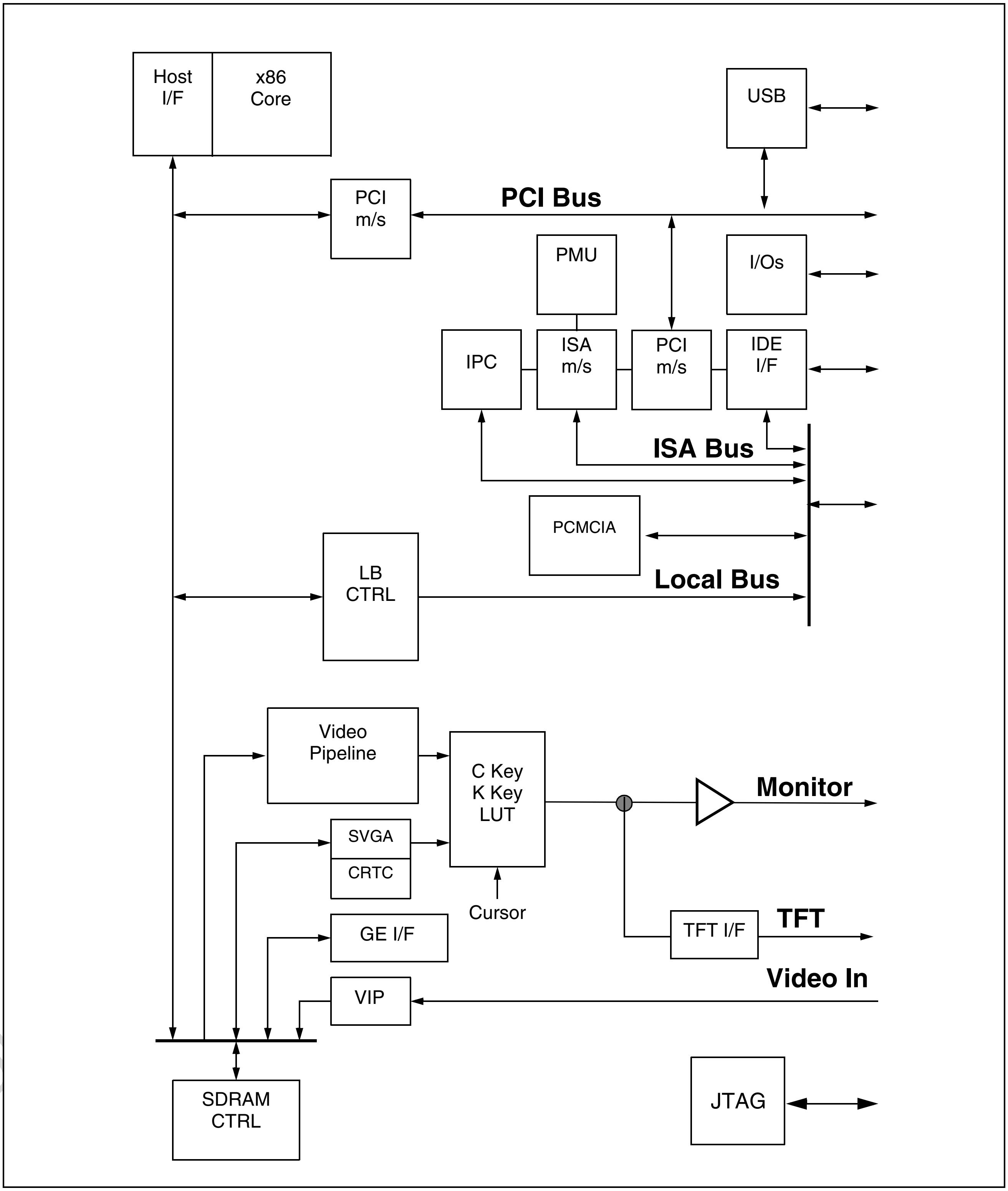
Lack of system activity for progressively longer periods of time is detected by the three power down timers. These timers can generate SMI interrupts to CPU so that the SMM software can put the system in decreasing states of power consumption. Alternatively, system activity in a power down state can generate an SMI interrupt to allow the software to bring the system back up to full power-on state. The chip-set supports up to three power down states described above; these correspond to decreasing levels of power savings.

Power down puts the STPC Atlas into suspend mode. The processor completes execution of the current instruction, any pending decoded instructions and associated bus cycles. During the suspend mode, internal clocks are stopped. Removing power-down, the processor resumes instruction fetching and begins execution in the instruction stream at the point it had stopped. Because of the static nature of the core, no internal data is lost.

1.6. JTAG

JTAG stands for Joint Test Action Group and is the popular name for IEEE Std. 1149.1, Standard Test Access Port and Boundary-Scan Architec-ture. This built-in circuitry is used to assist in the test, maintenance and support of functional circuit blocks. The circuitry includes a standard interface through which instructions and test data are communicated. A set of test features is defined, including a boundary-scan register so that a component is able to respond to a minimum set of test instructions.

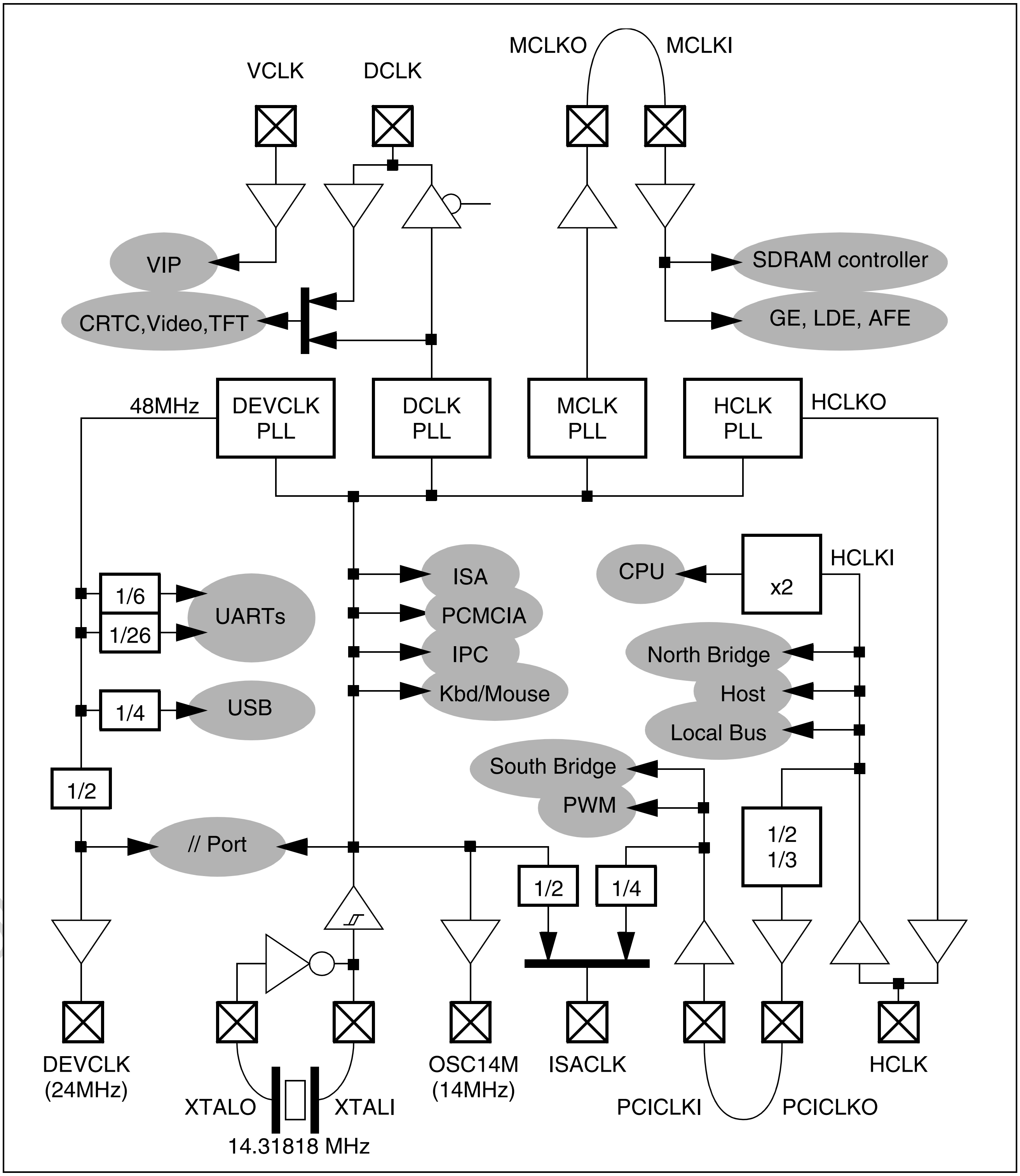
Figure 1-1. Functional description.



1.7. CLOCK TREE

The STPC Atlas integrates many features and generates all its clocks from a single 14MHz oscillator. This results in multiple clock domains as described in Figure 1-2.

Figure 1-2. STPC Atlas clock architecture



The speed of the PLLs is either fixed (DEVCLK), either programmable by strap option (HCLK) either programmable by software (DCLK, MCLK). When in synchronized mode, MCLK speed is fixed to HCLKO speed and HCLKI is generated from MCLKI.

Figure 1-3. Typical ISA-based Application.

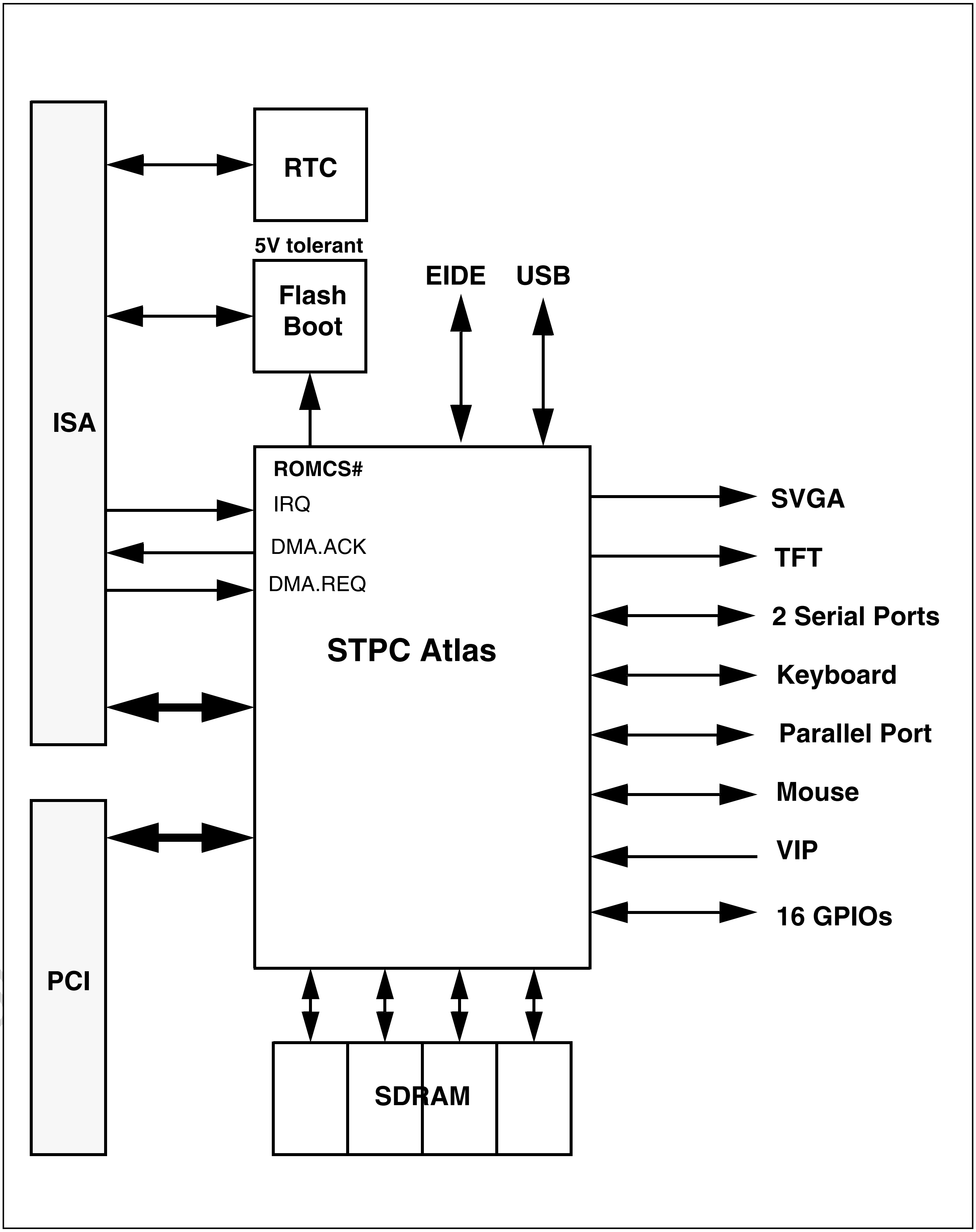


Figure 1-4. Typical PCMCIA-based Application.

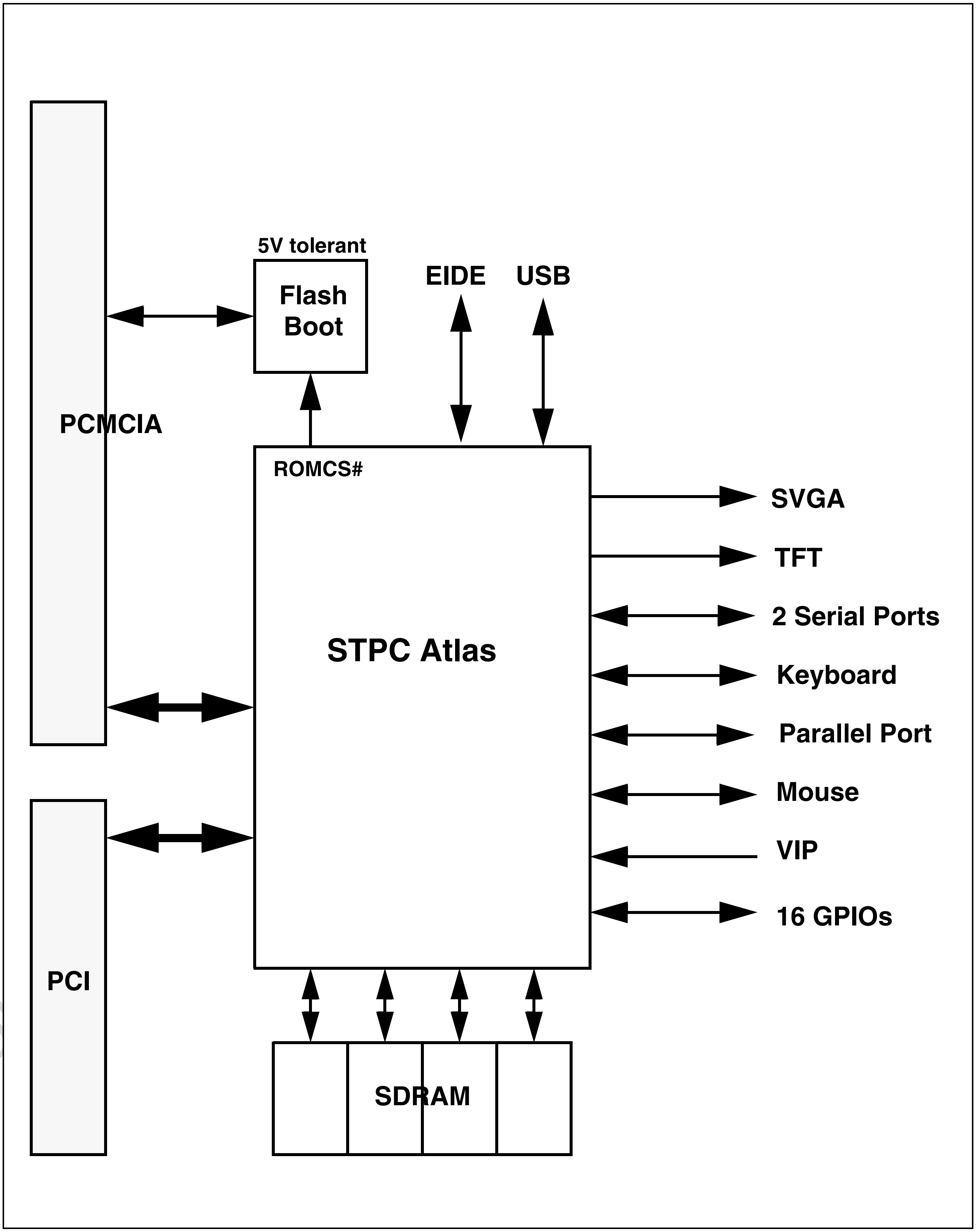
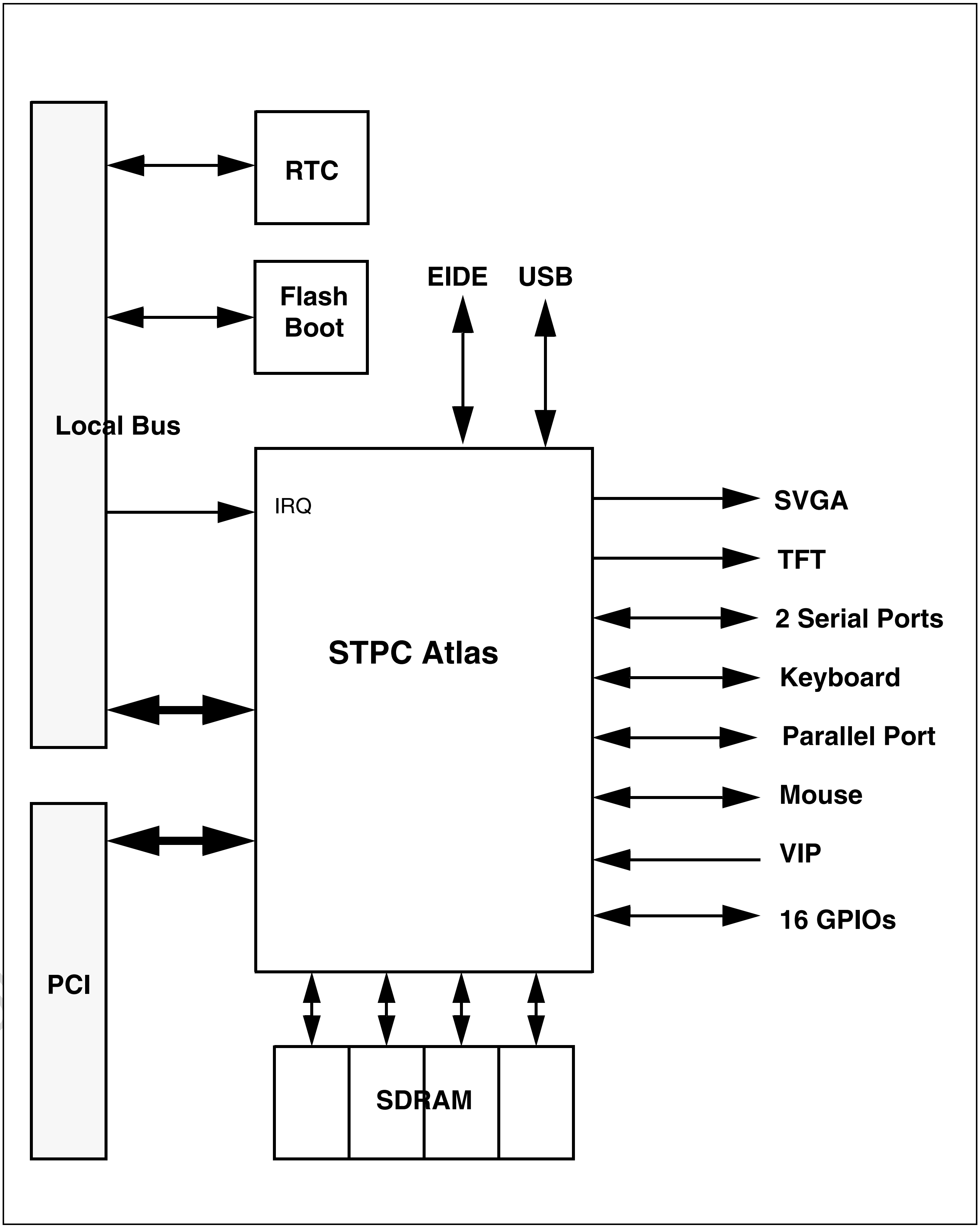


Figure 1-5. Typical Local-Bus-based Application.



2 PIN DESCRIPTION

2.1. INTRODUCTION

The STPC Atlas integrates most of the functionalities of the PC architecture. Therefore, many of the traditional interconnections between the host PC microprocessor and the peripheral devices are totally internal to the STPC Atlas. This offers improved performance due to the tight coupling of the processor core and it's peripherals. As a result many of the external pin connections are made directly to the on-chip peripheral functions.

Table 2-1 describes the physical implementation listing signal types and their functionalities. Table 2-2 provides a full pin listing and description.

Table 2-6 provides a full listing of the STPC Atlas package pin location physical connection. Please refer to the pin allocation drawing for reference.

Due to the number of pins available for the package, and the number of functional I/Os, some pins have several functions, selectable by strap option on Reset. Table 2-4 provides a summary of these pins and their functions.

Non multi-functional pins associated with a particular function are not available for use elsewhere when that function is disabled. For example, when in the ISA mode, the Local Bus is disabled totally and Local Bus pins are set to the tri-state (high-impedance) condition.

Table 2-1. Signal Description

Group name		Qty
Basic Clocks, Reset & Xtal (SYS)		19
SDRAM Controller (SDRAM)		95
PCI Controller		51
ISA Controller	80	100
Local Bus I/F	67	
PCMCIA Controller	62	
IDE Controller	34	
VGA Controller (VGA) / I^2C		10
Video Input Port		11
TFT output		24
USB Controller		6
Serial Interface		16
Keyboard/Mouse Controller		4
Parallel Port		18
GPIO Signals		16
JTAG Signals		5
Miscellaneous		5
Grounds		96
V_{DD} 3.3 V/2.5 V		36
Reserved		4
Total Pin Count		516

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
BASIC CLOCKS AND RESETS				
SYSRSTI#	I	SCHMITT_FT	System Reset / Power good	1
SYSRSTO#	O	BD8STRP_FT	Reset Output to System	1
XTALI	I	OSCI13B	14.31818 MHz Crystal Input External Oscillator Input	1
XTALO	O	OSCI13B	14.31818 MHz Crystal Output	1
PCI_CLKI	I	TLCHT_FT	33 MHz PCI Input Clock	1
PCI_CLKO	O	BT8TRP_TC	33 MHz PCI Output Clock	1
ISA_CLK, ISA_CLK2X	O	BT8TRP_TC	ISA Clock x1 and x2 Multiplexer Select Line for IPC	2
OSC14M	O	BD8STRP_FT	ISA bus synchronisation clock	1
HCLK	I/O	BD4STRP_FT	66 MHz Host Clock (Test pin)	1
DEV_CLK	O	BT8TRP_TC	24 MHz Peripheral Clock	1
DCLK	I/O	BD4STRP_FT	135 MHz Dot Clock	1
V_{DD}_xxx_PLL			2.5V Power Supply for PLL Clocks	7
MEMORY CONTROLLER				
MCLKI	I	TLCHT_TC	Memory Clock Input	1
MCLKO	O	BT8TRP_TC	Memory Clock Output	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
CS#[1:0]	O	BD8STRP_TC	DIMM Chip Select	2
CS#[3]/MA[12]/BA[1]	O	BD16STARUQP_TC	DIMM Chip Select Memory Address Bank Address	1
CS#[2]/MA[11]	O	BD16STARUQP_TC	DIMM Chip Select Memory Address	1
MA[10:0]	O	BD16STARUQP_TC	Memory Row & Column Address	11
BA[0]	O	BD16STARUQP_TC	Bank Address	1
RAS#[1:0]	O	BD16STARUQP_TC	Row Address Strobe	2
CAS#[1:0]	O	BD16STARUQP_TC	Column Address Strobe	2
MWE#	O	BD16STARUQP_TC	Write Enable	1
MD[0]	I/O	BD8STRUP_FT	Memory Data	1
MD[53:1]	I/O	BD8TRP_TC	Memory Data	53
MD[63:54]	I/O	BD8STRUP_FT	Memory Data	10
DQM[7:0]	O	BD8STRP_TC	Data Input/Ouput Mask	8
PCI INTERFACE				
AD[31:0]	I/O	BD8PCIARP_FT	Address / Data	32
CBE[3:0]	I/O	BD8PCIARP_FT	Bus Commands / Byte Enables	4
FRAME#	I/O	BD8PCIARP_FT	Cycle Frame	1
TRDY#	I/O	BD8PCIARP_FT	Target Ready	1
IRDY#	I/O	BD8PCIARP_FT	Initiator Ready	1
STOP#	I/O	BD8PCIARP_FT	Stop Transaction	1
DEVSEL#	I/O	BD8PCIARP_FT	Device Select	1
PAR	I/O	BD8PCIARP_FT	Parity Signal Transactions	1
PERR#	I/O	BD8PCIARP_FT	Parity Error	1
SERR#	O	BD8PCIARP_FT	System Error	1
LOCK#	I	TLCHT_FT	PCI Lock	1
PCI_REQ#[2:0]	I	BD8PCIARP_FT	PCI Request	3
PCI_GNT#[2:0]	O	BD8PCIARP_FT	PCI Grant	3
PCI_INT#[3:0]	I	BD4STRUP_FT	PCI Interrupt Request	4
ISA BUS INTERFACE				
LA[23:17]	O	BD8STRUP_FT	Unlatched Address Bus	7
SA[19:0]	O	BD8STRUP_FT	Latched Address Bus	20
SD[15:0]	I/O	BD8STRP_FT	Data Bus	16
IOCHRDY	I	BD8STRUP_FT	I/O Channel Ready	1
ALE	O	BD4STRP_FT	Address Latch Enable	1
BHE#	O	BD8STRUP_FT	System Bus High Enable	1
MEMR#, MEMW#	I/O	BD8STRUP_FT	Memory Read & Write	2
SMEMR#, SMEMW#	O	BD8STRP_FT	System Memory Read and Write	2
IOR#, IOW#	I/O	BD8STRUP_FT	I/O Read and Write	2
MASTER#	I	BD4STRUP_FT	Add On Card Owns Bus	1
MCS16#	I	BD4STRUP_FT	Memory Chip Select 16	1
IOCS16#	I	BD4STRUP_FT	I/O Chip Select 16	1
REF#	I	BD8STRP_FT	Refresh Cycle	1
AEN	O	BD8STRUP_FT	Address Enable	1
IOCHCK#	I	BD4STRUP_FT	I/O Channel Check (ISA)	1
RTCRW#	O	BD4STRP_FT	RTC Read / Write#	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
RTCDS#	O	BD4STRP_FT	RTC Data Strobe	1
RTCAS	O	BD4STRP_FT	RTC Address Strobe	1
RMRTCCS#	O	BD4STRP_FT	ROM / RTC Chip Select	1
GPIOCS#	I/O	BD4STRP_FT	General Purpose Chip Select	1
IRQ_MUX[3:0]	I	BD4STRP_FT	Multiplexed Interrupt Request	4
DACK_ENC[2:0]	O	BD4STRP_FT	DMA Acknowledge	3
DREQ_MUX[1:0]	I	BD4STRP_FT	Multiplexed DMA Request	2
TC	O	BD4STRP_FT	ISA Terminal Count	1
ISAOE#	I	BD4STRP_FT	ISA (0) / IDE (1) SELECTION	1
KBCS#	I/O	BD4STRP_FT	External Keyboard CHIP SELECT	1
ZWS#	I	BD4STRP_FT	ZERO WAIT STATE	1
PCMCIA INTERFACE				
RESET	O	BD8STRP_FT	Reset	1
A[23:0]	O	BD8STRUP_FT	Address Bus	24
D[15:0]	I/O	BD8STRP_FT	Data Bus	16
IORD#, IOWR#	O	BD8STRUP_FT	I/O Read and Write	2
WP / IOIS16#	I	BD4STRUP_FT	DMA Request // Write Protect I/O Size is 16 bit	1
BVD2, BVD1	I	BD4STRUP_FT	Battery Voltage Detect	2
READY# / IREQ#	I	BD4STRUP_FT	Busy / Ready# // Interrupt Request	1
WAIT#	I	BD8STRUP_FT	Wait	1
OE#	O	BD8STRUP_FT	Output Enable // DMA Terminal Count	1
WE#	O	BD4STRP_FT	Write Enable // DMA Terminal Count	1
REG#	O	BD4STRUP_FT	DMA Acknowledge // Register	1
CD2#, CD1#	I	BD4STRUP_FT	Card Detect	2
CE2#, CE1#	O	BD4STRP_FT	Card Enable	2
VCC5_EN	O	BD4STRP_FT	Power Switch control: 5 V power	1
VCC3_EN	O	BD8STRP_FT	Power Switch control: 3.3 V power	1
VPP_PGM	O	BD8STRP_FT	Power Switch control: Program power	1
VPP_VCC	O	BD4STRP_FT	Power Switch control: VCC power	1
GPI#	I	BD4STRP_FT	General Purpose Input	1
LOCAL BUS INTERFACE				
PA[24:20,15,9:8,3:0]	O	BD4STRP_FT	Address Bus [24:20], [15], [9:8], [3:0]	12
PA[19,11]	O	BD8STRP_FT	Address Bus [19], [11]	2
PA[18:16,14:12,7:4]	O	BD8STRUP_FT	Address Bus [18:16], [14:12], [7:4]	10
PA[10]	O	BD4STRUP_FT	Address Bus [10]	1
PD[15:0]	I/O	BD8STRP_FT	Data Bus [15:0]	16
PRD#	O	BD4STRUP_FT	Memory and I/O Read signal	1
PWR#	O	BD4STRUP_FT	Memory and I/O Write signal	1
PRDY	I	BD8STRP_FT	Data Ready	1
IOCS#[7:4]	O	BD4STRUP_FT	I/O Chip Select	4
IOCS#[3]	O	BD4STRP_FT	I/O Chip Select	1
IOCS#[2:0]	O	BD8STRUP_FT	I/O Chip Select	3
PBE#[1]	O	BD8STRP_FT	Upper Byte Enable (PD[15:8])	1
PBE#[0]	O	BD4STRUP_FT	Lower Byte Enable (PD[7:0])	1
FCS0#	O	BD4STRP_FT	Flash Bank 0 Chip Select	1
FCS1#	O	BT8TRP_TC	Flash Bank 1 Chip Select	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
FCS_0H#	O	BD8STRP_FT	Upper half Bank 0 Flash Chip Select	1
FCS_0L#	O	BD8STRP_FT	Lower half Bank 0 Flash Chip Select	1
FCS_1H#	O	BD8STRP_FT	Upper half Bank 1 Flash Chip Select	1
FCS_1L#	O	BD8STRP_FT	Lower half Bank 1 Flash Chip Select	1
IRQ_MUX[3:0][1]	I/O	BD4STRP_FT	Muxed Interrupt Lines	4
IDE CONTROLLER				
DD[15:12]	I/O	BD4STRP_FT	Data Bus	4
DD[11:0]	I/O	BD8STRUP_FT	Data Bus	12
DA[2:0]	O	BD8STRUP_FT	Address Bus	3
PCS1, PCS3	O	BD8STRUP_FT	Primary Chip Selects	2
SCS1, SCS3	O	BD8STRUP_FT	Secondary Chip Selects	2
DIORDY	O	BD8STRUP_FT	Data I/O Ready	1
PIRQ/SIRQ	I	BD4STRP_FT	Primary / Secondary Interrupt Request	2
PDRQ/SDRQ	I	BD4STRP_FT	Primary / Secondary DMA Request	2
PDACK#/SDACK#	O	BD8STRP_FT	Primary / Secondary DMA Acknowledge	2
PDIOR#/SDIOR#	O	BD8STRUP_FT	Primary / Secondary IO Read	2
PDIOW#/SDIOW#	O	BD8STRP_FT	Primary / Secondary IO Write	2
VGA CONTROLLER				
RED, GREEN, BLUE	O	VDDCO	Red, Green, Blue	3
VSYNC, HSYNC	I/O	BD4STRP_FT	Vertical & Horizontal Synchronisations	2
VREF_DAC	I	ANA	DAC Voltage reference	1
RSET	I	ANA	Resistor Set	1
COMP	I	ANA	Compensation	1
COL_SEL	O	BD4STRP_FT	Colour Select	1
I2C INTERFACE				
SCL / DDC[1]	I/O	BD4STRUP_FT	I²C Interface - Clock / VGA DDC[1]	1
SDA / DDC[0]	I/O	BD4STRUP_FT	I²C Interface - Data / VGA DDC[0]	1
TFT INTERFACE				
TFTR[5:2]	O	BD4STRP_TC	Red	4
TFTR[1:0]	O	BD4STRP_FT	Red	2
TFTG[5:2]	O	BD4STRP_TC	Green	4
,TFTG[1:0]	O	BD4STRP_FT	Green	2
TFTB[5:2]	O	BD4STRP_TC	Blue	4
TFTB[1:0]	O	BD4STRP_FT	Blue	2
TFTLINE	O	BD8STRP_TC	Horizontal Sync	1
TFTFRAME	O	BD4STRP_TC	Vertical Sync	1
TFTDE	O	BD4STRP_TC	Data Enable	1
TFTENVDD, TFTENVCC	O	BD4STRP_TC	Enable Vdd & Vcc of flat panel	2
TFTPWM	O	BD8STRP_TC	PWM back-light control	1
TFTDCLK	O	BT8TRP_TC	Dot clock for Flat Panel	1
VIDEO INPUT PORT				
VCLK	I/O	BD8STRP_FT	27-33 MHz Video Input Port Clock	1
VIN[7:0]	I	BD4STRP_FT	Video Input Data Bus	8
ODD_EVEN#	I/O	BD4STRP_FT	Video Input Odd/even Field	1
VCS	I/O	BD4STRP_FT	Video Input Horizontal Sync	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
USB INTERFACE				
OC	I	TLCHTU_TC	Over Current Detect	1
USBDPLS[0][1] USBDMNS[0][1]	I/O	USBDS_2V5	Universal Serial Bus Port 0	2
USBDPLS[1][1] USBDMNS[1][1]	I/O	USBDS_2V5	Universal Serial Bus Port 1	2
POWERON[1]	O	BT4CRP	USB power supply lines	1
SERIAL CONTROLLER				
CTS0#, CTS1#	I	TLCHT_FT	Clear to send, MSR[4] status bit	2
DCD0#, DCD1#	I	TLCHT_FT	Data Carrier detect, MSR[7] status bit	2
DSR0#, DSR1#	I	TLCHT_FT	Data set ready, MSR[5] status bit.	2
DTR0#, DTR1#	O	BD4STRP_TC	Data terminal ready, MSR[0] status bit	2
RI0#, RI1#	I	TLCHT_FT	Ring indicator, MSR[6] status bit	2
RTS0#, RTS1#	O	BD4STRP_TC	Request to send, MSR[1] status bit	2
RXD0, RXD1	I	TLCHT_FT	Receive data, Input Serial Input	2
TXD0, TXD1	O	BD4STRP_TC	Transmit data, Serial Output	2
KEYBOARD & MOUSE INTERFACE				
KBCLK	I/O	BD4STRP_TC	Keyboard Clock Line	1
KBDATA	I/O	BD4STRP_TC	Keyboard Data Line	1
MCLK	I/O	BD4STRP_TC	Mouse Clock Line	1
MDATA	I/O	BD4STRP_TC	Mouse Data Line	1
PARALLEL PORT				
PE	I	BD14STARP_FT	Paper End	1
SLCT	I	BD14STARP_FT	SELECT	1
BUSY#	I	BD14STARP_FT	BUSY	1
ERR#	I	BD14STARP_FT	ERROR	1
ACK#	I	BD14STARP_FT	Acknowledge	1
PDIR#	O	BD14STARP_FT	Parallel Device Direction	1
STROBE#	O	BD14STARP_FT	PCS / STROBE#	1
INIT#	O	BD14STARP_FT	INIT	1
AUTOFD#	O	BD14STARP_FT	Automatic Line Feed	1
SLCTIN#	O	BD14STARP_FT	SELECT IN	1
PPD[7:0]	I/O	BD14STARP_FT	Data Bus	8
GPIO SIGNALS				
GPIO[15:0]	I/O	BD4STRP_FT	General Purpose IOs	16
JTAG				
TCLK	I	TLCHT_FT	Test Clock	1
TRST	I	TLCHT_FT	Test Reset	1
TDI	I	TLCHTD_FT	Test Data Input	
TMS	I	TLCHT_FT	Test Mode Set	1
TDO	O	BT8TRP_TC	Test Data output	1
MISCELLANEOUS				
SCAN_ENABLE	I	TLCHTD_FT	Test Pin - Reserved	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-2. Definition of Signal Pins

Signal Name	Dir	Buffer Type[1]	Description	Qty
SPKRD	O	BD4STRP_FT	Speaker Device Output	1
Note[1]; See Table 2-3 for buffer type descriptions				

Table 2-3. Buffer Type Descriptions

Buffer	Description
ANA	Analog pad buffer
OSCI13B	Oscillator, 13 MHz, HCMOS
BT4CRP	LVTTL Output, 4 mA drive capability, Tri-State Control
BT8TRP_TC	LVTTL Output, 8 mA drive capability, Tri-State Control, Schmitt trigger
BD4STRP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, 5V tolerant
BD4STRUP_FT	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD4STRP_TC	LVTTL Bi-Directional, 4 mA drive capability, Schmitt trigger
BD8STRP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, 5V tolerant
BD8STRUP_FT	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger, Pull-Up, 5V tolerant
BD8STRP_TC	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger
BD8TRP_TC	LVTTL Bi-Directional, 8 mA drive capability, Schmitt trigger
BD8PCIARP_FT	LVTTL Bi-Directional, 8 mA drive capability, PCI compatible, 5V tolerant
BD14STARP_FT	LVTTL Bi-Directional, 14 mA drive capability, Schmitt trigger, IEEE1284 compliant, 5V tolerant
BD16STARUQP_TC	LVTTL Bi-Directional, 16 mA drive capability, Schmitt trigger
SCHMITT_FT	LVTTL Input, Schmitt trigger, 5V tolerant
TLCHT_FT	LVTTL Input, 5V tolerant
TLCHT_TC	LVTTL Input
TLCHTD_TC	LVTTL Input, Pull-Down
TLCHTU_TC	LVTTL Input, Pull-Up
USBDS_2V5	USB 1.1 compliant pad buffer
VDDCO	Analog output pad

2.2. SIGNAL DESCRIPTIONS

2.2.1. BASIC CLOCKS AND RESETS

SYSRSTI# *System Reset/Power good.* This input is low when the reset switch is depressed. Otherwise, it reflects the power supply's power good signal. PWGD is asynchronous to all clocks, and acts as a negative active reset. The reset circuit initiates a hard reset on the rising edge of PWGD.

Note that while Reset is being asserted, the signals on the device pins are in an unknown state.

SYSRSTO# *Reset Output to System.* This is the system reset signal and is used to reset the rest of the components (not on Host bus) in the system. The ISA bus reset is an externally inverted buffered version of this output and the PCI bus reset is an externally buffered version of this output.

XTALI *14.3 MHz Crystal Input*
XTALO *14.3 MHz Crystal Output.* These pins are provided for the connection of an external 14.318 MHz crystal to provide the reference clock for the internal frequency synthesizer, from which the HCLK and CLK24M signals are generated.

PCI_CLKI *33 MHz PCI Input Clock.* This signal must be connected to a clock generator and is usually connected to PCI_CLKO.

PCI_CLKO *33 MHz PCI Output Clock.* This is the master PCI bus clock output.

ISA_CLK *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces the Clock signal for the ISA bus. It is also used with ISA_CLK2X as the multiplexer control lines for the Interrupt Controller Interrupt input lines. This is a divided down version of the PCICLK or OSC14M.

ISA_CLKX2 *ISA Clock Output (also Multiplexer Select Line For IPC).* This pin produces a signal at twice the frequency of the ISA bus Clock signal. It is also used with ISA_CLK as the multiplexer control lines for the Interrupt Controller Interrupt input lines.

CLK14M *ISA bus synchronisation clock.* This is the buffered 14.318 MHz clock to the ISA bus.

HCLK *Host Clock.* This is the host clock. Its frequency can vary from 25 to 66 MHz. All host transactions and PCI transactions are synchronized to this clock. Host transactions executed by the DRAM controller are also driven by this clock.

DEV_CLK *24 MHz Peripheral Clock (floppy drive).* This 24 MHz signal is provided as a convenience for the system integration of a Floppy Disk driver function in an external chip. This clock signal is not available in Local Bus mode.

DCLK *135 MHz Dot Clock.* This is the dot clock, which drives graphics display cycles. Its frequency can be as high as 135 MHz, and it is required to have a worst case duty cycle of 60-40. For further details, refer to Section 3.1.4. bit 4.

2.2.2. MEMORY INTERFACE

MCLKI *Memory Clock Input.* This clock is driving the SDRAM controller, the graphics engine and display controller. This input should be a buffered version of the MCLKO signal with the track lengths between the buffer and the pin matched with the track lengths between the buffer and the Memory Banks.

MCLKO *Memory Clock Output.* This clock drives the Memory Banks on board and is generated from an internal PLL.

The STPC Atlas MClock signal can run up to 100MHz reliably, but PCB layout is so critical that the maximum guaranteed speed is 90MHz

CS#[1:0] *Chip Select* These signals are used to disable or enable device operation by masking or enabling all SDRAM inputs except MCLK, CKE, and DQM.

CS#[2]/MA[11] *Chip Select/Bank Address* This pin is CS#[2] in the case when 16-Mbit devices are used. For all other densities, it becomes MA[11].

CS#[3]/MA[12]/BA[1] *Chip Select/ Memory Address/ Bank Address* This pin is CS#[3] in the case when 16 Mbit devices are used. For all other densities, it becomes MA[12] when 2 internal banks devices are used and BA[1] when 4 internal bank devices are used.

MA[10:0] *Memory Address.* Multiplexed row and column address lines.

BA[0] *Bank Address.* Internal bank address line.

MD[63:0] *Memory Data.* This is the 64-bit memory data bus. This bus is also used as input at the rising edge of SYSRSTI# to latch in power-up configuration information into the ADPC strap registers.

RAS#[1:0] *Row Address Strobe.* There are two active-low row address strobe output signals. The RAS# signals drive the memory devices directly without any external buffering.

CAS#[1:0] *Column Address Strobe.* There are two active-low column address strobe output signals. The CAS# signals drive the memory devices directly without any external buffering.

MWE# *Write Enable.* Write enable specifies whether the memory access is a read (MWE# = H) or a write (MWE# = L). This single write enable controls all DRAMs. The MWE# signals drive the memory devices directly without any external buffering.

2.2.3. PCI INTERFACE

AD[31:0] *PCI Address/Data.* This is the 32-bit multiplexed address and data bus of the PCI. This bus is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions.

PBE[3:0]# *Bus Commands/Byte Enables.* These are the multiplexed command and Byte enable signals of the PCI bus. During the address phase they define the command and during the data phase they carry the Byte enable information. These pins are inputs when a PCI master other than the STPC Atlas owns the bus and outputs when the STPC Atlas owns the bus.

FRAME# *Cycle Frame.* This is the frame signal of the PCI bus. It is an input when a PCI master owns the bus and is an output when STPC Atlas owns the PCI bus.

TRDY# *Target Ready.* This is the target ready signal of the PCI bus. It is driven as an output when the STPC Atlas is the target of the current bus transaction. It is used as an input when STPC Atlas initiates a cycle on the PCI bus.

IRDY# *Initiator Ready.* This is the initiator ready signal of the PCI bus. It is used as an output when the STPC Atlas initiates a bus cycle on the PCI bus. It is used as an input during the PCI cycles targeted to the STPC Atlas to determine when the current PCI master is ready to complete the current transaction.

STOP# *Stop Transaction.* STOP# is used to implement the disconnect, retry and abort protocol of the PCI bus. It is used as an input for the bus cycles initiated by the STPC Atlas and is used as an output when a PCI master cycle is targeted to the STPC Atlas.

DEVSEL# *Device Select.* This signal is used as an input when the STPC Atlas initiates a bus cycle on the PCI bus to determine if a PCI slave device has decoded itself to be the target of the current transaction. It is asserted as an output either when the STPC Atlas is the target of the current PCI transaction or when no other device asserts DEVSEL# prior to the subtractive decode phase of the current PCI transaction.

PAR *Parity Signal Transactions.* This is the parity signal of the PCI bus. This signal is used to guarantee even parity across AD[31:0], CBE[3:0]#, and PAR. This signal is driven by the master during the address phase and data phase of write transactions. It is driven by the target during data phase of read transactions. (Its assertion is identical to that of the AD bus delayed by one PCI clock cycle)

PERR# *Parity Error*

SERR# *System Error.* This is the system error signal of the PCI bus. It may, if enabled, be asserted for one PCI clock cycle if target aborts a STPC Atlas initiated PCI transaction. Its assertion by either the STPC Atlas or by another PCI bus agent will trigger the assertion of NMI to the host CPU. This is an open drain output.

LOCK# *PCI Lock.* This is the lock signal of the PCI bus and is used to implement the exclusive bus operations when acting as a PCI target agent.

PCI_REQ#[2:0] *PCI Request.* These pins are the three external PCI master request pins. They indicates to the PCI arbiter that the external agents desire use of the bus.

PCI_GNT#[2:0] *PCI Grant.* These pins indicate that the PCI bus has been granted to the master requesting it on its PCI_REQ#.

PCI_INT#[3:0] *PCI Interrupt Request.* These are the PCI bus interrupt signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.

2.2.4. ISA BUS INTERFACE

LA[23:17] *Unlatched Address.* These unlatched ISA Bus pins address bits 23-17 on 16-bit devices. When the ISA bus is accessed by any cycle initiated from the PCI bus, these pins are in output mode. When an ISA bus master owns the bus, these pins are tristated.

SA[19:0] *Unlatched Address.* These are the 20 low bits of the system address bus of ISA. These pins are used as an input when an ISA bus master owns the bus and are outputs at all other times.

SD[15:0] *I/O Data Bus (ISA).* These are the external ISA databus pins.

IOCHRDY *IO Channel Ready.* IOCHRDY is the IO channel ready signal of the ISA bus and is driven as an output in response to an ISA master cycle targeted to the host bus or an internal register of the STPC Atlas. The STPC Atlas monitors this signal as an input when performing an ISA cycle on behalf of the host CPU, DMA master or refresh. ISA masters which do not monitor IOCHRDY are not guaranteed to work with the STPC Atlas since the access to the system memory can be considerably delayed due to CRT refresh or a write back cycle.

ALE *Address Latch Enable.* This is the address latch enable output of the ISA bus and is asserted by the STPC Atlas to indicate that LA23-17, SA19-0, AEN and SBHE# signals are valid. The ALE is driven high during refresh, DMA master or an ISA master cycles by the STPC Atlas.
ALE is driven low after reset.

BHE# *System Bus High Enable.* This signal, when asserted, indicates that a data Byte is being transferred on SD15-8 lines. It is used as an input when an ISA master owns the bus and is an output at all other times.

MEMR# *Memory Read.* This is the memory read command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.
The MEMR# signal is active during refresh.

MEMW# *Memory Write.* This is the memory write command signal of the ISA bus. It is used as an input when an ISA master owns the bus and is an output at all other times.

SMEMR# *System Memory Read.* The STPC Atlas generates SMEMR# signal of the ISA bus only when the address is below one MByte or the cycle is a refresh cycle.

SMEMW# *System Memory Write.* The STPC Atlas generates SMEMW# signal of the ISA bus only when the address is below one MByte.

IOR# *I/O Read.* This is the IO read command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

IOW# *I/O Write.* This is the IO write command signal of the ISA bus. It is an input when an ISA master owns the bus and is an output at all other times.

MASTER# *Add On Card Owns Bus.* This signal is active when an ISA device has been granted bus ownership.

MCS16# *Memory Chip Select16.* This is the decode of LA23-17 address pins of the ISA address bus without any qualification of the command signal lines. MCS16# is always an input. The STPC Atlas ignores this signal during IO and refresh cycles.

IOCS16# *IO Chip Select16.* This signal is the decode of SA15-0 address pins of the ISA address bus without any qualification of the command signals. The STPC Atlas does not drive IOCS16# (similar to PC-AT design). An ISA master access to an internal register of the STPC Atlas is executed as an extended 8-bit IO cycle.

REF# *Refresh Cycle.* This is the refresh command signal of the ISA bus. It is driven as an output when the STPC Atlas performs a refresh cycle on the ISA bus. It is used as an input when an ISA master owns the bus and is used to trigger a refresh cycle.
The STPC Atlas performs a pseudo hidden refresh. It requests the host bus for two host clocks to drive the refresh address and capture it in external buffers. The host bus is then relinquished while the refresh cycle continues on the ISA bus.

AEN *Address Enable.* Address Enable is enabled when the DMA controller is the bus owner to indicate that a DMA transfer will occur. The enabling of the signal indicates to IO devices to ignore the IOR#/IOW# signal during DMA transfers.

IOCHCK# *IO Channel Check.* IO Channel Check is enabled by any ISA device to signal an error condition that can not be corrected. NMI signal becomes active upon seeing IOCHCK# active if the corresponding bit in Port B is enabled.

GPIOCS# *I/O General Purpose Chip Select 1.* This output signal is used by the external latch on ISA bus to latch the data on the SD[7:0] bus. The latch can be use by PMU unit to control the external peripheral devices to power down or any other desired function.

RTCRW# *Real Time Clock RW#.* This pin is used as RTCRW#. This signal is asserted for any I/O write to port 71h.

RTCDS# *Real Time Clock DS*. This pin is used as RTCDS#. This signal is asserted for any I/O read to port 71h. Its polarity complies with the DS pin of the MT48T86 RTC device when configured with Intel timings.

RTCAS *Real time clock address strobe.* This signal is asserted for any I/O write to port 70h.

RMRTCCS# *ROM/Real Time clock chip select.* This pin is a multi-function pin. This signal is asserted if a ROM access is decoded during a memory cycle. It should be combined with MEMR# or MEMW# signals to properly access the ROM. During an IO cycle, this signal is asserted if access to the Real Time Clock (RTC) is decoded. It should be combined with IOR# or IOW# signals to properly access the real time clock.

IRQ_MUX[3:0] *Multiplexed Interrupt Request.* These are the ISA bus interrupt signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.
Note that IRQ8B, which by convention is connected to the RTC, is inverted before being sent to the interrupt controller, so that it may be connected directly to the IRQ# pin of the RTC.

ISAOE# *Bidirectional OE Control.* This signal controls the OE signal of the external transceiver that connects the IDE DD bus and ISA SA bus.

KBCS# *Keyboard Chip Select.* This signal is asserted if a keyboard access is decoded during a I/O cycle.

ZWS# *Zero Wait State.* This signal, when asserted by addressed device, indicates that current cycle can be shortened.

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Atlas before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Atlas using ISACLK and ISACLKX2 as the input selection strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the Byte count expires.

2.2.5. PCMCIA INTERFACE

RESET *Card Reset.* This output forces a hard reset to a PC Card.

A[25:0] *Address Bus.* These are the 25 low bits of the system address bus of the PCMCIA bus. These pins are used as an input when an PCMCIA bus owns the bus and are outputs at all other times.

D[15:0] *I/O Data Bus (PCMCIA).* These are the external PCMCIA databus pins.

IORD# *I/O Read.* This output is used with REG# to gate I/O read data from the PC Card, (only when REG# is asserted).

IOWR# *I/O Write.* This output is used with REG# to gate I/O write data from the PC Card, (only when REG# is asserted).

WP *Write Protect.* This input indicates the status of the Write Protect switch (if fitted) on memory PC Cards (asserted when the switch is set to write protect).

BVD1, BVD2 *Battery Voltage Detect.* These inputs will be generated by memory PC Cards that include batteries and are an indication of the condition of the batteries. BVD1 and BVD2 are kept asserted high when the battery is in good condition.

READY#/BUSY#/IREQ# *Ready/busy/Interrupt request.* This input is driven low by memory PC Cards to signal that their circuits are busy processing a previous write command.

WAIT# *Bus Cycle Wait.* This input is driven by the PC Card to delay completion of the memory or I/O cycle in progress.

OE# *Output Enable.* OE# is an active low output which is driven to the PC Card to gate Memory Read data from memory PC Cards.

WE#/PRGM# *Write Enable.* This output is used by the host for gating Memory Write data. WE# is also used for memory PC Cards that have programmable memory.

REG# *Attribute Memory Select.* This output is inactive (high) for all normal accesses to the Main Memory of the PC Card. I/O PC Cards will only respond to IORD# or IOWR# when REG# is active (low). Also see Section 2.2.7.

CD1#, CD2# *Card Detect.* These inputs provide for the detection of correct card insertion. CD#1 and CD#2 are positioned at opposite ends of the connector to assist in the detection process. These inputs are internally grounded on the PC Card therefore they will be forced low whenever a card is inserted in a socket.

CE1#, CE2# *Card Enable*. These are active low output signals provided from the PCIC. CE#1 enables even Bytes, CE#2 odd Bytes.

ENABLE# *Enable.* This output is used to activate/select a PC Card socket. ENABLE# controls the external address buffer logic.C card has been detected (CD#1 and CD#2 = '0').

ENIF# *ENIF*. This output is used to activate/select a PC Card socket.

EXT_DIR *EXternal Transceiver Direction Control.* This output is high during a read and low during a write. The default power up condition is write (low). Used for both Low and High Bytes of the Data Bus.

VCC_EN#, VPP1_EN0, VPP1_EN1, VPP 2_EN0, VPP2_EN1 *Power Control.* Five output signals used to control voltages (VPP1, VPP2 and VCC) to a PC Card socket.

GPI# *General Purpose Input. This signal is hardwired to 1.*

2.2.6. LOCAL BUS

PA[24:0] *Address Bus Output.*

PD[15:0] *Data Bus.* This is the 16-bit data bus. D[7:0] is the LSB and PD[15:8] is the MSB.

PRD#[1:0] *Read Control output*. These are memory and I/O Read signals. PRD0# is used to read the LSB and PRD1# to read the MSB.

PWR#[1:0] *Write Control output.* These are memory and I/O Write signals. PWR0# is used to write the LSB and PWR1# to write the MSB.

PRDY *Data Ready input.* This signal is used to create wait states on the bus. When high, it completes the current cycle.

FCS#[1:0] *Two Flash Memory Chip Select outputs.* These are the Programmable Chip Select signals for Flash memory.

IOCS#[7:0] *I/O Chip Select output.* These are the Programmable Chip Select signals for up to 4 external I/O devices.

PBE#[1:0] *Byte Enable.* These are the Byte enables that identifies on which databus the date is valid. PBE#[0] corresponds to PD[7:0] and PBE#[1] corresponds to PD[15:8]. These are normally used when 8 bit transfers are transfered across the 16 bit bus.

IRQ_MUX#[3:0] *Multiplexed Interrupt Lines.*

2.2.7. IPC

DACK_ENC[2:0] *DMA Acknowledge.* These are the ISA bus DMA acknowledge signals. They are encoded by the STPC Industrial before output and should be decoded externally using ISACLK and ISACLKX2 as the control strobes.

DREQ_MUX[1:0] *ISA Bus Multiplexed DMA Request.* These are the ISA bus DMA request signals. They are to be encoded before connection to the STPC Industrial using ISACLK and ISACLKX2 as the input selection strobes.

TC *ISA Terminal Count.* This is the terminal count output of the DMA controller and is connected to the TC line of the ISA bus. It is asserted during the last DMA transfer, when the Byte count expires.

2.2.8. IDE INTERFACE

DA[2:0] *Address.* These signals are connected to DA[2:0] of IDE devices directly or through a buffer. If the toggling of signals are to be masked during ISA bus cycles, they can be externally ORed with ISAOE# before being connected to the IDE devices.

DD[15:0] *Databus.* When the IDE bus is active, they serve as IDE signals DD[11:0]. IDE devices are connected to SA[19:8] directly and ISA bus is connected to these pins through two LS245 transceivers.

PCS1, PCS3, SCS1, SCS3 *Primary & Secondary Chip Selects.* These signals are used as the active high primary and secondary master & slave IDE chip select signals. These signals must be externally NANDed with the ISAOE# signal before driving the IDE devices to guarantee it is active only when ISA bus is idle. In Local Bus mode, they just need to be inverted.

DIORDY *Busy/Ready.* This pin serves as IDE signal DIORDY.

PIRQ *Primary Interrupt Request.*
SIRQ *Secondary Interrupt Request.*
Interrupt request from IDE channels.

PDRQ *Primary DMA Request.*
SDRQ *Secondary DMA Request.*
DMA request from IDE channels.

PDACK# *Primary DMA Acknowledge.*
SDACK# *Secondary DMA Acknowledge.*
DMA acknowledge to IDE channels.

PDIOR#, PDIOW# *Primary I/O Read & Write.*
SDIOR#, SDIOW# *Secondary I/O Read & Write*.
Primary & Secondary channel read & write.

2.2.9. MONITOR INTERFACE

RED, GREEN, BLUE *RGB Video Outputs.* These are the 3 analog colour outputs from the RAMDACs. These signals are sensitive to interference, therefore they need to be properly shielded.

VSYNC *Vertical Synchronisation Pulse.* This is the vertical synchronization signal from the VGA controller.

HSYNC *Horizontal Synchronisation Pulse.* This is the horizontal synchronization signal from the VGA controller.

VREF_DAC *DAC Voltage reference.* This pin is an input driving the digital to analog converters. This allows an external voltage reference source to be used.

RSET *Resistor Current Set.* This is the reference current input to the RAMDAC. Used to set the full-scale output of the RAMDAC.

COMP *Compensation.* This is the RAMDAC compensation pin. Normally, an external capacitor (typically 10nF) is connected between this pin and V_{DD} to damp oscillations.

DDC[1:0] *Direct Data Channel Serial Link.* These bidirectional pins are connected to CRTC register 3Fh to implement DDC capabilities. They conform to I^2C electrical specifications, they have open-collector output drivers which are internally connected to V_{DD} through pull-up resistors.

They can instead be used for accessing I^2C devices on board. DDC1 and DDC0 correspond to SCL and SDA respectively.

2.2.10. VIDEO INTERFACE

VCLK *Pixel Clock Input.*This signal is used to synchronise data being transferred from an external video device to either the frame buffer, or alternatively out the TV output in bypass mode. This pin can be sourced from STPC if no external VCLK is detected, or can be input from an external video clock source.

VIN[7:0] *YUV Video Data Input ITU-R 601 or 656.* Time multiplexed 4:2:2 luminance and chrominance data as defined in ITU-R Rec601-2 and Rec656 (except for TTL input levels). This bus typically carries a stream of Cb,Y,Cr,Y digital video at VCLK frequency, clocked on the rising edge (by default) of VCLK.

VCS *Line synchronisation Input.* This is the horizontal synchronisation of the incomming CCIR601 video.
The signal is synchronous to rising edge of VCLK.

ODD_EVEN *Frame Synchronisation Output.* This is the vertical synchronisation of the incomming CCIR601 video.
The signal is synchronous to rising edge of VCLK.
The default polarity for this pin is:

- odd (not-top) field: LOW level
- even (bottom) field: HIGH level

2.2.11. TFT INTERFACE SIGNALS

The TFT (Thin Film Transistor) interface converts signals from the CRT controller into control signals for an external TFT Flat Panel. The signals are listed below.

TFTFRAME, *Vertical Sync. pulse Output.*

TFTLINE, *Horizontal Sync. Pulse Output.*

TFTDE, *Data Enable.*

TFTR5-0, *Red Output.*

TFTG5-0, *Green Output.*

TFTB5-0, *Blue Output.*

TFTENVDD, *Enable VDD of Flat Panel.*

TFTENVCC, *Enable VCC of Flat Panel.*

PWM *PWM Back-Light Control.* This PWM is clocked by the PCI clock.

TFTDCLK, *Dot clock for the Flat Panel.*

2.2.12. USB INTERFACE

OC *OVER CURRENT DETECT* This signal is used to monitor the status of the USB power supply lines of both devices. USB port are disabled when OC signal is asserted.

USBDPL0, USBDMNS0 *UNIVERSAL SERIAL BUS DATA 0* This signal pair comprises the differential data signal for USB port 0.

USBDPL1, USBDMNS1 *UNIVERSAL SERIAL BUS PORT 1* This signal pair comprises the differential data signal for USB port 1.

POWERON *USB power supply lines*

2.2.13. SERIAL INTERFACE

RXD0, RXD1 *Serial Input.* Data is clocked in using RCLK/16.

TXD0, TXD1 *Serial Output.* Data is clocked out using TCLK/16 (TCLK=BAUD#).

DCD0#, DCD1# *Input Data carrier detect.*

RI0#, RI1# *Input Ring indicator.*

DSR0#, DSR1# *Input Data set ready.*

CTS0#, CTS1# *Input Clear to send.*

RTS0#, RTS1# *Output Request to send.*

DTR0#, DTR1# *Output Data terminal read.*

2.2.14. KEYBOARD/MOUSE INTERFACE

KBCLK, *Keyboard Clock line.* Keyboard data is latched by the controller on each negative clock edge produced on this pin. The keyboard can be disabled by pulling this pin low by software control.

KBDATA, *Keyboard Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to KBCLK.

MCLK, *Mouse Clock line.* Mouse data is latched by the controller on each negative clock edge produced on this pin. The mouse can be disabled by pulling this pin low by software control.

MDATA, *Mouse Data Line.* 11-bits of data are shifted serially through this line when data is being transferred. Data is synchronised to MCLK.

2.2.15. PARALLEL PORT

PE *Paper End.* Input status signal from printer.

SLCT *Printer Select.* Printer selected input.

BUSY# *Printer Busy*.
Input status signal from printer.

ERR# *Error*. Input status signal from printer.

ACK# *Acknowledge.*
Input status signal from printer.

PDDIR# *Parallel Device Direction.*
Bidirectional control line output.

STROBE# *PCS/Strobe#.*
Data transfer strobe line to printer.

INIT# *Initialize Printer.* This output sends an initialize command to the connected printer.

AUTOFD# *Automatic Line feed.* This output sends a command to the connected printer to automatically generate line feed on received carriage returns.

SLCTIN# *Select In.* Printer select output.

PPD[7-0] *Parallel Port Data Lines* Data transfer lines to printer. Bidirectional depending on modes.

2.2.16. MISCELLANEOUS

SPKRD *Speaker Drive.* This is the output to the speaker and is the AND of the counter 2 output with bit 1 of Port 61h and drives an external speaker driver. This output should be connected to a 7407 type high voltage driver.

SCAN_ENABLE *Reserved*. This pin is reserved for Test and Miscellaneous functions. It has to be set to ‘0’ or connected to ground in normal operation.

2.2.17. **COL_SEL** *Colour Select. JTAG INTERFACE*

TCLK *Test clock*

TDI *Test data input*

TMS *Test mode input*

TDO *Test data output*

TRST Test reset input

2.3 SIGNAL DETAIL

The muxing between ISA, LOCAL BUS and PCMCIA is performed by external strap options.

The resulting interface is then dynamically muxed with the IDE Interface.

Table 2-4. Multiplexed Signals (on the same pin)

IDE Pin Name	ISA Pin Name	PCMCIA Pin Names	Local Bus Pin Name
DIORDY	IOCHRDY	-	
DA[2]	LA[19]	*= 0*	
DA[1:0]	LA[18:17]	A[25:24]	
SCS3,SCS1	LA[23:22]	A[23:22]	
PCS3,PCS1	LA[21:20]	A[21:20]	
DD[15]	RMRTCCS#	ROMCS#	
DD[14]	KBCS#	*Hi-Z*	
DD[13:12]	RTCRW#, RTCDS#	*Hi-Z*	
DD[11:0]	SA[19:8]	A[19:8]	

Table 2-4. Multiplexed Signals (on the same pin)

IDE Pin Name	ISA Pin Name	PCMCIA Pin Names	Local Bus Pin Name
	SD[15:0]	D[15:0]	PD[15:0]
	RTCAS	*= 0*	FCS0#
	DEV_CLK	DEV_CLK	FCS1#
	SA[3]	A[3]	PRDY
	SA[2:0]	A[2:0]	IOCS#[2:0]
	SMEMW#	VPP_PGM	PBE#[1]
	IOCS16#	WP/IOIS16#	PBE#[0]
	MASTER#	BVD1	PRD#
	MCS16#	*= 0*	PWR#
	DACK_ENC [2:0]	*= 0x04*	PA[2:0]
	TC	*= 0*	PA[3]
	SA[7:4]	A[7:4]	PA[7:4]
	ZWS#	GPI#	PA[8]
	GPIOCS#	VCC5_EN	PA[9]
	IOCHCK#	BVD2	PA[10]
	REF#	RESET	PA[11]
	IOW#	IOWR#	PA[12]
	IOR#	IORD#	PA[13]
	MEMR#	*= 0*	PA[14]
	ALE	*= 0*	PA[15]
	AEN	WAIT#	PA[16]
	BHE#	OE#	PA[17]
	MEMW#	*= 0*	PA[18]
	SMEMR#	VCC3_EN	PA[19]
	DREQ_MUX#[1:0]	CE2#, CE1#	PA[21:20]
	Hi-Z	*Hi-Z*	PA[22]
	Hi-Z	VPP_VCC	PA[23]
	Hi-Z	WE#	PA[24]
	Hi-Z	REG#	IOCS#[7]
	Hi-Z	READY#	IOCS#[6]
	Hi-Z	CD1#, CD2#	IOCS#[5], IOCS#[4]
ISAOE# = 1	ISAOE# = 0	ISAOE# = 0	IOCS#[3]

Table 2-5. Signal value on Reset

Signal Name	SYSRSTI# active	SYSRSTI# inactive SYSRSTO# active	release of SYSRSTO#
BASIC CLOCKS AND RESETS			
XTALO	14MHz		
ISA_CLK	Low	7MHz	
ISA_CLK2X	14MHz		
OSC14M	14MHz		
DEV_CLK	24MHz		
HCLK	Oscillating at the speed defined by the strap options.		
PCI_CLKO	HCLK divided by 2 or 3, depending on the strap options.		
DCLK	17MHz		
MEMORY CONTROLLER			
MCLKO	66MHz if asynchonous mode, HCLK speed if synchronized mode.		
CS#[3:1]	High		

Table 2-5. Signal value on Reset

Signal Name	SYSRSTI# active	SYSRSTI# inactive SYSRSTO# active	release of SYSRSTO#
CS#[0]	High		SDRAM init sequence: Write Cycles
MA[10:0], BA[0]	0x00		
RAS#[1:0], CAS#[1:0]	High		
MWE#, DQM[7:0]	High		
MD[63:0]	Input		
PCI INTERFACE			
AD[31:0]	0x0000		First prefetch cycles when not in Local Bus mode.
CBE[3:0], PAR	Low		
FRAME#, TRDY#, IRDY#	Input		
STOP#, DEVSEL#	Input		
PERR#, SERR#	Input		
PCI_GNT#[2:0]	High		
ISA BUS INTERFACE			
ISAOE#	High		Low
RMRTCCS#	Hi-Z		First prefetch cycles when in ISA or PCMCIA mode. Address start is 0xFFFFF0
LA[23:17]	Unknown	0x00	
SA[19:0]	0xFFFXX	0xFFF03	
SD[15:0]	Unknown	0xFF	
BHE#, MEMR#	Unknown	High	
MEMW#, SMEMR#, SMEMW#, IOR#, IOW#	Unknown	High	
REF#	Unknown	High	
ALE, AEN	Low		
DACK_ENC[2:0]	Input		0x04
TC	Input		Low
GPIOCS#	Hi-Z		High
RTCDS#, RTCRW#, KBCS#	Hi-Z		
RTCAS	Unknown	Low	
PCMCIA INTERFACE			
RESET	Unknown	High	
A[23:0]	Unknown	0x00	First prefetch cycles using RMRTCCS#
D[15:0]	Unknown	0xFF	
IORD#, IOWR#, OE#	Unknown	High	
WE#, REG#	High		
CE2#, CE1#, VCC5_EN, VCC3_EN	High		
VPP_PGM, VPP_VCC	Low		
LOCAL BUS INTERFACE			
PA[24:0]	Unknown		First prefetch cycles
PD[15:0]	Unknown	0xFF	
PRD#	Unknown	High	
PBE#[1:0], FCS0#, FCS_0H#	High		
FCS_0L#, FCS1#, FCS_1H#, FCS_1L#	High		
PWR#, IOCS#[7:0]	High		
IDE CONTROLLER			
DD[15:0]	0xFF		
DA[2:0]	Unknown	Low	
PCS1, PCS3, SCS1, SCS3	Unknown	Low	
PDACK#, SDACK#	High		
PDIOR#, PDIOW#, SDIOR#, SDIOW#	High		
VGA CONTROLLER			
RED, GREEN, BLUE	Black		
VSYNC, HSYNC	Low		

Table 2-5. Signal value on Reset

Signal Name	SYSRSTI# active	SYSRSTI# inactive SYSRSTO# active	release of SYSRSTO#
COL_SEL	Unknown		
I2C INTERFACE			
SCL / DDC[1]	Input		
SDA / DDC[0]	Input		
TFT INTERFACE			
TFT[R,G,B][5:0]	0x00,0x00,0x00		
TFTLINE, TFTFRAME	Low		
TFTDE, TFTENVDD, TFTENVCC, TFTPWM	Low		
TFTDCLK	Oscillating at DCLK speed		
USB INTERFACE			
USBDPLS[1:0][1]	Low		
USBDMNS[1:0][1]	High		
POWERON[1]	Unknown	Low	
SERIAL CONTROLLER			
TXD0, RTS0#, DTR0#	High		
TXD1, RTS1#, DTR1#	High		
KEYBOARD & MOUSE INTERFACE			
KBCLK, MCLK	Low		
KBDATA, MDATA	Input		
PARALLEL PORT			
PDIR#, INIT#	Low		
STROBE#, AUTOFD#	High		
SLCTIN#	Unknown	Low	
PPD[7:0]	Unknown	0x00	
GPIO SIGNALS			
GPIO[15:0]	High		
JTAG			
TDO	High		
MISCELLANEOUS			
SPKRD	Low		

Table 2-6. Pinout

Pin#	Pin Name
D15	SYSRSETI#
C15	SYSRSETO#
AF21	XTALI
AF22	XTALO
AF23	PCI_CLKI
AF24	PCI_CLKO
E15	ISA_CLK
A16	ISA_CLK2X
AB18	OSC14M
AB24	HCLK
AB25	DEV_CLK[1]/FCS1#
AC18	DCLK
AF20	MCLKI
AF19	MCLKO
U5	MA[0]
V1	MA[1]
V2	MA[2]
V3	MA[3]
V4	MA[4]
V5	MA[5]
W1	MA[6]
W2	MA[7]
W3	MA[8]
W5	MA[9]
Y1	MA[10]
Y2	BA[0]
U3	RAS#[0]
U4	RAS#[1]
R5	CAS#[0]
T1	CAS#[1]
R4	MWE#
J4	MD[0]
J2	MD[1]
K5	MD[2]
K3	MD[3]
K1	MD[4]
L4	MD[5]
L2	MD[6]
M5	MD[7]
M3	MD[8]
M1	MD[9]
N4	MD[10]
N2	MD[11]
P1	MD[12]
P3	MD[13]
P5	MD[14]
R2	MD[15]
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
AA4	MD[16]
AB1	MD[17]
AB3	MD[18]
AC1	MD[19]
AC3	MD[20]
AD2	MD[21]
AF3	MD[22]
AE4	MD[23]
AF4	MD[24]
AD5	MD[25]
AF5	MD[26]
AC6	MD[27]
AF6	MD[28]
AC7	MD[29]
AE7	MD[30]
AB8	MD[31]
J3	MD[32]
J1	MD[33]
K4	MD[34]
K2	MD[35]
L5	MD[36]
L3	MD[37]
L1	MD[38]
M4	MD[39]
M2	MD[40]
N5	MD[41]
N3	MD[42]
N1	MD[43]
P2	MD[44]
P4	MD[45]
R1	MD[46]
R3	MD[47]
AA5	MD[48]
AB2	MD[49]
AB4	MD[50]
AC2	MD[51]
AD1	MD[52]
AE3	MD[53]
AD4	MD[54]
AC5	MD[55]
AB6	MD[56]
AE5	MD[57]
AB7	MD[58]
AD6	MD[59]
AE6	MD[60]
AD7	MD[61]
AF7	MD[62]
AC8	MD[63]
U1	CS#[0]
U2	CS#[1]
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
Y3	CS#[2]/MA[11]
Y4	CS#[3]/MA[12]/BA[1]
T2	DQM[0]
T4	DQM[1]
Y5	DQM[2]
AA2	DQM[3]
T3	DQM[4]
T5	DQM[5]
AA1	DQM[6]
AA3	DQM[7]
B3	AD[0]
A3	AD[1]
C4	AD[2]
B4	AD[3]
A4	AD[4]
D5	AD[5]
C5	AD[6]
B5	AD[7]
A5	AD[8]
D6	AD[9]
C6	AD[10]
B6	AD[11]
A6	AD[12]
E7	AD[13]
D7	AD[14]
C7	AD[15]
A9	AD[16]
E10	AD[17]
C10	AD[18]
B10	AD[19]
A10	AD[20]
E11	AD[21]
D11	AD[22]
C11	AD[23]
A11	AD[24]
E12	AD[25]
D12	AD[26]
C12	AD[27]
B12	AD[28]
A12	AD[29]
E13	AD[30]
D13	AD[31]
E6	CBE[0]
B7	CBE[1]
B9	CBE[2]
B11	CBE[3]
C9	FRAME#
E9	TRDY#
D9	IRDY#
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
B8	STOP#
A8	DEVSEL#
A7	PAR
D8	PERR#
E8	SERR#
C8	LOCK#
C14	PCI_REQ#[0]
B14	PCI_REQ#[1]
A14	PCI_REQ#[2]
A13	PCI_GNT#[0]
B13	PCI_GNT#[1]
C13	PCI_GNT#[2]
C20	LA[17][1]
B21	LA[18][1]
B20	LA[19][1]
E19	LA[20][1]
E18	LA[21][1]
C21	LA[22][1]
D19	LA[23][1]
P22	SA[0][1]
P23	SA[1][1]
P24	SA[2][1]
P25	SA[3][1]
P26	SA[4][1]
N26	SA[5][1]
N25	SA[6][1]
N24	SA[7][1]
N23	SA[8][1]
N22	SA[9][1]
M26	SA[10][1]
M25	SA[11][1]
M24	SA[12][1]
M23	SA[13][1]
M22	SA[14][1]
L26	SA[15][1]
L25	SA[16][1]
L24	SA[17][1]
L23	SA[18][1]
L22	SA[19][1]
K24	SD[0][1]
J26	SD[1][1]
J25	SD[2][1]
J24	SD[3][1]
K23	SD[4][1]
K22	SD[5][1]
H26	SD[6][1]
H25	SD[7][1]
H24	SD[8][1]
G26	SD[9][1]
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
G25	SD[10][1]
G24	SD[11][1]
J22	SD[12][1]
J23	SD[13][1]
F26	SD[14][1]
F25	SD[15][1]
F23	IOCHRDY[1]
D20	ALE[1]
K25	BHE#[1]
F24	MEMR#[1]
A22	MEMW#[1]
G23	SMEMR#[1]
E21	SMEMW#[1]
H22	IOR#[1]
E26	IOW#[1]
E25	MASTER#[1]
E24	MCS16#[1]
C22	IOCS16#[1]
G22	REF#[1]
E17	AEN[1]
A23	IOCHCK#[1]
U25	RTCRW#[1]
U26	RTCDS#[1]
U24	RTCAS[1]/FCS0#
U23	RMRTCCS#[1]
D22	GPIOCS#[1]
D24	IRQ_MUX[0]
E23	IRQ_MUX[1]
C26	IRQ_MUX[2]
F22	IRQ_MUX[3]
A24	DACK_ENC[0]
C23	DACK_ENC[1][1]
B23	DACK_ENC[2][1]
D26	DREQ_MUX[0][1]
D25	DREQ_MUX[1][1]
B24	TC[1]
B15	PCI_INT#[0]
A15	PCI_INT#[1]
E14	PCI_INT#[2]
D14	PCI_INT#[3]
B16	ISAOE#[1]
B22	KBCS#[1]
K26	ZWS#[1]
R23	PIRQ
R24	SIRQ
T22	PDRQ
T23	SDRQ
R25	PDACK#
R26	SDACK#
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
T25	PDIOR#
T24	PDIOW#
R22	SDIOR#
T26	SDIOW#
D18	PA[22]
C19	PA[23]
B19	PA[24]
A17	FCS_0H
B17	FCS_0L
C16	FCS_1H
E16	FCS_1L
D17	IOCS#[4]
C18	IOCS#[5]
B18	IOCS#[6]
C17	IOCS#[7]
AD8	RED
AF8	GREEN
AC9	BLUE
AB10	VSYNC
AF9	HSYNC
AB9	VREF_DAC
AD9	RSET
AE8	COMP
AE9	VDD_DAC
AC10	VSS_DAC
AB15	VCLK
AF16	VIN[0]
AE16	VIN[1]
AC16	VIN[2]
AB16	VIN[3]
AF17	VIN[4]
AE17	VIN[5]
AD17	VIN[6]
AB17	VIN[7]
AD18	ODD_EVEN#
AF18	VCS
AE10	TFTR0
AF10	TFTR1
AB11	TFTR2
AD11	TFTR3
AE11	TFTR4
AF11	TFTR5
AB12	TFTG0
AC12	TFTG1
AD12	TFTG2
AE12	TFTG3
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
AF12	TFTG4
AB13	TFTG5
AC13	TFTB0
AD13	TFTB1
AE13	TFTB2
AF13	TFTB3
AF14	TFTB4
AE14	TFTB5
AB14	TFTLINE
AC14	TFTFRAME
AF15	TFTDE
AE15	TFTENVDD
AD15	TFTENVCC
AC15	TFTPWM
AD14	TFTDCLK
D21	OC
A20	USBDMNS[0]
A18	USBDMNS[1]
A21	USBDPLS[0]
A19	USBDPLS[1]
E20	POWERON
AC22	CTS0#
AC24	CTS1#
AD21	DCD0#
AE24	DCD1#
AC21	DSR0#
AD25	DSR1#
AD22	DTR0#
AC26	DTR1#
AD23	RI0#
AA22	RI1#
AE22	RTS0#
AC25	RTS1#
AB21	RXD0
AD26	RXD1
AE23	TXD0
AB23	TXD1
AD20	KBCLK
AB19	KBDATA
AC20	MDATA
AB20	MCLK
AA23	PE
W24	SLCT
W23	BUSY
W25	ERR#
W26	ACK#
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
V22	PDDIR
V24	STROBE#
V25	INIT#
V26	AUTOFD#
U22	SLCTIN#
Y22	PPD[0]
AA24	PPD[1]
AA25	PPD[2]
AA26	PPD[3]
Y24	PPD[4]
Y25	PPD[5]
Y26	PPD[6]
W22	PPD[7]
AC19	SCL / DDC[1]
AD19	SDA / DDC[0]
C2	GPIO[0]
C1	GPIO[1]
D3	GPIO[2]
D2	GPIO[3]
D1	GPIO[4]
E4	GPIO[5]
E3	GPIO[6]
E2	GPIO[7]
E1	GPIO[8]
F5	GPIO[9]
F4	GPIO[10]
F3	GPIO[11]
F2	GPIO[12]
G5	GPIO[13]
G4	GPIO[14]
G2	GPIO[15]
H2	TCLK
J5	TRST
H5	TDI
H3	TMS
H1	TDO
G1	SCAN_ENABLE
AD10	COL_SEL
C25	SPKRD
AD16	VDD_DCLK_PLL
Y23	VDD_DEVCLK_PLL
AE20	VDD_HCLKI_PLL
AB26	VDD_HCLKO_PLL
AE19	VDD_MCLKI_PLL
AE18	VDD_MCLKO_PLL
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
AE21	VDD_PCICLK_PLL
F13	VDD_CORE
F15	VDD_CORE
F17	VDD_CORE
K6	VDD_CORE
M21	VDD_CORE
N6	VDD_CORE
P21	VDD_CORE
R6	VDD_CORE
U21	VDD_CORE
AA10	VDD_CORE
AA12	VDD_CORE
AA14	VDD_CORE
A2	VDD
A25	VDD
B1	VDD
B26	VDD
F7	VDD
F11	VDD
F20	VDD
G6	VDD
G21	VDD
H6	VDD
J21	VDD
K21	VDD
U6	VDD
V6	VDD
Y6	VDD
Y21	VDD
AA7	VDD
AA16	VDD
AA18	VDD
AA20	VDD
AE01	VDD
AE26	VDD
AF02	VDD
AF25	VDD
A1	GND
A26	GND
B2	GND
B25	GND
C3	GND
C24	GND
D4	GND
D10	GND
D16	GND
D23	GND
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
E5	GND
E22	GND
F6	GND
F8	GND
F9	GND
F10	GND
F12	GND
F14	GND
F16	GND
F18	GND
F19	GND
F21	GND
H4	GND
H21	GND
H23	GND
J6	GND
L6	GND
L11:16	GND
L21	GND
M6	GND
M11:16	GND
N11:16	GND
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
N21	GND
P6	GND
P11:16	GND
R11:16	GND
R21	GND
T6	GND
T11:16	GND
T21	GND
V21	GND
V23	GND
W4	GND
W6	GND
W21	GND
AA6	GND
AA8	GND
AA9	GND
AA11	GND
AA13	GND
AA15	GND
AA17	GND
AA19	GND
AA21	GND
Note[1]; This signal is multiplexed see Table 2-4	

Table 2-6. Pinout

Pin#	Pin Name
AB5	GND
AB22	GND
AC4	GND
AC11	GND
AC17	GND
AC23	GND
AD3	GND
AD24	GND
AE2	GND
AE25	GND
AF1	GND
AF26	GND
G3	*Reserved*
F1	*Reserved*
Note[1]; This signal is multiplexed see Table 2-4	

3 STRAP OPTION

This chapter defines the STPC Atlas Strap Options and their locations. Some strap options are left programmable for future versions of silicon. The strap options are sampled at a specific point of the boot process. This is shown in detail in Figure 4-3

Signal	Designation	Location	Actual Settings	Set to '0'	Set to '1'
MD1	Reserved[2]	Not accessible	Pull Up	-	-
MD2	HCLK Speed	Index 5F,bit 6	User defined	See Section 3.1.3	
MD3		Index 5F,bit 7	User defined		
MD[4]	PCI_CLKO Divisor	Index 4A,bit 1	Pull-up	See Section 3.1.1.	
MD[5]	MCLK Synchro (see Section 3.1.1.)	Index 4A,bit 2	User defined	Async	Sync
MD[6]	PCI_CLKO Programming	Index 4A,bit 6	User defined	See Section 3.1.1.	
MD[7]		Index 4A,bit 7	Pull-down		
MD[8]	ISA / PCMCIA / Local Bus	Index 4A,bit 3	User defined	See Section 3.1.1.	
MD[9]		Index 4A,bit 3	User defined		
MD10	Reserved[2]	Index 4B,bit 2	Pull down	-	-
MD11	Reserved[2]	Index 4B,bit 3	Pull down	-	-
MD12	Reserved[2]	Index 4B,bit 4	Pull up	-	-
MD13	Reserved[2]	Index 4B,bit 5	Pull up	-	-
MD14	CPU clock Multiplication	Index 4B,bit 6	Pull-up	See Section 3.1.2	
MD15	Reserved[2]	Not accessible	Pull up	-	-
MD16	Reserved[2]	Not accessible	Pull up	-	-
MD17	PCI_CLKO Divisor	Index 4A,bit 0	User defined	See Section 3.1.1.	
MD18	HCLK Pad Direction	Index 4C,bit 2	Pull-up	Input	Output
MD19	MCLK Pad Direction	Index 4C,bit 3	Pull-up	Hi-Z	Output
MD20	DCLK Pad Direction	Index 4C,bit 4	User defined	Input	Output
MD21	Reserved[2]	Index 5F,bit 0	Pull up	-	-
MD23	Reserved[2]	Index 5F,bit 2	Pull up	-	-
MD24	HCLK PLL Speed	Index 5F,bit 3	User defined	See Section 3.1.3	
MD25		Index 5F,bit 4	User defined		
MD26		Index 5F,bit 5	User defined		
MD27	Reserved[2]	Not accessible	Pull up	-	-
MD28	Reserved[2]	Not accessible	Pull up	-	-
MD29	Reserved[2]	Not accessible	Pull up	-	-
MD30	Reserved[2]	Not accessible	Pull up	-	-
MD31	Reserved[2]	Not accessible	Pull up		
MD32	Reserved[2]	Not accessible	Pull up		
MD33	Reserved[2]	Not accessible	Pull up		
MD34	Reserved[2]	Not accessible	Pull up		
MD35	Reserved[2]	Not accessible	Pull up		
MD36	Local Bus Boot Device Size	Index 4B,bit 0	User defined	8-bit	16-bit
MD37	Reserved[2]	Not accessible	Pull down	-	-
MD38	Reserved[2]	Not accessible	Pull down	-	-
MD40	CPU clock Multiplication	Index 4B,bit 7	User defined	See Section 3.1.2	

Note[1]: Strap options on TC/PA[3] and DACK_ENC[2:0]/PA[2:0] are required for all the STPC Atlas Configurations (ISA, PCMCIA, Local Bus).

Note[2]: Must be implemented.

Signal	Designation	Location	Actual Settings	Set to '0'	Set to '1'
MD41	Reserved[2]	Not accessible	Pull down	-	-
MD42	Reserved[2]	Not accessible	Pull up	-	-
MD 43	Reserved[2]	Not accessible	Pull down	-	-
MD 45	CPUCLK/HCKL Deskew Programming	Not accessible	User defined	See Section 3.1.5	
MD 46		Not accessible	User defined		
MD 47	Reserved[2]	Not accessible	Pull down	-	-
MD 48	Reserved[2]	Not accessible	Pull up	-	-
MD 50	Internal UART2 (see Section 3.1.4.)	Index 4C,bit 0	User defined	Disable	Enable
MD 51	Internal UART1 (see Section 3.1.4.)	Index 4C,bit 1	User defined	Disable	Enable
MD 52	Internal Kbd / Mouse (see Section 3.1.4.)	Index 4C,bit 6	User defined	Disable	Enable
MD 53	Internal Parallel Port (see Section 3.1.4.)	Index 4C,bit 7	User defined	Disable	Enable
TC[1]	Reserved[2]	Hardware	Pull up	-	-
DACK_ENC[2][1]	Reserved[2]	Hardware	Pull up	-	-
DACK_ENC[1][1]	Reserved[2]	Hardware	Pull up	-	-
DACK_ENC[0][1]	Reserved[2]	Hardware	Pull up	-	-

Note[1]: Strap options on TC/PA[3] and DACK_ENC[2:0]/PA[2:0] are required for all the STPC Atlas Configurations (ISA, PCMCIA, Local Bus).
Note[2]: Must be implemented.

3.1 STRAP OPTION REGISTER DESCRIPTION

3.1.1. STRAP REGISTER 0

This register is read only.

STRAP0 Access = 0022h/0023h Regoffset =04Ah

7	6	5	4	3	2	1	0
MD[7]	MD[6]	MD[9]	MD[8]	RSV	MD[5]	MD[4]	MD[17]
This register defaults to the values sampled on the MD pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-6	MD[7:6]	PCICLK PLL set-up: The value sampled on MD[7:6] controls the PCICLK PLL programming according to the PCICLK frequency. MD7 MD6 0 0 PCICLK frequency between 16 & 32 MHz 0 1 PCICLK frequency between 32 & 64 MHz 1 X Reserved
Bits 5-4	MD[9:8]	Mode selection: MD9 MD8 0 0 ISA mode: ISA enabled, PCMCIA & Local Bus disabled 0 1 PCMCIA mode: PCMCIA enabled, ISA & Local Bus disabled 1 0 Local Bus mode: Local Bus enabled, ISA & PCMCIA disabled 1 1 Reserved
Bit 3	Rsv	Reserved
Bit 2	MD[5]	Host Memory synchronization. This bit reflects the value sampled on [MD5] and controls the MCLK/HCLK synchronization. 0: MCLK and HCLK not synchronized 1: MCLK and HCLK synchronized.
Bits 1-0	MD[4], MD[17]	PCICLK division: These bits reflect the values sampled on [MD4] and MD[17] to select the PCICLK frequency. MD4 MD17 0 X PCI Clock output = HCLK / 4 1 0 PCI Clock output = HCLK / 3 1 1 PCI Clock output = HCLK / 2

3.1.2 STRAP REGISTER 1

This register is read only.

STRAP1 Access = 0022h/0023h Regoffset =04Bh

7	6	5	4	3	2	1	0
MD[40]	MD[14]	RSV	RSV	RSV	RSV	RSV	MD[36]
This register defaults to the values sampled on the MD pins after reset							

Bit Number Sampled	**Mnemonic**	**Description**
Bits 7-6	MD[40] & MD[14]	CPU Clock Multiplication (486 mode): MD14 MD40 1 0 X 1 1 1 X 2 All other settings are reserved HCLK maximum speed is 66MHz and in CPU mode X2. Operation in X1 mode is only guaranteed up to 66MHz.
Bits 5-1	Rsv	Reserved
Bit 0	MD[36]	These bits reflect the values sampled on MD[36] and determines the Local Bus Boot device width: 0: 8-bit Boot Device 1: 16-bit Boot Device

3.1.3 HCLK PLL STRAP REGISTER

This register is read only.

HCLK_STRAP0 Access = 0022h/0023h Regoffset =05Fh

7	6	5	4	3	2	1	0
RSV		MD[26]	MD[25]	MD[24]	RSV		
This register defaults to the values sampled on the MD pins after reset							

Bit Number Sampled	Mnemonic	Description
Bits 7-6	Rsv	These bits are fixed to ‘0’
Bits 5-3	MD[26:24]	These pins reflect the values sampled on MD[26:24] pins respectively and control the Host clock frequency synthesizer as shown in Table 3-1
Bits 2-0	Rsv	Reserved

Table 3-1. HCLK Frequency Configuration

MD[3]	MD[2]	MD[26]	MD[25]	MD[24]	HCLK Speed
0	0	0	0	0	25 MHz
0	0	0	0	1	50 MHz
0	0	0	1	0	60 MHz
0	0	0	1	1	66 MHz
All other settings are reserved					

3.1.4. STRAP REGISTER 2

This register is read only with the exception of bit 4

STRAP2 Access = 0022h/0023h Regoffset =04Ch

7	6	5	4	3	2	1	0
MD[53]	MD[52]	RSV	MD[20]	MD[19]	MD[18]	MD[51]	MD[50]
This register defaults to the values sampled on the MD pins after reset							

Bit Number Sampled	Mnemonic	Description
Bit 7	MD[53]	This bit reflects the value sampled on MD[53] pin and determines whether the internal Parallel Port Controller is used 0: Internal Parallel Port Controller is disabled 1: Internal Parallel Port Controller is enabled
Bit 6	MD[52]	This bit reflects the value sampled on MD[52] pin and determines whether the internal Keyboard controller is used 0: Internal Keyboard Controller is disabled 1: Internal Keyboard Controller is enabled
Bit 5	Rsv	Reserved
Bit 4	MD[20]	This bit reflects the value sampled on MD[20] pin and controls the Dot clock pin (DCLK) direction as follows: 0: Input. 1: Output of the internal frequency synthesizer DCLK PLL.
Bit 3	MD[19]	This bit reflects the value sampled on MD[19] pin and controls the Memory clock output pin (MCLKO) as follows: 0: Tristated. 1: Output of the internal frequency synthesizer MCLKO PLL.
Bit 2	MD[18]	This bit reflects the value sampled on MD[18] pin and controls the Host clock pin (HCLK) direction as follows: 0: Input. 1: Output of the internal frequency synthesizer HCLK PLL.
Bit 1	MD[51]	This bit reflects the value sampled on MD[51] pin and determines whether the internal UART1 is enabled: 0: Internal UART1 is disabled 1: Internal UART1 is enabled
Bit 0	MD[50]	This bit reflects the value sampled on MD[50] pin and determines whether the internal UART2 is enabled: 0: Internal UART2 is disabled 1: Internal UART2 is enabled

3.1.5 CPUCLK/HCKL DESKEW PROGRAMMING

MD[45]	MD[46]	Description
1	0	HCLK between 33MHz and 64MHz
0	1	HCLK between 64MHz and 133MHz
All other settings are reserved		

Note that these straps are not accessible by software.

3.2 TYPICAL STRAP OPTION IMPLEMENTATION

Table 3-1.shows the detailed Strap options required to boot the STPC in ISA mode with a Host Clock Frequency of 66MHz in X2 mode with internal keyboard/mouse, UARTS and parallel port enabled.

Table 3-1. Typical Strap Option Implementation

Signal	Designation	Actual Settings	Description
MD1	Reserved[2]	Pull Up	-
MD2	HCLK Speed	Pull down	HCLK = 66MHz
MD3		Pull down	
MD[4]	PCI_CLKO Divisor	Pull up	PCICLK = HCLK/2
MD[5]	MCLK Synchro (see Section 3.1.1.)	Pull down	Asynchronous
MD[6]	PCI_CLKO Programming	Pull up	PCICLK PLL Window = 32MHz - 64MHz
MD[7]		Pull down	
MD[8]	ISA / PCMCIA / Local Bus	Pull down	ISA Mode
MD[9]		Pull down	
MD10	Reserved[2]	Pull down	-
MD11	Reserved[2]	Pull down	-
MD14	CPU clock Multiplication	Pull up	X2 Mode
MD15	Reserved[2]	Pull up	-
MD16	Reserved[2]	Pull up	-
MD17	PCI_CLKO Divisor	Pull up	PCICLK = HCLK/2
MD18	HCLK Pad Direction	Pull up	Output
MD19	MCLK Pad Direction	Pull up	Output
MD20	DCLK Pad Direction	Pull up	Output
MD21	Reserved[2]	Pull up	-
MD23	Reserved[2]	Pull up	-
MD24	HCLK PLL Speed	Pull up	HCLK = 66MHz
MD25		Pull up	
MD26		Pull down	
MD27	Reserved[2]	Pull up	-
MD28	Reserved[2]	Pull up	-
MD29	Reserved[2]	Pull up	-
MD30	Reserved[2]	Pull up	-
MD31	Reserved[2]	Pull up	
MD32	Reserved[2]	Pull up	
MD33	Reserved[2]	Pull up	
MD34	Reserved[2]	Pull up	

Note[1]: Strap options on TC/PA[3] and DACK_ENC[2:0]/PA[2:0] are required for all the STPC Atlas Configurations (ISA, PCMCIA, Local Bus).
Note[2]: Must be implemented.

Table 3-1. Typical Strap Option Implementation

Signal	Designation	Actual Settings	Description
MD35	Reserved[2]	Pull up	
MD36	Local Bus Boot Device Size	User defined	Not Applicable
MD37	Reserved[2]	Pull down	-
MD38	Reserved[2]	Pull down	-
MD40	CPU clock Multiplication	Pull up	X2 mode
MD41	Reserved[2]	Pull down	-
MD42	Reserved[2]	Pull up	-
MD 43	Reserved[2]	Pull down	-
MD 45	CPUCLK/HCKL Deskew Programming	Pull down	HCLK between 64MHz and 133MHz
MD 46		Pull up	
MD 47	Reserved[2]	Pull down	-
MD 48	Reserved[2]	Pull up	-
MD 50	Internal UART2 (see Section 3.1.4.)	Pull up	Enable
MD 51	Internal UART1 (see Section 3.1.4.)	Pull up	Enable
MD 52	Internal Kbd / Mouse (see Section 3.1.4.)	Pull up	Enable
MD 53	Internal Parallel Port (see Section 3.1.4.)	Pull up	Enable
TC[1]	Reserved[2]	Pull up	-
DACK_ENC[2][1]	Reserved[2]	Pull up	-
DACK_ENC[1][1]	Reserved[2]	Pull up	-
DACK_ENC[0][1]	Reserved[2]	Pull up	-

Note[1]: Strap options on TC/PA[3] and DACK_ENC[2:0]/PA[2:0] are required for all the STPC Atlas Configurations (ISA, PCMCIA, Local Bus).
Note[2]: Must be implemented.

4 ELECTRICAL SPECIFICATIONS

4.1. INTRODUCTION

The electrical specifications in this chapter are valid for the STPC Atlas.

4.2. ELECTRICAL CONNECTIONS

4.2.1. POWER/GROUND CONNECTIONS/ DECOUPLING

Due to the high frequency of operation of the STPC Atlas, it is necessary to install and test this device using standard high frequency techniques. The high clock frequencies used in the STPC Atlas and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the VSS and VDD pins.

4.2.2. UNUSED INPUT PINS

No unused input pin should be left unconnected unless they have an integrated pull-up or pull-down. Connect active-low inputs to VDD through a 20 kΩ (±10%) pull-up resistor and active-high inputs to VSS. For bi-directionnal active-high inputs, connect to VSS through a 20 kΩ (±10%) pull-up resistor to prevent spurious operation.

4.2.3. RESERVED DESIGNATED PINS

Pins designated as reserved should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.3. ABSOLUTE MAXIMUM RATINGS

The following table lists the absolute maximum ratings for the STPC Atlas device. Stresses beyond those listed under Table 4-1 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those specified in section "Operating Conditions".

Exposure to conditions beyond those outlined in Table 4-1 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings (Table 4-1) may also result in reduced useful life and reliability.

4.3.1. 5V TOLERANCE

The STPC is capable of running with I/O systems that operate at 5 V such as PCI and ISA devices. Certain pins of the STPC tolerate inputs up to 5.5 V. Above this limit the component is likely to sustain permanent damage.

All 5 volt tolerant pins are outlined in Table 2-3 Buffer Type Descriptions.

Table 4-1. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Units
V_{DDx}	DC Supply Voltage	-0.3	4.0	V
V_{CORE}	DC Supply Voltage for Core	-0.3	2.7	V
V_I, V_O	Digital Input and Output Voltage	-0.3	VDD + 0.3	V
V_{5T}	5Volt Tolerance	-0.3	5.5	V
V_{ESD}	ESD Capacity (Human body mode)	-	2000	V
T_{STG}	Storage Temperature	-40	+150	°C
T_{OPER}	Operating Temperature (Note 1)	0	+85	°C
		-40	+115	°C
P_{TOT}	Maximum Power Dissipation (package)	-	4.8	W

Note 1: The figures specified apply to the Tcase of a STPC device that is soldered to a board, as detailed in the Design Guidelines Section, for Commercial and Industrial temperature ranges.

4.4. DC CHARACTERISTICS

Table 4-2. DC Characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V_{DD}	3.3V Operating Voltage		3.0	3.3	3.6	V
V_{CORE}	2.5V Operating Voltage		2.45	2.5	2.7	V
P_{DD}	3.3V Supply Power	$3.0V < V_{DD} < 3.6V$			0.24	W
P_{CORE}	2.5V Supply Power[1]	$2.45V < V_{CORE} < 2.7V$			4.1	W
V_{IL}	Input Low Voltage	Except XTALI	-0.3		0.8	V
		XTALI	-0.3		0.8	V
V_{IH}	Input High Voltage	Except XTALI	2.1		V_{DD}+0.3	V
		XTALI	2.35		V_{DD}+0.3	V
I_{LK}	Input Leakage Current	Input, I/O	-5		5	µA
	Integrated Pull up/down			50		KΩ
Note 1; Power consumption is heavily dependant on the clock frequencies and on the enabled features. See details in Table 4-5. to Table 4-8..						

Table 4-3. PAD buffers DC Characteristics

Buffer Type	I/O count	V_{IH} min (V)	V_{IL} max (V)	V_{OH} min (V)	V_{OL} max (V)	I_{OL} min (mA)	I_{OH} max (mA)	C_{load} max (pF)	Derating (ps/pF)[1]	C_{IN} (pF)
ANA	10	2.35	0.9	-	-	-	-	-	-	-
OSCI13B	2	2.1	0.8	2.4	0.4	2	- 2	50	-	-
BT4CRP	1	-	-	0.85*V_{DD}	0.4	4	- 4	100	30	5.61
BT8TRP_TC	7	-	-	2.4	0.4	8	- 8	200	21	6.89
BD4STRP_FT	64	2	0.8	2.4	0.4	4	- 4	100	42	5.97
BD4STRUP_FT	14	2	0.8	2.4	0.4	4	- 4	100	41	5.97
BD4STRP_TC	26	2	0.8	2.4	0.4	4	- 4	100	42	5.83
BD8STRP_FT	30	2	0.8	2.4	0.4	8	- 8	200	23	5.96
BD8STRUP_FT	47	2	0.8	2.4	0.4	8	- 8	200	23	5.96
BD8STRP_TC	12	2	0.8	2.4	0.4	8	- 8	200	21	7.02
BD8TRP_TC	53	2	0.8	2.4	0.4	8	- 8	200	21	7.03
BD8PCIARP_FT	50	0.5*V_{DD}	0.3*V_{DD}	0.9*V_{DD}	0.1*V_{DD}	1.5	- 0.5	200	15	6.97
BD14STARP_FT	18	2	0.8	2.4	0.4	14	-14	100	71	6.20
BD16STARUQP_TC	19	2	0.8	2.4	0.4	16	-16	400	12	9.34
SCHMITT_FT	1	2	0.8	-	-	-	-	-	-	5.97
TLCHT_FT	16	2	0.8	-	-	-	-	-	-	5.97
TLCHT_TC	1	2	0.8	-	-	-	-	-	-	5.97
TLCHTD_TC	1	2	0.8	-	-	-	-	-	-	5.97
TLCHTU_TC	1	2	0.8	-	-	-	-	-	-	5.97
USBDS_2V5 (slow)	4	2	0.8	2.4	0.4	-	-	100	45.2	8.41
USBDS_2V5 (fast)									98.8	
Note 1: time to output variation depending on the capacitive load.										

Table 4-4. RAMDAC DC Specification

Symbol	Parameter	Min	Max
Vref_dac	Voltage Reference	1.00 V	1.24 V
INL	Integrated Non Linear Error	-	3 LSB
DNL	Differentiated Non Linear Error	-	1 LSB
BLC	Black Level Current	1.0 mA	2.0 mA
WLC	White Level Current	15.00 mA	18.50 mA

Table 4-5. VGA RAMDAC Power Consumption

DCLK (MHz)	DAC mode (State)	P_{Max} (mW)	
		VDD_DAC = 2.45V	VDD_DAC = 2.7V
-	Shutdown	0	0
6.25 - 135	Active	150	180

Table 4-6. 2.5V Power Consumptions (V_{CORE} + VDD_x_PLL + VDD_DAC)

HCLK (MHz)	CPUCLK (MHz)	MCLK (MHz)	Mode	DCLK (MHz)	PMU (State)	P_{Max} (W)	
						$V_{2.5V}$=2.45V	$V_{2.5V}$=2.7V
66	133 (x2)	66	SYNC	Stopped	Stop Clock	1.5	1.9
					Full Speed	2.5	3.0
				135	Stop Clock	2.1	2.6
					Full Speed	2.1	3.6
66	133 (x2)	90	ASYNC	Stopped	Stop Clock	1.9	2.4
					Full Speed	2.8	3.5
				135	Stop Clock	2.5	3.1
					Full Speed	3.3	4.1

Note 1: PCI clock at 33MHz

Table 4-7. 3.3V Power Consumptions (V_{DD})

HCLK (MHz)	CPUCLK (MHz)	MCLK (MHz)	DCLK (MHz)	PMU (State)	P_{Max} (mW)
66	133 (x2)	66	6.26	Full Speed	**130**
			135		**215**
66	133 (x2)	90	6.26	Full Speed	**150**
			135		**240**

Table 4-8. PLL Power Consumptions

PLL name	P_{Max} (mW)	
	VDD_PLL = 2.45V	VDD_PLL = 2.7V
VDD_DCLK_PLL	5	10
VDD_DEVCLK_PLL	5	10
VDD_HCLKI_PLL	5	10
VDD_HCLKO_PLL	5	10
VDD_MCLKI_PLL	5	10
VDD_MCLKO_PLL	5	10
VDD_PCICLK_PLL	5	10

4.5. AC CHARACTERISTICS

This section lists the AC characteristics of the STPC interfaces including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 and Figure 4-2. The rising clock edge reference level VREF and other reference levels are shown in Table 4-9 below. Input or output signals must cross these levels during testing.

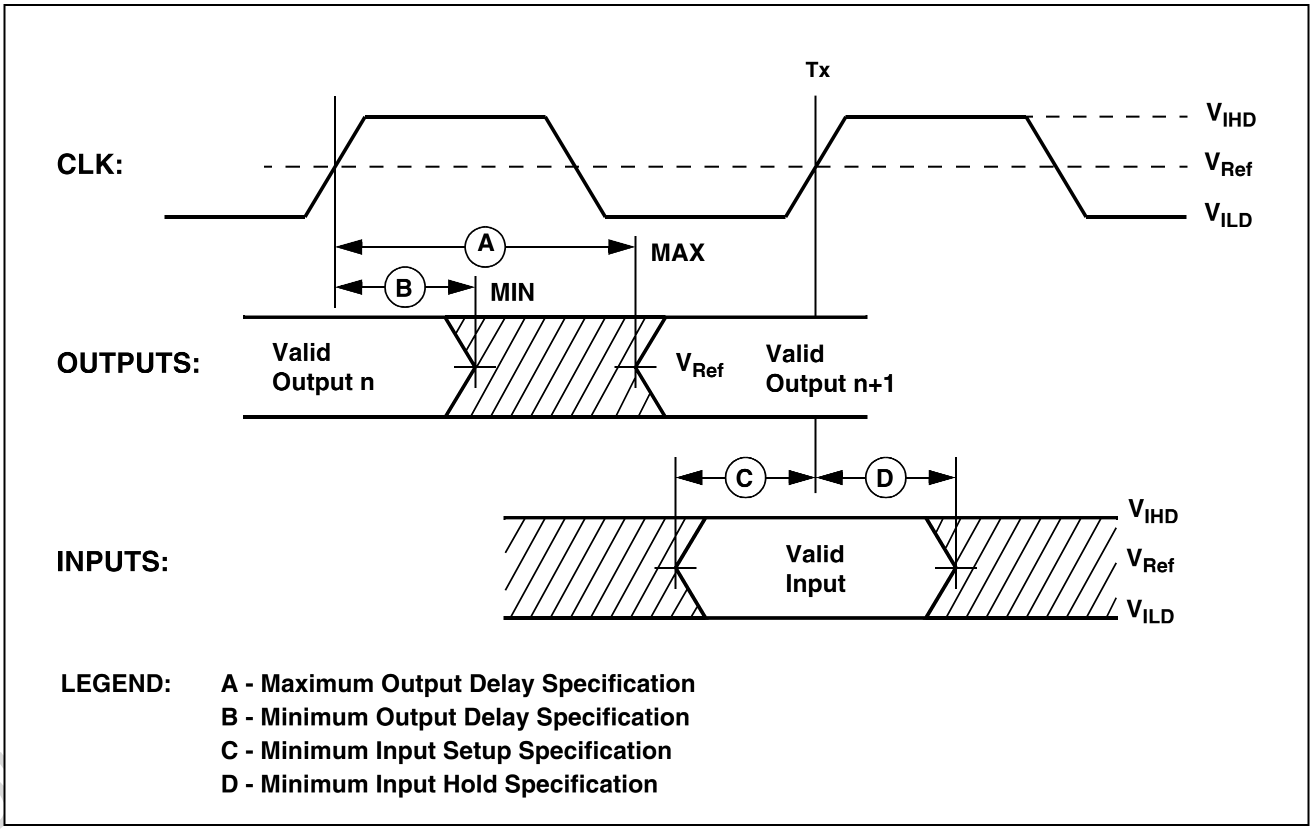
Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

Table 4-9. Drive Level and Measurement Points for Switching Characteristics

Symbol	Value	Units
V_{REF}	1.5	V
V_{IHD}	2.5	V
V_{ILD}	0.0	V

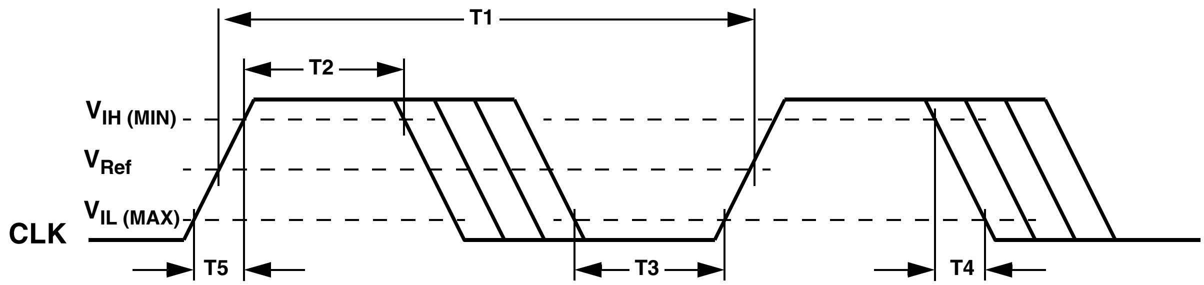
Note: Refer to Figure 4-1.

Figure 4-1. Drive Level and Measurement Points for Switching Characteristics



4.5.1. POWER ON SEQUENCE

Figure 4-2. CLK Timing Measurement Points



LEGEND:
- ***T1 - One Clock Cycle***
- ***T2 - Minimum Time at*** V_{IH}
- ***T3 - Minimum Time at*** V_{IL}
- ***T4 - Clock Fall Time***
- ***T5 - Clock Rise Time***

NOTE; All sIgnals are sampled on the rising edge of the CLK.

Figure 4-3 describes the power-on sequence of the STPC, also called cold reset.

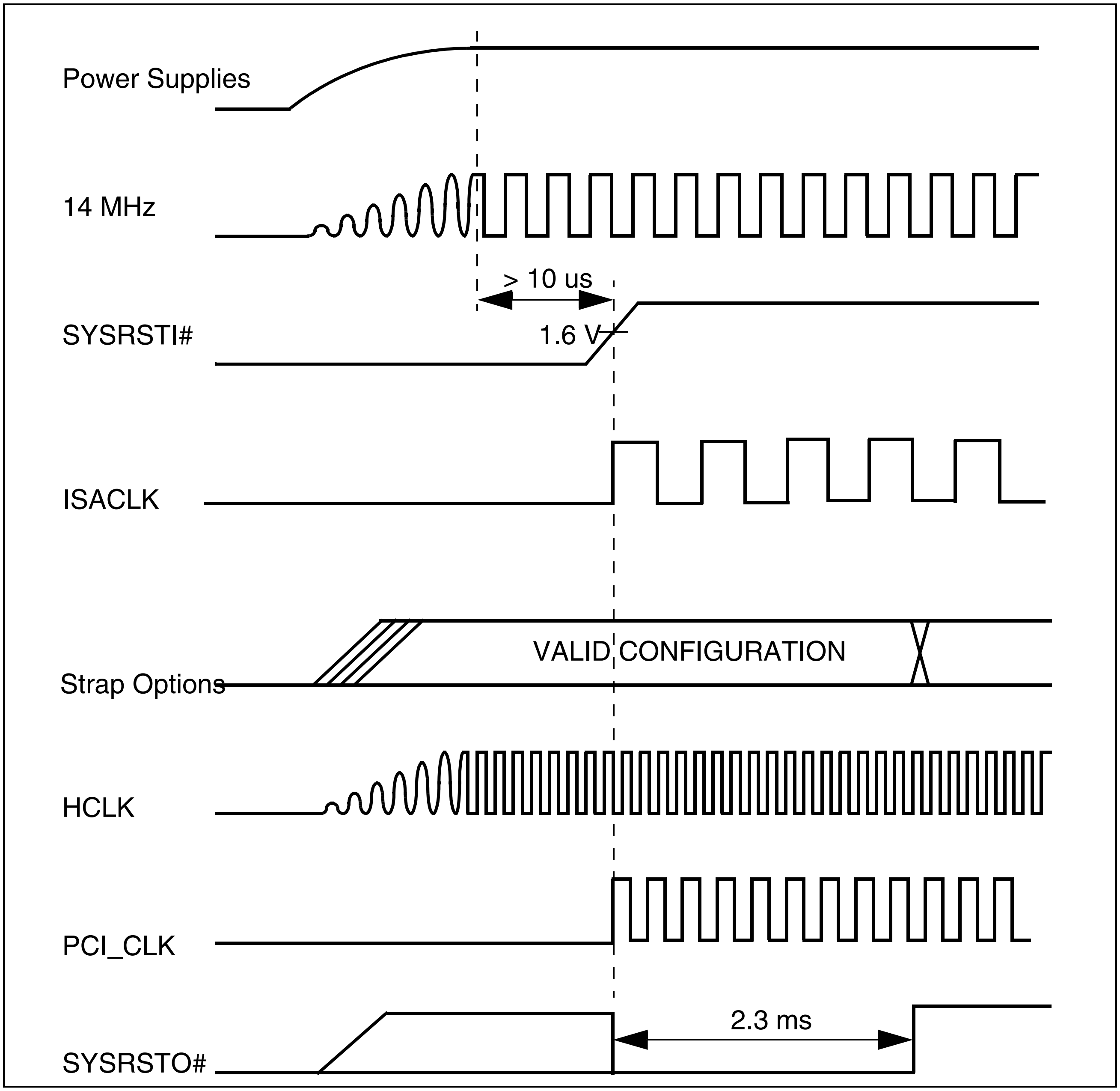
There is no dependency between the different power supplies and there is no constraint on their rising time.

SYSRSTI# as no constraint on its rising edge but must stay active until power supplies are all within specifications, a margin of 10µs is even recommended to let the STPC PLLs and strap options stabilize.

Strap Options are continuously sampled during SYSRSTI# low and must remain stable. Once SYSRSTI# is high, they MUST NOT CHANGE until SYSRSTO# goes high.

Bus activity starts only few clock cycles after the release of SYSRSTO#. The toggling signals depend on the STPC configuration.
In ISA mode, activity is visible on PCI prior to the ISA bus as the controller is part of the south bridge.
In Local Bus mode, the PCI bus is not accessed and the Flash Chip Select is the control signal to monitor.

Figure 4-3. Power-on timing diagram



4.5.2 RESET SEQUENCE

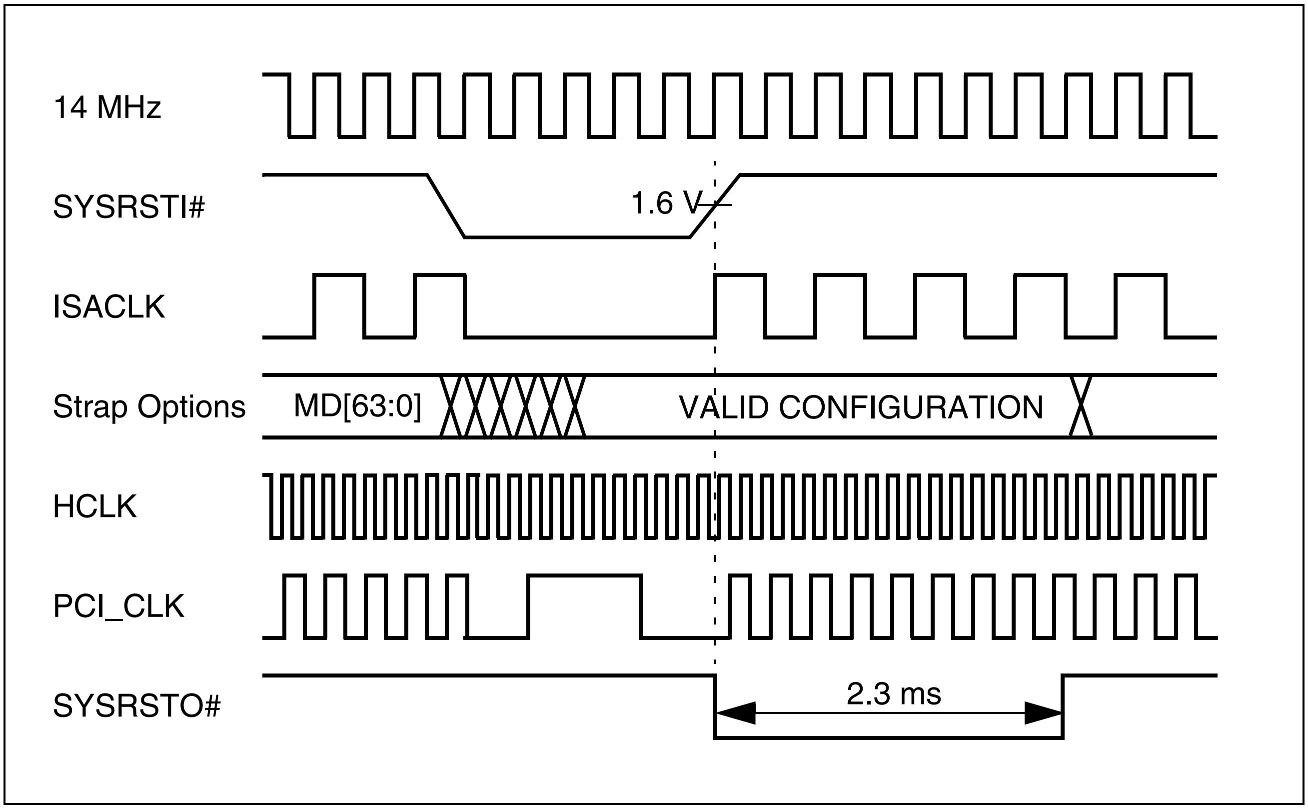
Figure 4-4 describes the reset sequence of the STPC, also called warm reset.

The constraints on the strap options and the bus activities are the same as for the cold reset.
The SYSRSTI# pulse duration must be long enough to have all the strap options stabilized and must be adjusted depending on resistor values.

It is mandatory to have a clean reset pulse without glitches as the STPC could then sample invalid strap option setting and enter into an umpredictable mode.

While SYSRSTI# is active, the PCI clock PLL runs in open loop mode at a speed of few 100's KHz.

Figure 4-4. Reset timing diagram



4.5.3. SDRAM INTERFACE

Figure 4-5, Table 4-10, Table 4-11 lists the AC characteristics of the SDRAM interface. The MCLKx clocks are the input clock of the SDRAM devices.

Figure 4-5. SDRAM Timing Diagram

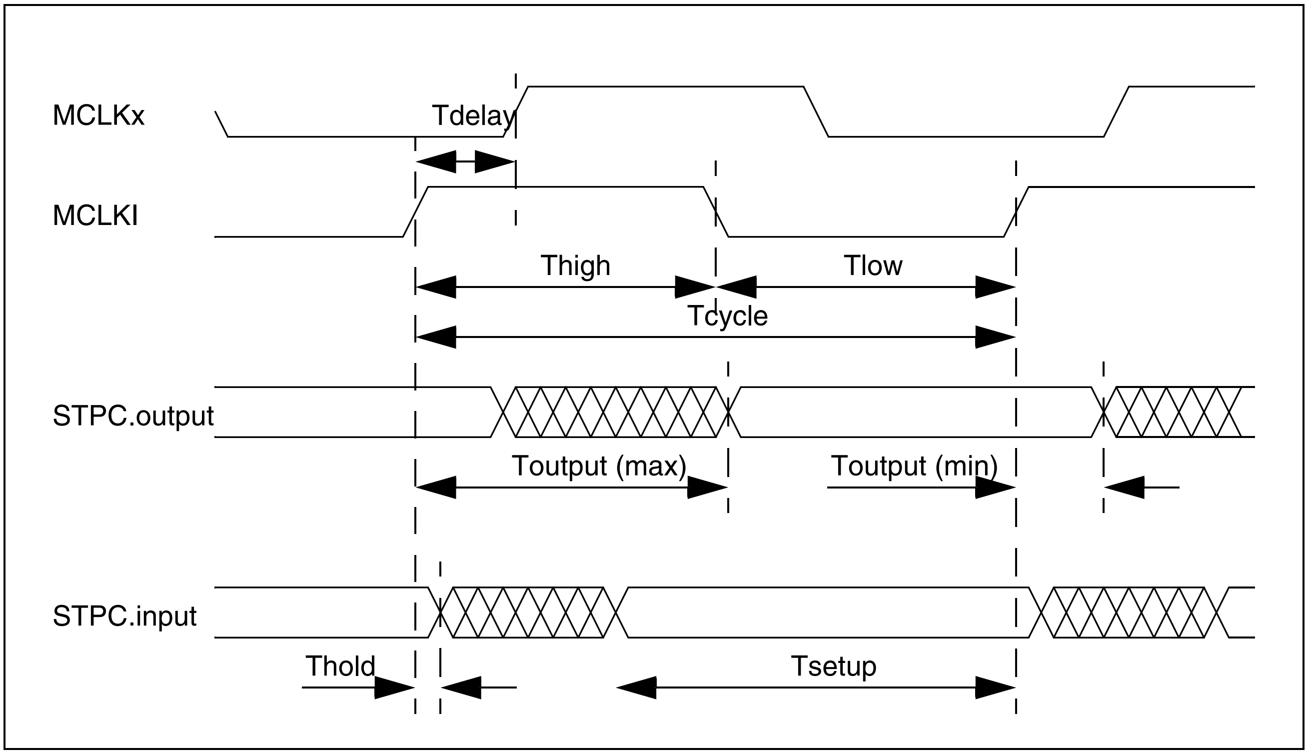


Table 4-10. SDRAM Bus AC Timings - Commercial Temperature Range

Name	Parameter	Min	Typ	Max	Unit
Tcycle	MCLKI Cycle Time	11			ns
Thigh	MCLKI High Time	4			ns
Tlow	MCLKI Low Time	4			ns
	MCLKI Rising Time			1	ns
	MCLKI Falling Time			1	ns
Tdelay	MCLKx to MCLKI delay	0.5	1	1.5	ns
Toutput	MCLKI to RAS# Valid	1.6		5.2	ns
	MCLKI to CAS# Valid	1.6		5.2	ns
	MCLKI to CS# Valid	1.6		5.2	ns
	MCLKI to DQM[ ] Outputs Valid	1.35		5.2	ns
	MCLKI to MD[ ] Outputs Valid	1.35		5.2	ns
	MCLKI to MA[ ] Outputs Valid	1.6		5.2	ns
	MCLKI to MWE# Valid	1.6		5.2	ns
Tsetup	MD[63:0] setup to MCKLI	4.7			ns
Thold	MD[63:0] hold from MCKLI	-0.36		2.3	ns
Note: These timings are for a load of 50pF, part running at 100MHz and ReadCLK activated and set to 0					

The PC100 memory is recommended to reach 90MHz operation.

Table 4-11. SDRAM Bus AC Timings - Industrial Temperature Range

Name	Parameter	Min	Typ	Max	Unit
Tcycle	MCLKI Cycle Time	11			ns
Thigh	MCLKI High Time	4			ns
Tlow	MCLKI Low Time	4			ns
	MCLKI Rising Time			1	ns
	MCLKI Falling Time			1	ns
Tdelay	MCLKx to MCLKI delay	0.5	1	1.5	ns
Toutput	MCLKI to RAS# Valid	1.7		6.5	ns
	MCLKI to CAS# Valid	1.7		6.5	ns
	MCLKI to CS# Valid	1.7		6	ns
	MCLKI to DQM[ ] Outputs Valid	2		6	ns
	MCLKI to MD[ ] Outputs Valid	2		7.8	ns
	MCLKI to MA[ ] Outputs Valid	1.7		6.5	ns
	MCLKI to MWE# Valid	1.7		6	ns
Tsetup	MD[63:0] setup to MCKLI	4.7			ns
Thold	MD[63:0] hold from MCKLI	-0.36		2.3	ns
Note: These timings are for a load of 50pF, part running at 90MHz and ReadCLK not activated					

The PC100 memory is recommended to reach 90MHz operation.

4.5.4 PCI INTERFACE

Figure 4-6 and Table 4-12. list the AC characteristics of the PCI interface. PCICLKx stands for any PCI device clock input.

Figure 4-6. PCI Timing Diagram

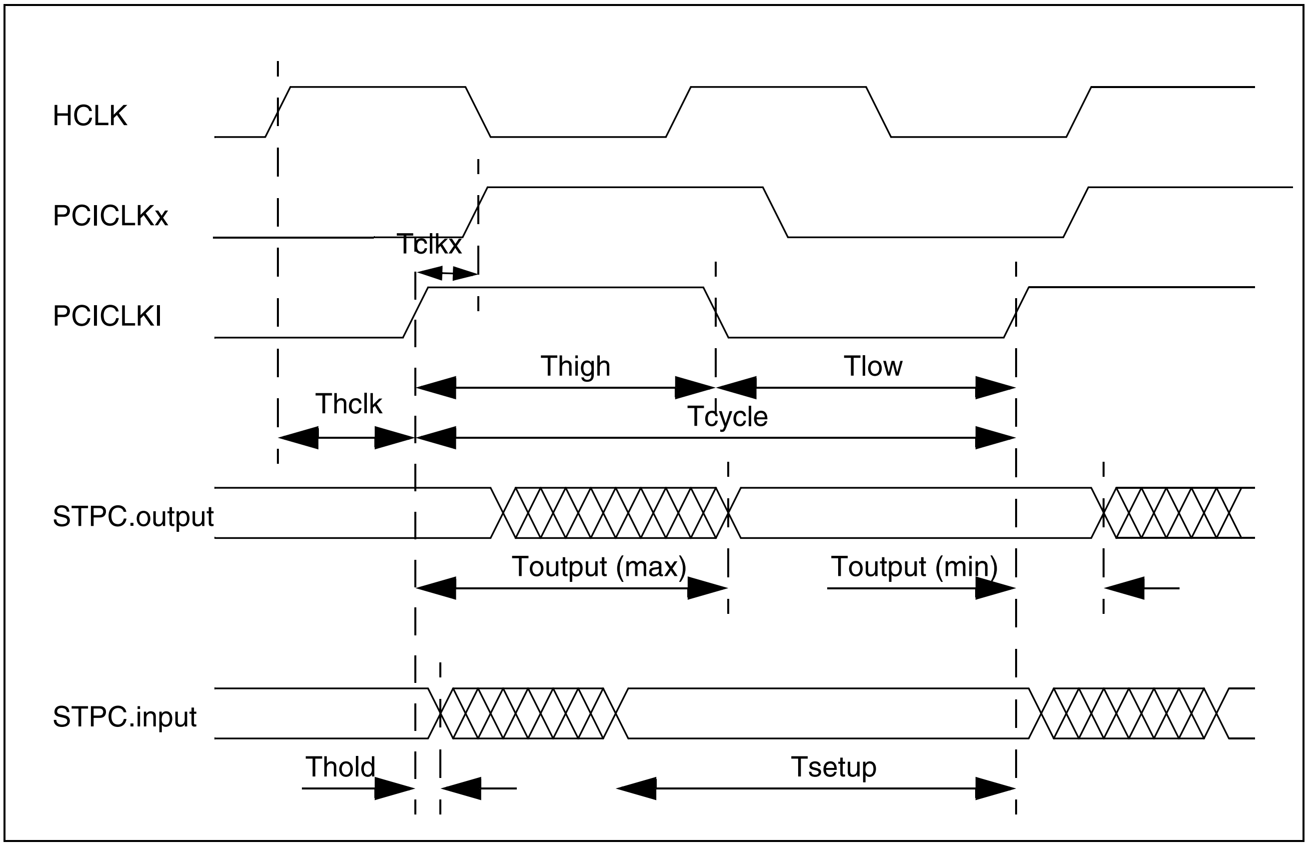


Table 4-12. PCI Bus AC Timings

Name	Parameter	Min	Typ	Max	Unit
	HCLK to PCICLKO delay (MD[30:27] = 1111)	4.4	5.0	5.7	ns
Thclk	HCLK to PCICLKI delay	6.5	7.5	8.5	ns
Tclkx	PCICLKI to PCICLKx skew	-0.5	0.3	1.0	ns
Tcycle	PCICLKI Cycle Time	30			ns
Thigh	PCICLKI High Time	13			ns
Tlow	PCICLKI Low Time	13			ns
Note: These timings are for a load of 50pF.					

4.5.5 IPC INTERFACE

Table 4-13 lists the AC characteristics of the IPC interface.

Figure 4-7. IPC timing diagram

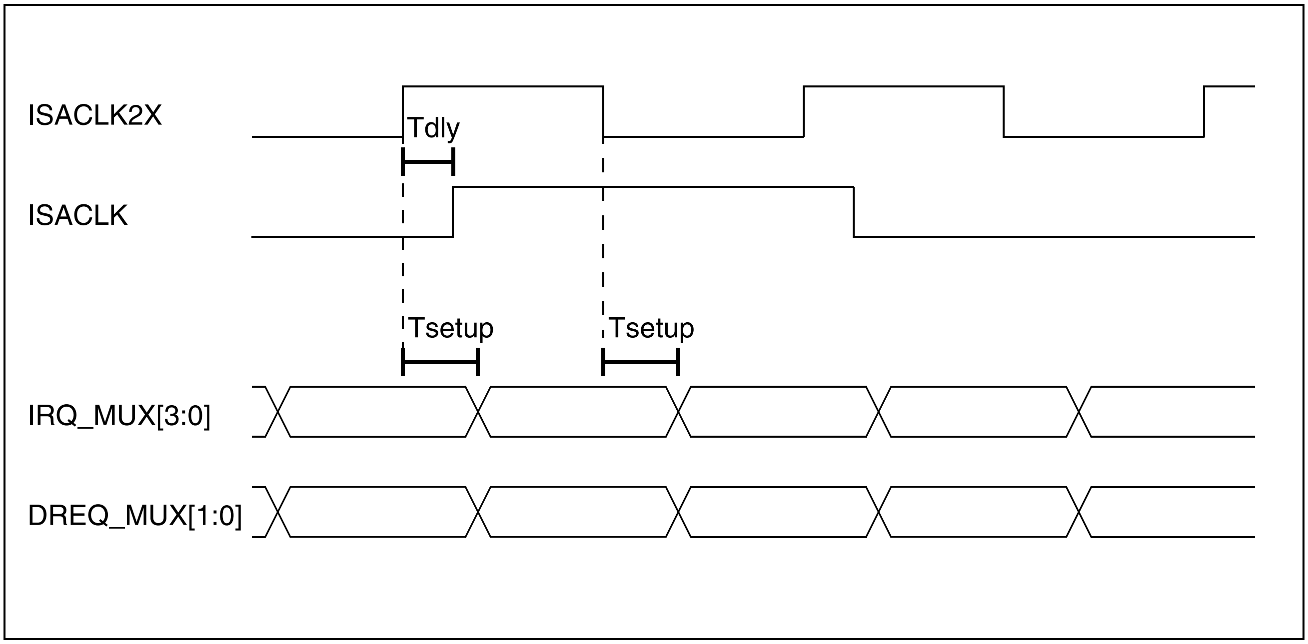


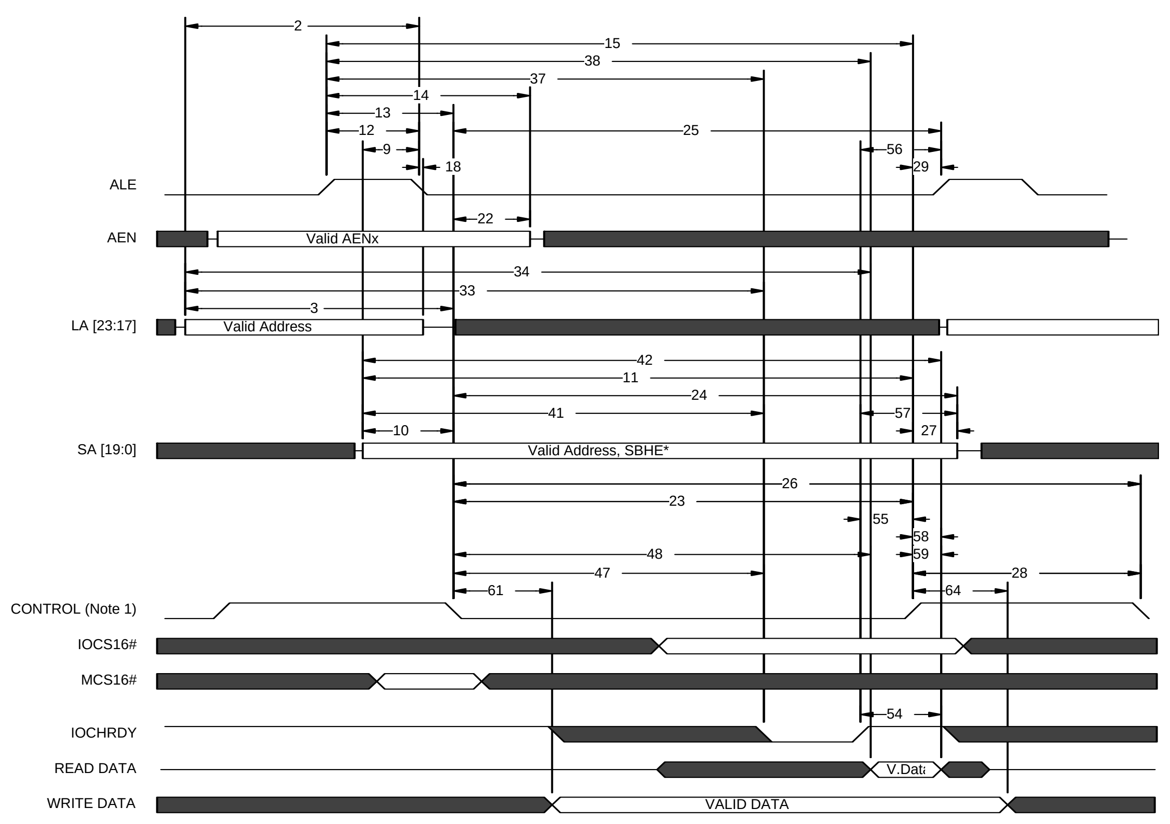
Table 4-13. IPC Interface AC Timings

Name	Parameter	Min	Max	Unit
T_{setup}	IRQ_MUX[3:0] Input setup to ISACLK2X	0	-	nS
T_{setup}	DREQ_MUX[1:0] Input setup to ISACLK2X	0	-	nS

4.5.6 ISA INTERFACE AC TIMING CHARACTERISTICS

Figure 4-8 and Table 4-14 list the AC characteristics of the ISA interface.

Figure 4-8. ISA Cycle (ref Table 4-14.)



Note 1: Stands for SMEMR#, SMEMW#, MEMR#, MEMW#, IOR# & IOW#.
The clock has not been represented as it is dependent on the ISA Slave mode.

Table 4-14. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
2	LA[23:17] valid before ALE# negated	5T		Cycles
3	**LA[23:17] valid before MEMR#, MEMW# asserted**			
3a	Memory access to 16-bit ISA Slave	5T		Cycles
3b	Memory access to 8-bit ISA Slave	5T		Cycles
9	SA[19:0] & SBHE valid before ALE# negated	1T		Cycles
10	**SA[19:0] & SBHE valid before MEMR#, MEMW# asserted**			
10a	Memory access to 16-bit ISA Slave	2T		Cycles
10b	Memory access to 8-bit ISA Slave	2T		Cycles
10	**SA[19:0] & SHBE valid before SMEMR#, SMEMW# asserted**			
Note: The signal numbering refers to Figure 4-8				

Table 4-14. ISA Bus AC Timing

Name	Parameter	Min	Max	Units
10c	Memory access to 16-bit ISA Slave	2T		Cycle
10d	Memory access to 8-bit ISA Slave	2T		Cycle
10e	SA[19:0] & SBHE valid before IOR#, IOW# asserted	2T		Cycles
11	**ISACLK2X to IOW# valid**			
11a	Memory access to 16-bit ISA Slave - 2BCLK	2T		Cycles
11b	Memory access to 16-bit ISA Slave - Standard 3BCLK	2T		Cycles
11c	Memory access to 16-bit ISA Slave - 4BCLK	2T		Cycles
11d	Memory access to 8-bit ISA Slave - 2BCLK	2T		Cycles
11e	Memory access to 8-bit ISA Slave - Standard 3BCLK	2T		Cycles
12	ALE# asserted before ALE# negated	1T		Cycles
13	**ALE# asserted before MEMR#, MEMW# asserted**			
13a	Memory Access to 16-bit ISA Slave	2T		Cycles
13b	Memory Access to 8-bit ISA Slave	2T		Cycles
13	**ALE# asserted before SMEMR#, SMEMW# asserted**			
13c	Memory Access to 16-bit ISA Slave	2T		Cycles
13d	Memory Access to 8-bit ISA Slave	2T		Cycles
13e	ALE# asserted before IOR#, IOW# asserted	2T		Cycles
14	**ALE# asserted before AL[23:17]**			
14a	Non compressed	15T		Cycles
14b	Compressed	15T		Cycles
15	**ALE# asserted before MEMR#, MEMW#, SMEMR#, SMEMW# negated**			
15a	Memory Access to 16-bit ISA Slave- 4 BCLK	11T		Cycles
15e	Memory Access to 8-bit ISA Slave- Standard Cycle	11T		Cycles
18a	ALE# negated before LA[23:17] invalid (non compressed)	14T		Cycles
18a	ALE# negated before LA[23:17] invalid (compressed)	14T		Cycles
22	**MEMR#, MEMW# asserted before LA[23:17]**			
22a	Memory access to 16-bit ISA Slave.	13T		Cycles
22b	Memory access to 8-bit ISA Slave.	13T		Cycles
23	**MEMR#, MEMW# asserted before MEMR#, MEMW# negated**			
23b	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
23e	Memory access to 8-bit ISA Slave Standard cycle	9T		Cycles
23	**SMEMR#, SMEMW# asserted before SMEMR#, SMEMW# negated**			
23h	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
23l	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
23	**IOR#, IOW# asserted before IOR#, IOW# negated**			
23o	Memory access to 16-bit ISA Slave Standard cycle	9T		Cycles
23r	Memory access to 8-bit ISA Slave Standard cycle	9T		Cycles
24	**MEMR#, MEMW# asserted before SA[19:0]**			
24b	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
24d	Memory access to 8-bit ISA Slave - 3BLCK	10T		Cycles
24e	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
24f	Memory access to 8-bit ISA Slave - 7BCLK	10T		Cycles
24	**SMEMR#, SMEMW# asserted before SA[19:0]**			
24h	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
Note: The signal numbering refers to Figure 4-8				

Table 4-14. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	24i	Memory access to 16-bit ISA Slave - 4BCLK	10T		Cycles
	24k	Memory access to 8-bit ISA Slave - 3BCLK	10T		Cycles
	24l	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
24	**IOR#, IOW# asserted before SA[19:0]**				
	24o	I/O access to 16-bit ISA Slave Standard cycle	19T		Cycles
	24r	I/O access to 16-bit ISA Slave Standard cycle	19T		Cycles
25	**MEMR#, MEMW# asserted before next ALE# asserted**				
	25b	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25d	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
25	**SMEMR#, SMEMW# asserted before next ALE# asserted**				
	25e	Memory access to 16-bit ISA Slave - 2BCLK	10T		Cycles
	25f	Memory access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25h	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
25	**IOR#, IOW# asserted before next ALE# asserted**				
	25i	I/O access to 16-bit ISA Slave Standard cycle	10T		Cycles
	25k	I/O access to 16-bit ISA Slave Standard cycle	10T		Cycles
26	**MEMR#, MEMW# asserted before next MEMR#, MEMW# asserted**				
	26b	Memory access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26d	Memory access to 8-bit ISA Slave Standard cycle	12T		Cycles
26	**SMEMR#, SMEMW# asserted before next SMEMR#, SMEMW# asserted**				
	26f	Memory access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26h	Memory access to 8-bit ISA Slave Standard cycle	12T		Cycles
26	**IOR#, IOW# asserted before next IOR#, IOW# asserted**				
	26i	I/O access to 16-bit ISA Slave Standard cycle	12T		Cycles
	26k	I/O access to 8-bit ISA Slave Standard cycle	12T		Cycles
28	**Any command negated to MEMR#, SMEMR#, MEMR#, SMEMW# asserted**				
	28a	Memory access to 16-bit ISA Slave	3T		Cycles
	28b	Memory access to 8-bit ISA Slave	3T		Cycles
28	**Any command negated to IOR#, IOW# asserted**				
	28c	I/O access to ISA Slave	3T		Cycles
29a	MEMR#, MEMW# negated before next ALE# asserted		1T		Cycles
29b	SMEMR#, SMEMW# negated before next ALE# asserted		1T		Cycles
29c	IOR#, IOW# negated before next ALE# asserted		1T		Cycles
33	**LA[23:17] valid to IOCHRDY negated**				
	33a	Memory access to 16-bit ISA Slave - 4 BCLK	8T		Cycles
	33b	Memory access to 8-bit ISA Slave - 7 BCLK	14T		Cycles
34	**LA[23:17] valid to read data valid**				
	34b	Memory access to 16-bit ISA Slave Standard cycle	8T		Cycles
	34e	Memory access to 8-bit ISA Slave Standard cycle	14T		Cycles
37	**ALE# asserted to IOCHRDY# negated**				
	37a	Memory access to 16-bit ISA Slave - 4 BCLK	6T		Cycles
	37b	Memory access to 8-bit ISA Slave - 7 BCLK	12T		Cycles
	37c	I/O access to 16-bit ISA Slave - 4 BCLK	6T		Cycles
	37d	I/O access to 8-bit ISA Slave - 7 BCLK	12T		Cycles
Note: The signal numbering refers to Figure 4-8					

Table 4-14. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
38	**ALE# asserted to read data valid**				
	38b	Memory access to 16-bit ISA Slave Standard Cycle	4T		Cycles
	38e	Memory access to 8-bit ISA Slave Standard Cycle	10T		Cycles
	38h	I/O access to 16-bit ISA Slave Standard Cycle	4T		Cycles
	38l	I/O access to 8-bit ISA Slave Standard Cycle	10T		Cycles
41	**SA[19:0] SBHE valid to IOCHRDY negated**				
	41a	Memory access to 16-bit ISA Slave	6T		Cycles
	41b	Memory access to 8-bit ISA Slave	12T		Cycles
	41c	I/O access to 16-bit ISA Slave	6T		Cycles
	41d	I/O access to 8-bit ISA Slave	12T		Cycles
42	**SA[19:0] SBHE valid to read data valid**				
	42b	Memory access to 16-bit ISA Slave Standard cycle	4T		Cycles
	42e	Memory access to 8-bit ISA Slave Standard cycle	10T		Cycles
	42h	I/O access to 16-bit ISA Slave Standard cycle	4T		Cycles
	42l	I/O access to 8-bit ISA Slave Standard cycle	10T		Cycles
47	**MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# asserted to IOCHRDY negated**				
	47a	Memory access to 16-bit ISA Slave	2T		Cycles
	47b	Memory access to 8-bit ISA Slave	5T		Cycles
	47c	I/O access to 16-bit ISA Slave	2T		Cycles
	47d	I/O access to 8-bit ISA Slave	5T		Cycles
48	**MEMR#, SMEMR#, IOR# asserted to read data valid**				
	48b	Memory access to 16-bit ISA Slave Standard Cycle	2T		Cycles
	48e	Memory access to 8-bit ISA Slave Standard Cycle	5T		Cycles
	48h	I/O access to 16-bit ISA Slave Standard Cycle	2T		Cycles
	48l	I/O access to 8-bit ISA Slave Standard Cycle	5T		Cycles
54	**IOCHRDY asserted to read data valid**				
	54a	Memory access to 16-bit ISA Slave	1T(R)/2T(W)		Cycles
	54b	Memory access to 8-bit ISA Slave	1T(R)/2T(W)		Cycles
	54c	I/O access to 16-bit ISA Slave	1T(R)/2T(W)		Cycles
	54d	I/O access to 8-bit ISA Slave	1T(R)/2T(W)		Cycles
55a	IOCHRDY asserted to MEMR#, MEMW#, SMEMR#, SMEMW#, IOR#, IOW# negated		1T		Cycles
55b	IOCHRY asserted to MEMR#, SMEMR# negated (refresh)		1T		Cycles
56	IOCHRDY asserted to next ALE# asserted		2T		Cycles
57	IOCHRDY asserted to SA[19:0], SBHE invalid		2T		Cycles
58	MEMR#, IOR#, SMEMR# negated to read data invalid		0T		Cycles
59	MEMR#, IOR#, SMEMR# negated to data bus float		0T		Cycles
61	**Write data before MEMW# asserted**				
	61a	Memory access to 16-bit ISA Slave	2T		Cycles
	61b	Memory access to 8-bit ISA Slave (Byte copy at end of start)	2T		Cycles
61	**Write data before SMEMW# asserted**				
	61c	Memory access to 16-bit ISA Slave	2T		Cycles
	61d	Memory access to 8-bit ISA Slave	2T		Cycles
61	**Write Data valid before IOW# asserted**				
Note: The signal numbering refers to Figure 4-8					

Table 4-14. ISA Bus AC Timing

Name	Parameter		Min	Max	Units
	61e	I/O access to 16-bit ISA Slave	2T		Cycles
	61f	I/O access to 8-bit ISA Slave	2T		Cycles
64a	MEMW# negated to write data invalid - 16-bit		1T		Cycles
64b	MEMW# negated to write data invalid - 8-bit		1T		Cycles
64c	SMEMW# negated to write data invalid - 16-bit		1T		Cycles
64d	SMEMW# negated to write data invalid - 8-bit		1T		Cycles
64e	IOW# negated to write data invalid		1T		Cycles
64f	MEMW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master		1T		Cycles
64g	IOW# negated to copy data float, 8-bit ISA Slave, odd Byte by ISA Master		1T		Cycles
Note: The signal numbering refers to Figure 4-8					

4.5.7. LOCAL BUS INTERFACE

Figure 4-3 to Figure 4-12 and Table 4-16 list the AC characteristics of the Local Bus interface.

Figure 4-9. Synchronous Read Cycle

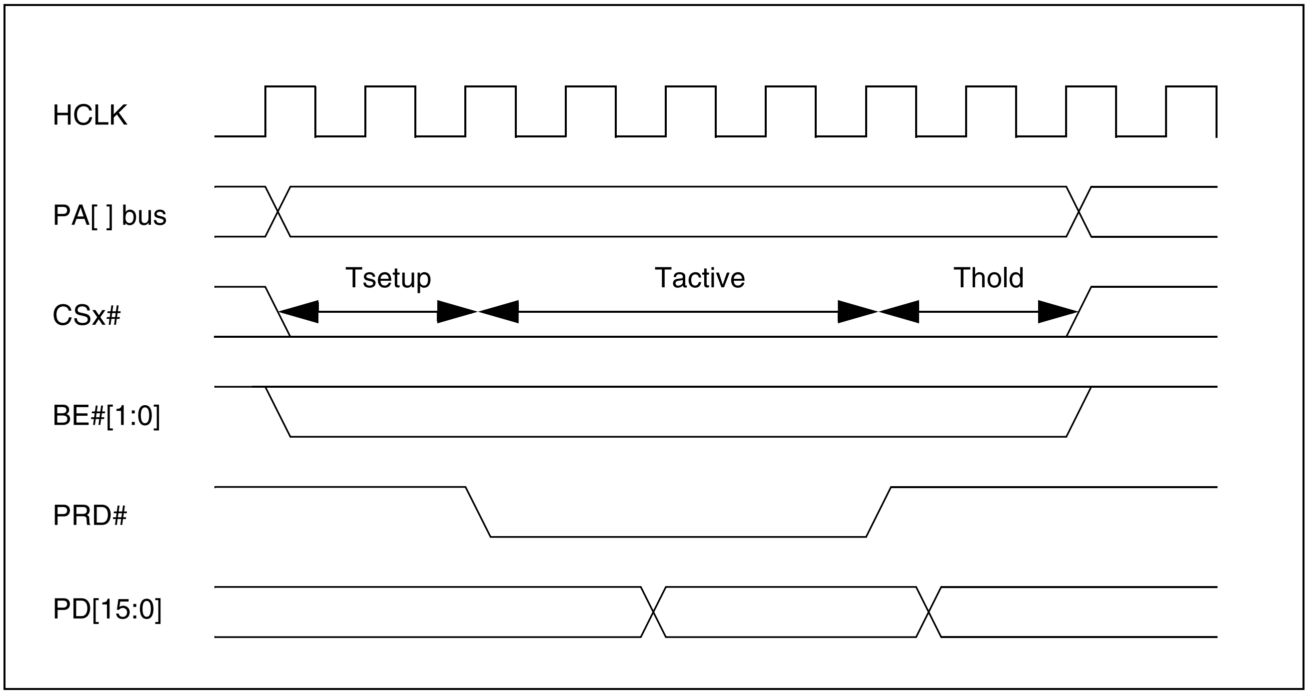


Figure 4-10. Asynchronous Read Cycle

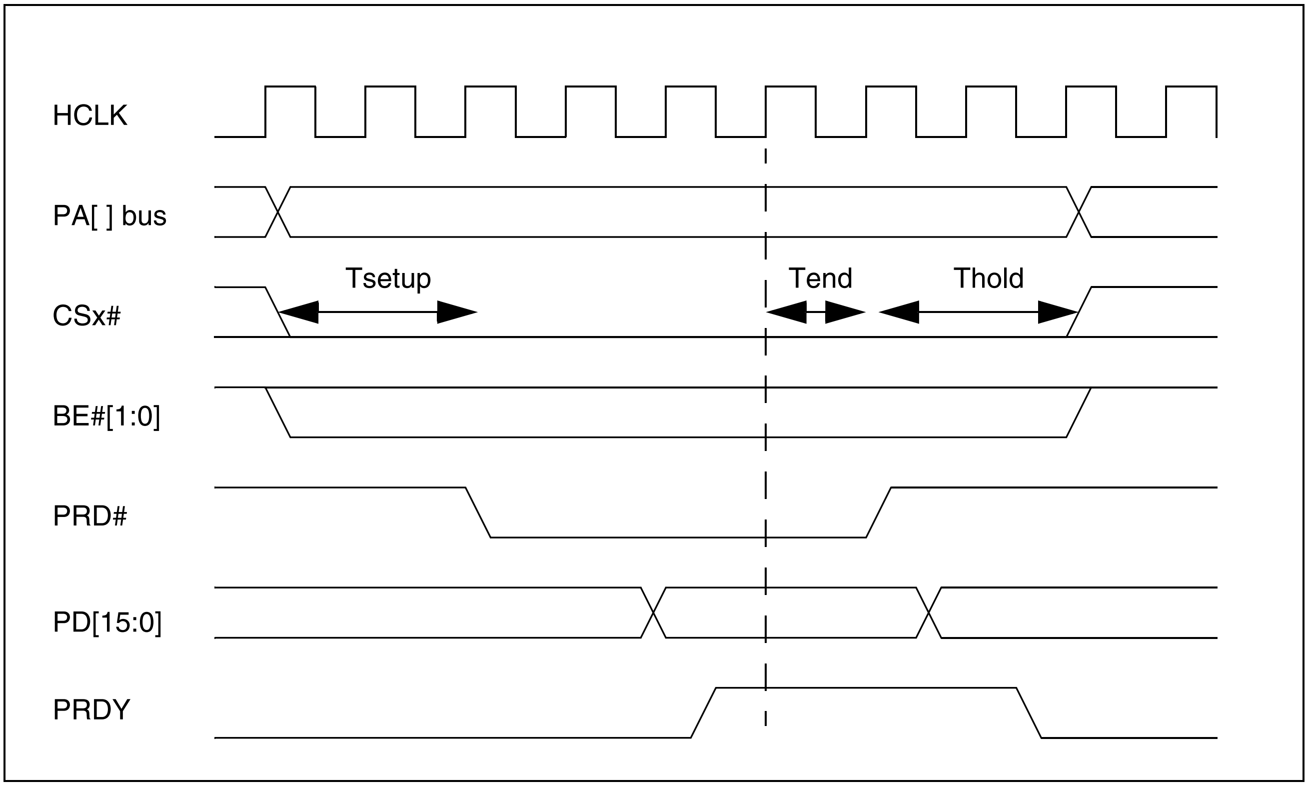


Figure 4-11. Synchronous Write Cycle

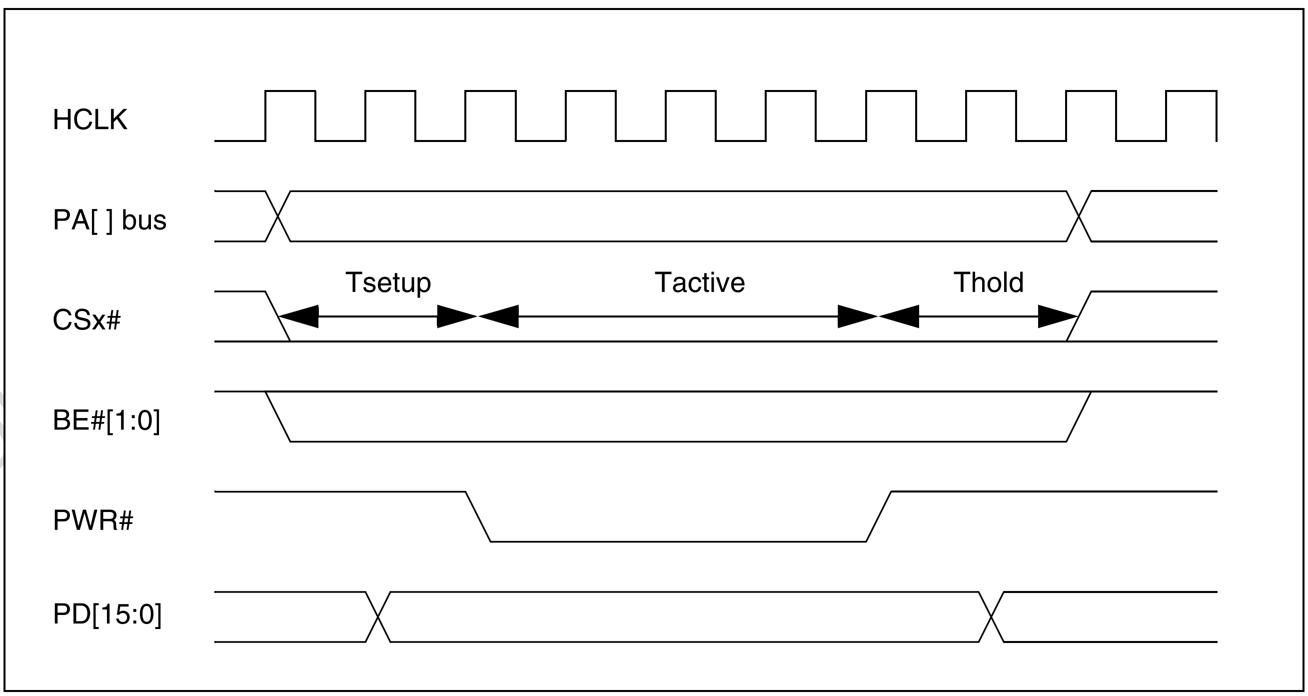
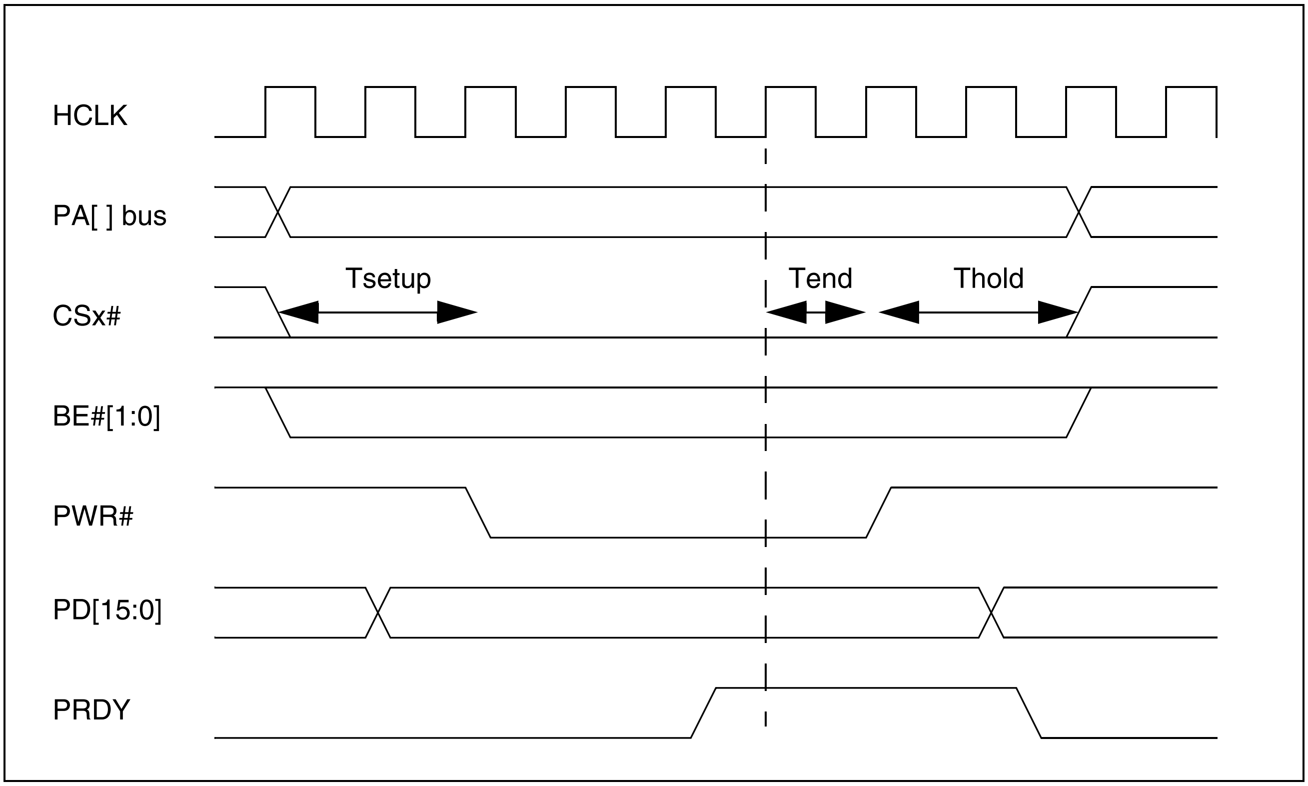


Figure 4-12. Asynchronous Write Cycle



The Table 4-15. below refers to Vh, Va, Vs which are the register value for Setup time, Active Time and Hold time, as described in the Programming Manual.

Table 4-15. Local Bus cycle lenght

Cycle	T_{setup}	T_{active}	T_{hold}	T_{end}	Unit
Memory (FCSx#)	4 + Vh	2 + Va	4 + Vs	4	HCLK
Peripheral (IOCSx#)	4 + Vh	2 + Va	4 + Vs	4	HCLK

Table 4-16. Local Bus Interface AC Timing

Name	Parameters	Min	Max	Units
	HCLK to PA bus	-	15	nS
	HCLK to PD bus	-	15	nS
	HCLK to FCS#[1:0]	-	15	nS
	HCLK to IOCS#[3:0]	-	15	nS
	HCLK to PWR#, PRD#	-	15	nS
	HCLK to BE#[1:0]	-	15	nS
	PD[15:0] Input setup to HCLK	-	4	nS
	PD[15:0] Input hold to HCLK	2	-	nS
	PRDY Input setup to HCLK	-	4	nS
	PRDY Input hold to HCLK	2	-	nS

4.5.8 PCMCIA INTERFACE

Table 4-17 lists the AC characteristics of the PCMCIA interface.

Table 4-17. PCMCIA Interface AC Timing

Name	Parameters	Min	Max	Units
t27	Input setup to ISACLK2X	24		nS
t28	Input hold from ISACLK2X	5		nS
t29	ISACLK2X to IORD	-	55	nS
t30	ISACLK2X to IORW	-	55	nS
t31	ISACLK2X to AD[25:0]	-	25	nS
t32	ISACLK2X to OE#	2	55	nS
t33	ISACLK2X to WE#	2	55	nS
t34	ISACLK2X to DATA[15:0]	0	35	nS
t35	ISACLK2X to INPACK	2	55	nS
t36	ISACLK2X to CE1#	7	65	nS
t37	ISACLK2X to CE2#	7	65	nS
t38	ISACLK2X to RESET	2	55	nS

4.5.9 IDE INTERFACE

Figure 4-13, Figure 4-14 and Table 4-18 lists the AC characteristics of the IDE interface.

Figure 4-13. IDE PIO timing diagram

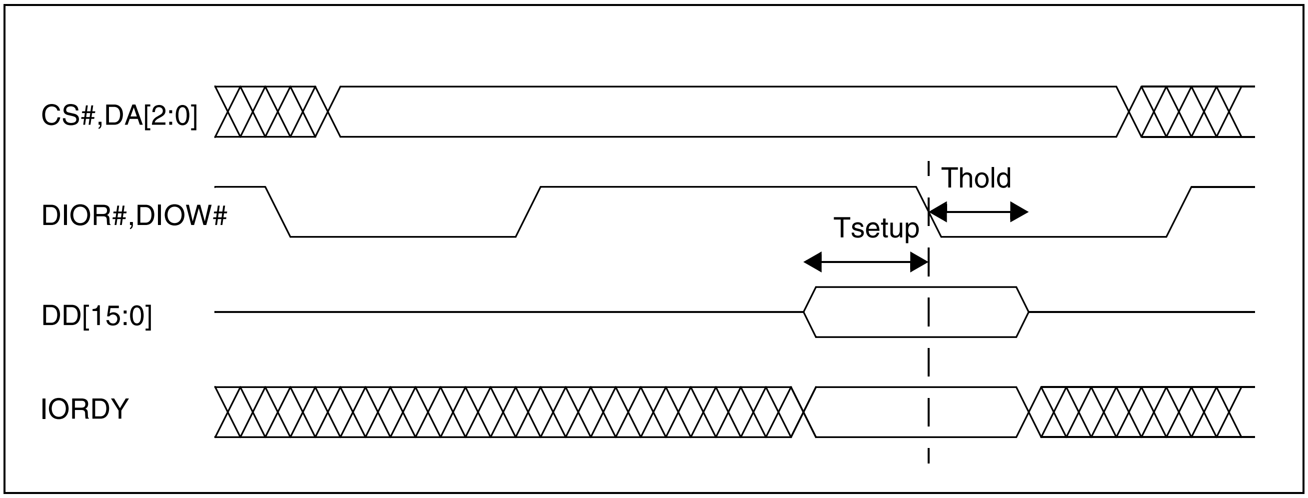


Figure 4-14. IDE DMA timing diagram

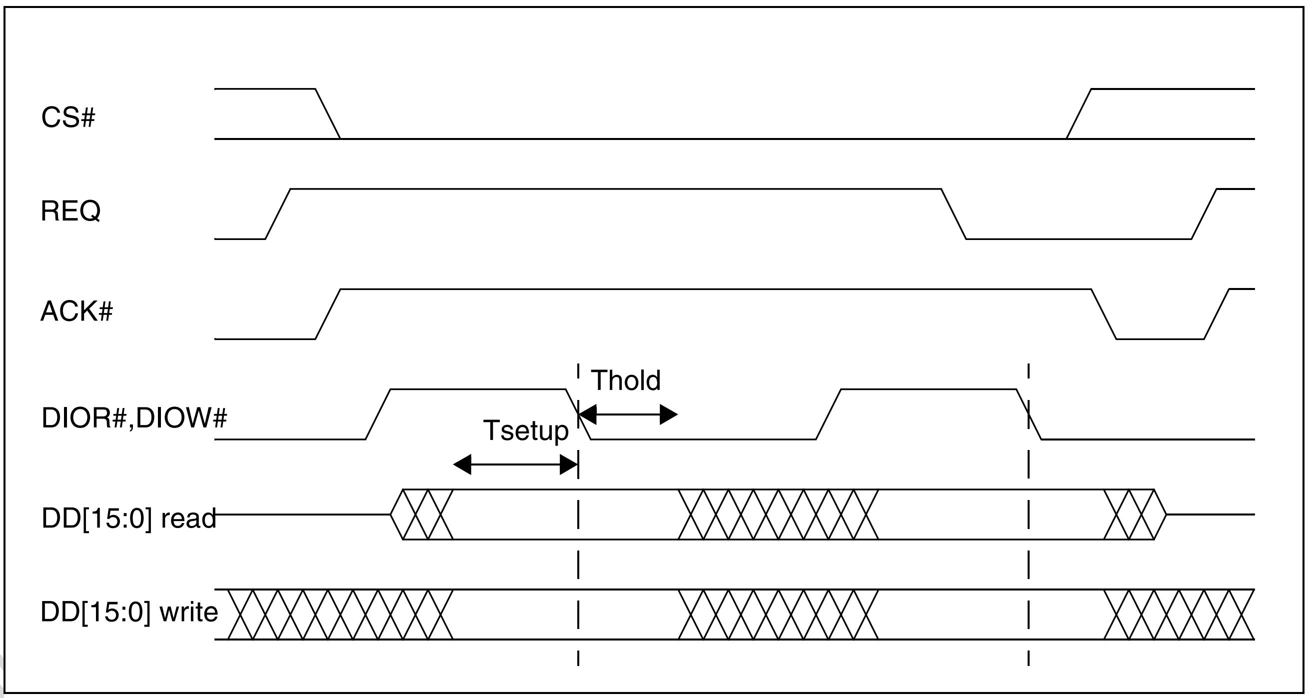


Table 4-18. IDE Interface Timing

Name	Parameters	Min	Max	Units
Tsetup	DD[15:0] setup to PIOR#/SIOR# falling	15	-	ns
Thold	DD[15:0} hold to PIOR#/SIOR# falling	0	-	ns

4.5.10 TFT INTERFACE

Table 4-19 lists the AC characteristics of the TFT interface.

Table 4-19. TFT Interface Timings

Name	Parameters	Min	Max	Units
	DCLK (input) to R[5:0], G[5:0], B[5;0]			nS
	DCLK (input) to FPLINE			nS
	DCLK (input) to FPFRAME			nS
	DCLK (output) to R[5:0], G[5:0], B[5;0]		15	nS
	DCLK (output) to FPLINE		15	nS
	DCLK (output) to FPFRAME		15	nS

4.5.11 USB INTERFACE

The USB interface integrated into the STPC device is compliant with the USB 1.1 standard.

4.5.12 KEYBOARD & MOUSE INTERFACES

Table 4-20 and Table 4-21 list the AC characteristics of the Keyboard and Mouse interfaces.

Table 4-20. Keyboard Interface AC Timing

Name	Parameters	Min	Max	Units
	Input setup to KBCLK	5	-	nS
	Input hold to KBCLK	1	-	nS
	KBCLK to KBDATA	-	12	nS

Table 4-21. Mouse Interface AC Timing

Name	Parameters	Min	Max	Units
	Input setup to MCLK	5	-	nS
	Input hold to MCLK	1	-	nS
	MCLK to MDATA	-	12	nS

4.5.13 IEEE1284 INTERFACE

Table 4-22 lists the AC characteristics of the Keyboard and Mouse interfaces.

Table 4-22. Parallel Interface AC Timing

Name	Parameters	Min	Max	Units
	STROBE# to BUSY setup	0	-	nS
	PD bus to AUTPFD# hold	0	-	nS
	PB bus to BUSY setup	0	-	nS

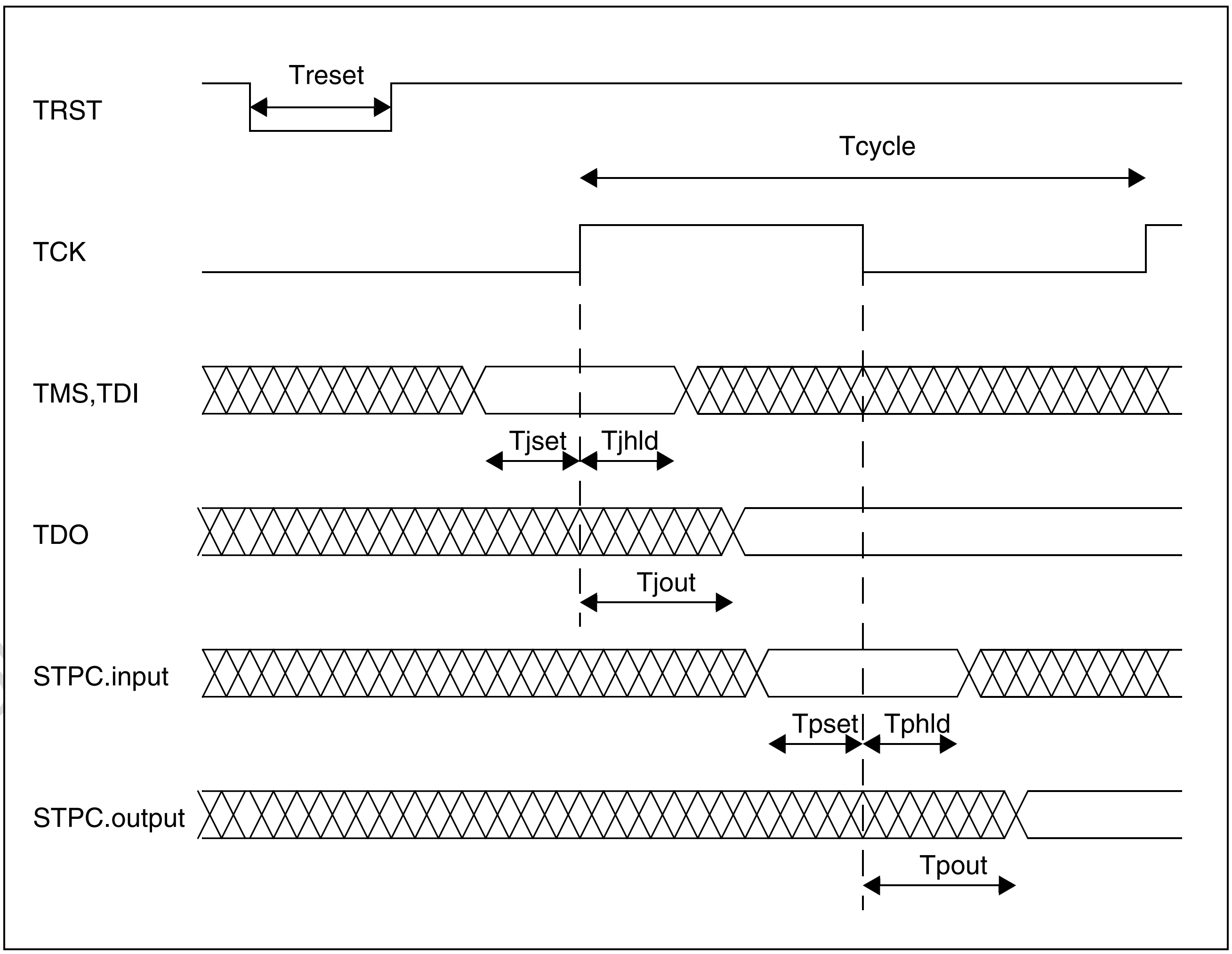
4.5.14 JTAG INTERFACE

Figure 4-15 lists the AC characteristics of the JTAG interface.

Table 4-23. JTAG AC Timings

Name	Parameter	Min	Max	Unit
Treset	TRST pulse width	1		Tcycle
Tcycle	TCLK period	400		ns
	TCLK rising time		20	ns
	TCLK falling time		20	ns
Tjset	TMS setup time	200		ns
Tjhld	TMS hold time	200		ns
Tjset	TDI setup time	200		ns
Tjhld	TDI hold time	200		ns
Tjout	TCLK to TDO valid		30	ns
Tpset	STPC pin setup time	30		ns
Tphld	STPC pin hold time	30		ns
Tpout	TCLK to STPC pin valid		30	ns

Figure 4-15. JTAG timing diagram



5 MECHANICAL DATA

5.1. 516-PIN PACKAGE DIMENSION

The pin numbering for the STPC 516-pin Plastic BGA package is shown in Figure 5-1.

Dimensions are shown in Figure 5-2, Table 5-1. and Figure 5-3, Table 5-2..

Figure 5-1. 516-Pin PBGA Package - Top View

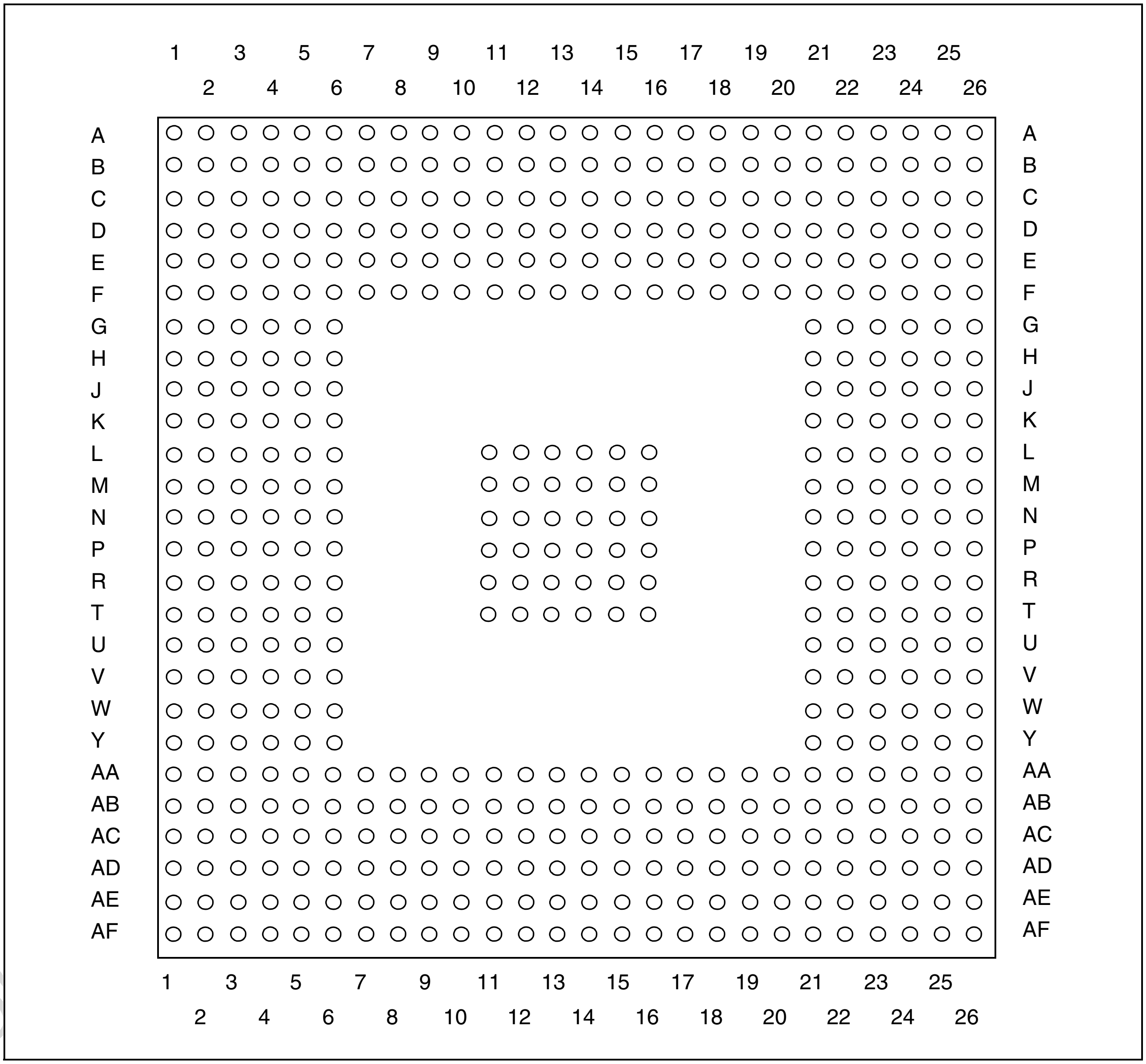


Figure 5-2. 516-pin PBGA Package - PCB Dimensions

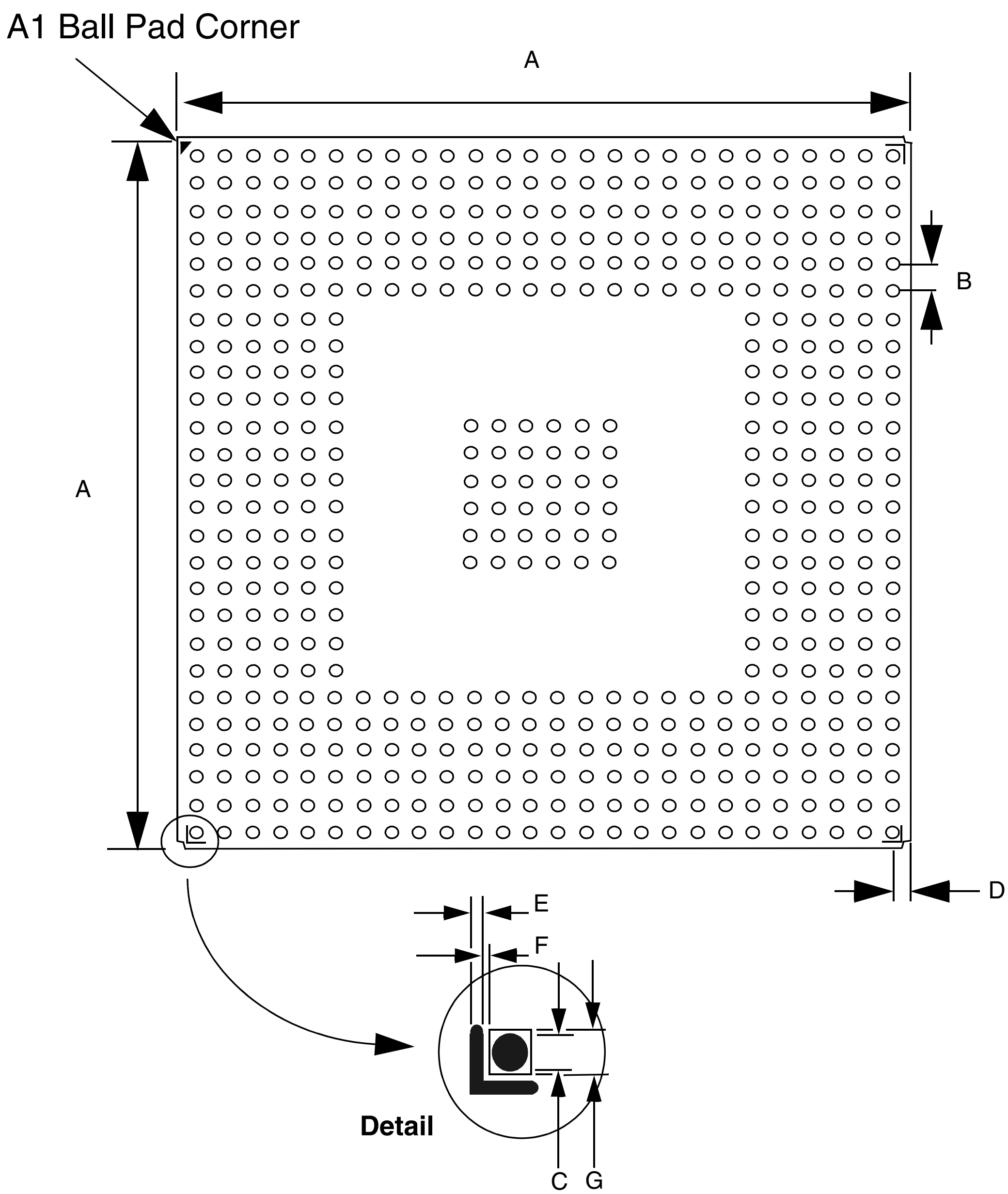


Table 5-1. 516-pin PBGA Package - PCB Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	34.80	35.00	35.20	1.370	1.378	1.386
B	1.22	1.27	1.32	0.048	0.050	0.052
C	0.60	0.76	0.90	0.024	0.030	0.035
D	1.57	1.62	1.67	0.062	0.064	0.066
E	0.15	0.20	0.25	0.006	0.008	0.001

Table 5-1. 516-pin PBGA Package - PCB Dimensions

F	0.05	0.10	0.15	0.002	0.004	0.006
G	0.75	0.80	0.85	0.030	0.032	0.034

Figure 5-3. 516-pin PBGA Package - Dimensions

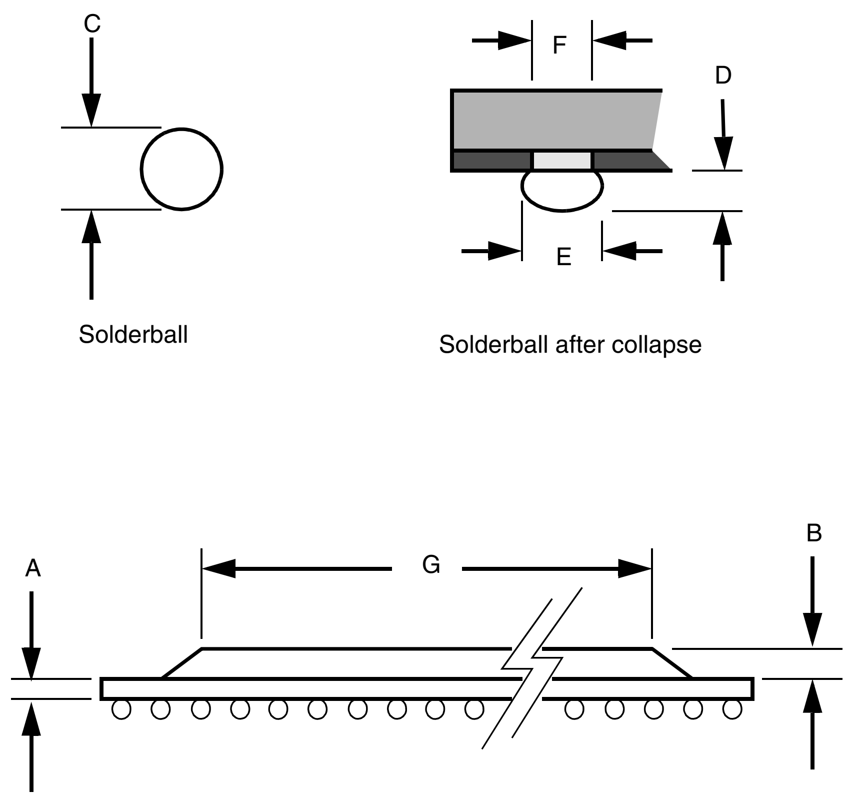


Table 5-2. 516-pin PBGA Package - Dimensions

Symbols	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.56	0.62	0.020	0.022	0.024
B	1.12	1.17	1.22	0.044	0.046	0.048
C	0.60	0.76	0.92	0.024	0.030	0.036
D	0.52	0.53	0.54	0.020	0.021	0.022
E	0.63	0.78	0.93	0.025	0.031	0.037
F	0.60	0.63	0.66	0.024	0.025	0.026
G		30.0			11.8	

5.2. 516-PIN PACKAGE THERMAL DATA

516-pin PBGA package has a Power Dissipation Capability of 4.5W which increases to 6W when used with a Heatsink.

The structure in shown in Figure 5-4.

Thermal dissipation options are illustrated in Figure 5-5 and Figure 5-6.

Figure 5-4. 516-Pin PBGA Structure

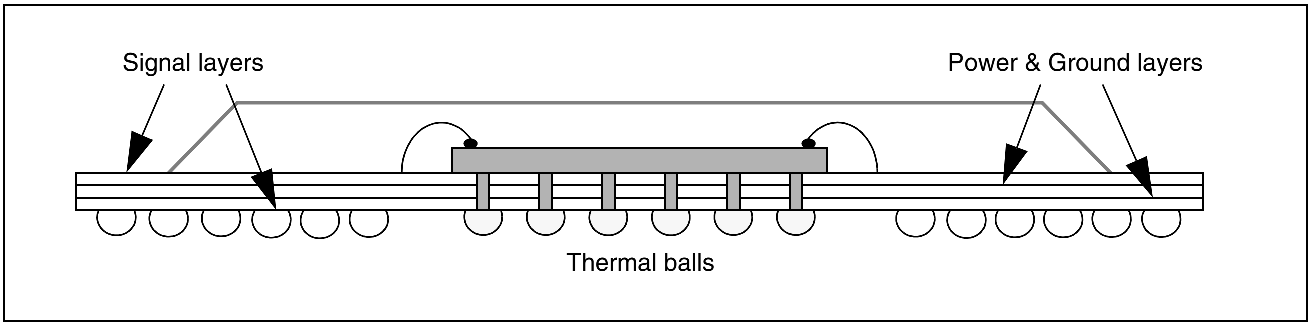


Figure 5-5. Thermal Dissipation Without Heatsink

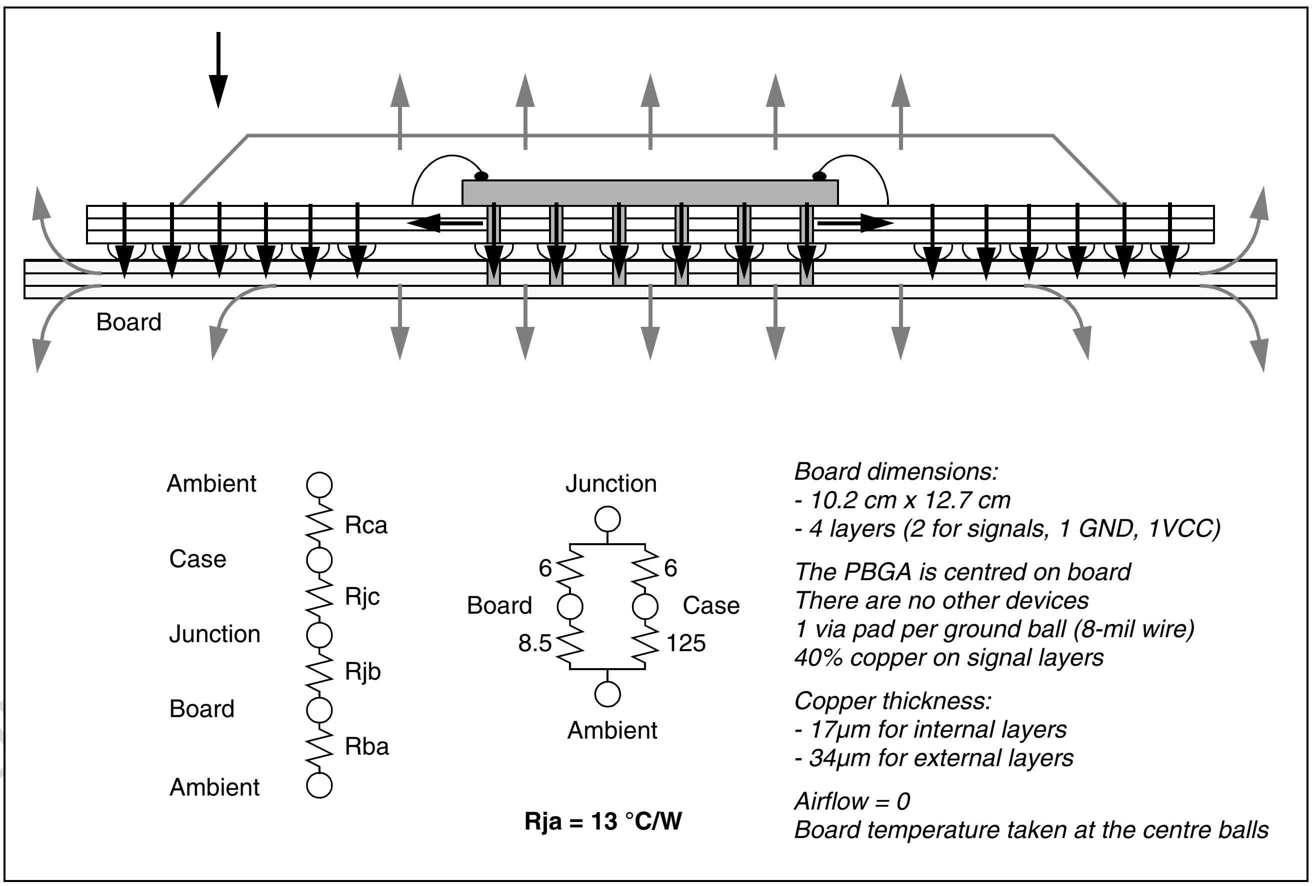
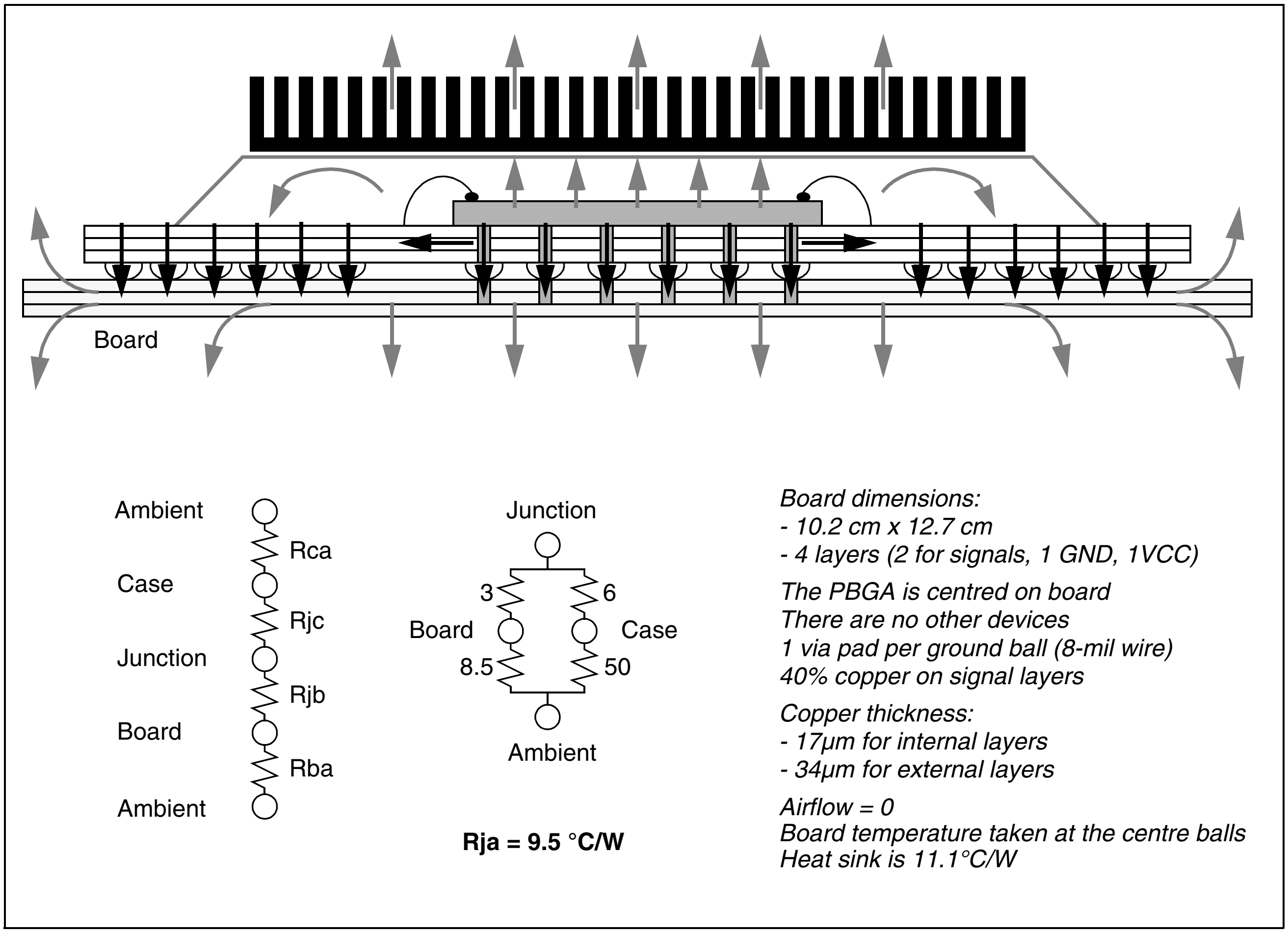


Figure 5-6. Thermal Dissipation With Heatsink



5.3. SOLDERING RECOMMENDATIONS

High quality, low defect soldering requires identifying the **optimum temperature profile** for reflowing the solder paste, therefore optimizing the process. The heating and cooling rise rates must be compatible with the solder paste and components. A typical profile consists of a preheat, dryout, reflow and cooling sections.

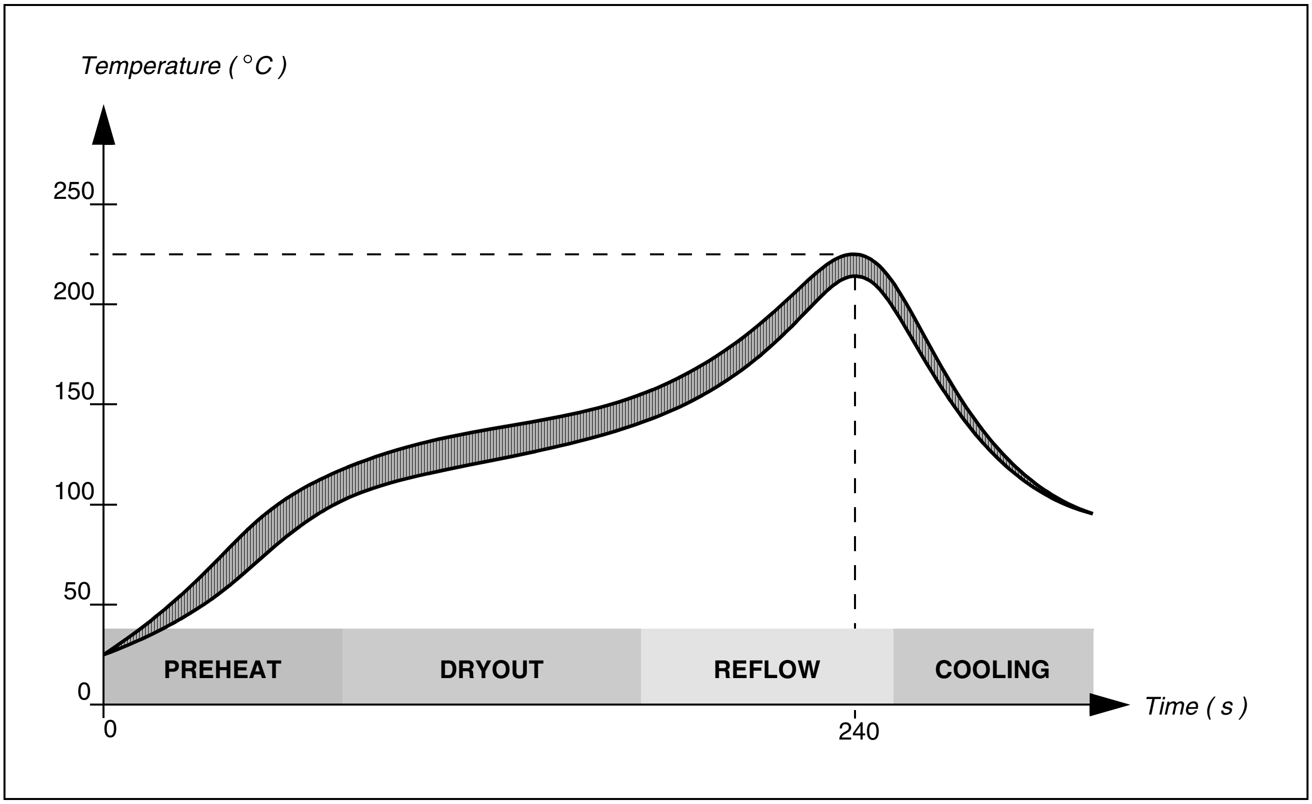
The most critical parameter in the **preheat section** is to minimize the rate of temperature rise to less than 2°C / second, in order to minimize thermal shock on the semi-conductor components.

Dryout section is used primarily to ensure that the solder paste is fully dried before hitting reflow temperatures.

Solder reflow is accomplished in the **reflow zone**, where the solder paste is elevated to a temperature greater than the melting point of the solder. Melting temperature must be exceeded by approximately 20°C to ensure quality reflow.

In reality the profile is not a line, but rather **a range of temperatures** all solder joints must be exposed. The total temperature deviation from component thermal mismatch, oven loading and oven uniformity must be within the band.

Figure 5-7. Reflow soldering temperature range



6 DESIGN GUIDELINES

6.1. TYPICAL APPLICATIONS

The STPC Atlas is well suited for many applications. Some of the possible implementations are described below.

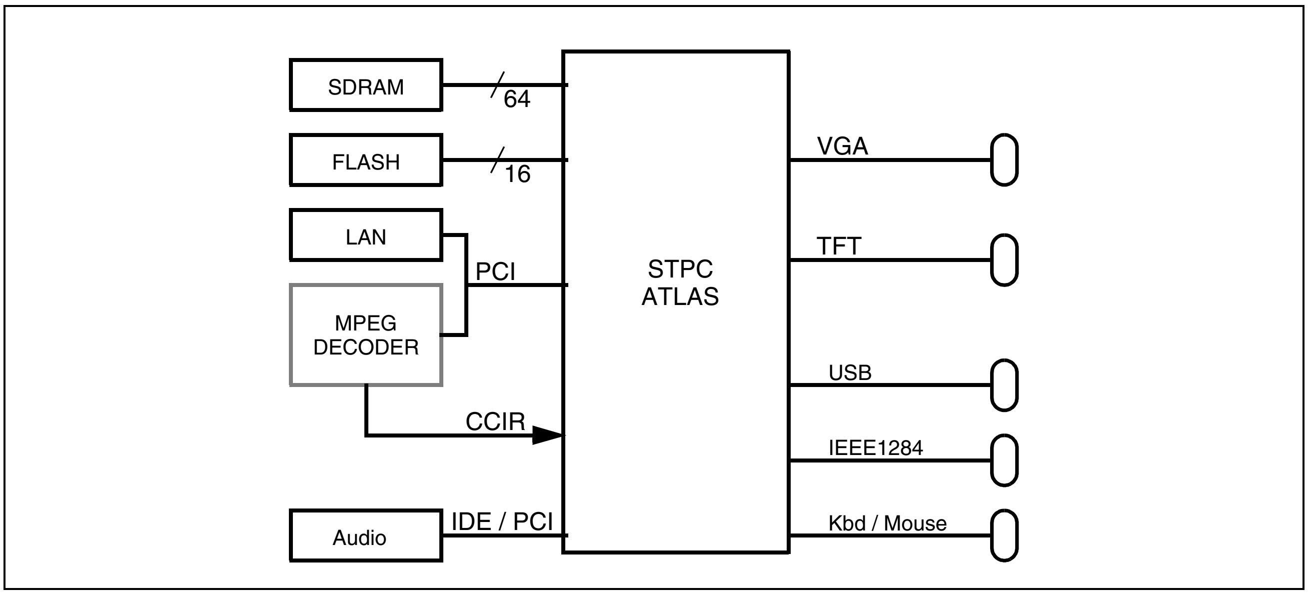
6.1.1. THIN CLIENT

A Thin-Client is a terminal running ICA™ (Citrix) or RDP™ (Microsoft) protocol. The display is computed by the server and sent in a compressed way to the terminal for display. The same streaming approach is used for sending the keyboard/mouse/USB data to the server.

These protocols have room for dedicated data channels in case the terminal is not 'thin' and can execute locally some applications, hence optimizing the bandwidth usage. For example, if a terminal has browsing or MPEG decoding capability, the server will provide internet source files or MPEG streaming.

The same hardware can run X-terminal protocol and can be reconfigured by the server when booting on the network by uploading a different OS and application.

Figure 6-1. Thin-Client - Block Diagram



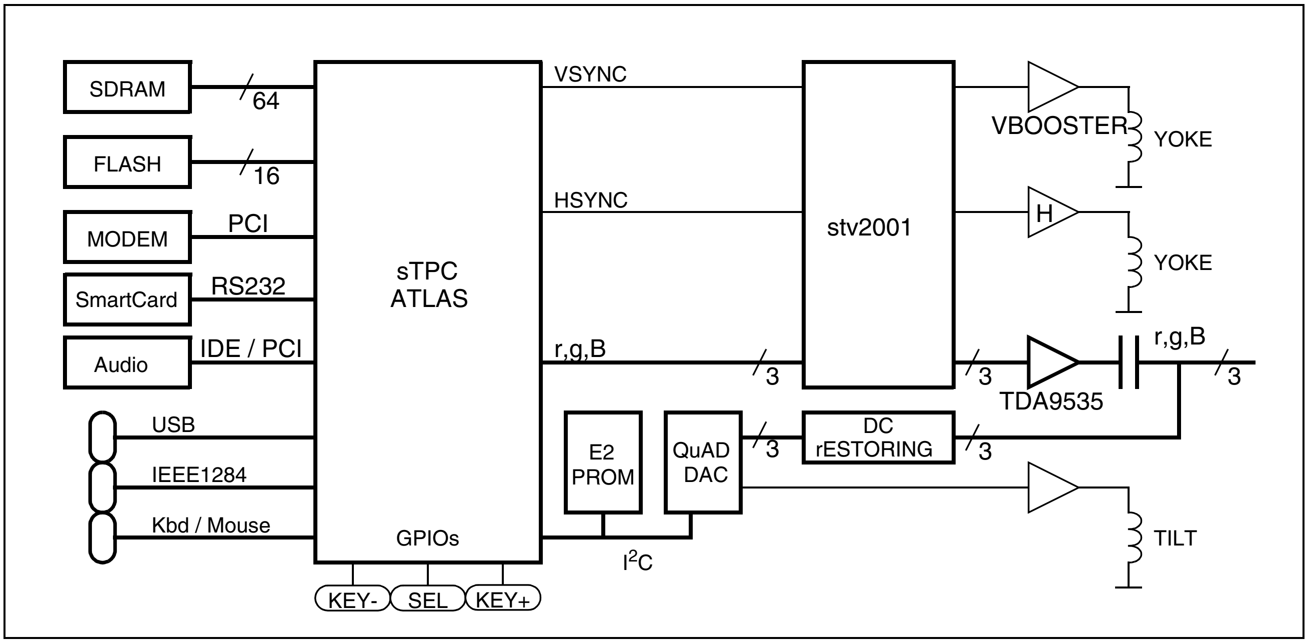
6.1.2. INTERNET TERMINAL

The internet terminal described here is an optimized implementation where the STPC Atlas board is integrated into the CRT itself. The advantages are a reduced overall cost and a good image definition.

The STPC Atlas platform being integrated into the monitor itself enables the choice of a limited amount of horizontal frequencies and simplifies the CRT driving stage:
- 1024x768: 56.5KHz horizontal, 70Hz vertical
- 800x600: 53.7KHz horizontal, 85Hz vertical

Like for the Thin-Client, an external MPEG decoder can be connected to the STPC Atlas through the PCI bus and the Video Input Port.
The same concept can be applied using a TFT display instead of a CRT.

Figure 6-2. Internet Terminal - Block Diagram



6.2. STPC CONFIGURATION

The STPC is a very flexible product thanks to decoupled clock domains and to strap options enabling a user-optimized configuration.

As some trade off are often necessary, it is important to do an analysis of the application needs prior to design a system based on this product. The applicative constraints are usually the following:
- CPU performance
- graphics / video performances
- power consumption
- PCI bandwidth
- booting time
- EMC

Some other elements can help to tune the choice:
- Code size of CPU Consuming tasks
- Data size and location

On the STPC side, the configurable parameters are the following:
- Synchronous / asynchronous mode
- HCLK speed
- MCLK speed
- Local Bus / ISA bus

6.2.1. LOCAL BUS / ISA BUS

The selection between the ISA bus and the Local Bus is relatively simple. The first one is a standard bus but slow. The Local Bus is fast and programmable but doesn't support any DMA nor external master mechanisms. The Table 6-1 below summarize the selection:

Table 6-1. Bus mode selection

Need	Selection
Legacy I/O device (Floppy, ...), Super I/O	ISA Bus
DMA capability (Soundblaster)	ISA Bus
Flash, SRAM, basic I/O device	Local Bus
Fast boot	Local Bus
Boot flash of 4MB or more	Local Bus
Programmable Chip Select	Local Bus

Before implementing a function requiring DMA capability on the ISA bus, it is recommended to check if it exists on PCI, or if it can be implemented differently, in order to use the local bus mode.

6.2.2. CLOCK CONFIGURATION

The CPU clock and the memory clock are independent unless the "synchronous mode" strap option is set (see the STRAP OPTIONS chapter). The potential clock configurations are then

Table 6-2. Main STPC modes

C	Mode	HCLK MHz	CPU clock clock ratio	MCLK MHz
1	Synchronous	66	133 (x2)	66
2	Asynchronous	66	133 (x2)	90

The advantage of the synchronous mode compared to the asynchronous mode is a lower latency when accessing SDRAM from the CPU or the PCI (saves 4 MCLK cycles for the first access of the burst). For the same CPU to Memory transfer performance, MCLK has to be roughly higher by 20MHz between SYNC and ASYNC modes to get the same system performance level (example: 66MHz SYNC = 86MHz ASYNC) .
In all cases, use SDRAM with CAS Latency equals to 2 (CL2) for the best performances.

The advantage of the asynchronous mode is the capability to reprogram the MCLK speed on the fly. This could help for applications where power consumption must be optimized.

The last, and more complex, information to consider is the behaviour of the software. In case high CPU or FPU computation is needed, it is sometime better to be in DX2-133/MCLK=66 synchronous mode than DX2-133/MCLK=90 asynchronous mode. This depends on the locality of the number crunching code and the amount of data manipulated.

The Table 6-3 below gives some examples. The right column correspond to the configuration number as described in Table 6-2 :

Table 6-3. Clock mode selection

Constraints	C
Need CPU power Critical code fits into L1 cache	1
Need CPU power Code or data does not fit into L1 cache	3
Need flexible SDRAM speed	2

Obviously, the values for HCLK or MCLK can be reduced compared to Table 6-2 in case there is no need to push the device at its limits, or when avoiding to use specific frequency ranges (FM radio band for example).

6.3. ARCHITECTURE RECOMMENDATIONS

This section describes the recommend implementations for the STPC interfaces. For more details, download the **Reference Schematics** from the STPC web site.

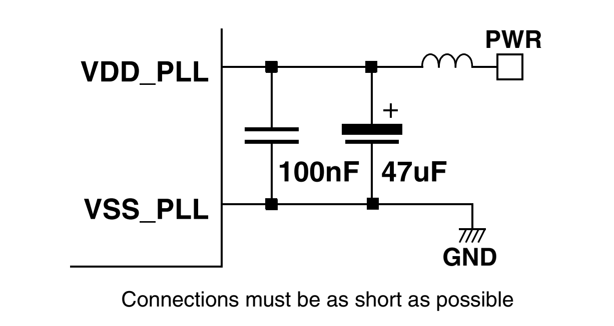
6.3.1. POWER DECOUPLING

An appropriate decoupling of the various STPC power pins is mandatory for optimum behaviour. When insufficient, the integrity of the signals is deteriorated, the stability of the system is reduced and EMC is increased.

6.3.1.1. PLL decoupling

This is the most important as the STPC clocks are generated from a single 14MHz stage using multiple PLLs which are highly sensitive analog cells. The frequencies to filter are the 25-50 KHz range which correspond to the internal loop bandwidth of the PLL and the 10 to 100 MHz frequency of the output. PLL power pins can be tied together to simplify the board layout.

Figure 6-3. PLL decoupling



6.3.1.2. Decoupling of 3.3V and Vcore

A power plane for each of these supplies with one decoupling capacitance for each power pin is the minimum. The use of multiple capacitances with values in decade is the best (for example: 10pF, 1nF, 100nF, 10uF), the smallest value, the closest to the power pin. Connecting the various digital power planes through capacitances will reduce furthermore the overall impedance and electrical noise.

6.3.2. 14MHZ OSCILLATOR STAGE

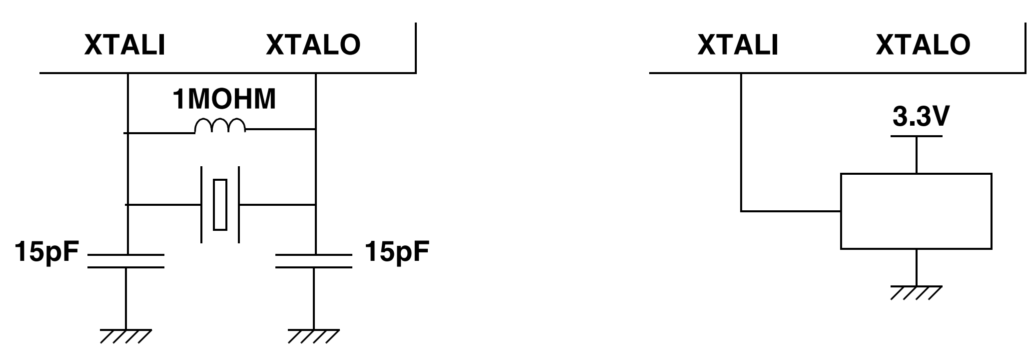
The 14.31818 MHz oscillator stage can be implemented using a quartz, which is the preferred and cheaper solution, or using an external 3.3V oscillator.

The crystal must be used in its series-cut fundamental mode and not in overtone mode. It must have an Equivalent Series Resistance (ESR, sometimes referred to as Rm) of less than 50 Ohms (typically 8 Ohms) and a shunt capacitance (Co) of less than 7 pF. The balance capacitors of 16 pF must be added, one connected to each pin, as described in Figure 6-4.

In the event of an external oscillator providing the master clock signal to the STPC device, the LVTTL signal should be connected to XTALI, as described in Figure 6-4.

As this clock is the reference for all the other on-chip generated clocks, it is **strongly recommended to shield this stage**, including the 2 wires going to the STPC balls, in order to reduce the jitter to the minimum and reach the optimum system stability.

Figure 6-4. 14.31818 MHz stage



6.3.3. SDRAM

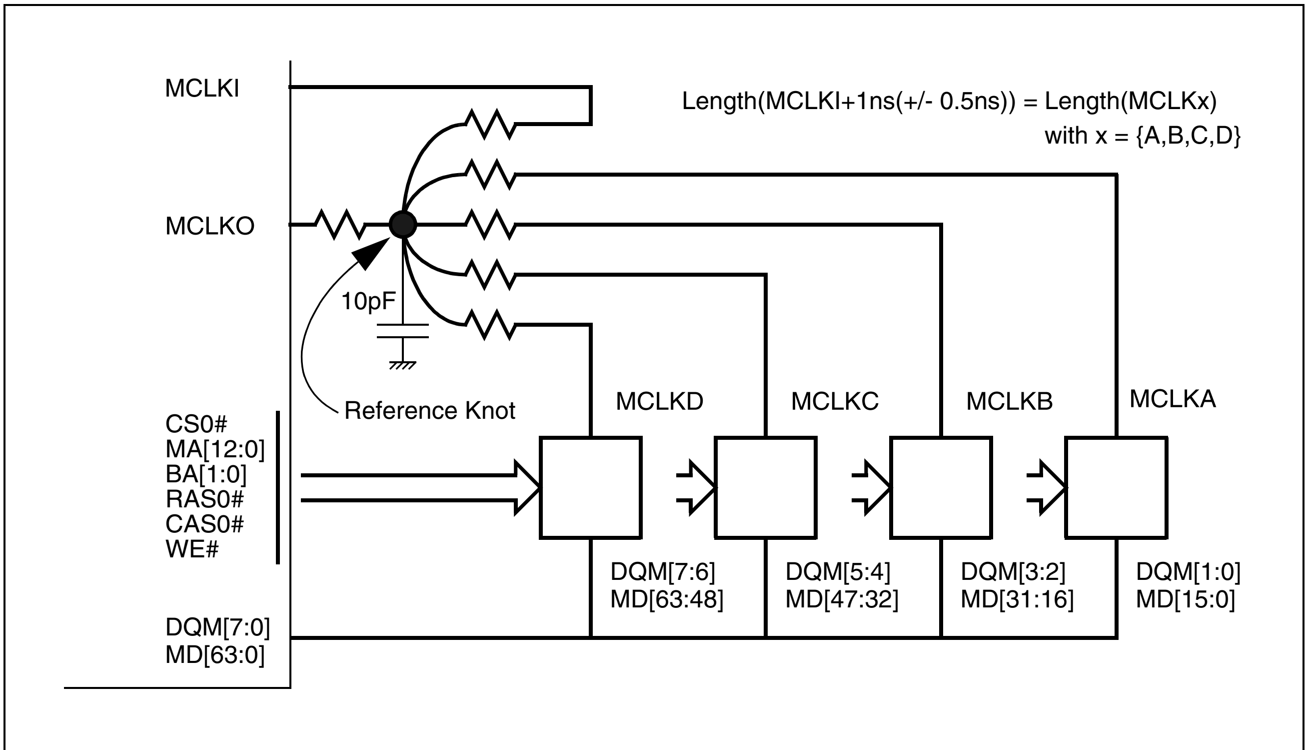
The STPC provides all the signals for SDRAM control. Up to 128 MBytes of main memory are supported. All Banks must be 64 bits wide. Up to 4 memory banks are available when using 16Mbit devices. Only up to 2 banks can be connected when using 64Mbit and 128Mbit components due to the reallocation of CS2# and CS3# signals. This is described in Table 6-4 and Table 6-5.

Graphics memory resides at the beginning of Bank 0. Host memory begins at the top of graphics memory and extends to the top of populated SDRAM. Bank 0 must always be populated.

Figure 6-5, Figure 6-6 and Figure 6-7 show some typical implementations.

The purpose of the serial resistors is to reduce signal oscillation and EMI by filtering line reflections. The capacitance in Figure 6-5 has a filtering effect too, while it is used for propagation delay compensation in the 2 other figures.

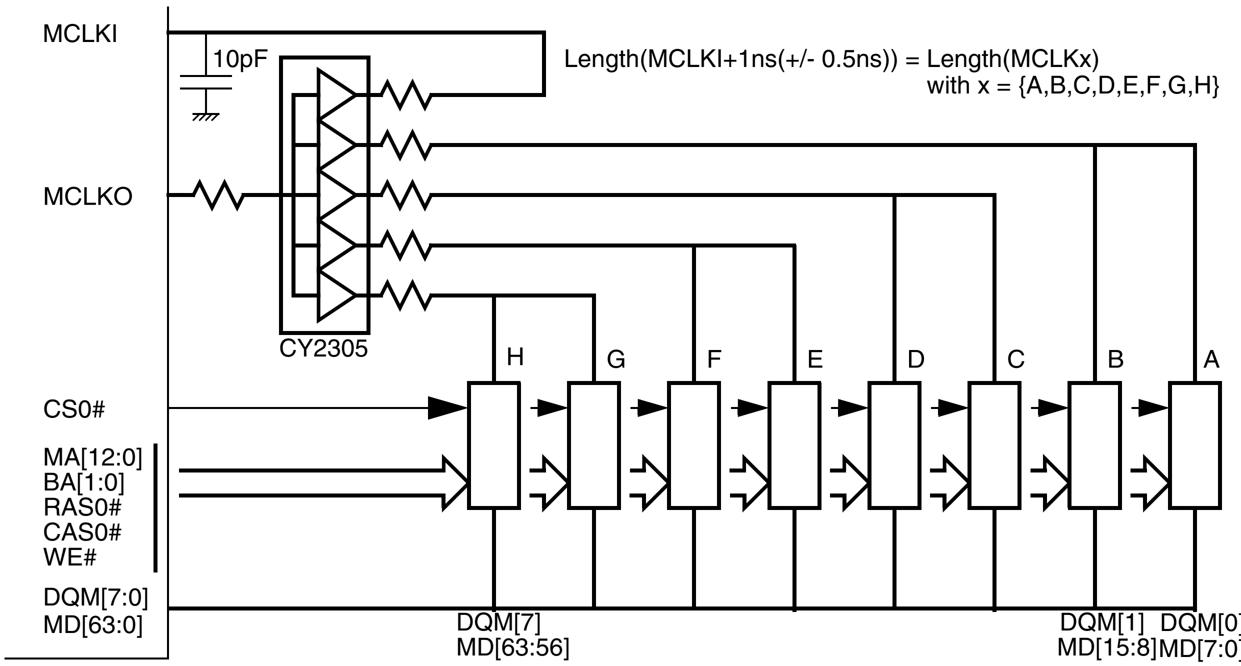
Figure 6-5. One Memory Bank with 4 Chips (16-bit)



Refer to Section 4.5.3. for detailed timing constraints.

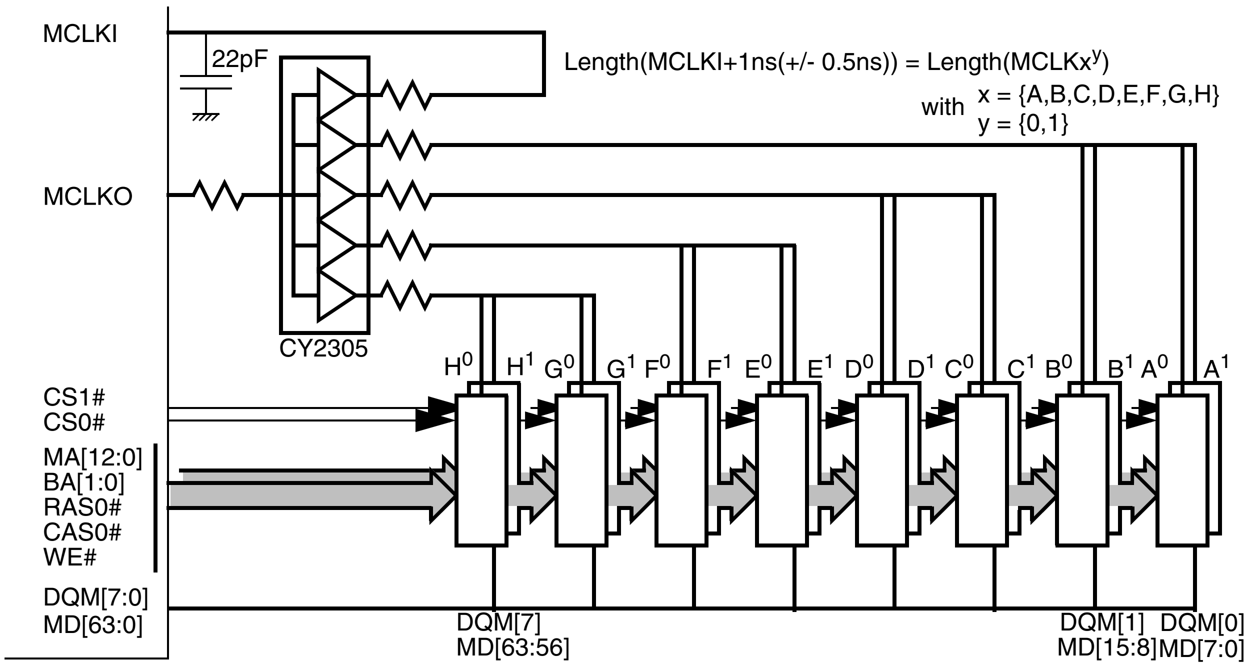
For other implementations like 32-bit SDRAM devices, refers to the SDRAM controller signal multiplexing and address mapping described in the following Table 6-4 and Table 6-5.

Figure 6-6. One Memory Banks with 8 Chips (8-bit)



Refer to Section 4.5.3. for detailed timing constraints.

Figure 6-7. Two Memory Banks with 8 Chips (8-bit)



Refer to Section 4.5.3. for detailed timing constraints.

Table 6-4. DIMM Pinout

SDRAM Density	16 Mbit	64/128 Mbit	64/128 Mbit	STPC I/F
Internal Banks	2 Banks	2 Banks	4 Banks	
DIMM Pin Number				
...	MA[10:0]	MA[10:0]	MA[10:0]	MA[10:0]
123	-	MA11	MA11	CS2# (MA11)
126	-	MA12	-	CS3# (MA12)
39	-	-	BA1 (MA12)	CS3# (BA1)
122	BA0 (MA11)	BA0 (MA13)	BA0 (MA13)	BA0

Table 6-5. Address Mapping

Address Mapping: 16 Mbit - 2 internal banks														
STPC I/F	BA0			MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS Address	A11			A22	A21	A2	A19	A18	A17	A16	A15	A14	A13	A12
CAS Address	A11			0	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3
Address Mapping: 64/128 Mbit - 2 internal banks														
STPC I/F	BA0	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS Address	A11	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
CAS Address	A11	0	0	0	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3
Address Mapping: 64/128 Mbit - 4 internal banks														
STPC I/F	BA0	BA1	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
RAS Address	A11	A12	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
CAS Address	A11	A12	0	0	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3

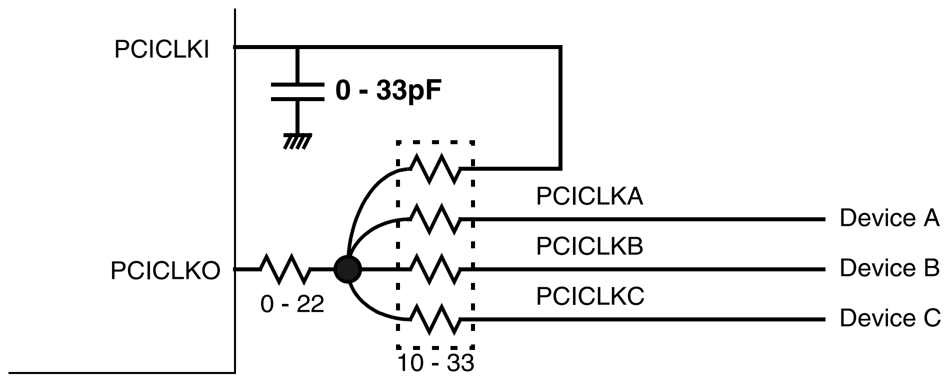
6.3.4. PCI BUS

The PCI bus is always active and the following control signals must be pulled-up to 3.3V or 5V through 8K2 resistors even if this bus is not connected to an external device: FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, LOCK#, SERR#, PERR#, PCI_REQ#[2:0].

PCI_CLKO must be connected to PCI_CLKI through a 10 to 33 Ohms resistor. Figure 6-8 shows a typical implementation.

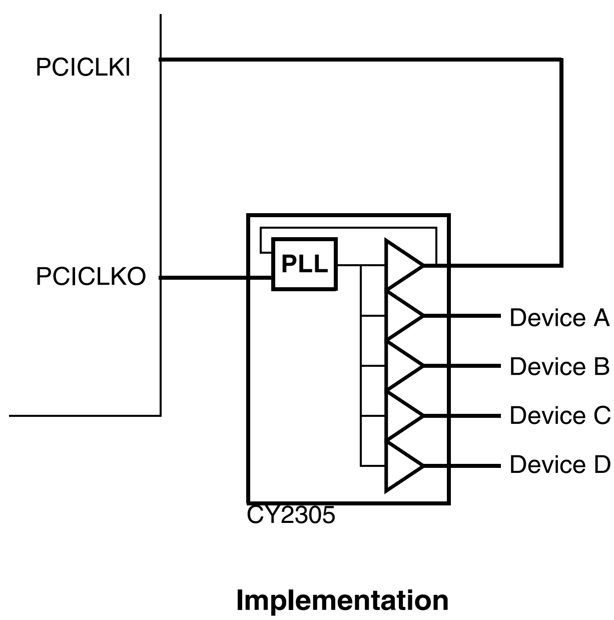
For more information on layout constraints, go to the **place and route recommendations** section.

Figure 6-8. Typical PCI clock routing



In the case of higher clock load it is recommended to use a zero-delay clock buffer as described in Figure 6-9. This approach is also recommended when implementing the delay on PCICLKI according to the PCI section of the **Electrical Specifications** chapter.

Figure 6-9. PCI clock routing with zero-delay clock buffer

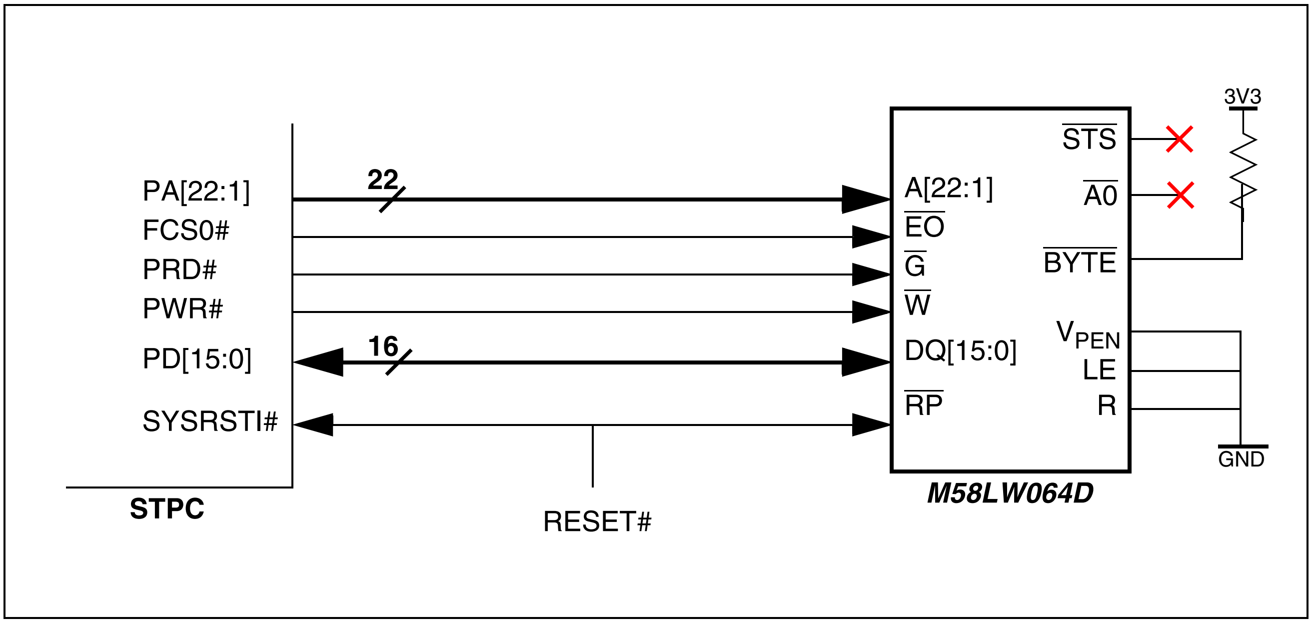


6.3.5. LOCAL BUS

The local bus has all the signals to directly connect flash devices or I/O devices.

Figure 6-10 describes how to connect a 16-bit boot flash (the corresponding strap options must be set accordingly).

Figure 6-10. Typical 16-bit boot flash implementation

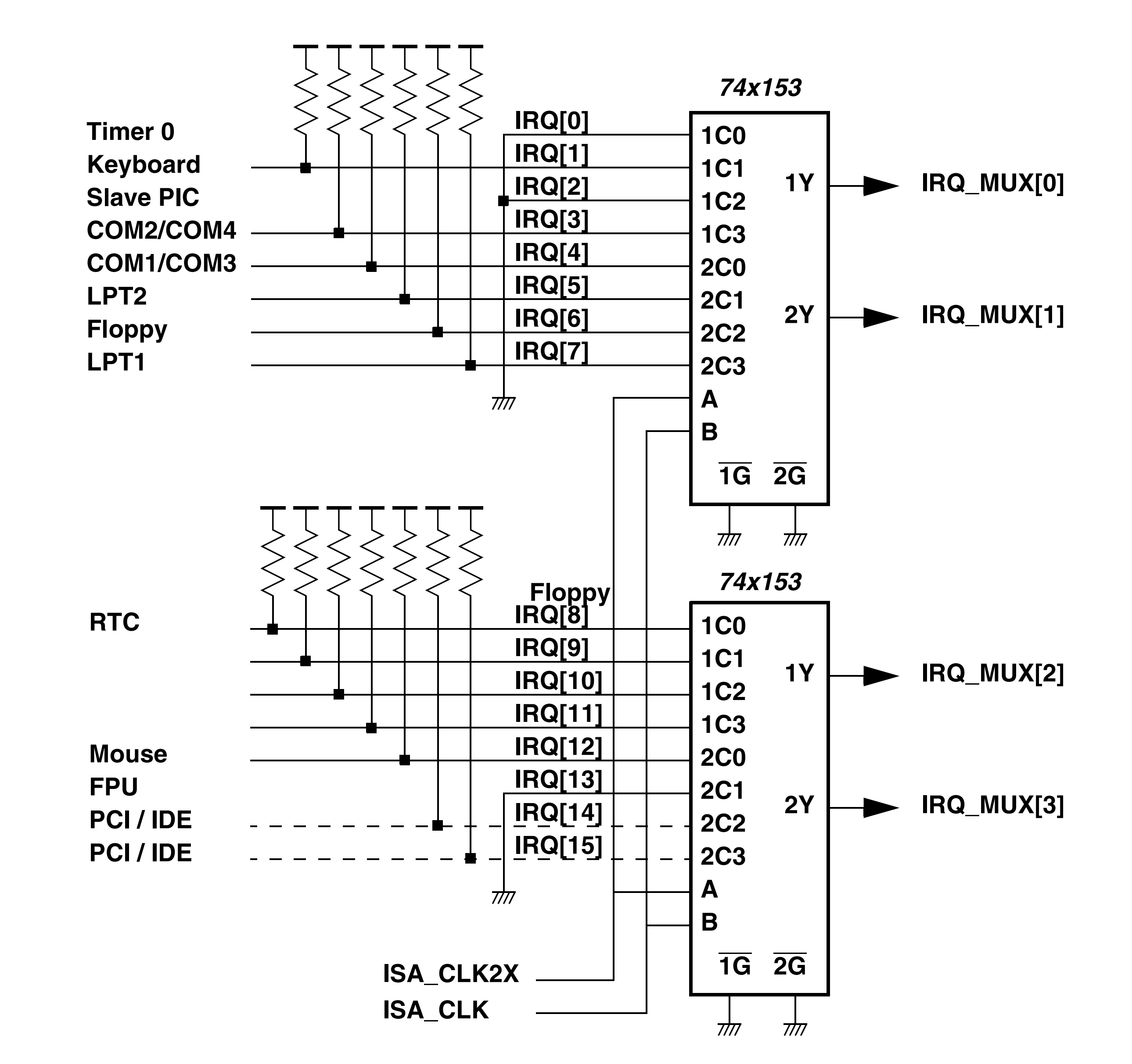


6.3.6. IPC

Most of the IPC signals are multiplexed: Interrupt inputs, DMA Request inputs, DMA Acknowledge outputs. The figure below describes a complete implementation of the IRQ[15:0] time-multiplexing.

When an interrupt line is used internally, the corresponding input can be grounded. In most of the embedded designs, only few interrupts lines are necessary and the glue logic can be simplified.

Figure 6-11. Typical IRQ multiplexing

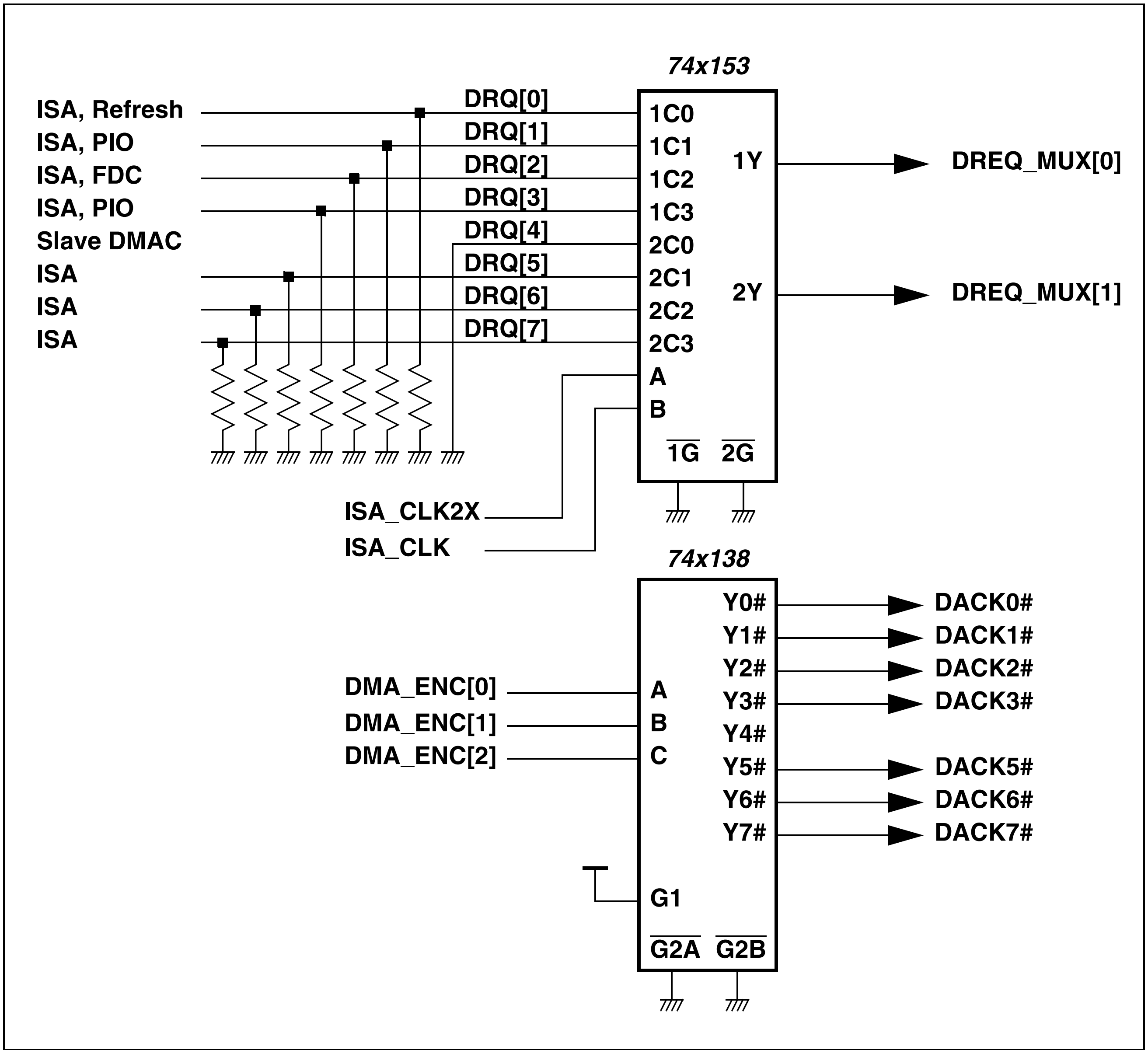


When the interface is integrated into the STPC, the corresponding interrupt line can be grounded as it is connected internally.

For example, if the integrated IDE controller is activated, the IRQ[14] and IRQ[15] inputs can be grounded.

The figure below describes a complete implementation of the external glue logic for DMA Request time-multiplexing and DMA Acknowledge demultiplexing. Like for the interrupt lines, this logic can be simplified when only few DMA channels are used in the application.
This glue logic is not needed in Local bus mode as it does not support DMA transfers.

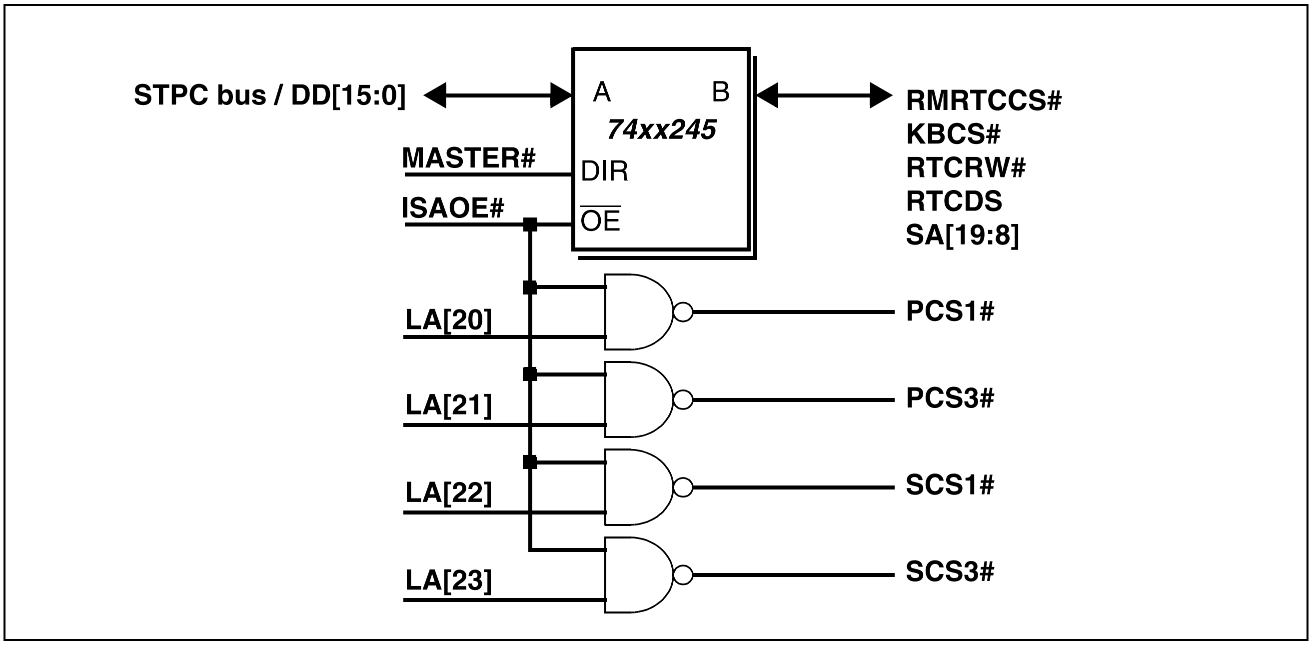
Figure 6-12. Typical DMA multiplexing and demultiplexing



6.3.7. IDE / ISA DYNAMIC DEMULTIPLEXING

Some of the ISA bus signals are dynamically multiplexed to optimize the pin count. Figure 6-13 describes how to implement the external glue logic to demultiplex the IDE and ISA interfaces. In Local Bus mode the two buffers are not needed and the NAND gates can be simplified to inverters.

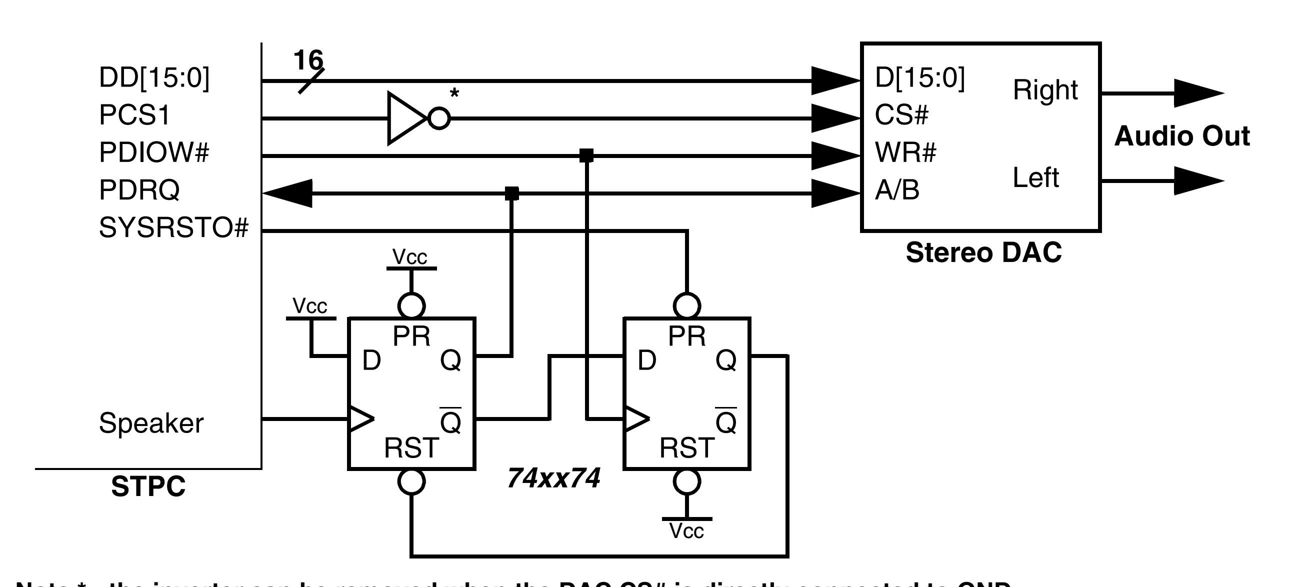
Figure 6-13. Typical IDE / ISA Demultiplexing



6.3.8. BASIC AUDIO USING IDE INTERFACE

When the application requires only basic audio capabilities, an audio DAC on the IDE interface can avoid using a PCI-based audio device(see Figure 6-14). This low cost solution is not CPU consuming thanks to the DMA controller implemented in the IDE controller and can generate 16-bit stereo sound. The clock speed is programmable when using the speaker output.

Figure 6-14. Basic audio on IDE



Note * : the inverter can be removed when the DAC CS# is directly connected to GND

6.3.9. VGA INTERFACE

The STPC integrates a voltage reference and video buffers. The amount of external devices is then limited to the minimum as described in the Figure 6-15.

All the resistors and capacitors have to be as close as possible to the STPC while the circuit protector DALC112S1 must be close to the VGA connector.

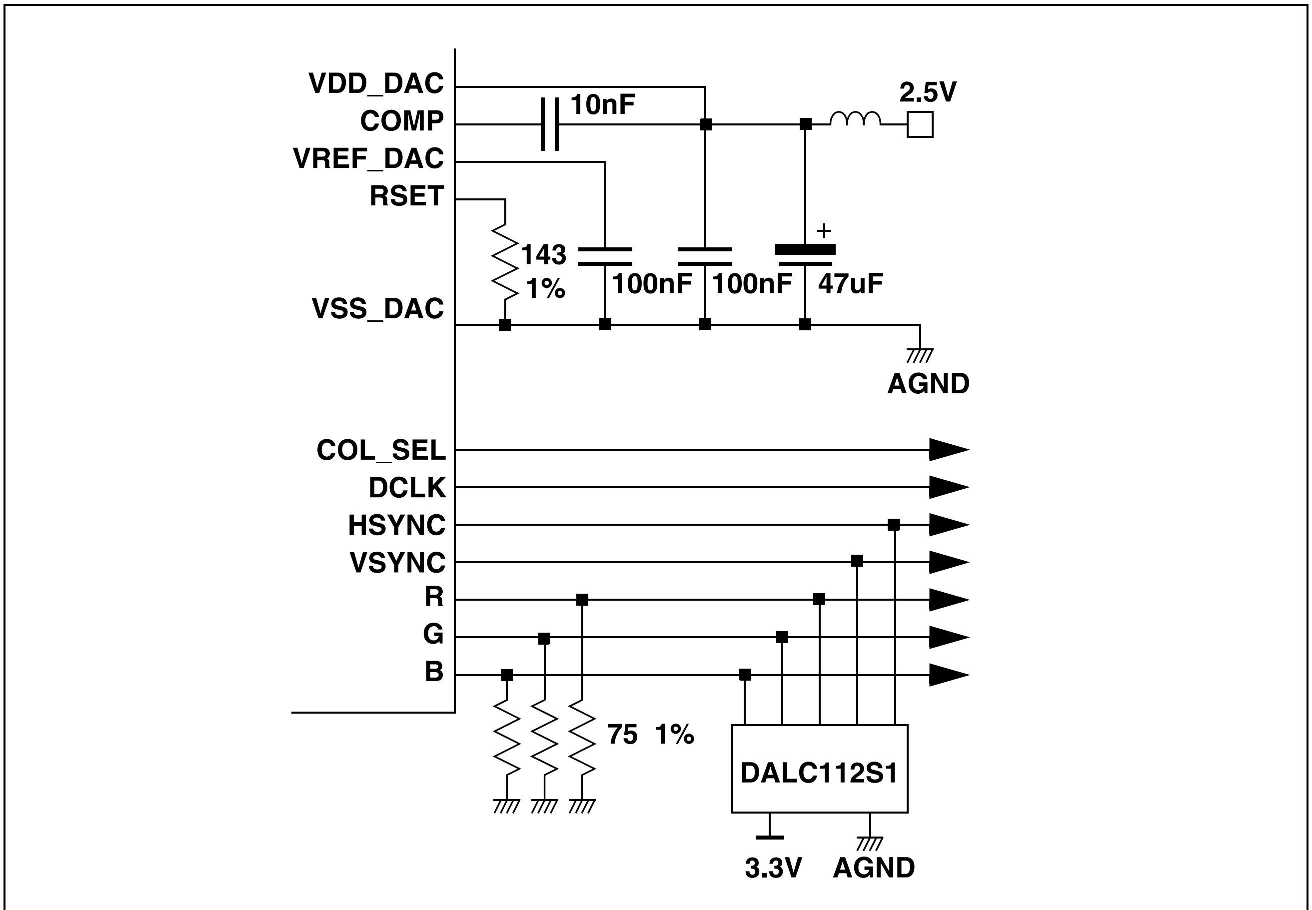
The DDC[1:0] lines, not represented here, have also to be protected when they are used on the VGA connector.

COL_SEL can be used when implementing the Picture-In-Picture function outside the STPC, for example when multiplexing an analog video source. In that case, the CRTC of the STPC has to be genlocked to this analog source.

DCLK is usually used by the TFT display which has RGB inputs in order to synchronise the picture at the level of the pixel.

When the VGA interface is not needed, the signals R, G, B, HSYNC, VSYNC, COMP, RSET can be left unconnected, VSS_DAC and VDD_DAC must then be connected to GND.

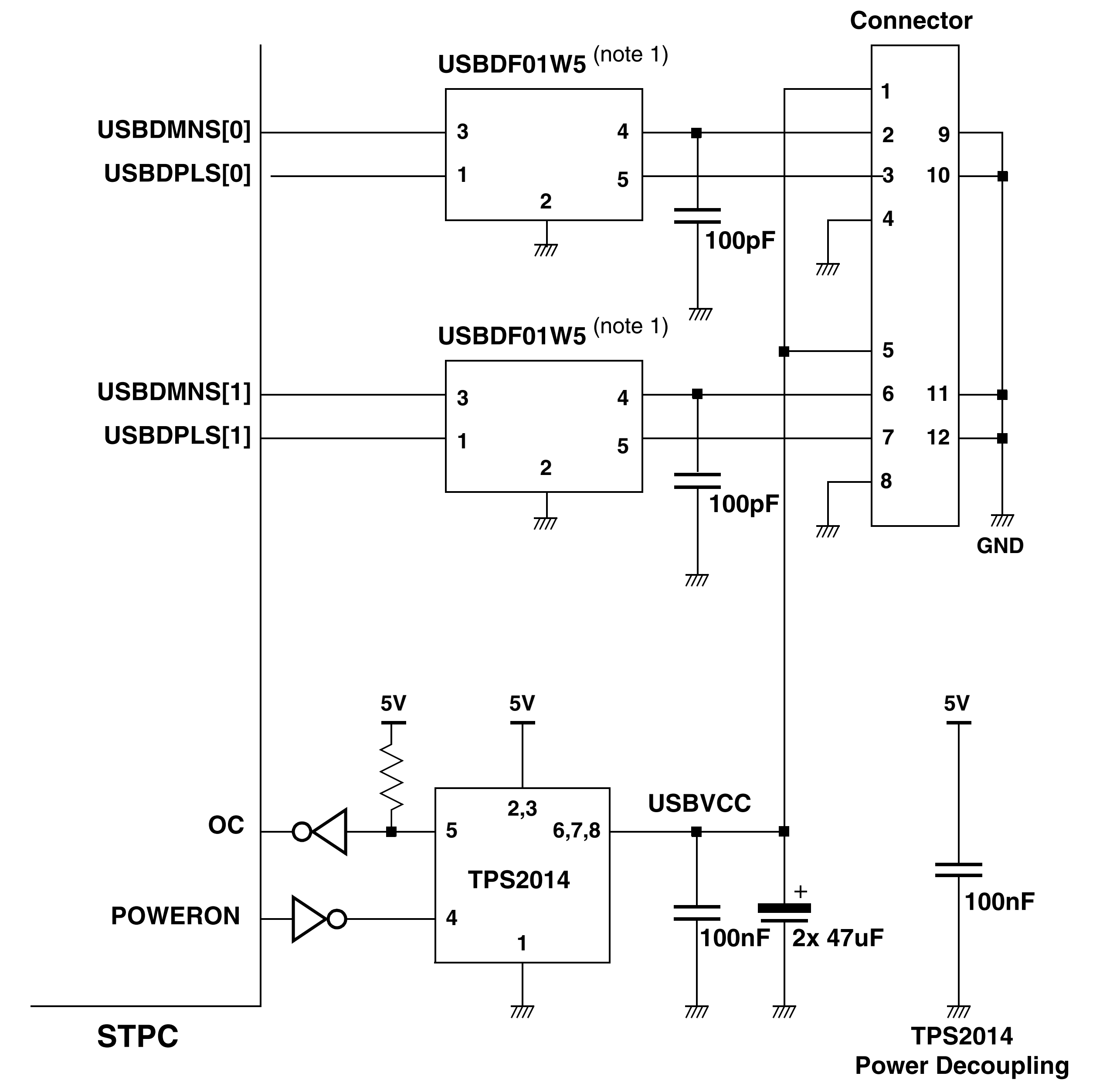
Figure 6-15. Typical VGA implementation



6.3.10. USB INTERFACE

The STPC integrates a USB host interface with a 2-port Hub. The only external device needed are the ESD protection circuits USBDF01W5 and a USB power supply controller. Figure 6-16 describes a typical implementation using these devices.

Figure 6-16. Typical USB implementation

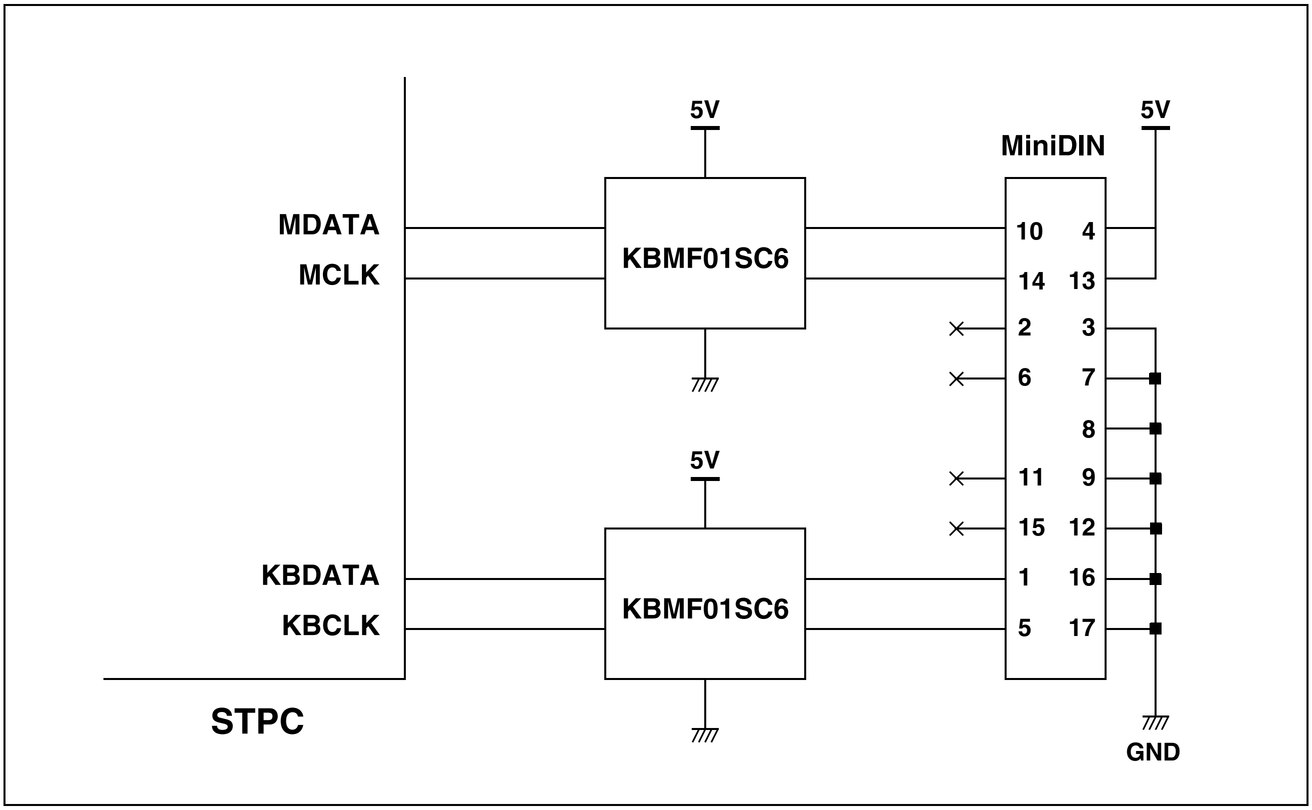


Note 1: The ESD protection will be adequate for most applications. In some instances, problems may occur if the devices on the USB chain do not have enough power to drive the signals adequately. We therefore recommend that you replace the part with discrete components and reduce the value of the capacitor.

6.3.11. KEYBOARD/MOUSE INTERFACE

The STPC integrates a PC/AT+ keyboard and PS/2 mouse controller. The only external devices needed are the ESD protection circuits KBMF01SC6. Figure 6-17 describes a typical implementation using a dual minidin connector.

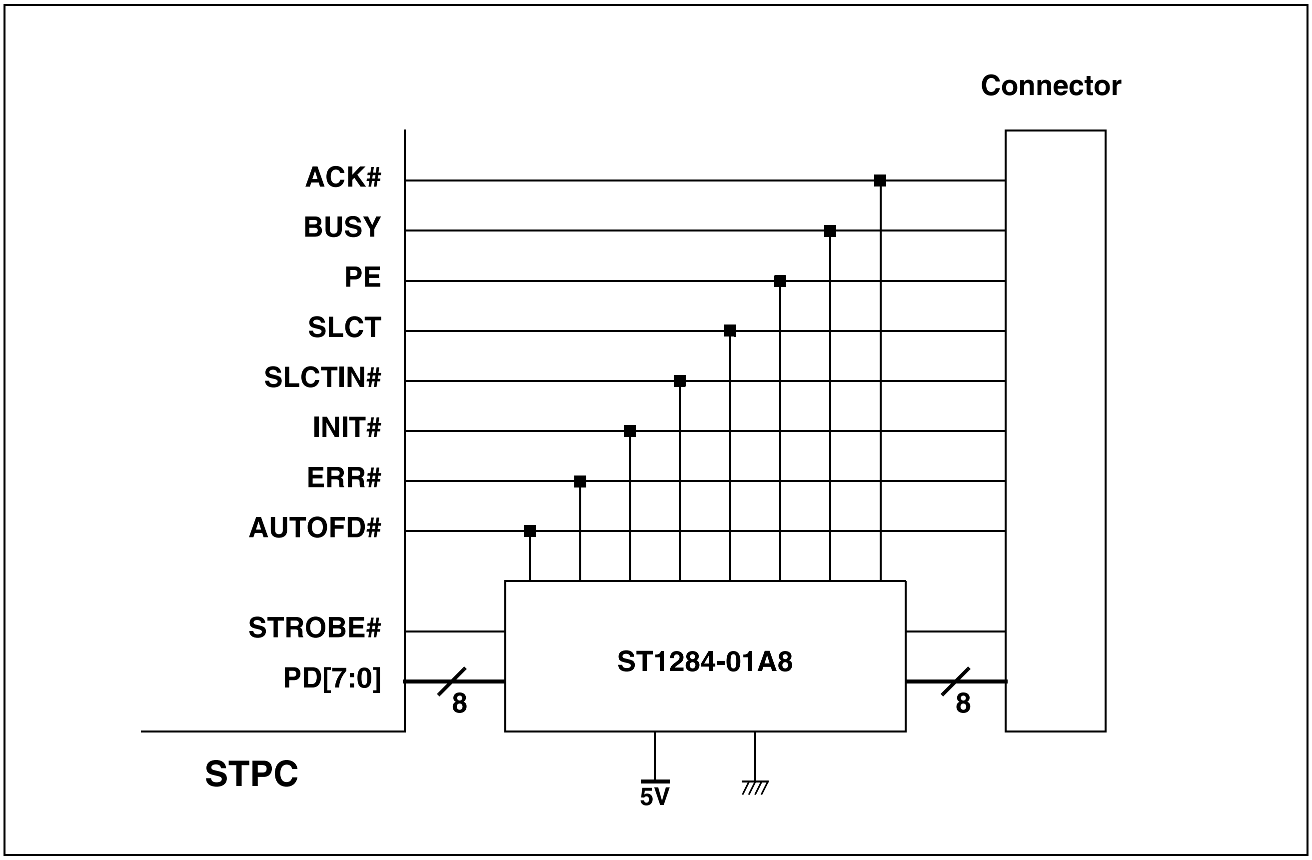
Figure 6-17. Typical Keyboard / Mouse implementation



6.3.12. PARALLEL PORT INTERFACE

The STPC integrates a parallel port where the only external device needed is the ESD protection circuits ST1284-01A8. Figure 6-18 describes a typical implementation using this device.

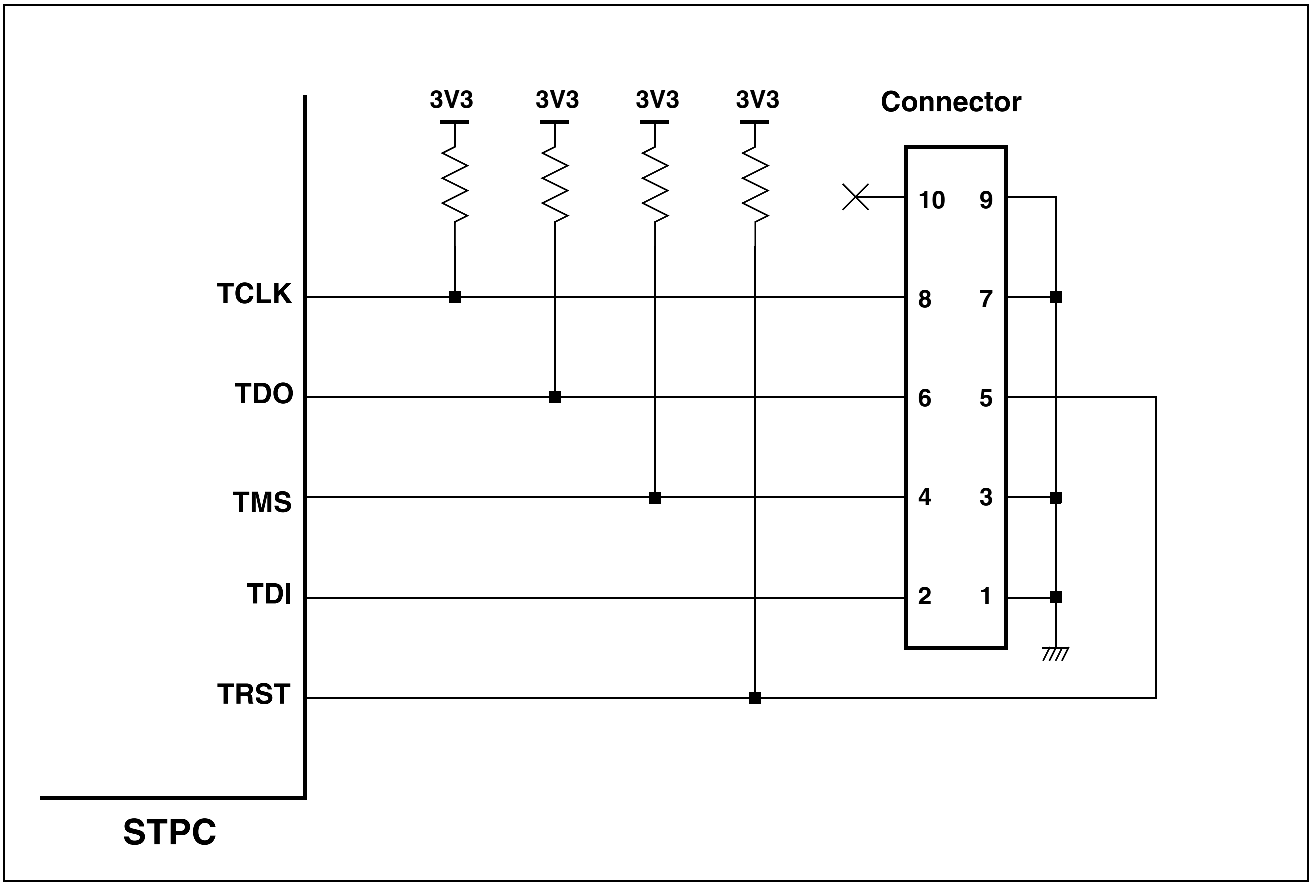
Figure 6-18. Typical parallel port implementation



6.3.13. JTAG INTERFACE

The STPC integrates a JTAG interface for scan-chain and on-board testing. The only external device needed are the pull up resistors. Figure 6-19 describes a typical implementation using these devices.

Figure 6-19. Typical JTAG implementation



6.4. PLACE AND ROUTE RECOMMENDATIONS

6.4.1. GENERAL RECOMMENDATIONS

Some STPC Interfaces run at high speed and need to be carefully routed or even shielded like:

1) Memory Interface
2) PCI bus
3) Graphics and video interfaces
4) 14 MHz oscillator stage

All clock signals have to be routed first and shielded for speeds of 27MHz or higher. The high speed signals follow the same constraints, as for the memory and PCI control signals.

The next interfaces to be routed are Memory, PCI, and Video/graphics.

All the analog noise-sensitive signals have to be routed in a separate area and hence can be routed indepedently.

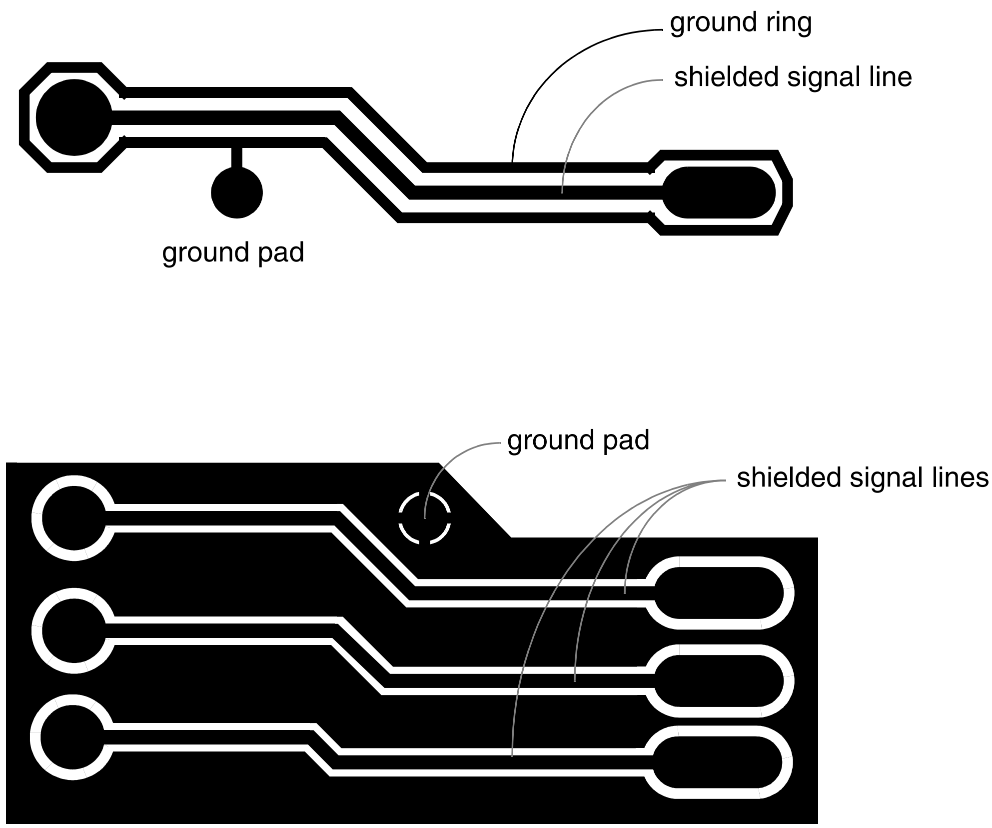
6.4.2. PLL DEFINITION AND IMPLIMENTATION

PLLs are analog cells which supply the internal STPC Clocks. To get the cleanest clock, the jitter on the power supply must be reduced as much as possible. This will result in a more stable system.

Each of the integrated PLL has a dedicated power pin so a single power plane for all of these PLLs, or one wire for each, or any solution in between which help the layout of the board can be used.

Powering these pins with one Ferrite + capacitances is enough. We recommend at least 2 capacitances: one 'big' (few uF) for power storage, and one or 2 smalls (100nF + 1nF) for noise filtering.

Figure 6-20. Shielding signals



6.4.3. MEMORY INTERFACE

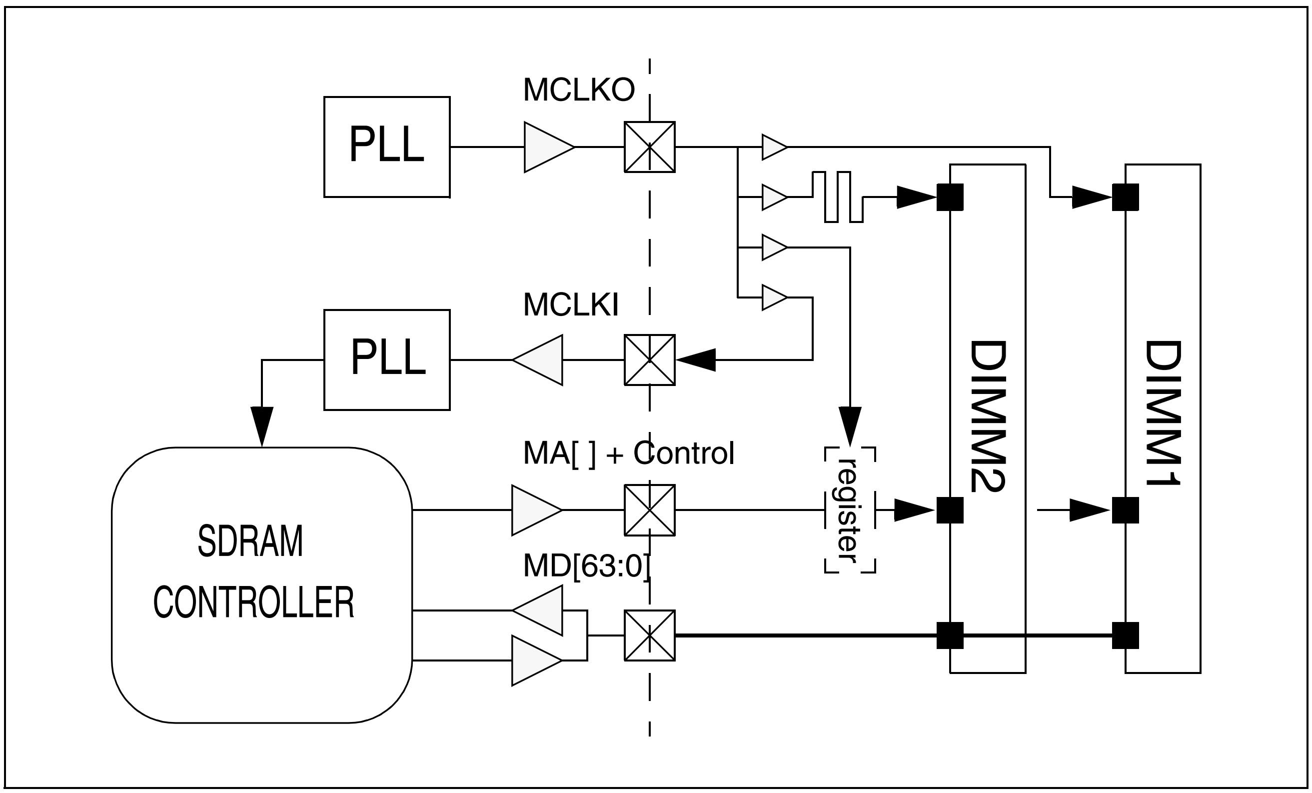
6.4.3.1. Introduction

In order to achieve SDRAM memory interfaces which work at clock frequencies of 90 MHz and above, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration. The guidelines described below are related to SDRAM components on DIMM modules. For applications where the memories are directly soldered to the motherboard, the PCB should be laid out such that the trace lengths fit within the constraints shown here. The traces could be slightly shorter since the extra routing on the DIMM PCB is no longer present but it is then up to the user to verify the timings.

6.4.3.2. SDRAM Clocking Scheme

The SDRAM Clocking Scheme deserves a special mention here. Basically the memory clock is generated on-chip through a PLL and goes directly to the MCLKO output pin of the STPC. The nominal frequency is 90 MHz. Because of the high load presented to the MCLK on the board by the DIMMs it is recommended to rebuffer the MCLKO signal on the board and balance the skew to the clock ports of the different DIMMs and the MCLKI input pin of STPC.

Figure 6-21. Clock Scheme



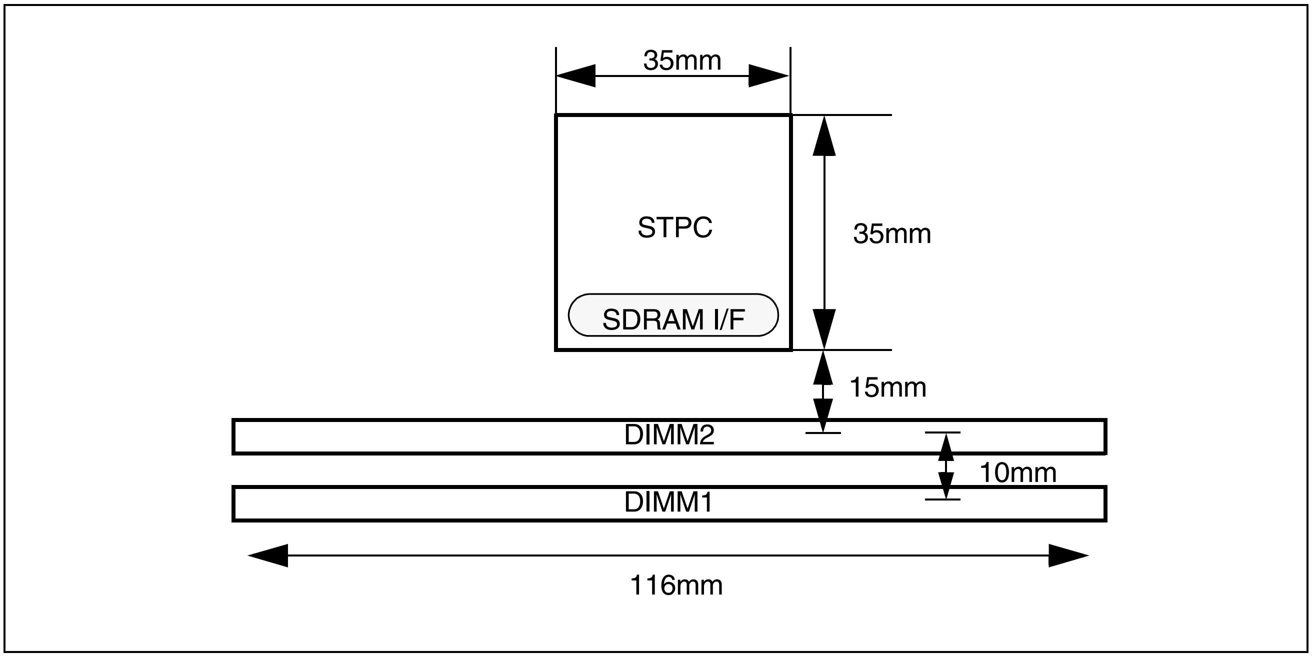
6.4.3.3. Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown in Figure 6-22. Because all of the memory interface signal balls are located in the same region of the STPC device, it is possible to orientate the device to reduce the trace lengths. The worst case routing length to the DIMM1 is estimated to be 100 mm.

Solid power and ground planes are a must in order to provide good return paths for the signals and to reduce EMI and noise. Also there should be ample high frequency decoupling between the power and ground planes to provide a low impedance path between the planes for the return paths for signal routings which change layers. If possible, the traces should be routed adjacent to the same power or ground plane for the length of the trace.

For the SDRAM interface, the most critical signal is the clock. Any skew between the clocks at the

Figure 6-22. DIMM placement

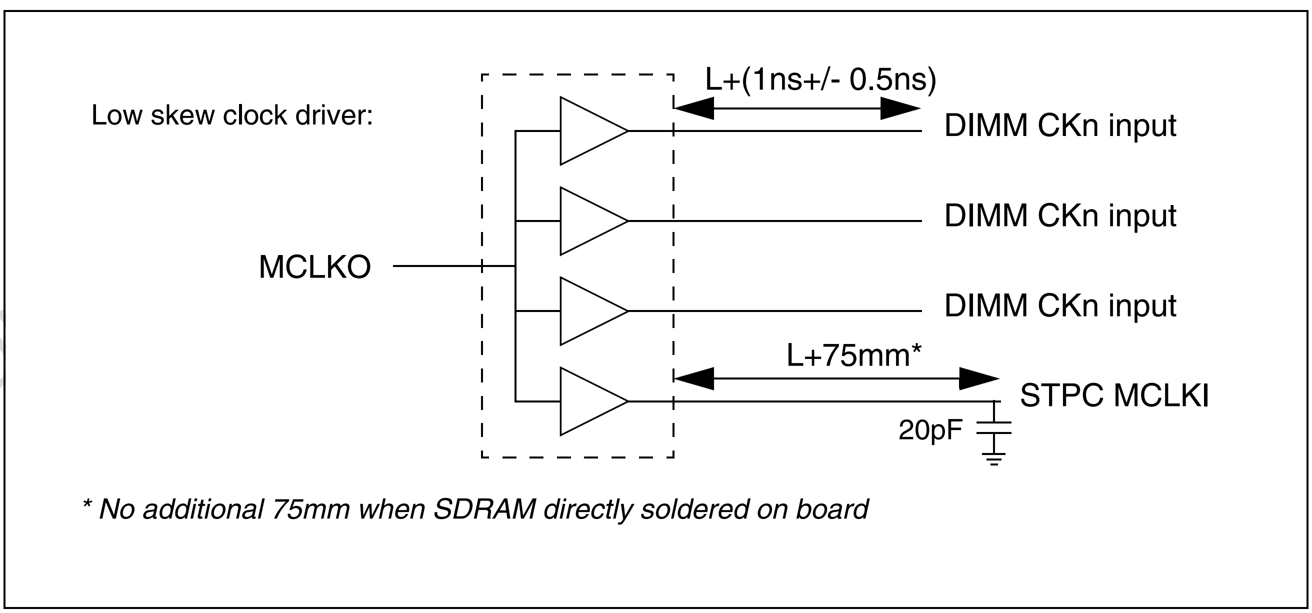


SDRAM components and the memory controller will impact the timing budget. In order to get well matched clocks at all components it is recommended that all the DIMM clock pins, STPC memory clock input (MCLKI) and any other component using the memory clock are individually driven from a low skew clock driver with matched routing lengths specified in Section 4.5.3. . In other words, all clock line lengths that go from the buffer to the memory chips (MCLKx) and from the buffer to the STPC (MCLKI) must follow this equation;

MCLKx = MCLKI+(1ns+/-0.5ns).

This is shown in Figure 6-23.

Figure 6-23. Clock Routing



The maximum skew between pins for this part is 250ps. The important factors for the clock buffer are a consistent drive strength and low skew between the outputs. The delay through the buffer is not important so it does not have to be a zero delay PLL type buffer. The trace lengths from the clock driver to the DIMM CKn pins should be matched exactly. Since the propagation speed can vary between PCB layers, the clocks should be routed in a consistent way. The routing to the STPC memory input should be longer by 75 mm to compensate for the extra clock routing on the DIMM. Also a 20 pF capacitor should be placed as near as possible to the clock input of the STPC to compensate for the DIMM's higher clock load. The impedance of the trace used for the clock routing should be matched to the DIMM clock trace impedance (60-75 ohms).To minimise crosstalk the clocks should be routed with spacing to adjacent tracks of at least twice the clock trace width. For designs which use SDRAMs directly mounted on the motherboard PCB all the clock trace lengths should be matched to the constraints given in Figure 6-23 and in Section 4.5.3. .

The DIMM sockets should be populated starting with the furthest DIMM from the STPC device first (DIMM1). There are two types of DIMM devices; single-row and dual-row. The dual-row devices require two chip select signals to select between the two rows. A STPC device with 4 chip select control lines could control either 4 single-row DIMMs or 2 dual-row DIMMs. When only 2 chip select control lines are activated, only two single-row DIMMs or one dual-row DIMM can be controlled.

6.4.3.4. Summary

For unbuffered DIMMs the address/control signals will be the most critical for timing. The simulations show that for these signals the best way to drive them is to use a parallel termination. For applications where speed is not so critical series termination can be used as this will save power. Using a low impedance such as 50Ω for these critical traces is recommended as it both reduces the delay and the overshoot.

The other memory interface signals will typically be not as critical as the address/control signals. Using lower impedance traces is also beneficial for the other signals but if their timing is not as critical as the address/control signals they could use the default value. Using a lower impedance implies using wider traces which may have an impact on the routing of the board.

The layout of this interface can be validated by an electrical simulation using the IBIS model available on the STPC web site.

6.5. CLOCK TOPOLOGY FOR ON-BOARD SDRAM

Figure 4-5 and Figure 6-25 give the recommended clock topology and the resulting IBIS simulation in the case of four on-board SDRAM devices and no clock buffer.

Figure 6-24. Recommended topology for 4 on-board SDRAMs (IBIS model)

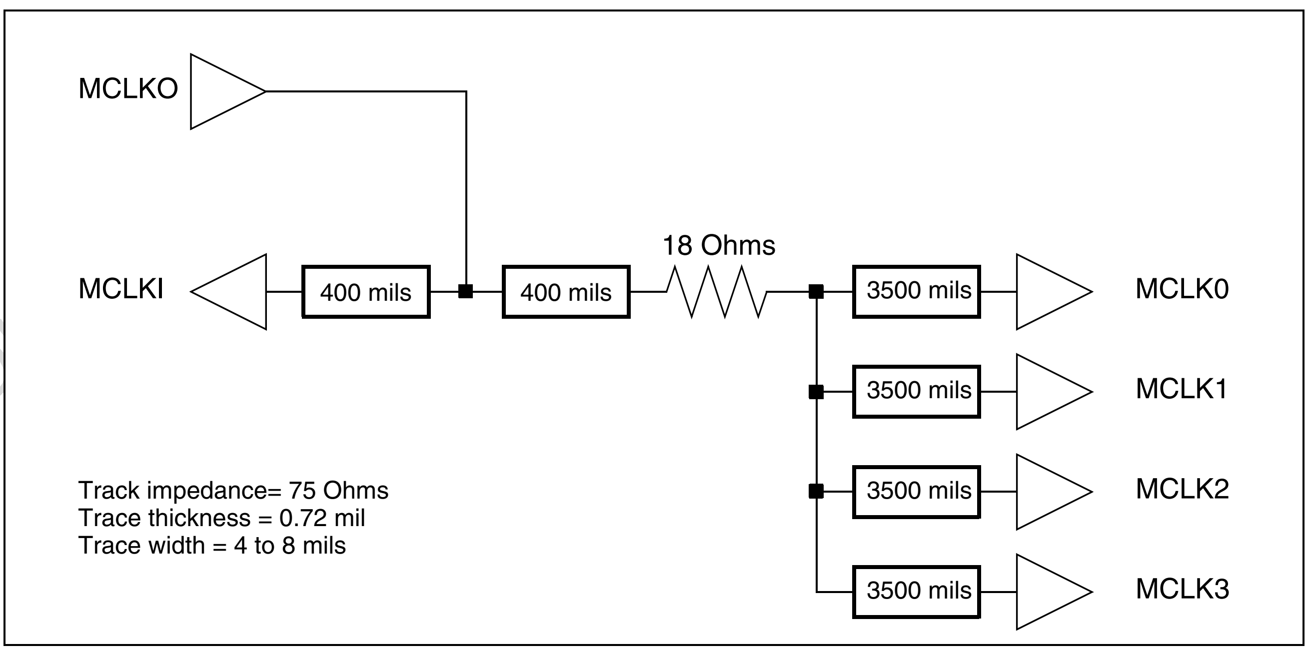
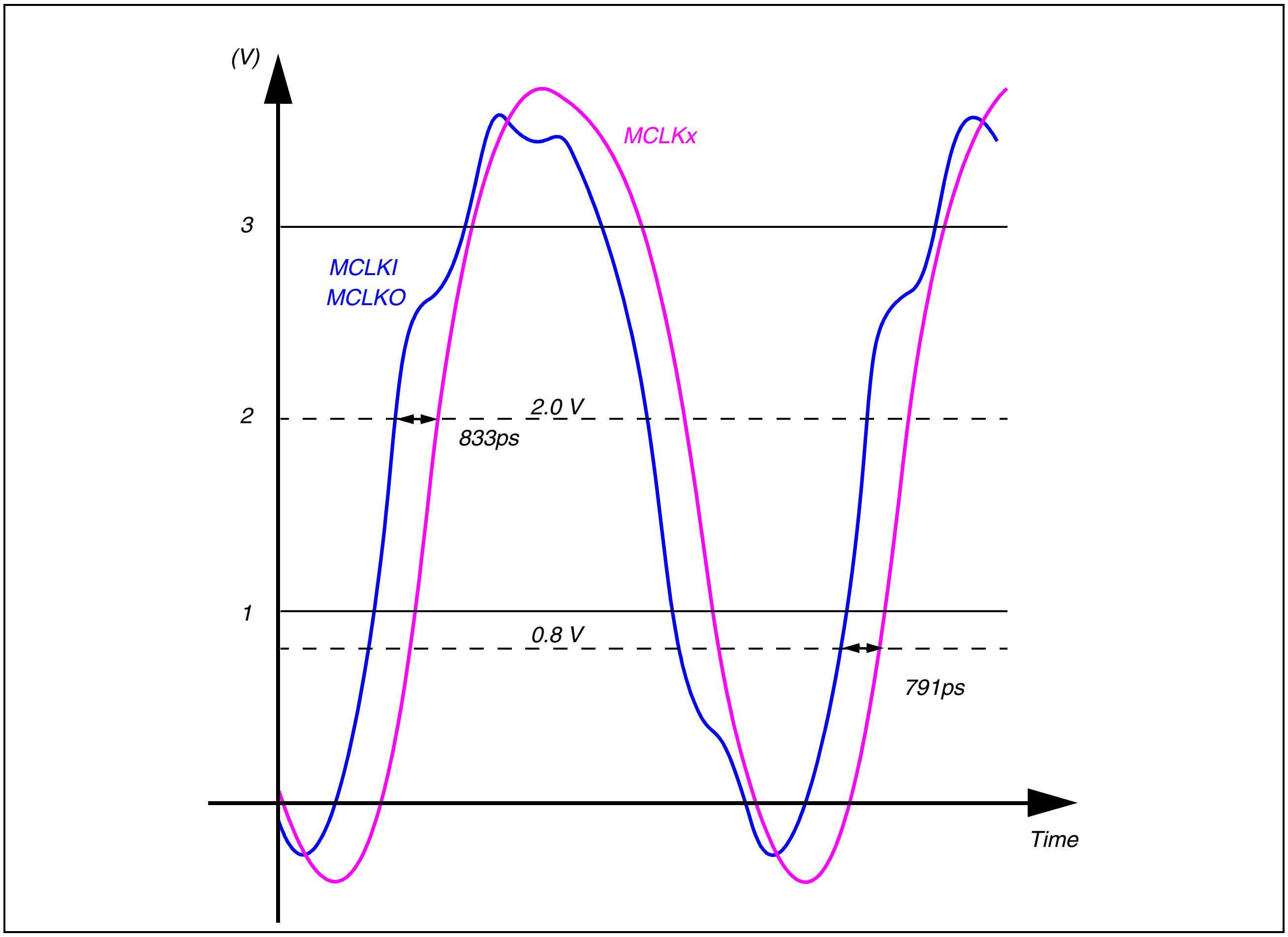


Figure 6-25. IBIS Simulation for on-board SDRAM / 90MHz



6.5.0.1. Clock topology for standard DIMM

Figure 6-26 and Figure 6-27 give the recommended clock topology and the resulting IBIS simulation in the case of a standard DIMM with the use of a clock buffer.

Figure 6-26. Recommended topology for DIMM (IBIS model)

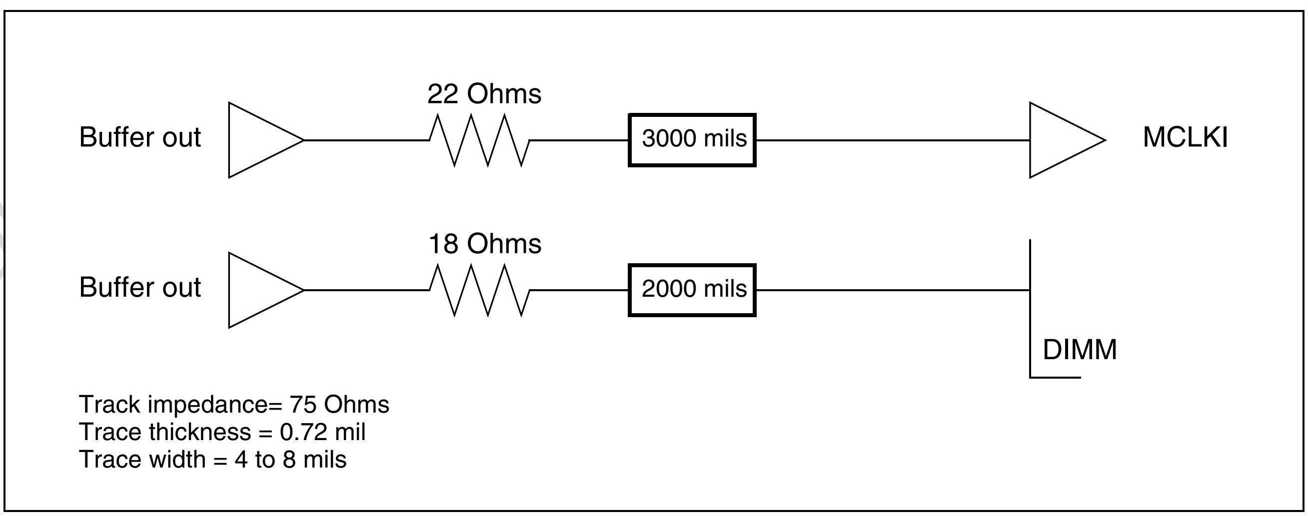
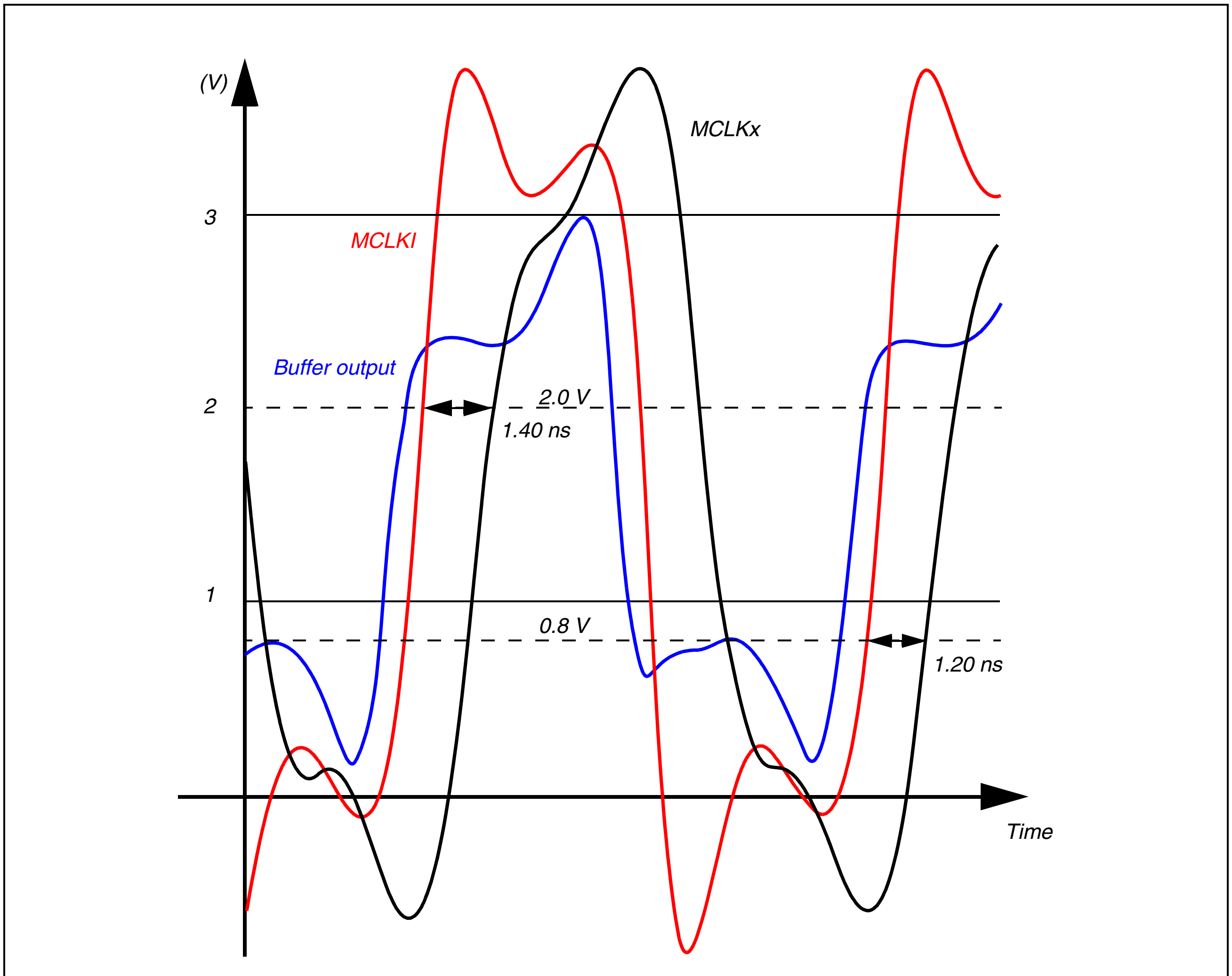


Figure 6-27. IBIS Simulation for DIMM / 90MHz



6.5.1. PCI INTERFACE

6.5.1.1. Introduction

In order to achieve a PCI interface which work at clock frequencies up to 33MHz, careful consideration has to be given to the timing of the interface with all the various electrical and physical constraints taken into consideration.

6.5.1.2. PCI Clocking Scheme

The PCI Clocking Scheme deserves a special mention here. Basically the PCI clock (PCICLKO) is generated on-chip from HCLK through a programmable delay line and a clock divider. The nominal frequency is 33MHz. This clock must be looped to PCICLKI and goes to the internal South Bridge through a deskewer. On the contrary, the internal North Bridge is clocked by HCLK, putting some additionnal constraints on T_0 and T_1.

6.5.1.3. Board Layout Issues

The physical layout of the motherboard PCB assumed in this presentation is as shown in Figure 6-29. For the PCI interface, the most critical signal is the clock. Any skew between the clocks at the PCI components and the STPC will impact the timing budget. In order to get well matched clocks at all components it is recommended that all the PCI clocks are individually driven from a serial resistance with matched routing lengths. In other words, all clock line lengths that go from the resistor to the PCI chips (PCICLKx) must be identical.

The figure below is for PCI devices soldered on-board. In the case of a PCI slot, the wire length must be shortened by 2.5" to compensate the clock layout on the PCI board. The maximum clock skew between all devices is 2ns according to PCI specifications.

The Figure 6-30 describes a typical clock delay implementation. The exact timing constraints are listed in the PCI section of the **Electrical Specifications** Chapter.

Figure 6-28. Clock Scheme

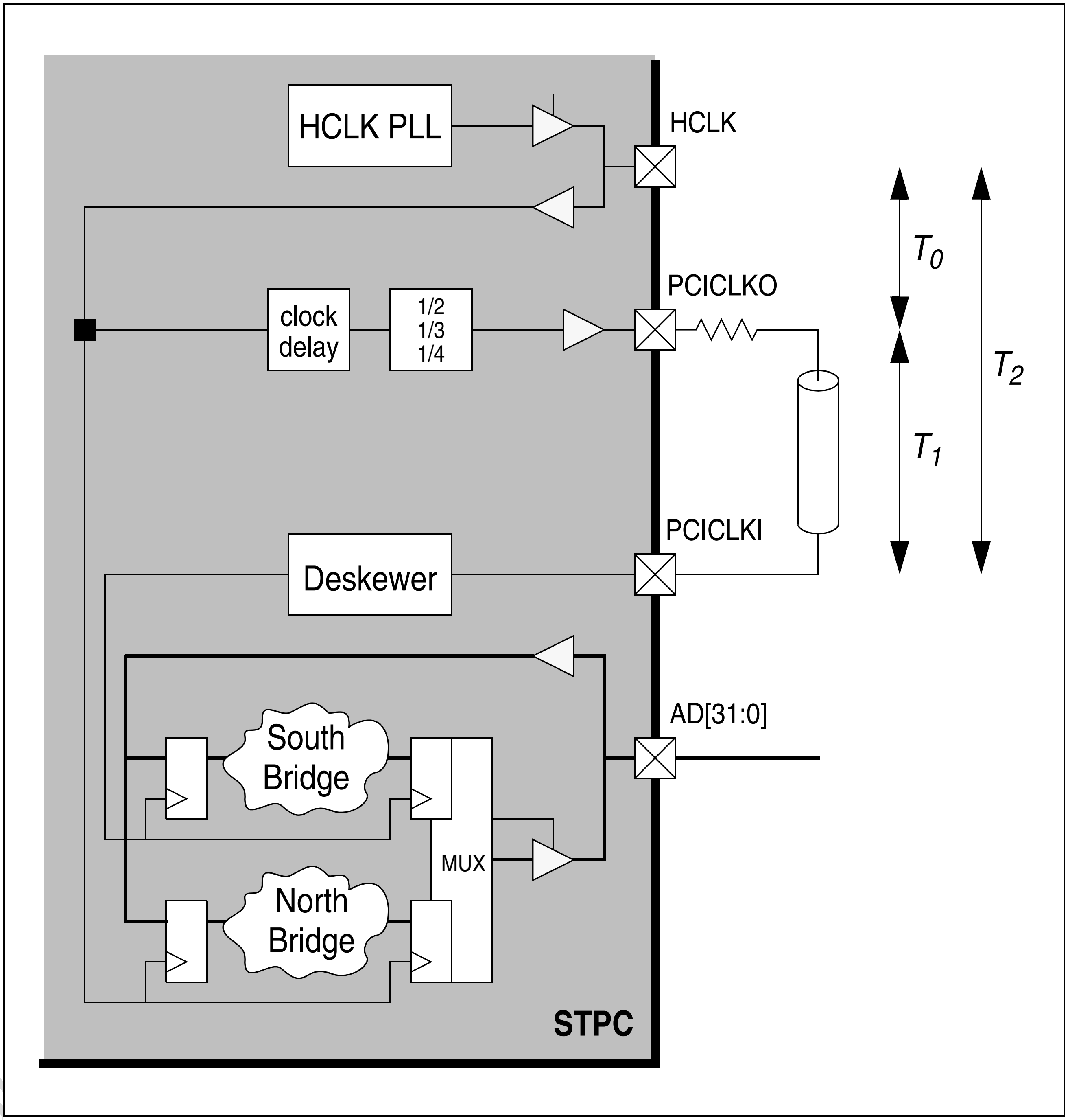
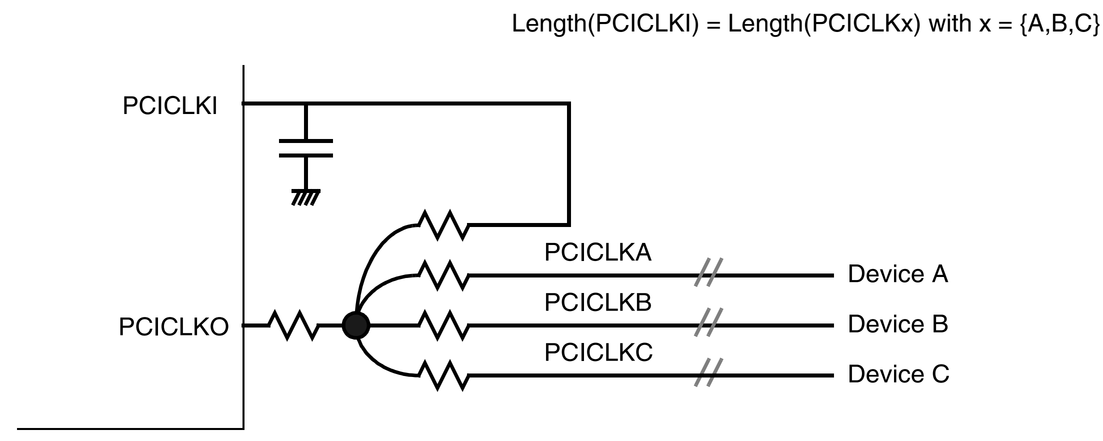
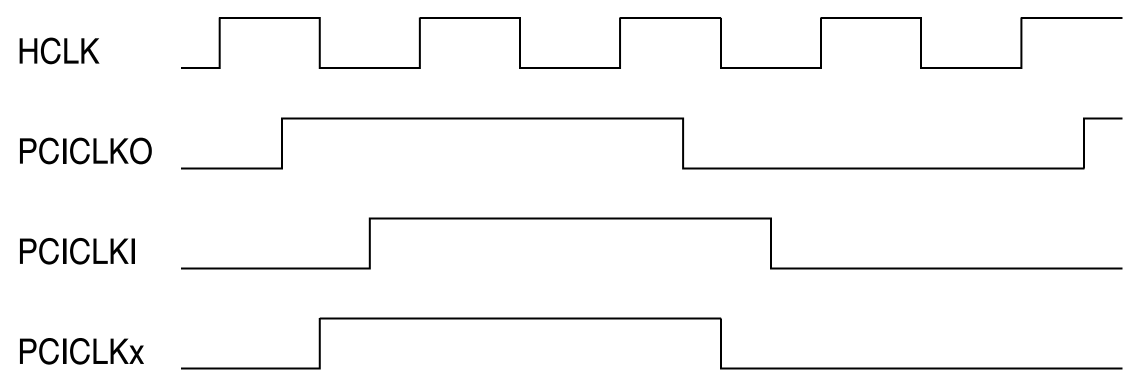


Figure 6-29. Typical PCI clock routing



Note: The value of 22 Ohms corresponds to tracks with Z_0 = 70 Ohms.

Figure 6-30. Clocks relationships



6.5.2. THERMAL DISSIPATION

6.5.2.1. Power saving

Thermal dissipation of the STPC depends mainly on supply voltage. When the system does not need to work at the upper voltage limit, it may therefore be beneficial to reduce the voltage to the lower voltage limit, where possible. This could save a few 100's of mW.

The second area to look at is unused interfaces and functions. Depending on the application, some input signals can be grounded, and some blocks not powered or shutdown. Clock speed dynamic adjustment is also a solution that can be used along with the integrated power management unit.

6.5.2.2. Thermal balls

The standard way to route thermal balls to ground layer implements only one via pad for each ball pad, connected using a 8-mil wire.

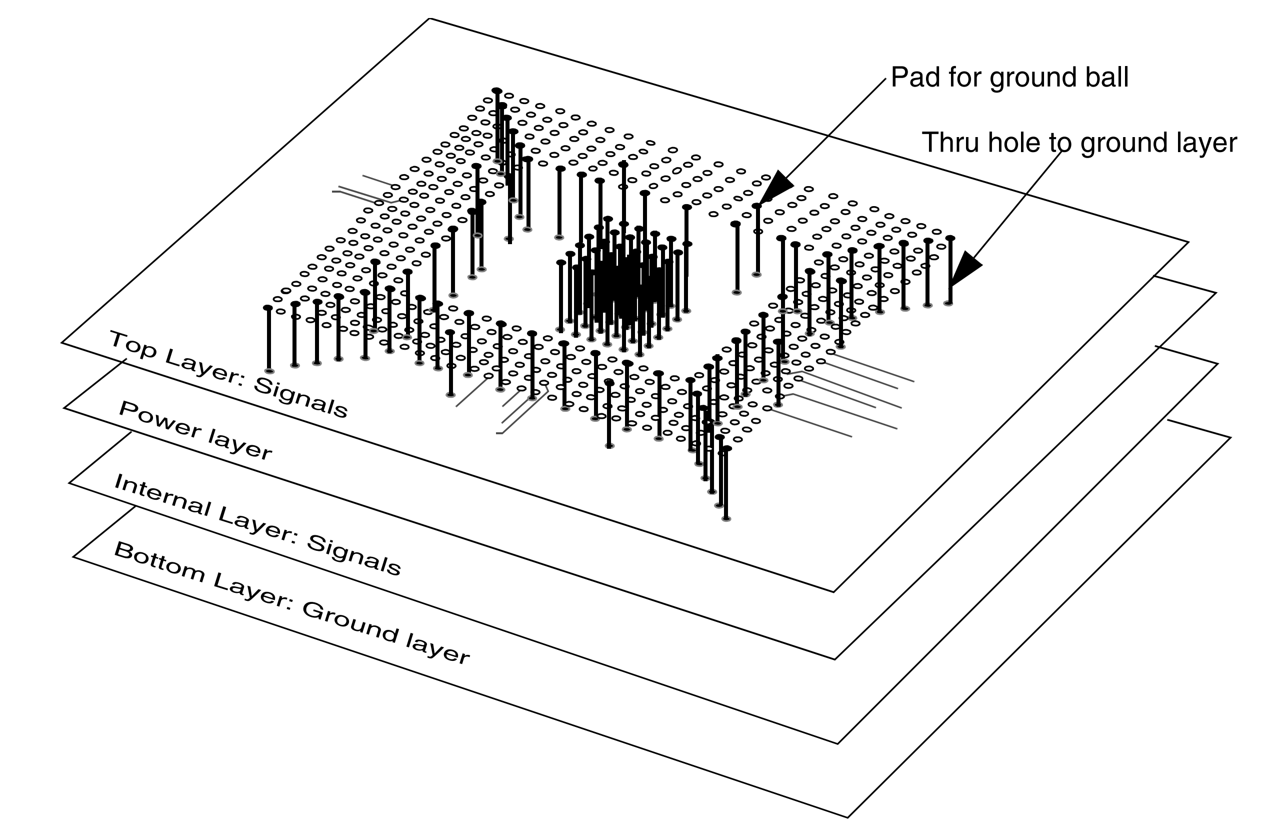
With such configuration the Plastic BGA package does 90% of the thermal dissipation through the ground balls, and especially the central thermal balls which are directly connected to the die. The remaining 10% is dissipated through the case. Adding a heat sink reduces this value to 85%.

As a result, some basic rules must be followed when routing the STPC in order to avoid thermal problems.

As the whole ground layer acts as a heat sink, the ground balls must be directly connected to it, as illustrated in Figure 5-2. If one ground layer is not enough, a second ground plane may be added.

When possible, it is important to avoid other devices on-board using the PCB for heat dissipation, like linear regulators, as this would heat the STPC itself and reduce the temperature range of the whole system, In case these devices can not use a separate heat sink, they must not be located just near the STPC

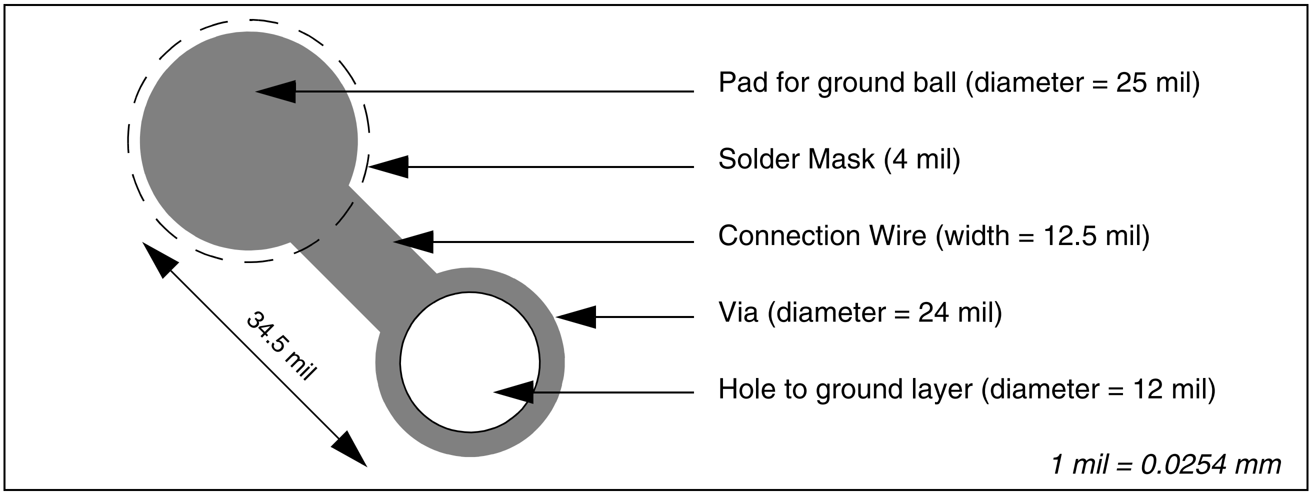
Figure 6-31. Ground Routing



When considering thermal dissipation, one of the most important parts of the layout is the connection between the ground balls and the ground layer.

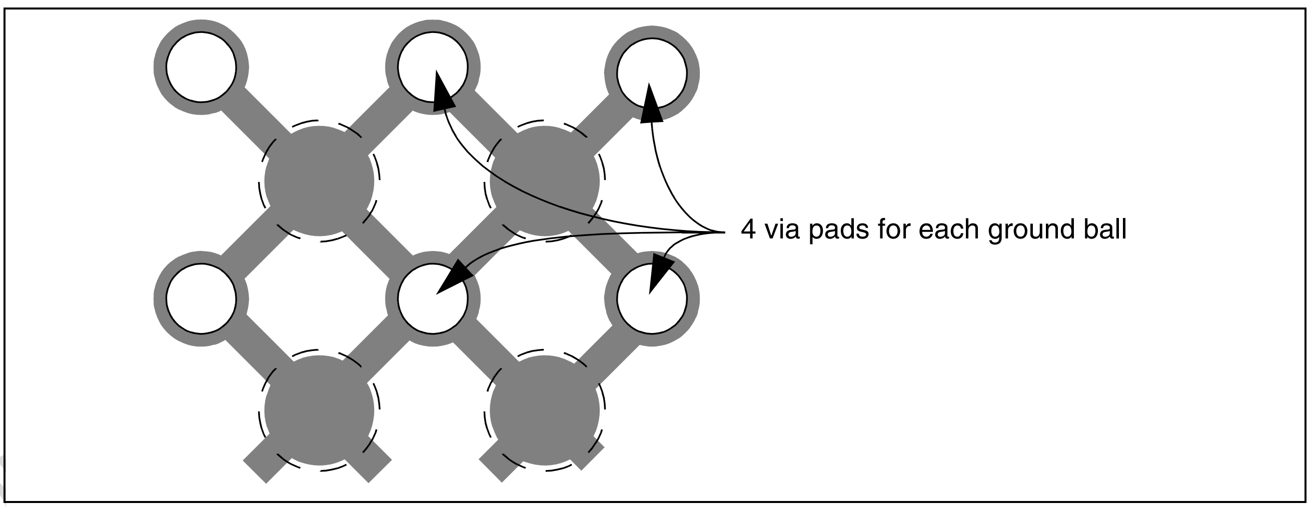
A 1-wire connection is shown in Figure 5-1. The use of a 8-mil wire results in a thermal resistance of 105°C/W assuming copper is used (418 W/m.°K). This high value is due to the thickness (34 µm) of the copper on the external side of the PCB.

Figure 6-32. Recommended 1-wire Power/Ground Pad Layout



Considering only the central matrix of 36 thermal balls and one via for each ball, the global thermal resistance is 2.9°C/W. This can be easily improved using four 12.5 mil wires to connect to the four vias around the ground pad link as in Figure 6-33. This gives a total of 49 vias and a global resistance for the 36 thermal balls of 0.5°C/W.

Figure 6-33. Recommended 4-wire Ground Pad Layout

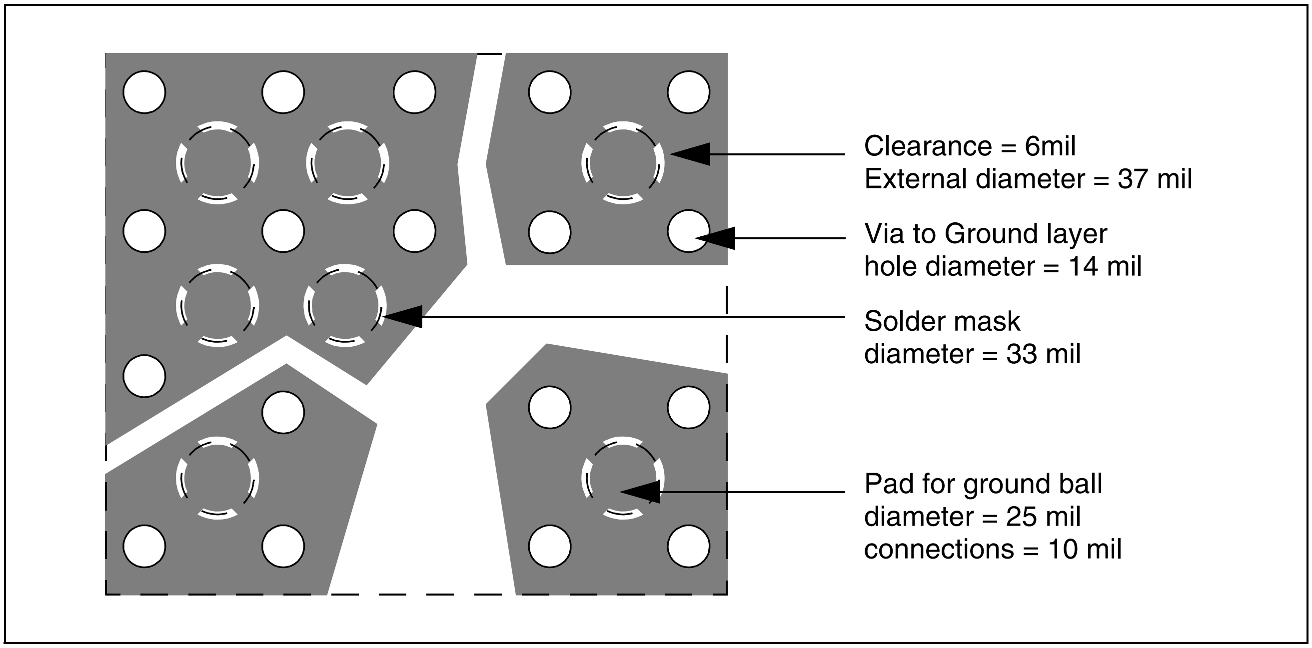


The use of a ground plane like in Figure 6-34 is even better.

To avoid solder wicking over to the via pads during soldering, it is important to have a solder mask of 4 mil around the pad (NSMD pad). This gives a diameter of 33 mil for a 25 mil ground pad.

To obtain the optimum ground layout, place the vias directly under the ball pads. In this case no local board distortion is tolerated.

Figure 6-34. Optimum Layout for Central Ground Ball - top layer



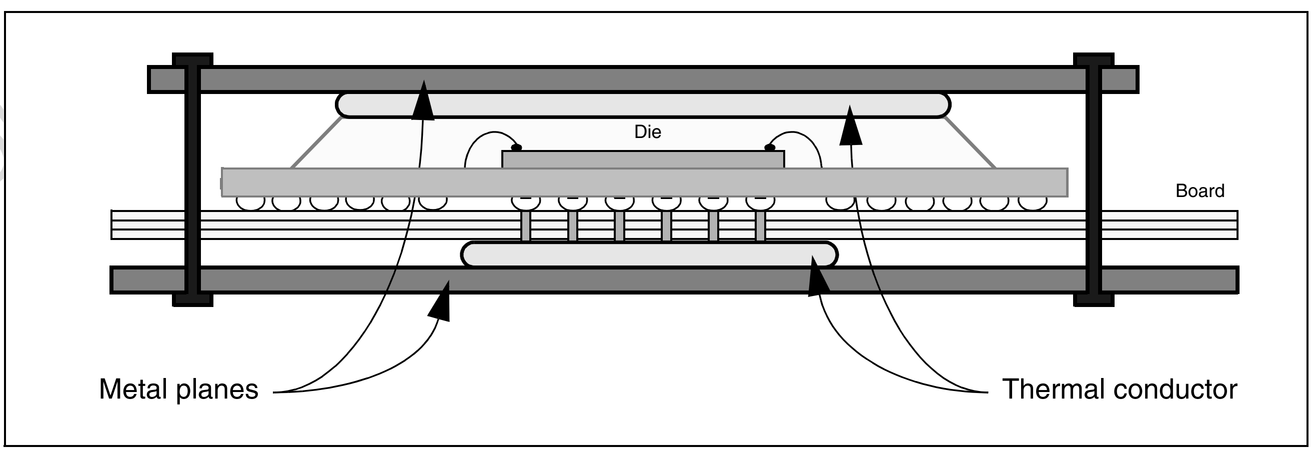
6.5.2.3. Heat dissipation

The thickness of the copper on PCB layers is typically 34 µm for external layers and 17 µm for internal layers. This means that thermal dissipation is not good; high board temperatures are concentrated around the devices and these fall quickly with increased distance.

Where possible, place a metal layer inside the PCB; this improves dramatically the spread of heat and hence the thermal dissipation of the board.

The possibility of using the whole system box for thermal dissipation is very useful in cases of high internal temperatures and low outside temperatures. Bottom side of the PBGA should be thermally connected to the metal chassis in order to propagate the heat flow through the metal. Thermally connecting also the top side will improve furthermore the heat dissipation. Figure 6-35 illustrates such an implementation.

Figure 6-35. Use of Metal Plate for Thermal Dissipation



As the PCB acts as a heat sink, the layout of top and ground layers must be done with care to maximize the board surface dissipating the heat. The only limitation is the risk of losing routing channels. Figure 6-36 and Figure 6-37 show a routing with a good thermal dissipation thanks to an optimized placement of power and signal vias. The ground plane should be on bottom layer for the best heat spreading (thicker layer than internal ones) and dissipation (direct contact with air). .

Figure 6-36. Layout for Good Thermal Dissipation - top layer

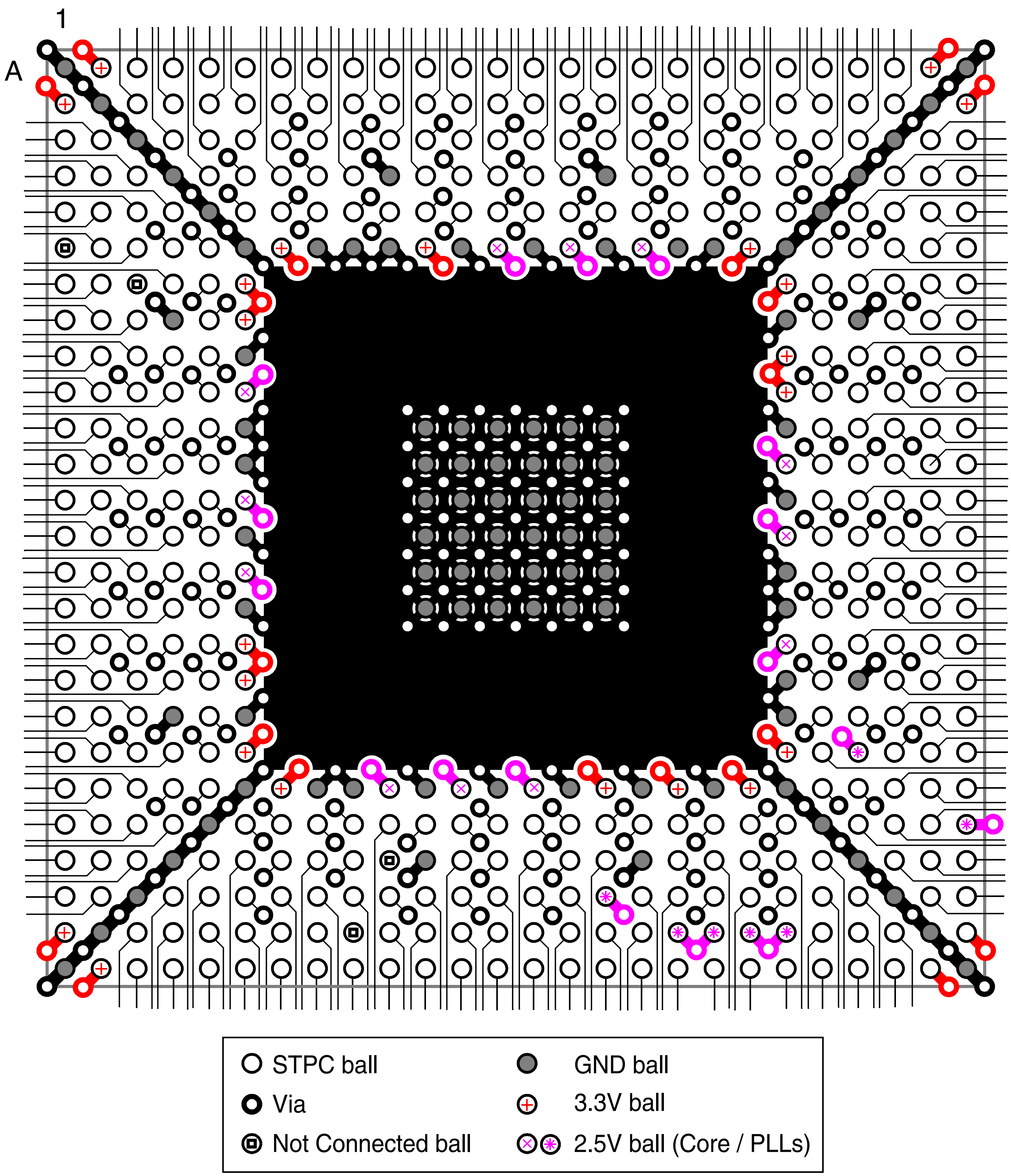
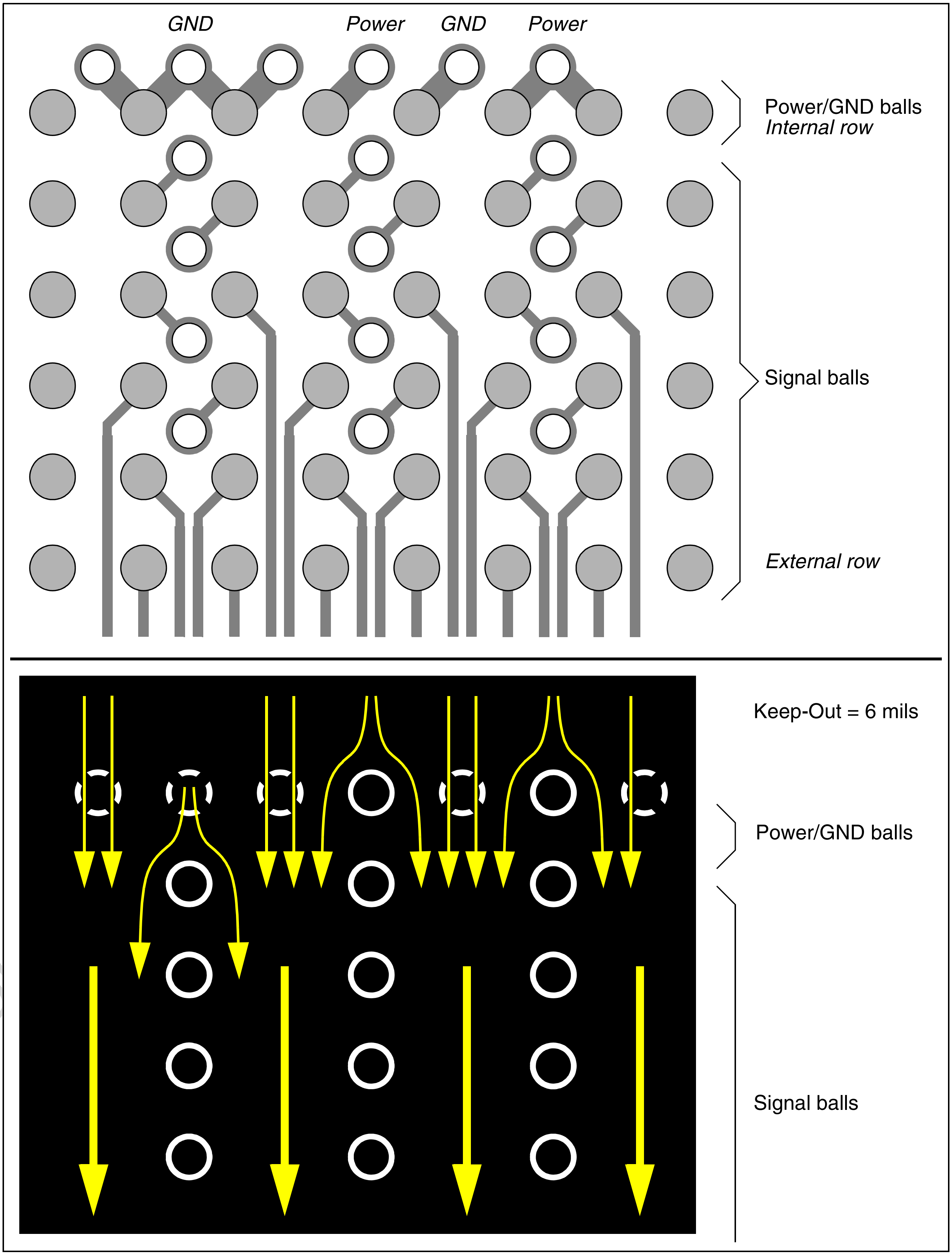


Figure 6-37. Recommend signal wiring (top & ground layers) with corresponding heat flow



6.6. DEBUG METHODOLOGY

In order to bring a STPC-based board to life with the best efficiency, it is recommended to follow the check-list described in this section.

6.6.1. POWER SUPPLIES

In parallel with the assembly process, it is useful to get a bare PCB to check the potential short-circuits between the various power and ground planes. This test is also recommended when the first boards are back from assembly. This will avoid bad surprises in case of a short-circuit due to a bad soldering.

When the system is powered, all power supplies, including the PLL power pins must be checked to be sure the right level is present. See Table 4-2 for the exact supported voltage range:

VDD_CORE: 2.5V
VDD_xxxPLL: 2.5V
VDD: 3.3V

6.6.2. BOOT SEQUENCE

6.6.2.1. Reset input

The checking of the reset sequence is the next step. The waveform of SYSRSTI# must complies with the timings described in Figure 4-3. This signal must not have glitches and must stay low until the 14.31818MHz output (OSC14M) is at the right frequency and the strap options are stabilized to a valid configuration.

In case this clock is not present, check the 14MHz oscillator stage (see Figure 6-4).

6.6.2.2. Strap options

The STPC has been designed in a way to allow configurations for test purpose that differs from the functional configuration. In many cases, the troubleshootings at this stage of the debug are the resulting of bad strap options. This is why it is mandatory to check they are properly setup and sampled during the boot sequence.

The list of all the strap options is summarized at the beginning of Section 3.

6.6.2.3. Clocks

Once OSC14M is checked and correct, the next signals to measure are the Host clock (HCLK), PCI clocks (PCI_CLKO, PCI_CLKI) and Memory clock (MCLKO, MCLKI).

HCLK must run at the speed defined by the corresponding strap options (see Table 3-1). In x2 CPU clock mode, this clock must be limited to 66MHz.

PCI_CLKI and PCI_CLKO must be connected as described in Figure 6-29 and not be higher than 33MHz. Their speed depends on HCLK and on the divider ratio defined by the MD[4] and MD[17] strap options as described in Section 3.
To ensure a correct behaviour of the device, the PCI deskewing logic must be configured properly by the MD[7:6] strap options according to Section 3. For timings constraints, refers to Section 4.

1) MCLKI and MCLKO must be connected as described in Figure 6-5 to Figure 6-7 depending on the SDRAM implementation. The memory clock must run at HCLK speed when in synchronous mode and must not be higher than 90MHz in any case. The MCLK interface will run 100MHz operation is possible but board layout is so critical that 90MHz maximum operation is recommended.

6.6.2.4. Reset output

If SYSRSTI# and all clocks are correct, then the SYSRSTO# output signal should behave as described in Figure 4-3.

6.6.3. ISA MODE

Prior to check the ISA bus control signals, PCI_CLKI, ISA_CLK, ISA_CLK2X, and DEV_CLK must be running properly. If it is not the case, it is probably because one of the previous steps has not been completed.

6.6.3.1. First code fetches

When booting on the ISA bus, the two key signals to check at the very beginning are RMRTCCS# and FRAME#.

The first one is a Chip Select for the boot flash and is multiplexed with the IDE interface. It should toggle together with ISAOE# and MEMRD# to fetch the first 16 bytes of code. This corresponds to the loading of the first line of the CPU cache.

In case RMRTCCS# does not toggle, it is then necessary to check the PCI FRAME# signal. Indeed the ISA controller is part of the South Bridge and all ISA bus cycles are visible on the PCI bus.

If there is no activity on the PCI bus, then one of the previous steps has not been checked properly. If there is activity then there must be something conflicting on the ISA bus or on the PCI bus.

6.6.3.2. Boot Flash size

The ISA bus supports 8-bit and 16-bit memory devices. In case of a 16-bit boot flash, the signal MEMCS16# must be activated during RMRTCCS# cycle to inform the ISA controller of a 16-bit device.

6.6.3.3. POST code

Once the 16 first bytes are fetched and decoded, the CPU core continue its execution depending on the content of these first data. Usually, it corresponds to a JUMP instruction and the code fetching continues, generating read cycles on the ISA bus.

Most of the BIOS and boot loaders are reading the content of the flash, decompressing it in SDRAM, and then continue the execution by jumping to the entry point in RAM. This boot process ends with a JUMP to the entry point of the OS launcher.
These various steps of the booting sequence are codified by the so-called POST codes (Power-On Self-Test). A 8-bit code is written to the port 80H at the beginning of each stage of the booting process (I/O write to address 0080H) and can be displayed on two 7-segment display, enabling a fast visual check of the booting completion level.
Usually, the last POST code is 0x00 and corresponds to the jump into the OS launcher.

When the execution fails or hangs, the lastest written code stays visible on that display, indicating either the piece of code to analyse, either the area of the hardware not working properly.

6.6.4. LOCAL BUS MODE

As the Local Bus controller is located into the Host interface, there is no access to the cycles on the PCI, reducing the amount of signals to check.

6.6.4.1. First code fetches

When booting on the Local Bus, the key signal to check at the very beginning is FCS0#. This signal is a Chip Select for the boot flash and should toggle together with PRD# to fetch the first 16 bytes of code. This corresponds to the loading of the first line of the CPU cache.
In case FCS0# does not toggle, then one of the previous steps has not been done properly, like HCLK speed and CPU clock multiplier (x1, x2).

6.6.4.2. Boot Flash size

The Local Bus support 8-bit and 16-bit boot memory devices only.

6.6.4.3. POST code

Like in ISA mode, POST codes can be implemented on the Local Bus. The difference is that an IOCS# must be programmed at I/O address 80H prior to writing these code, the POST display being connected to this IOCS# and to the lower 8 bits of the bus.

6.6.5. SUMMARY

Here is a check-list for the STPC board debug from power-on to CPU execution.

For each step, in case of failure, verify first the corresponding balls of the STPC:
- check if the voltage or activity is correct
- search for potential shortcuts.

For troubleshooting in steps 5 to 10, verify the related strap options:
- value & connection. Refer to Section 3.
- see Figure 4-3 for timing constraints

Steps 8a and 9a are for debug in ISA mode while steps 8b and 9b are for Local Bus mode.

6.6.6. PCMCIA mode

As the STPC uses the RMRTCCS# signal for booting in that mode, the methodology is the same as for the ISA bus. The PCMCIA cards being 3.3V or 5V, the boot flash device must be 5V tolerant when directly connected on the address and data busses. An other solution is to isolate the flash from the PCMCIA lines using 5V tolerant LVTTL buffers.

	Check:	How?	Troubleshooting
1	Power supplies	Verify that voltage is within specs: - this must include HF & LF noise - avoid full range sweep Refer to Table 4-1 for values	Measure voltage near STPC balls: - use very low GND connection. Add some decoupling capacitor: - the smallest, the nearest to STPC balls.
2	14.318 MHz	Verify OSC14M speed	The 2 capacitors used with the quartz must match with the capacitance of the crystal. Try other values.
3	SYSRSTI# (Power Good)	Measure SYSRSTI# of STPC See Figure 4-3 for waveforms.	Verify reset generation circuit: - device reference - components value

	Check:	How?	Troubleshooting
5	HCLK	Measure HCLK is at selected frequency 25MHz < HCLK < 66MHz	HCLK wire must be as short as possible
6	PCI clocks	Measure PCICLKO: - maximum is 33MHz by standard - check it is at selected frequency - it is generated from HCLK by a division (1/2, 1/3 or 1/4) Check PCICLKI equals PCICLKO	Verify PCICLKO loops to PCICLKI. Verify maximum skew between any PCI clock branch is below 2ns. In Synchronous mode, check MCLKI.
7	Memory clocks	Measure MCLKO: - use a low-capacitance probe - maximum is 90MHz - check it is at selected frequency - In SYNC mode MCLK=HCLK - in ASYNC mode, default is 66MHz Check MCLKI equals MCLKO	Verify load on MCLKI. Verify MCLK programming (BIOS setting).
4	SYSRSTO#	Measure SYSRSTO# of STPC See Figure 4-3 for waveforms.	Verify SYSRSTI# duration. Verify SYSRSTI# has no glitch Verify clocks are running.
8a	PCI cycles	Check PCI signals are toggling: - FRAME#, IRDY#, TRDY#, DEVSEL# - these signals are active low. Check, with a logic analyzer, that first PCI cycles are the expected ones: memory read starting at address with lower bits to 0xFFF0	Verify PCI slots If the STPC don't boot - verify data read from boot memory is OK - ensure Flash is correctly programmed - ensure CMOS is cleared.
9a	ISA cycles to boot memory	Check RMRTCCS# & MEMRD# Check directly on boot memory pin	Verify MEMCS16#: - must not be asserted for 8-bit memory Verify IOCHRDY is not be asserted Verify ISAOE# pin: - it controls IDE / ISA bus demultiplexing
8b	Local Bus cycles to boot memory	Check FCS0# & PRD# Check directly on boot memory pin	Verify HCLK speed and CPU clock mode.
9b		Check, with a logic analyzer, that first Local Bus cycles are the expected one: memory read starting at the top of boot memory less 16 bytes	If the STPC don't boot - verify data read from boot memory is OK - ensure Flash is correctly programmed - ensure CMOS is cleared.
10	The CPU fills its first cache line by fetching 16 bytes from boot memory. Then, first instructions are executed from the CPU. Any boot memory access done after the first 16 bytes are due to the instructions executed by the CPU => Minimum hardware is correctly set, CPU executes code. Please have a look to the Bios Writer's Guide or Programming Manual to go further with your board testing.		

7 ORDERING DATA

7.1. ORDERING CODES

ST PC I2 H E Y C

STMicroelectronics Prefix → ST

Product Family → PC
- PC: PC Compatible

Product ID → I2
- I2: Atlas

Core Speed → H
- G: 120 MHz
- H: 133 MHz

Memory Speed → E
- D: 90 MHz
- E: 100 MHz

Package → Y
- Y: 516 Overmoulded BGA

Temperature Range → C
- C: Commercial
  - Tcase = 0 to +85°C
- I: Industrial
  - Tcase = -40 to +115°C

7.2 AVAILABLE PART NUMBERS

Part Number	Core Frequency (MHz)	CPU Mode	Memory Interface Speed (MHz)	Tcase Range (C)	Operating Voltage (V)
STPCI2HEYC[1]	133	X2	90	0°C to +85°C	2.45 - 2.7
STPCI2GDYI	120	X2	90	-40°C to +115°C	3.0 - 3.6

Note 1:
The STPC Atlas MClock signal can run up to 100MHz reliably, but PCB layout is so critical that the maximum guaranteed speed is 90MHz

8 REVISION HISTORY

Date	Revision	Description of Changes
Mar 04	1.1	Second release
Jan 05	3	Revision number incremented from 1.1 to 3 due to Internal Document Management System change Modified Figure 6-9.PCI clock routing with zero-delay clock buffer Added two capacitors (100pF) in Figure 6-16.Typical USB implementation.