CY8CTST120, CY8CTMG120, CY8CTMA120

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Silicon Errata for CY8CTST120, CY8CTMG120, and CY8CTMA120

This document describes the errata for the TrueTouch™ devices CY8CTST120, CY8CTMA120, and CY8CTMG120. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's data sheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8CTxx120	CY8CTST120-56LFXI
	CY8CTST120-56LFXIT
	CY8CTST120-00AXI
	CY8CTMG120-56LFXI
	CY8CTMG120-56LFXIT
	CY8CTMG120-00AXI
	CY8CTMA120-56LFXI
	CY8CTMA120-56LFXIT
	CY8CTMA120-00AXI

Errata Summary

The following table defines the errata applicability to available CY8CTxx120 family devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. Internal Main Oscillator (IMO) tolerance deviation at temperature extremes	CY8CTxx120	A	Silicon fix is planned.
[2]. The DP line of the USB interface may pulse low when the PSoC device wakes from sleep, causing an unexpected wakeup of the host computer	CY8CTxx120	A	Use workaround.
[3]. Invalid Flash reads may occur if Vdd is pulled to -0.5V just before power on	CY8CTxx120	A	Use workaround.
[4]. PMA Index Register fails to auto increment with CPU_Clock set to SysClk/1 (24 MHz)	CY8CTxx120	A	Use workaround.

1. Internal Main Oscillator (IMO) tolerance deviation at temperature extremes.

- **PROBLEM DEFINITION**
  Asynchronous digital communication interfaces may fail framing beyond 0 to 70°C. This problem does not affect end product usage between 0 and 70°C.
- **PARAMETERS AFFECTED**
  The IMO frequency tolerance. The worst case deviation when operated below 0°C and above +70°C and within the upper and lower data sheet temperature range is ±5%.
- **TRIGGER CONDITION**
  The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±4% when operated beyond the temperature range of 0 to +70°C.
- **SCOPE OF IMPACT**
  This problem may affect UART, IrDA, and FSK implementations.
- **WORKAROUND**
  Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
- **FIX STATUS**
  The cause of this problem and its solution has been identified. Silicon fix is planned to correct the deficiency in silicon.

2. The DP line of the USB interface may pulse low when the PSoC® device wakes from sleep causing an unexpected wakeup of the host computer

- **PROBLEM DEFINITION**
  When the device is operating at 4.75V to 5.25V and the 3.3V regulator is enabled, a short low pulse may be created on the DP signal line during device wakeup. The 15 µs to 20 µs low pulse of the DP line may be interpreted by the host computer as a de-attach or the beginning of a wakeup.
- **PARAMETERS AFFECTED**
  The bandgap reference voltage used by the 3.3V regulator decreases during sleep due to leakage. Upon device wakeup, the bandgap is re-enabled and after a delay for settling, the 3.3V regulator is enabled. On some devices the 3.3V regulator that is used to generate the USB DP signal may be enabled before the bandgap is fully stabilized. This can cause a low pulse on the regulator output and DP signal line until the bandgap stabilizes. In applications where Vdd is 3.3V, the regulator is not used; therefore, the DP low pulse is not generated.
- **WORKAROUND**
  To prevent the DP signal from pulsing low, keep the bandgap enabled during sleep. The most efficient method is to set the No Buzz bit in the OSC_CR0 register. The No Buzz bit keeps the bandgap powered and output stable during sleep. Setting the No Buzz bit results in a nominal 100 µA increase to sleep current. Leaving the analog reference block enabled during sleep also resolves this issue because it forces the bandgap to remain enabled. An example to disable the No Buzz bit is as follows.

  Assembly

```
M8C_SetBank1
or    reg[OSC_CR0], 0x20
M8C_SetBank0
```

  C

```
OSC_CR0 |= 0x20;
```

3. Invalid Flash reads may occur if Vdd is pulled to -0.5V just before power on.

- **PROBLEM DEFINITION**
  When Vdd of the device is pulled below ground just before power on, the first read from each 8K Flash page may be corrupted. This issue does not affect Flash page 0 because it is the selected page upon reset.
- **PARAMETERS AFFECTED**
  When Vdd is pulled below ground before power on, an internal Flash reference may deviate from its nominal voltage. The reference deviation tends to result in the first Flash read from that page returning 0xFF. During the first read from each page, the reference is reset. This results in all future reads returning the correct value. A short delay of 5 µs before the first real read provides time for the reference voltage to stabilize.
- **WORKAROUND**
  To prevent an invalid Flash read, a dummy read from each Flash page must occur before use of the pages. A delay of 5 µs must occur after the dummy read and before a real read. The dummy reads occurs as soon as possible and must be located in Flash page 0 before a read from any other Flash page. An example to read a byte of memory from each Flash page follows. Place it in boot.tpl and boot.asm immediately after the 'start:' label.

```
// dummy read from each 8K Flash page
// page 1
mov A, 0x20                 // MSB
mov X, 0x00                 // LSB
romx
// wait at least 5 µs
mov X, 14
loop1:
dec X
jnz loop1
```

4. PMA Index Register fails to auto increment with CPU_Clock set to SysClk/1 (24 MHz).

- **PROBLEM DEFINITION**
  When the device is operating at 4.75 to 5.25V and the CPU_Clock is set to SysClk/1 (24 MHz), the USB PMA Index Register may fail to increment automatically when used in an OUT endpoint configuration at full speed. When the application program attempts to use the bReadOutEP() function, the first byte in the PMA buffer is always returned.
- **PARAMETERS AFFECTED**
  An internal flip-flop hold problem associated with Index Register increment function. All reads of the associated RAM originate from the first byte. The hold problem has no impact on other circuits or functions within the device.
- **WORKAROUND**
  To make certain that the index register properly increments, set the CPU_Clock to SysClk/2 (12 MHz) during the read of the PMA buffer. An example for the clock adjustment method is listed below.

  PSoC Designer™ 4.3 User Module Workaround: PSoC Designer Release 4.3 and subsequent releases includes a revised full speed USB User Module, which includes the revised firmware as shown in the following example.

```
;;
;; 24Mhz read PMA workaround
;;
       M8C_SetBank1
       mov A, reg[OSC_CR0]
       push A
```

```
        and A, 0xf8 ;clear the clock bits (briefly chg the cpu_clk to 3Mhz)
        or A, 0x02 ;will set clk to 12Mhz

        mov reg[OSC_CR0],A ;clk is now set at 12Mhz
        M8C_SetBank0
.loop:
       mov A, reg[PMA0_DR] ; Get the data from the PMA space
       mov [X], A ; save it in data array
       inc X ; increment the pointer
       dec [USB_APITemp+1] ; decrement the counter
       jnz .loop ; wait for count to zero out
;;
;; 24Mhz read PMA workaround (back to previous clock speed)
;;
        pop A ;recover previous reg[OSC_CR0] value
        M8C_SetBank1
        mov reg[OSC_CR0],A ;clk is now set at previous value
        M8C_SetBank0
;; end 24Mhz read PMA workaround
```

References

[1] Document # 001-46932 CY8CTST120 TrueTouch™ Single-Touch Touchscreen Controller (Final)
[2] Document # 001-46929 CY8CTMG120 TrueTouch™ Multi-Touch Gesture Touchscreen Controller (Final)
[3] Document # 001-46901 CY8CTMA120 TrueTouch™ Multi-Touch All-Point Touchscreen Controller (Final)

Document History

Document Title: Silicon Errata for CY8CTST120, CY8CTMG120, and CY8CTMA120

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Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2572224	09/25/08	KRY	New errata for Touchscreen device.

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