XILINX®

IMPORTANT NOTICE
All new designs should use XC3000A. Information on XC3000 is presented here as a reference for existing designs. XC3000 bitstreams are upward compatible to XC3000A without modification.

XC3000 Logic Cell Array Family

Product Specification

Features

- Industry-leading FPGA family with five device types
  - Logic densities from 1,000 to 6,000 gates
  - Up to 144 user-definable I/Os
- Guaranteed 70- to 125-MHz toggle rates, 9 to 5.5 ns logic delays
- Advanced CMOS static memory technology
  - Low quiescent and active power consumption
- XC3000-specific features
  - Ultra-low current option in Power-Down mode
  - 4-mA output sink and source current
  - Broad range of package options includes plastic and ceramic quad flat packs, plastic leaded chip carriers and pin grid arrays
  - 100% bitstream compatible with the XC3100 family
  - Commercial, industrial, military, “high rel”, and MIL-STD-883 Class B grade devices
  - Easy migration to XC3300 series of HardWire mask-programmed devices for high-volume production

Description

XC3000 is the original family of devices in the XC3000 class of Field Programmable Gate Array (FPGA) architectures. The XC3000 family has a proven track record in addressing a wide range of design applications, including general logic replacement and sub-systems integration. For a thorough description of the XC3000 architecture see the preceding pages of this data book.

The XC3000 Family covers a range of nominal device densities from 2,000 to 9,000 gates, practically achievable densities from 1,000 to 6,000 gates. Device speeds, described in terms of maximum guaranteed toggle frequencies, range from 70 to 125 MHz. The performance of a completed design depends upon placement and routing implementation, so, like with any gate array, the final verification of device utilization and performance can only be known after the design has been placed and routed.

Device	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3020	64	8 x 8	64	256	16	14,779
XC3030	100	10 x 10	80	360	20	22,176
XC3042	144	12 x 12	96	480	24	30,784
XC3064	224	16 x 14	120	688	32	46,064
XC3090	320	16 x 20	144	928	40	64,160

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to +100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

DC Characteristics Over Operating Conditions

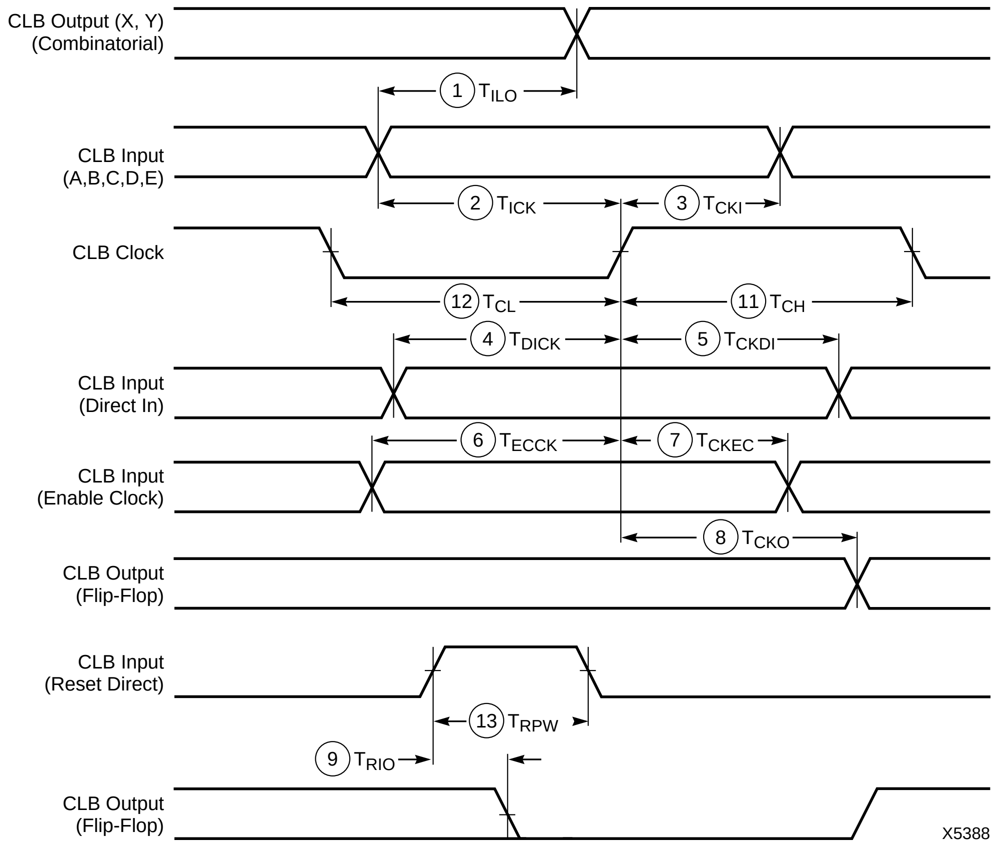
Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)	Commercial		0.40	V
V_{OH}	High-level output voltage (@ I_{OH} = –4.0 mA, V_{CC} min)	Industrial	3.76		V
V_{OL}	Low-level output voltage (@ I_{OL} = 4.0 mA, V_{CC} min)	Industrial		0.40	V
V_{CCPD}	Power-down supply voltage ($\overline{PWRDWN}$ must be Low)		2.30		V
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})[1]	XC3020		50	µA
		XC3030		80	µA
		XC3042		120	µA
		XC3064		170	µA
		XC3090		250	µA
I_{CCO}	Quiescent LCA supply current in addition to I_{CCPD}[2] Chip thresholds programmed as CMOS levels			500	µA
	Chip thresholds programmed as TTL levels			10	mA
I_{IL}	Input Leakage Current		–10	+10	µA
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 10 15	 pF pF
	Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			 15 20	 pF pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0 V (sample tested)		0.02	0.17	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low			3.4	mA

Note: 1. Devices with much lower I_{CCPD} tested and guaranteed at V_{CC} = 3.2 V, T = 25°C can be ordered with a Special Product Code.

XC3020 SPC0107: I_{CCPD} = 1 µA
XC3030 SPC0107: I_{CCPD} = 2 µA
XC3042 SPC0107: I_{CCPD} = 3 µA
XC3064 SPC0107: I_{CCPD}= 4 µA
XC3090 SPC0107: I_{CCPD}= 5 µA

2. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

CLB Switching Characteristic Guidelines



Buffer (Internal) Switching Characteristic Guidelines

	Speed Grade	-70	-100	-125	Units
Description	**Symbol**	**Max**	**Max**	**Max**	
Global and Alternate Clock Distribution*					
Either: **Normal** IOB input pad through clock buffer to any CLB or IOB clock input	T_{PID}	8.0	7.5	7.0	ns
Or: **Fast** (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PIDC}	6.5	6.0	5.7	ns
TBUF driving a Horizontal Longline (L.L.)*					
I to L.L. while T is Low (buffer active)	T_{IO}	5.0	4.7	4.5	ns
T↓ to L.L. active and valid with single pull-up resistor	T_{ON}	11.0	10.0	9.0	ns
T↓ to L.L. active and valid with pair of pull-up resistors	T_{ON}	12.0	11.0	10.0	ns
T↑ to L.L. High with single pull-up resistor	T_{PUS}	24.0	22.0	17.0	ns
T↑ to L.L. High with pair of pull-up resistors	T_{PUF}	17.0	15.0	12.0	ns
BIDI					
Bidirectional buffer delay	T_{BIDI}	2.0	1.8	1.7	ns

* Timing is based on the XC3042, for other devices see XACT timing calculator.

CLB Switching Characteristic Guidelines (continued)

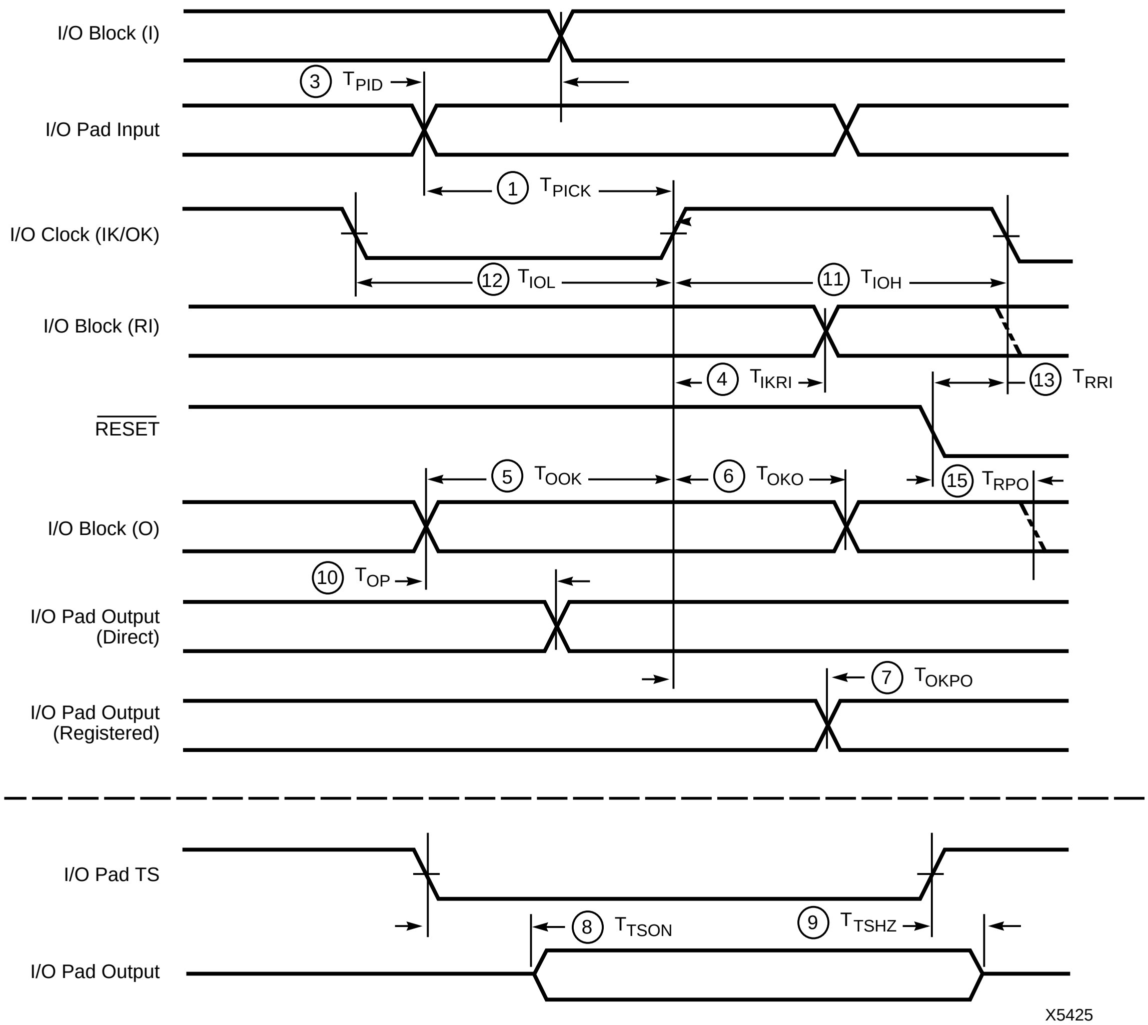
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

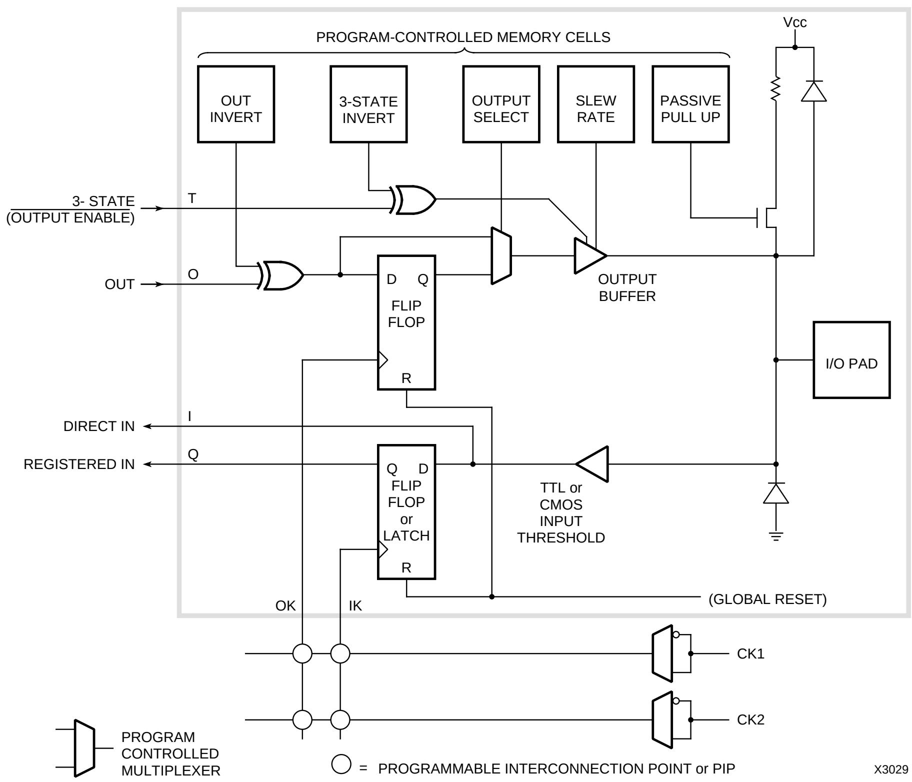
Speed Grade			-70		-100		-125		
Description		**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delay									
Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		9.0		7.0		5.5	ns
Sequential delay									
Clock k to outputs X or Y	8	T_{CKO}		6.0		5.0		4.5	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		13.0		10.0		8.0	ns
Set-up time before clock K									
Logic Variables A, B, C, D, E	2	T_{ICK}	8.0		7.0		5.5		ns
Data In DI	4	T_{DICK}	5.0		4.0		3.0		ns
Enable Clock EC	6	T_{ECCK}	7.0		5.0		4.5		ns
Reset Direct inactive RD			1.0		1.0		1.0		ns
Hold Time after clock K									
Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		0		ns
Data In DI	5	T_{CKDI}	4.0		2.0		1.5		ns
Enable Clock EC	7	T_{CKEC}	0		0		0		ns
Clock									
Clock High time	11	T_{CH}	5.0		4.0		3.0		ns
Clock Low time	12	T_{CL}	5.0		4.0		3.0		ns
Max flip-flop toggle rate		F_{CLK}	70		100		125		MHz
Reset Direct (RD)									
RD width	13	T_{RPW}	8.0		7.0		6.0		ns
delay from rd to outputs X or Y	9	T_{RIO}		8.0		7.0		6.0	ns
Global Reset (RESET Pad)*									
RESET width (Low)		T_{MRW}	25.0		21.0		20.0		ns
delay from RESET pad to outputs X or Y		T_{MRQ}		23.0		19.0		17.0	ns

*Timing is based on the XC3042, for other devices see XACT timing calculator.

Note: The CLB K to Q output delay (T_{CKO}, #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI}, #5) of any CLB on the same die.

IOB Switching Characteristic Guidelines





IOB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-70		-100		-125		Units
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays (Input)									
Pad to Direct In (I)	3	T_{PID}		6		4		3	ns
Pad to Registered In (Q) with latch transparent		T_{PTG}		21		17		16	ns
Clock (IK) to Registered In (Q)	4	T_{IKRI}		5.5		4		3	ns
Set-up Time (Input)									
Pad to Clock (IK) set-up time	1	T_{PICK}	20		17		16		ns
Propagation Delays (Output)									
Clock (OK) to Pad (fast)	7	T_{OKPO}		13		10		9	ns
same (slew rate limited)	7	T_{OKPO}		33		27		24	ns
Output (O) to Pad (fast)	10	T_{OPF}		9		6		5	ns
same (slew-rate limited)	10	T_{OPS}		29		23		20	ns
3-state to Pad begin hi-Z (fast)	9	T_{TSHZ}		8		8		7	ns
same (slew-rate limited)	9	T_{TSHZ}		28		25		24	ns
3-state to Pad active and valid (fast)	8	T_{TSON}		14		12		11	ns
same (slew -rate limited)	8	T_{TSON}		34		29		27	ns
Set-up and Hold Times (Output)									
Output (O) to clock (OK) set-up time	5	T_{OOK}	10		9		8		ns
Output (O) to clock (OK) hold time	6	T_{OKO}	0		0		0		ns
Clock									
Clock High time	11	T_{IOH}	5		4		3		ns
Clock Low time	12	T_{IOL}	5		4		3		ns
Max. flip-flop toggle rate		F_{CLK}	70		100		125		MHz
Global Reset Delays (based on XC3042)									
RESET Pad to Registered In (Q)	13	T_{RRI}		25		24		23	ns
RESET Pad to output pad (fast)	15	T_{RPO}		35		33		29	ns
(slew-rate limited)	15	T_{RPO}		53		45		42	ns

Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). For larger capacitive loads, see XAPP 024. Typical slew rate limited output rise/fall times are approximately four times longer.
2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
3. Input pad setup time and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but the subtracted value cannot be less than zero (i.e., negative hold time). Negative hold time means that the delay in the input data is adequate for the **external system hold time** to be zero, provided the input clock uses the Global signal distribution from pad to IK .

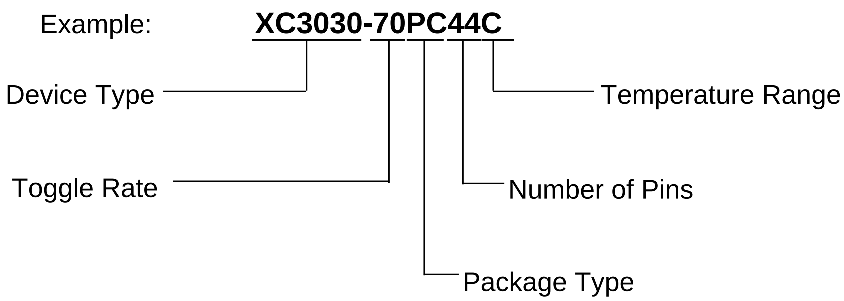
For a detailed description of the device architecture, see pages 2-105 through 2-123.

For a detailed description of the configuration modes and their timing, see pages 2-124 through 2-132.

For detailed lists of package pin-outs, see pages 2-140 through 2-150.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		44	64	68	84		100				132		144	160	164	175		176	208	223
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM. PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP-BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100	PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3020	-50					M B				M B										
	-70			C I	C I	C I M B	C I			C M B										
	-100			C I	C I	C I M B	C I			C M B										
	-125			C	C	C	C													
XC3030	-50					M														
	-70	C I		C I	C I	C I M	C I	C												
	-100	C I		C I	C I	C I M	C I	C												
	-125	C		C	C	C	C	C												
XC3042	-50					M B				M B		M B								
	-70				C I	C I M B	C I	C		C M B	C	C I M B								
	-100				C I	C I M B	C I	C		C M B	C	C I M B								
	-125				C	C	C	C			C	C								
XC3064	-50											M								
	-70				C I						C I	C I M		C I						
	-100				C I						C I	C I M		C I						
	-125				C						C	C		C						
XC3090	-50														M B		M B			
	-70				C I									C I	C M B	C I	C I M B		C I	
	-100				C I									C I	C M B	C I	C I M B		C I	
	-125				C									C		C	C		C	

C = Commercial = 0° to +70° C I = Industrial = -40° to +85° C M = Mil Temp = -55° to +125° C B = MIL-STD-883C Class B

Parentheses indicate future product plans