Cyclone III Device Family Errata Sheet

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This errata sheet provides updated technical information for Cyclone® III devices. This document addresses known device issues and includes methods to work around the issues.

Table 1 lists the specific issues and which Cyclone III devices each issue affects.

Table 1. Cyclone III Device Family Issues

Issue	Affected Devices	Solution
M9K Memory Block Read Issue	All 65-nm and some 60-nm Cyclone III and Cyclone III LS devices. For more information, refer to Table 2.	For a solution, refer to M9K Memory Block Read Issue. Fixed in: Cyclone III 60-nm: EP3C55, EP3C80, and EP3C120 devices, Revision B Cyclone III LS: EP3CLS150 and EP3CLS200 devices, Revision B
External Memory Specification for DDR2 SDRAM Full Rate on the Column I/O	All Cyclone III devices	For a solution, refer to External Memory Specification for DDR2 SDRAM.
MSEL pins may be sensed at a different setting than was intended if connected to V_{CCIO} for logic high and V_{CCIO} sags below 0.75 after power on reset and before configuration starts.	All Cyclone II devices	For a solution, refer to MSEL Pin Connection.
Momentary current surge from the V_{CCINT} supply after configuration.	EP3C25 ES Revision B and C EP3C120 ES Revision A	Fixed in: EP3C25 Revision D EP3C120 Revision B EP3C120 Revision C

M9K Memory Block Read Issue

The Cyclone III M9K embedded memory blocks may exhibit bit error in which the read bit is a 1 when the expected bit is a 0. The problem is caused by bitline coupling in the read output. The issue is rare and requires the presence of multiple conditions for the M9K block to be susceptible to the bit error. The conditions include the use model of the M9K block, the application data pattern, and the operating conditions.

Designs using the M9K blocks in dual clock and widest data width (×32 or ×36) modes are most susceptible to the bit error. Designs using the M9K blocks in single clock or narrower data width modes are not affected when operating within data sheet specifications. The problem is highly data-pattern dependent and triggered by specific data bit combinations. Lastly, the problem can be exacerbated by lower temperature and lower voltage operations. The presence of all these conditions does not imply a bit error would necessarily occur. In addition, if some or all of the conditions are not present, the error will not occur.

This issue only affects the read operation. The M9K write operation and the M9K memory cell array content are not affected. In addition, the issue is not a wear-out mechanism and does not affect the long-term reliability of the devices.

The affected Cyclone III and Cyclone III LS devices can be distinguished by the die revision identifier (**Z**) and the fab process code identifier (αα) found in the Altera® date code marked on the top side of the device. Figure 1 shows the date code format. Table 2 lists the devices affected by the M9K memory read issue.

Figure 1. Altera Data Code Marking Format

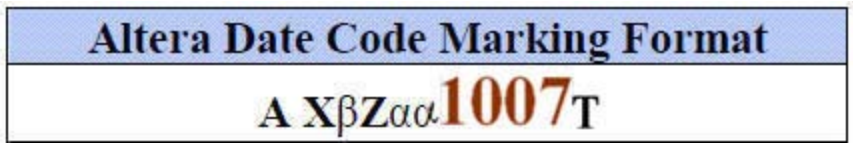

Table 2. Affected Devices

Device	Die Revision (Z)	Fab Process Code (αα)
Cyclone III 65-nm: All devices	All Revisions	A5, A0
Cyclone III 60-nm: EP3C55, EP3C80, and EP3C120 devices	A	AA
Cyclone III LS: EP3CLS150 and EP3CLS200 devices	A	AA

Quartus II Software Workaround

A Quartus II software solution is available to work around this issue. To resolve the problem, the solution disables up to eight data bits in the widest data width mode. Applying the software solution may require additional M9K resources. If a fitter error occurs, contact Altera for additional support.

For more information about applying this solution, refer to the "How do I resolve the M9K memory block read issue in Cyclone III devices using the Quartus II software solution?" section in the Knowledge Database.

External Memory Specification for DDR2 SDRAM

In the Quartus® II software version 9.0, the Cyclone III C7, C8, I7, and A7 speed grades supported full-rate DDR2 SDRAM with a maximum clock rate of up to 167 MHz and the Cyclone III C6 speed grade supported full-rate DDR2 SDRAM with a maximum clock rate of up to 200 MHz on column I/Os.

In the Quartus II software version 9.1 and beyond, the Cyclone III all speed grades full-rate DDR2 SDRAM maximum clock rate specifications on column I/Os have been downgraded. The current specifications are listed in Table 3.

The downgrade of the maximum clock rate is due to the Quartus II software tool's inability to achieve push-button placement at the faster clock rates with the DDR2 SDRAM High-Performance Controller II.

If you are using the High-Performance Controller, you are not affected by this downgrade.

Both Quartus II version 9.0 and 9.1 specifications refer to the DDR2 SDRAM AFI-based PHY.

To achieve a higher clock rate in your system, refer to this Solution.

Table 3. Full-Rate DDR2 SDRAM Support for Cyclone III Devices

Memory Standard	Device	Speed Grade	Maximum Clock Rate (MHz)
			Column I/O
			Single Chip Select
DDR2 SDRAM	Cyclone III	C6	167 *(1)*
		C7	150 *(2)*
		C8, I7, A7	150 *(1)*

Note to Table 3:

(1) You must use 267-MHz memory component speed grade when using the Class I I/O standard and a 333-MHz memory component speed grade when using the Class II I/O standard.

(2) You must use a 200-MHz memory component speed grade.

MSEL Pin Connection

Altera has identified an issue with Cyclone III MSEL pins connected to V_{CCIO} for logic high. If V_{CCIO} sags below 0.75 V after power on reset and before configuration starts, the MSEL pins may be sensed at a different setting than was intended. The device might then require a power cycle to recover. This issue does not occur when the device is in user mode or when configuration has started.

Solution

Connect MSEL pins to V_{CCA} for a logic high. If V_{CCA} sags below the device's POR trip point then the POR circuit will reset the device. If you have already connected the MSEL pins to V_{CCIO} on your board, make sure that V_{CCIO} rises monotonically to its recommended operating condition voltage level and stays within the voltage min and max. A monotonic rise will prevent the issue from occurring.

Configuration Transition Current Issue

Cyclone III EP3C25 ES Revision B and C and EP3C120 ES Revision A devices might exhibit a momentary current surge from the V_{CCINT} supply after configuration. If your system's V_{CCINT} supply does not provide this current, the Cyclone III device might not transition into user mode as intended. This issue will be fixed in all production devices. While the size of the current surge is dependent on your design and on Quartus II placement and routing, the following currents are maximums for each device.

Table 4. Transition Current

Device	Peak Current from V_{CCINT} Supply During Transition
EP3C25	600 mA
EP3C120	3 A

If you use JTAG for initialization, the duration of the current surge is a maximum of 74 TCK clock periods. If you use the CLKUSR pin for initialization, the duration of the current surge is a maximum of 74 CLKUSR clock periods. Otherwise, the duration of the current surge is a maximum of 15 µs. The fastest rise time within the surge is 150 ns.

Workaround

To ensure V_{CCINT} voltage level stability during the transition from configuration mode to user mode, the system needs to supply the peak transition current. Table 5 lists the maximum V_{CCINT} supply impedance allowed to meet the current surge while maintaining voltage level stability. Additionally, Table 5 lists typical capacitors, along with a voltage regulator, that can produce a V_{CCINT} supply impedance that is at or lower than the maximum

Table 5. V_{CCINT} Supply Impedance and Typical Capacitors

Device	Maximum V_{CCINT} Supply Impedance	Typical V_{CCINT} Capacitor
EP3C25	0.25 Ω	100 µF low ESR tantalum and 10 µF ceramic
EP3C120	0.05 Ω	470 µF low ESR tantalum and 100 µF ceramic

Note to Table 5:

(1) Impedances as listed result in a V_{CCINT} drop of no more than 150 mV.

(2) Impedance is over the range of DC to 2.4 MHz.

(3) Minimum capacitors at one each per Cyclone III device to meet the transition current surge. Normal user mode operation likely requires additional bulk and decoupling capacitors.

Typically a robust V_{CCINT} power system designed to handle Cyclone III user mode operation meets the above impedances. For example, the V_{CCINT} power systems on the Cyclone III FPGA Starter Kit board (3C25) and the Cyclone III FPGA Development Kit board (3C120) are below the maximum impedances.

3.3-V I/O Power Static Current Issue

Altera has identified an issue with static current in I/O banks powered at 3.3-V V_{CCIO} on Cyclone III EP3C25 Revision B and C and EP3C120 Revision A and B engineering sample devices. The affected devices might draw more current than expected as stated in Table 6. You should take the additional I/O current into consideration when designing the V_{CCIO} power system on your board. This issue does not affect I/O banks powered at 3.15 V V_{CCIO} or below.

Table 6. Additional I/O Current

Device	Maximum Increase of ICCIO Per I/O Banks Powered at 3.3-V V_{CCIO}
EP3C25	8 mA
EP3C120	15 mA

Note to Table 6;

(1) This current increase per 3.3-V I/O bank is in addition to the existing power estimations shown in the PowerPlay Early Power Estimator or Quartus II PowerPlay Power Analyzer tools.

This issue will be fixed in production silicon for the EP3C25 Revision D and EP3C120 Revision C and their later revisions.

Document Revision History

Table 7 lists the revision history for this errata sheet.

Table 7. Document Revision History

Date	Version	Changes Made
June 2010	3.0	■ Added "M9K Memory Block Read Issue" on page 1. ■ Added "External Memory Specification for DDR2 SDRAM" on page 2.
July 2007	2.0	■ Added "Configuration Transition Current Issue" on page 3. ■ Added "3.3-V I/O Power Static Current Issue" on page 4.
2003	1.0	Initial release.

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