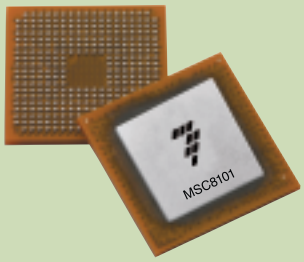
Digital Signal Processors

MSC8101



The Network DSP with Enhanced Filter Coprocessor (EFCOP)

The MSC8101 integrated network-ready DSP is optimized for networking infrastructure applications. With its unique combination of an SC140 DSP core, programmable Communications Processor Module (CPM) and PowerPC® bus interface, the MSC8101 offers advanced signal processing performance, flexible network connectivity and seamless system integration.

The MSC8101 is designed for demanding network infrastructure applications requiring very high performance, large amounts of on-chip memory and networking capabilities such as 2.5G and 3G wireless infrastructure systems, packet telephony solutions (VoIP), and packet aggregation. It can also provide a network interface for a DSP farm of MSC8102 devices.

Next-generation networking infrastructure systems are based on a configurable open architecture platform that supports real-time voice, fax and data on a packet-switched network. Through its integrated CPM, the MSC8101 has the unique ability to connect to the network, manage the Layer 2 and Layer 3 protocols, and extract data directly from the network.

What Is EFCOP?

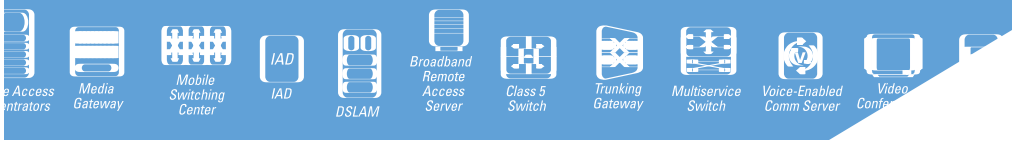
The MSC8101 integrates an Enhanced Filter Coprocessor (EFCOP)—a dedicated, programmable filter multiply accumulate (fMAC) peripheral module that operates in parallel with, and at the same frequency as, the SC140 core. It is optimized for filter operations such as FIR and IIR filters and can be used for running filter-based algorithms, such as echo cancellation, while the core is free to perform other operations, like voice coding. The EFCOP delivers the potential to increase channel density while enhancing voice quality in multichannel applications such as wireless transcoders and media gateways. With its four Arithmetic Logic Units (ALUs), plus its EFCOP running at the core frequency, the MSC8101 offers up to 1500 MMACs of signal processing performance in a low-power 17 mm x 17 mm package.

The MSC8101 CPM is a programmable 32-bit RISC protocol machine that allows connectivity to standard network backbones: ATM, Fast Ethernet and fast TDM highways. This 200 MHz CPM engine is derived from Freescale's popular MPC8260 PowerQUICC II™ microprocessor. An integrated, 100 MHz, 64-bit PowerPC bus interface allows easy connection to multimaster PowerPC-based systems and direct connectivity to PowerPC bus peripherals.

Time-to-Market…Time-to-Money

In order to minimize development time, a comprehensive set of software, hardware and development tools and application software modules supports the MSC8101. Baseline development tools include the assembler, linker, C compiler, optimizer, simulator and other utilities—all supplied by Metrowerks.

The StarCore® SC140 core was designed with C compilation in mind, and the compiler provides efficient code optimization while maintaining optimum code density. In addition, Freescale offers a wide choice of integrated development environments (IDEs) and real-time operating systems (RTOSes) through third-party suppliers. Another key factor in accelerating time-to-market is the availability of optimized application software modules, both in C code and assembly, for use in the customer's application. Freescale is working with a variety of third-party developers to develop complete packet telephony solutions and along with individual software examples, including speech coders, echo cancellers, and fax and modem modules. In addition to low cost EVMs, Freescale offers complete Application Development Systems and MSC8101- and PowerQUICC II-based reference designs.

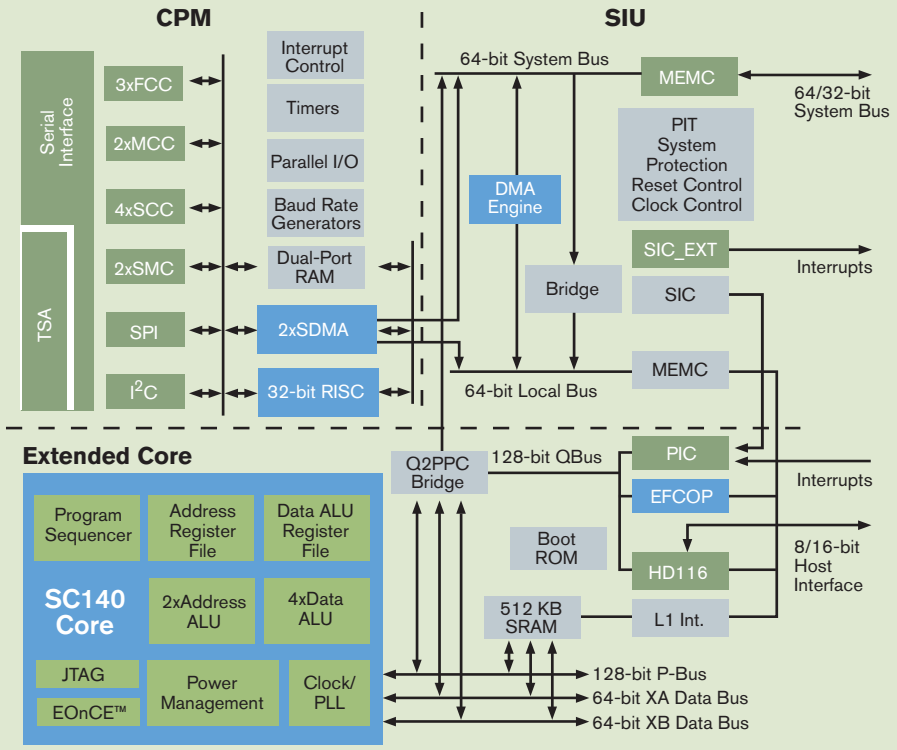


freescale semiconductor

Product Features

> Up to 300 MHz SC140 Core
  - Up to 1200 MMACs, 3000 RISC MIPS
> Additional 300 MMACs using 32-bit EFCOP
> Up to 100 MHz 64/32-bit, 60x Power PC Bus
> Up to 200 MHz CPM supporting:
  - 155 Mbps ATM
  - 10/100 Mbps Ethernet
  - Up to four E1/T1
> 512 KB (256K words) of on-chip SRAM
> 16-channel DMA Controller
> Eight-bank memory controller
  - SDRAM, SRAM, DRAM, EPROM, Flash
> 16-bit host interface
> Low power consumption—0.86W
> Enhanced On-Chip Emulation (EOnCE)
> Space-saving 17 mm x 17 mm FC-PBGA package

MSC8101 BLOCK DIAGRAM



Key Advantages

High Performance

> High-speed 250, 275, 300 MHz SC140 core yields 1000–1200 MMACs, up to 1500 MMACs with EFCOP
> Four orthagonal data ALUs provide excellent flexibility
> Efficiently executes up to six parallel instructions in one clock cycle

Compatibility

> C programming supports fast time-to-market
> High code density results in lower system costs
> Highly maintainable due to use of C code
> Software compatibility across the StarCore family

Low Power Dissipation

> Supports plastic packaging
> Enables a variety of applications

Software Development Tools

> Tools integrated under an IDE
> Real-time debug capability
> Optimized C compiler generates efficient control and DSP code
> Low overhead operating systems

Learn More

For more information about Freescale's products, please visit **www.freescale.com/smartnetworks**.

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

MSC8101FS
REV 6

freescale semiconductor