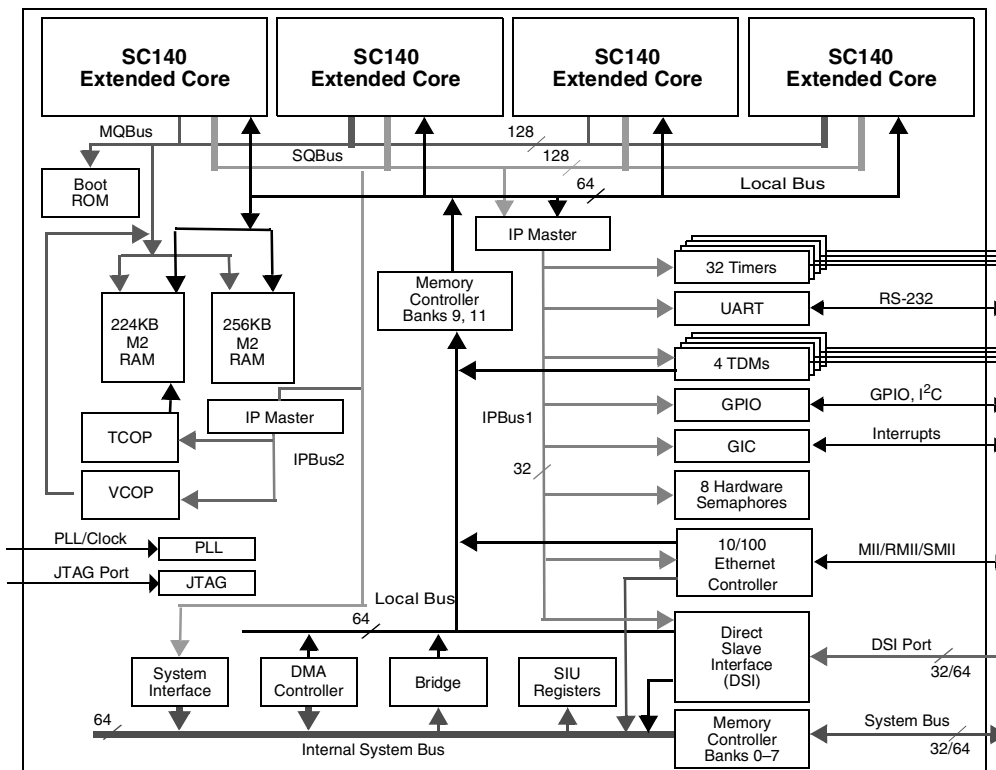


# MSC8126

## Quad Core 16-Bit Digital Signal Processor



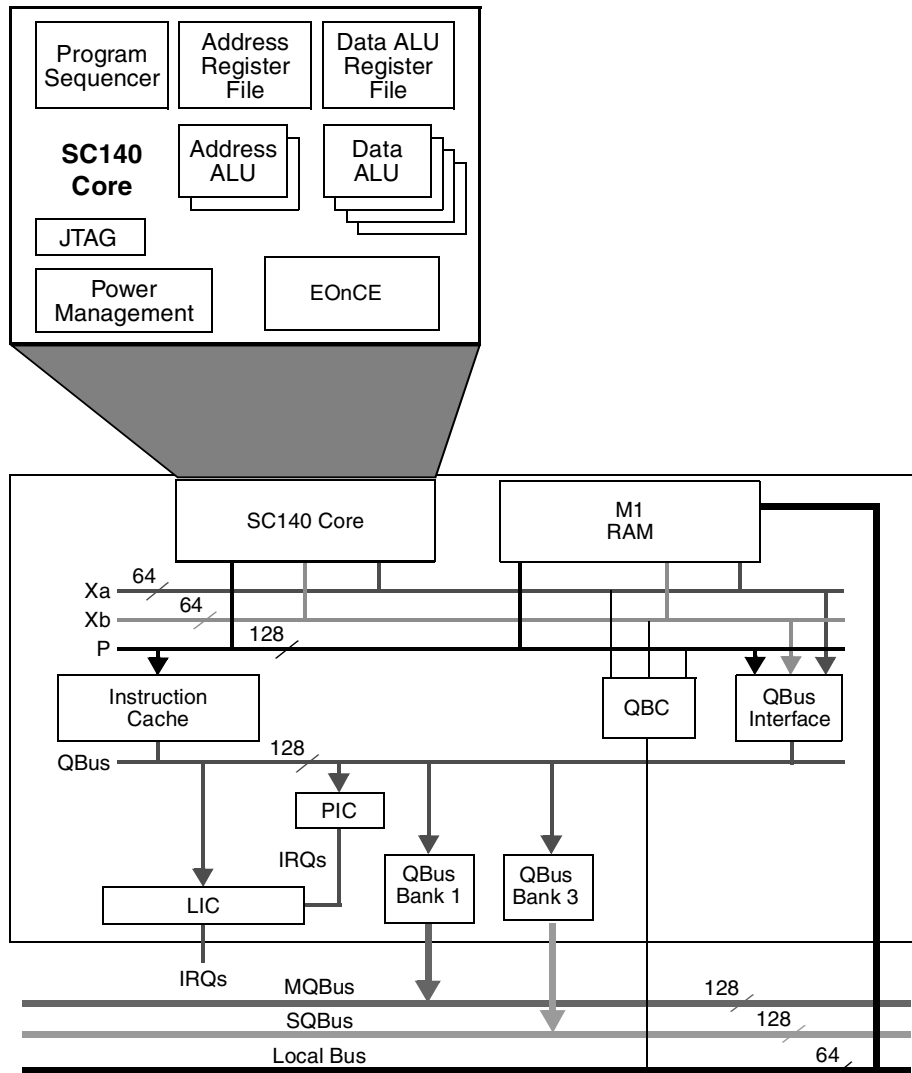
*The raw processing power of this highly integrated system-on-a-chip device enables developers to create next-generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability, and upgradeability. The MSC8126 is offered in two core speed levels: 400 and 500 MHz*

**Note:** The arrows show the direction from which the transfer originates.

**Figure 1.** MSC8126 Block Diagram

The MSC8126 is a highly integrated system-on-a-chip that combines four SC140 extended cores with a turbo coprocessor (TCOP), a Viterbi coprocessor (VCOP), an RS-232 serial interface, four time-division multiplexed (TDM) serial interfaces, thirty-two general-purpose timers, a flexible system interface unit (SIU), an Ethernet interface, and a multi-channel DMA engine. The four extended cores can deliver a total 6400/8000 DSP MMACS performance at 400/500 MHz. Each core has four arithmetic logic units (ALUs), internal memory, a write buffer, and two interrupt controllers (see **Figure 2**). The MSC8126 device targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications. The MSC8126 delivers enhanced performance while maintaining low power dissipation and greatly reduces system cost.

**Note:** This document contains information on a new product. Specifications and information herein are subject to change without notice.



- Notes:**
1. The arrows show the data transfer direction.
  2. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

**Figure 2.** SC140 Extended Core Block Diagram

## Features

The tables in this section list the features of the MSC8126 device.

**Table 1.** Extended SC140 Cores and Core Memories

Feature	Description
<b>SC140 Core</b>	<p>Four SC140 cores:</p> <ul style="list-style-type: none"> <li>• Up to 8000 MMACS using 16 ALUs running at up to 500 MHz.</li> <li>• A total of 1436 KB of internal SRAM (224 KB per core).</li> </ul> <p>Each SC140 core provides the following:</p> <ul style="list-style-type: none"> <li>• Up to 2000 MMACS using an internal 500 MHz clock. A MAC operation includes a multiply-accumulate command with the associated data move and pointer update.</li> <li>• 4 ALUs per SC140 core.</li> <li>• 16 data registers, 40 bits each.</li> <li>• 27 address registers, 32 bits each.</li> <li>• Hardware support for fractional and integer data types.</li> <li>• Very rich 16-bit wide orthogonal instruction set.</li> <li>• Up to six instructions executed in a single clock cycle.</li> <li>• Variable-length execution set (VLES) that can be optimized for code density and performance.</li> <li>• IEEE® Std. 1149.1™ JTAG port.</li> <li>• Enhanced on-device emulation (EOnCE) with real-time debugging capabilities.</li> </ul>
<b>Extended Core</b>	<p>Each SC140 core is embedded within an extended core that provides the following:</p> <ul style="list-style-type: none"> <li>• 224 KB M1 memory that is accessed by the SC140 core with zero wait states.</li> <li>• Support for atomic accesses to the M1 memory.</li> <li>• 16 KB instruction cache, 16 ways.</li> <li>• A four-entry write buffer that frees the SC140 core from waiting for a write access to finish.</li> <li>• External cache support by asserting the global signal (GBL) when predefined memory banks are accessed.</li> <li>• Programmable interrupt controller (PIC).</li> <li>• Local interrupt controller (LIC).</li> </ul>
<b>Multi-Core Shared Memories</b>	<ul style="list-style-type: none"> <li>• M2 memory (shared memory): <ul style="list-style-type: none"> <li>— A 476 KB memory working at the core frequency.</li> <li>— Accessible from the local bus.</li> <li>— Accessible from all four SC140 cores using the MQBus.</li> </ul> </li> <li>• 4 KB bootstrap ROM.</li> </ul>
<b>M2-Accessible Multi-Core Bus (MQBus)</b>	<ul style="list-style-type: none"> <li>• A QBus protocol multi-master bus connecting the four SC140 cores and the VCOP to the M2 memory.</li> <li>• Data bus access of up to 128-bit read and up to 64-bit write.</li> <li>• Operation at the SC140 core frequency.</li> <li>• A central efficient round-robin arbiter controlling SC140 core access on the MQBus.</li> <li>• Atomic operation control of access to M2 memory by the four SC140 cores and the local bus.</li> </ul>

**Table 2.** Phase-Lock Loop (PLL)

Feature	Description
<b>Internal PLL</b>	<ul style="list-style-type: none"> <li>• Generates up to 500 MHz core clock and up to 166 MHz bus clocks for the 60x-compatible local and system buses and other modules.</li> <li>• PLL values are determined at reset based on configuration signal values.</li> </ul>

**Table 3.** Buses and Memory Controller

Feature	Description
<b>60x-Compatible System Bus</b>	<ul style="list-style-type: none"> <li>• 64/32-bit data and 32-bit address 60x bus.</li> <li>• Support for multiple-master designs.</li> <li>• Four-beat burst transfers (eight-beat in 32-bit wide mode).</li> <li>• Port size of 64, 32, 16, and 8 controlled by the internal memory controller.</li> <li>• Bus can access external memory expansion or off-device peripherals, or it can enable an external host device to access internal resources.</li> <li>• Slave support, direct access by an external host to internal resources including the M1 and M2 memories.</li> <li>• On-device arbitration between up to four master devices.</li> </ul>
<b>Direct Slave Interface (DSI)</b>	<p>A 32/64-bit wide slave host interface that operates only as a slave device under the control of an external host processor.</p> <ul style="list-style-type: none"> <li>• 21–25 bit address, 32/64-bit data.</li> <li>• Direct access by an external host to internal and external resources, including the M1 and the M2 memories as well as external devices on the system bus.</li> <li>• Synchronous and asynchronous accesses, with burst capability in the synchronous mode.</li> <li>• Dual or Single strobe modes.</li> <li>• Write and read buffers improve host bandwidth.</li> <li>• Byte enable signals enables 1, 2, 4, and 8 byte write access granularity.</li> <li>• Sliding window mode enables access with reduced number of address pins.</li> <li>• Chip ID decoding enables using one <math>\overline{CS}</math> signal for multiple DSPs.</li> <li>• Broadcast <math>\overline{CS}</math> signal enables parallel write to multiple DSPs.</li> <li>• Big-endian, little-endian, and munged little-endian support.</li> </ul>
<b>3-Mode Signal Multiplexing</b>	<ul style="list-style-type: none"> <li>• 64-bit DSI, 32-bit system bus.</li> <li>• 32-bit DSI, 64-bit system bus.</li> <li>• 32-bit DSI, 32-bit system bus, and Ethernet.</li> </ul>
<b>Memory Controller</b>	<p>Flexible eight-bank memory controller:</p> <ul style="list-style-type: none"> <li>• Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine.</li> <li>• Glueless interface to SRAM, 133 MHz page mode SDRAM, DRAM, EPROM, Flash memory, and other user-definable peripherals.</li> <li>• Byte enables for either 64-bit or 32-bit bus width mode.</li> <li>• Eight external memory banks (banks 0–7). Two additional memory banks (banks 9, 11) control IPBus peripherals and internal memories. Each bank has the following features: <ul style="list-style-type: none"> <li>— 32-bit address decoding with programmable mask.</li> <li>— Variable block sizes (32 KB to 4 GB).</li> <li>— Selectable memory controller machine.</li> <li>— Two types of data errors check/correction: normal odd/even parity and read-modify-write (RMW) odd/even parity for single accesses.</li> <li>— Write-protection capability.</li> <li>— Control signal generation machine selection on a per-bank basis.</li> <li>— Support for internal or external masters on the system bus.</li> <li>— Data buffer controls activated on a per-bank basis.</li> <li>— Atomic operation.</li> <li>— RMW data parity check (on system bus only).</li> <li>— Extensive external memory-controller/bus-slave support.</li> <li>— Parity byte select pin, which enables a fast, glueless connection to RMW-parity devices (on the system bus only).</li> <li>— Data pipeline to reduce data set-up time for synchronous devices.</li> </ul> </li> </ul>

Table 4. DMA Controller

Feature	Description
<b>Multi-Channel DMA Controller</b>	<ul style="list-style-type: none"> <li>• 16 time-multiplexed unidirectional channels.</li> <li>• Services up to four external peripherals.</li> <li>• Supports <math>\overline{DONE}</math> or <math>\overline{DRACK}</math> protocol on two external peripherals.</li> <li>• Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates: <ul style="list-style-type: none"> <li>— A watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination.</li> <li>— A hungry request to indicate that the FIFO can accept more data.</li> </ul> </li> <li>• Priority-based time-multiplexing between channels using 16 internal priority levels.</li> <li>• Round-robin time-multiplexing between channels.</li> <li>• A flexible channel configuration: <ul style="list-style-type: none"> <li>— All channels support all features.</li> <li>— All channels connect to the system bus or local bus.</li> </ul> </li> <li>• Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO.</li> </ul>

Table 5. Serial Interfaces

Feature	Description
<b>Time-Division Multiplexing (TDM)</b>	<p>Up to four independent TDM modules, each with the following features:</p> <ul style="list-style-type: none"> <li>• Optional operating configurations: <ul style="list-style-type: none"> <li>— Totally independent receive and transmit channels, each having one data line, one clock line, and one frame sync line.</li> <li>— Four data lines with one clock and one frame sync shared among the transmit and receive lines.</li> </ul> </li> <li>• Glueless interface to E1/T1 framers and MVIP, SCAS, and H.110 buses.</li> <li>• Hardware A-law/<math>\mu</math>-law conversion.</li> <li>• Up to 66 Mbps per TDM (66 MHz bit clock if one data line is used, 33 MHz if two data lines are used, 16.7 MHz if four data lines are used).</li> <li>• Up to 256 channels.</li> <li>• Up to 16 MB per channel buffer (granularity 8 bytes), where A/<math>\mu</math> law buffer size is double (granularity 16 byte).</li> <li>• Receive buffers share one global write offset pointer that is written to the same offset relative to their start address.</li> <li>• Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address.</li> <li>• All channels share the same word size.</li> <li>• Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering.</li> <li>• Each channel can be programmed to be active or inactive.</li> <li>• 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively.</li> <li>• The TDM Transmitter Sync Signal (TxTSYN) can be configured as either input or output.</li> <li>• Frame Sync and Data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock.</li> <li>• Frame sync can be programmed as active low or active high.</li> <li>• Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame.</li> <li>• MSB or LSB first support.</li> </ul>

Table 5. Serial Interfaces (Continued)

Feature	Description
Ethernet Controller	<ul style="list-style-type: none"> <li>• Designed to comply with <b>IEEE</b> Std 802.3™, 802.3u™, 802.3x™, and 802.3ac™</li> <li>• Three Ethernet physical interfaces: <ul style="list-style-type: none"> <li>— 10/100 Mbps MII.</li> <li>— 10/100 Mbps RMII.</li> <li>— 10/100 Mbps SMII.</li> </ul> </li> <li>• Full and half-duplex support.</li> <li>• <b>IEEE</b> Std 802.3 full-duplex flow control (automatic PAUSE frame generation or software programmed PAUSE frame generation and recognition).</li> <li>• Support of out-of-sequence transmit queue (for initiating flow-control).</li> <li>• Programmable maximum frame length supports jumbo frames (up to 9.6k) and IEEE Std. 802.1 virtual local area network (VLAN) tags and priority.</li> <li>• Retransmission from transmit FIFO following a collision.</li> <li>• CRC generation and verification of inbound/outbound packets.</li> <li>• Address recognition: <ul style="list-style-type: none"> <li>— Each exact match can be programmed to be accepted or rejected.</li> <li>— Broadcast address (accept/reject).</li> <li>— Exact match 48-bit individual (unicast) address.</li> <li>— Hash (256-bit hash) check of individual (unicast) addresses.</li> <li>— Hash (256-bit hash) check of group (multicast) addresses.</li> <li>— Promiscuous mode.</li> </ul> </li> <li>• Pattern matching: <ul style="list-style-type: none"> <li>— Up to 16 unique 4-byte patterns.</li> <li>— Pattern match on bit-basis.</li> <li>— Matching range up to 256 bytes deep into the frame.</li> <li>— Offsets to a maximum of 252 bytes.</li> <li>— Programmable pattern size in 4-byte increments up to 64 bytes.</li> <li>— Accept or reject frames if a match is detected.</li> <li>— Up to eight unicast addresses for exact matches.</li> <li>— Pattern matching accepts/rejects IP addresses.</li> </ul> </li> <li>• Filing of receive frames based on pattern match; prioritization of frames.</li> <li>• Insertion with expansion or replacement for transmit frames; VLAN tag insertion.</li> <li>• RMON statistics.</li> <li>• Master DMA on the local bus for fetching descriptors and accessing the buffers.</li> <li>• Serial interface can be exposed either on GPIO pins or on the high ms bits of the DSI/system when the DSI and the system bus are both 32 bits.</li> <li>• MPC8260(PQ2) 8 byte width buffer descriptor mode as well as 32 byte width buffer descriptor mode.</li> <li>• MII Bridge (MIIGSK): <ul style="list-style-type: none"> <li>— Programmable selection of the 50 MHz RMII reference clock source (external or internal).</li> <li>— Independent 2 bit wide transmit and receive data paths.</li> <li>— Six operating modes.</li> <li>— Four general-purpose control signals.</li> <li>— Programmable transmitted inter-frame bits to support inter-frame gap for frames in the SMII domain.</li> </ul> </li> <li>• SMII features: <ul style="list-style-type: none"> <li>— Multiplexed with GPIO signals.</li> <li>— Convey complete MII information between the PHY and MAC.</li> <li>— Allow direct MAC-to-MAC communication in SMII mode.</li> <li>— Can generate an interrupt request line while receiving inter-frame segments.</li> </ul> </li> </ul>

**Table 5.** Serial Interfaces (Continued)

Feature	Description
<b>UART</b>	<ul style="list-style-type: none"> <li>• Two signals for transmit data and receive data.</li> <li>• No clock, asynchronous mode.</li> <li>• Can be serviced either by the SC140 DSP cores or an external host on the system bus or the DSI.</li> <li>• Full-duplex operation.</li> <li>• Standard mark/space non-return-to-zero (NRZ) format.</li> <li>• 13-bit baud rate selection.</li> <li>• Programmable 8-bit or 9-bit data format.</li> <li>• Separately enabled transmitter and receiver.</li> <li>• Programmable transmitter output polarity.</li> <li>• Two receiver wake-up methods: <ul style="list-style-type: none"> <li>— Idle line wake-up.</li> <li>— Address mark wake-up.</li> </ul> </li> <li>• Separate receiver and transmitter interrupt requests.</li> <li>• Eight flags, the first five can generate interrupt request: <ul style="list-style-type: none"> <li>— Transmitter empty.</li> <li>— Transmission complete.</li> <li>— Receiver full.</li> <li>— Idle receiver input.</li> <li>— Receiver overrun.</li> <li>— Noise error.</li> <li>— Framing error.</li> <li>— Parity error.</li> </ul> </li> <li>• Receiver framing error detection.</li> <li>• Hardware parity checking.</li> <li>• 1/16 bit-time noise detection.</li> <li>• Maximum bit rate 6.25 Mbps.</li> <li>• Single-wire and loop operations.</li> </ul>
<b>General-Purpose I/O (GPIO) Port</b>	<ul style="list-style-type: none"> <li>• 32 bidirectional signal lines that either serve the peripherals or act as programmable I/O ports.</li> <li>• Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode.</li> </ul>
<b>I<sup>2</sup>C Software Module</b>	<ul style="list-style-type: none"> <li>• Booting from a serial EEPROM.</li> <li>• Uses GPIO timing.</li> </ul>

**Table 6.** Miscellaneous Modules

Feature	Description
<b>Timers</b>	<p>Two modules of 16 timers each.</p> <ul style="list-style-type: none"> <li>• Cyclic or one-shot.</li> <li>• Input clock polarity control.</li> <li>• Interrupt request when counting reaches a programmed threshold.</li> <li>• Pulse or level interrupts.</li> <li>• Dynamically updated programmed threshold.</li> <li>• Read counter any time.</li> </ul> <p>Watchdog mode for the timers that connect to the device.</p>
<b>Hardware Semaphores</b>	<p>Eight coded hardware semaphores, locked by simple write access without need for read-modify-write mechanism.</p>
<b>Global Interrupt Controller (GIC)</b>	<ul style="list-style-type: none"> <li>• Consolidation of chip maskable interrupt and non-maskable interrupt sources and routing to <math>\overline{\text{INT\_OUT}}</math>, <math>\overline{\text{NMI\_OUT}}</math>, and to the cores.</li> <li>• Generation of 32 virtual interrupts (eight to each SC140 core) by a simple write access.</li> <li>• Generation of virtual <math>\overline{\text{NMI}}</math> (one to each SC140 core) by a simple write access.</li> </ul>

Table 7. Coprocessors

Feature	Description
VCOP	<ul style="list-style-type: none"> <li>• Fully programmable feed-forward channel decoding, feed-forward channel equalization and traceback sessions.</li> <li>• Up to 400 3GPP 12.2kbps AMR channels (channel decoding, number of channels linear to frequency).</li> <li>• Up to 200 blind transport format detect (BTFD) channels according to the 3GPP standard. Number of channels linear to frequency.</li> <li>• For channel decoding: <ul style="list-style-type: none"> <li>— Constraint length between <math>K = 5</math> and <math>K = 9</math>.</li> <li>— Puncture Codes.</li> <li>— Rate 1/2, 1/3, 1/4 and 1/6.</li> <li>— Four fully programmable polynomials (rate 1/6 is implemented by three polynomials only).</li> <li>— History buffer with up to 768 stages for 3G standards.</li> <li>— Input symbols are 8-bit (256 levels) signed soft symbols.</li> <li>— Output is hard decision (1-bit).</li> </ul> </li> <li>• For GSM channel equalization: <ul style="list-style-type: none"> <li>— Fully programmable 4 to 6 estimated channel autocorrelation coefficients (S-Parameters).</li> <li>— History buffer with up to 4090 stages for GSM.</li> <li>— Matched filter input is 8-bit (256 levels).</li> <li>— SOVA assist algorithm.</li> <li>— Output 8-bit coded delta values for SOVA assist algorithm, 1-bit hard decision traceback and history buffer or recursive traceback.</li> </ul> </li> <li>• Fully programmable block length for all sessions.</li> <li>• Programmable traceback methods of Max Path, Min Path or End State.</li> <li>• Programmable learning period length for the traceback session.</li> <li>• Supports the start of feed-forward according to a presaved PM memory content. However the history buffer is not saved. Therefore the traceback is according to the current block only.</li> <li>• Each SC140 core can program the VCOP parameters while the VCOP is in IDLE mode and then the VCOP can run independently on the whole block of data.</li> <li>• Dumping path metrics to the internal memory on up to 12 predefined stages as needed for BTFD applications.</li> <li>• Interrupt lines and status bits notify the cores on session completion.</li> <li>• Performance monitoring unit with 6 monitored behaviors.</li> </ul>
TCOP	<ul style="list-style-type: none"> <li>• Full support of 3GPP and CDMA2000 standards in Turbo decode.</li> <li>• Handles up to 20 turbo-coding 384 kbps channels.</li> <li>• 8 state PCCC with polynomial as supported by the 3G standards.</li> <li>• Iterative decoding structure based on maximum a-posteriori probability (MAP), with calculations performed in the LOG domain.</li> <li>• Encoding rate of 1/2, 1/3, 1/4, 1/5 with programmable puncturing for the parity symbols.</li> <li>• Full flexibility interleave function via a look-up table.</li> <li>• Flexible block size (1–32767 bits).</li> <li>• MAX log MAP and log MAP (MAX*) approximation.</li> <li>• Programmable MAX*, using linear approximation.</li> <li>• Programmable number of iterations, with resolution of half iteration (one MAP).</li> <li>• Fully automatic execution when the GO command executes.</li> <li>• High data rates (for multi-channel systems or multiple channel accumulating to high data rates).</li> <li>• Can stop processing after every MAP when soft lambda all reach a programmable quality threshold.</li> <li>• Minimum and maximum number of iterations to execute in conjunction with the stop criteria.</li> <li>• The SC140 core or host can stop the processing after every MAP during run time.</li> <li>• Automatic, internal normalization for <math>\alpha</math>, <math>\beta</math> overflow handling, with zero overhead.</li> <li>• Automatic, internal <math>\Lambda</math> clipping for <math>\Lambda</math> overflow handling, with zero overhead.</li> <li>• Additional least significant bit in <math>\alpha</math>, <math>\beta</math>, <math>\gamma</math> arithmetic guarding against precision loss during the gamma calculation due to the division by 2.</li> </ul>



**Table 8.** Power and Packaging

Feature	Description
<b>Reduced Power Dissipation</b>	<ul style="list-style-type: none"> <li>• Low power CMOS design.</li> <li>• Separate power supply for internal logic (1.2 V) and I/O (3.3 V).</li> <li>• Low-power standby modes.</li> <li>• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent).</li> </ul>
<b>Packaging</b>	<ul style="list-style-type: none"> <li>• 0.8 mm pitch Flip-Chip Plastic Ball-Grid Array (FC-PBGA).</li> <li>• 431-connection (ball).</li> <li>• Lead-free or lead-bearing spheres</li> <li>• 20 mm × 20 mm.</li> </ul>

**Table 9.** Software Support

Feature	Description
<b>Real-Time Operating System (RTOS)</b>	<p>The real-time operating system (RTOS) fully supports device architecture (multi-core, memory hierarchy, ICache, timers, DMA controller, interrupts, peripherals), as follows:</p> <ul style="list-style-type: none"> <li>• High-performance and deterministic, delivering predictive response time.</li> <li>• Optimized to provide low interrupt latency with high data throughput.</li> <li>• Preemptive and priority-based multitasking.</li> <li>• Fully interrupt/event driven.</li> <li>• Small memory footprint.</li> <li>• Comprehensive set of APIs.</li> </ul>
<b>Multi-Core Support</b>	<ul style="list-style-type: none"> <li>• One instance of kernel code in all four SC140 cores.</li> <li>• Dynamic and static memory allocation from local memory (M1) and shared memory (M2).</li> </ul>
<b>Distributed System Support</b>	<p>Transparent inter-task communications between tasks running inside the SC140 cores and the other tasks running in on-board devices or remote network devices:</p> <ul style="list-style-type: none"> <li>• Messaging mechanism between tasks using mailboxes and semaphores.</li> <li>• Networking support; data transfer between tasks running inside and outside the device using networking protocols.</li> <li>• Integrated device drivers for such peripherals as TDM, UART, and external buses.</li> </ul>
<b>Software Support</b>	<ul style="list-style-type: none"> <li>• Task debugging utilities integrated with compilers and vendors.</li> <li>• Board support package (BSP) for the application development system (ADS).</li> <li>• Integrated development environment (IDE): <ul style="list-style-type: none"> <li>— C/C++ compiler with in-line assembly so developers can generate highly optimized DSP code. Translates C/C++ code into parallel fetch sets and maintains high code density.</li> <li>— Librarian. User can create libraries for modularity.</li> <li>— A collection of C/C++ functions for developer use.</li> <li>— Highly efficient linker to produce executables from object code.</li> <li>— Seamlessly integrated real-time, non-intrusive multi-mode debugger for debugging highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode.</li> <li>— Device simulation models enable design and simulation before hardware availability.</li> <li>— Profiler using a patented binary code instrumentation (BCI) technique helps developers identify program design inefficiencies.</li> <li>— Version control. CodeWarrior® includes plug-ins for ClearCase, Visual SourceSafe, and CVS.</li> </ul> </li> </ul>
<b>Boot Options</b>	<ul style="list-style-type: none"> <li>• External memory.</li> <li>• External host.</li> <li>• UART.</li> <li>• TDM.</li> <li>• I<sup>2</sup>C</li> </ul>

**Table 10.** Application Development System (ADS) Board

Feature	Description
<b>MSC8126ADS</b>	<ul style="list-style-type: none"> <li>• Host debug through single JTAG connector supports both processors.</li> <li>• MSC8103 as the MSC8126 host with both devices on the board. The MSC8103 system bus connects to the MSC8126 DSI.</li> <li>• Flash memory for stand-alone applications.</li> <li>• Communications ports: <ul style="list-style-type: none"> <li>— 10/100Base-T.</li> <li>— 155 Mbit ATM over Optical.</li> <li>— T1/E1 TDM interface.</li> <li>— H.110.</li> <li>— Voice codec.</li> <li>— RS-232.</li> <li>— High-density (MICTOR) logic analyzer connectors to monitor MSC8126 signals</li> <li>— 6U cPCI form factor.</li> </ul> </li> <li>• Emulates MSC8126 DSP farm by connecting to three other ADS boards.</li> </ul>

## Product Documentation

The documents listed in **Table 11** are required for a complete description of the MSC8126 and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale Semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back of this document.

**Table 11.** MSC8126 Documentation

Name	Description	Order Number
<i>MSC8126 Technical Data</i>	MSC8126 features list and physical, electrical, timing, and package specifications.	MSC8126
<i>MSC8126 User's Guide</i>	User information includes system functionality, getting started, and programming topics.	MSC8126UG
<i>MSC8126 Reference Manual</i>	Detailed functional description of the MSC8126 memory and peripheral configuration, operation, and register programming.	MSC8126RM
<i>SC140 DSP Core Reference Manual</i>	Detailed description of the SC140 family processor core and instruction set.	MNSC140CORE
Application Notes	Documents describing specific applications or optimized device operation including code examples.	See the website product page.



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