

Technical Data

DSP56303/D
Rev. 7, 1/2002

24-Bit Digital Signal
Processor



digital dna™

The DSP56303 is intended for use in telecommunication applications, such as multi-line voice/data/fax processing, video conferencing, audio applications, control, and general digital signal processing.

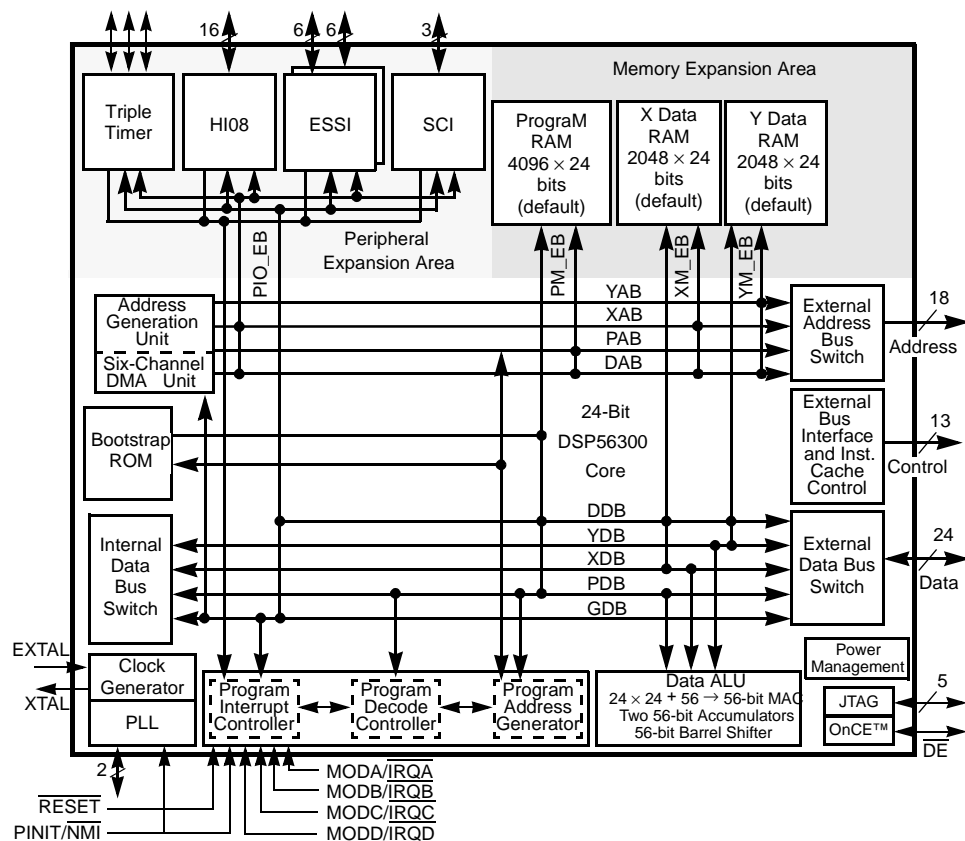


Figure 1. DSP56303 Block Diagram

The DSP56303 is a member of the DSP56300 core family of programmable CMOS Digital Signal Processors (DSPs). This family uses a high-performance, single clock cycle per instruction engine providing a twofold performance increase over Motorola's popular DSP56000 core family while retaining code compatibility.

Significant architectural features of the DSP56300 core family include a barrel shifter, 24-bit addressing, instruction cache, and DMA. The DSP56303 offers 100 MIPS using an internal 100 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a rich instruction set and low power dissipation, as well as increasing levels of speed and power to enable wireless, telecommunications, and multimedia products.

Table of Contents

| | | |
|-------------------|---|------|
| | DSP56303 Features..... | iii |
| | Target Applications..... | iv |
| | Product Documentation..... | iv |
| Chapter 1 | Signal/ Connection Descriptions | |
| | 1.1 Signal Groupings..... | 1-1 |
| | 1.2 Power..... | 1-3 |
| | 1.3 Ground..... | 1-3 |
| | 1.4 Clock..... | 1-4 |
| | 1.5 PLL..... | 1-4 |
| | 1.6 External Memory Expansion Port (Port A)..... | 1-5 |
| | 1.7 Interrupt and Mode Control..... | 1-8 |
| | 1.8 Host Interface (HI08)..... | 1-9 |
| | 1.9 Enhanced Synchronous Serial Interface 0 (ESSI0)..... | 1-13 |
| | 1.10 Enhanced Synchronous Serial Interface 1 (ESSI1)..... | 1-14 |
| | 1.11 Serial Communication Interface (SCI)..... | 1-16 |
| | 1.12 Timers..... | 1-17 |
| | 1.13 JTAG and OnCE Interface..... | 1-18 |
| Chapter 2 | Specifications | |
| | 2.1 Introduction..... | 2-1 |
| | 2.2 Maximum Ratings..... | 2-1 |
| | 2.4 Thermal Characteristics..... | 2-2 |
| | 2.5 DC Electrical Characteristics..... | 2-3 |
| | 2.6 AC Electrical Characteristics..... | 2-4 |
| Chapter 3 | Packaging | |
| | 3.1 Pin-Out and Package Information..... | 3-1 |
| | 3.2 TQFP Package Description..... | 3-2 |
| | 3.3 TQFP Package Mechanical Drawing..... | 3-9 |
| | 3.4 MAP-BGA Package Description..... | 3-10 |
| | 3.5 MAP-BGA Package Mechanical Drawing..... | 3-19 |
| Chapter 4 | Design Considerations | |
| | 4.1 Thermal Design Considerations..... | 4-1 |
| | 4.2 Electrical Design Considerations..... | 4-2 |
| | 4.3 Power Consumption Considerations..... | 4-4 |
| | 4.4 PLL Performance Issues..... | 4-5 |
| | 4.5 Input (EXTAL) Jitter Requirements..... | 4-5 |
| Appendix A | Power Consumption Benchmark | |
| Index | | |

Data Sheet Conventions

$\overline{\text{OVERBAR}}$ Used to indicate a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
 "asserted" Means that a high true (active high) signal is high or that a low true (active low) signal is low
 "deasserted" Means that a high true (active high) signal is low or that a low true (active low) signal is high

| Examples: | Signal/Symbol | Logic State | Signal State | Voltage |
|-----------|-------------------------|-------------|--------------|-------------------------------|
| | $\overline{\text{PIN}}$ | True | Asserted | $V_{\text{IL}}/V_{\text{OL}}$ |
| | $\overline{\text{PIN}}$ | False | Deasserted | $V_{\text{IH}}/V_{\text{OH}}$ |
| | PIN | True | Asserted | $V_{\text{IH}}/V_{\text{OH}}$ |
| | PIN | False | Deasserted | $V_{\text{IL}}/V_{\text{OL}}$ |

Note: Values for V_{IL} , V_{OL} , V_{IH} , and V_{OH} are defined by individual product specifications.

DSP56303 Features

High-Performance DSP56300 Core

- 100 million instructions per second (MIPS) with a 100 MHz clock at 3.3 V nominal
- Object code compatible with the DSP56000 core with highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24×24 -bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), on-chip instruction cache controller, on-chip memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts
- Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
- Phase Lock Loop (PLL) allows change of low-power Divide Factor (DF) without loss of lock and output clock with skew elimination
- Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)

On-Chip Peripherals

- Enhanced DSP56000-like 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs
- Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
- Serial communications interface (SCI) with baud rate generator
- Triple timer module
- Up to thirty-four programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

On-Chip Memories

- 192×24 -bit bootstrap ROM
- 128 K RAM total
- Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable:

| Program RAM Size | Instruction Cache Size | X Data RAM Size | Y Data RAM Size | Instruction Cache | Switch Mode |
|-----------------------|------------------------|-----------------------|-----------------------|-------------------|-------------|
| 4096×24 -bit | 0 | 2048×24 -bit | 2048×24 -bit | disabled | disabled |
| 3072×24 -bit | 1024×24 -bit | 2048×24 -bit | 2048×24 -bit | enabled | disabled |
| 2048×24 -bit | 0 | 3072×24 -bit | 3072×24 -bit | disabled | enabled |
| 1024×24 -bit | 1024×24 -bit | 3072×24 -bit | 3072×24 -bit | enabled | enabled |

Off-Chip Memory Expansion

- Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines
- Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines
- External memory expansion port
- Chip Select Logic for glueless interface to static random access memory (SRAMs)
- On-chip DRAM Controller for glueless interface to dynamic random access memory (DRAMs)

Reduced Power Dissipation

- Very low-power CMOS design
- Wait and Stop low-power standby modes
- Fully static design specified to operate down to 0 Hz (dc)
- Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

Packaging

The DSP56303 is available in a 144-pin TQFP package or a 196-pin MAP-BGA package.

Target Applications

- Multi-line voice/data/fax processing
- Video conferencing
- Audio applications
- Control

Product Documentation

The three documents listed in the following table are required for a complete description of the DSP56303 and are necessary to design properly with the part. Documentation is available from the following sources. (See the back cover for details.)

- A local Motorola distributor
- A Motorola semiconductor sales office
- A Motorola Literature Distribution Center
- The World Wide Web (WWW)

Table 1. DSP56303 Documentation

| Name | Description | Order Number |
|--------------------------------|---|---------------|
| <i>DSP56300 Family Manual</i> | Detailed description of the DSP56300 family processor core and instruction set | DSP56300FM/AD |
| <i>DSP56303 User's Manual</i> | Detailed functional description of the DSP56303 memory configuration, operation, and register programming | DSP56303UM/D |
| <i>DSP56303 Technical Data</i> | DSP56303 features list and physical, electrical, timing, and package specifications | DSP56303/D |

1.1 Signal Groupings

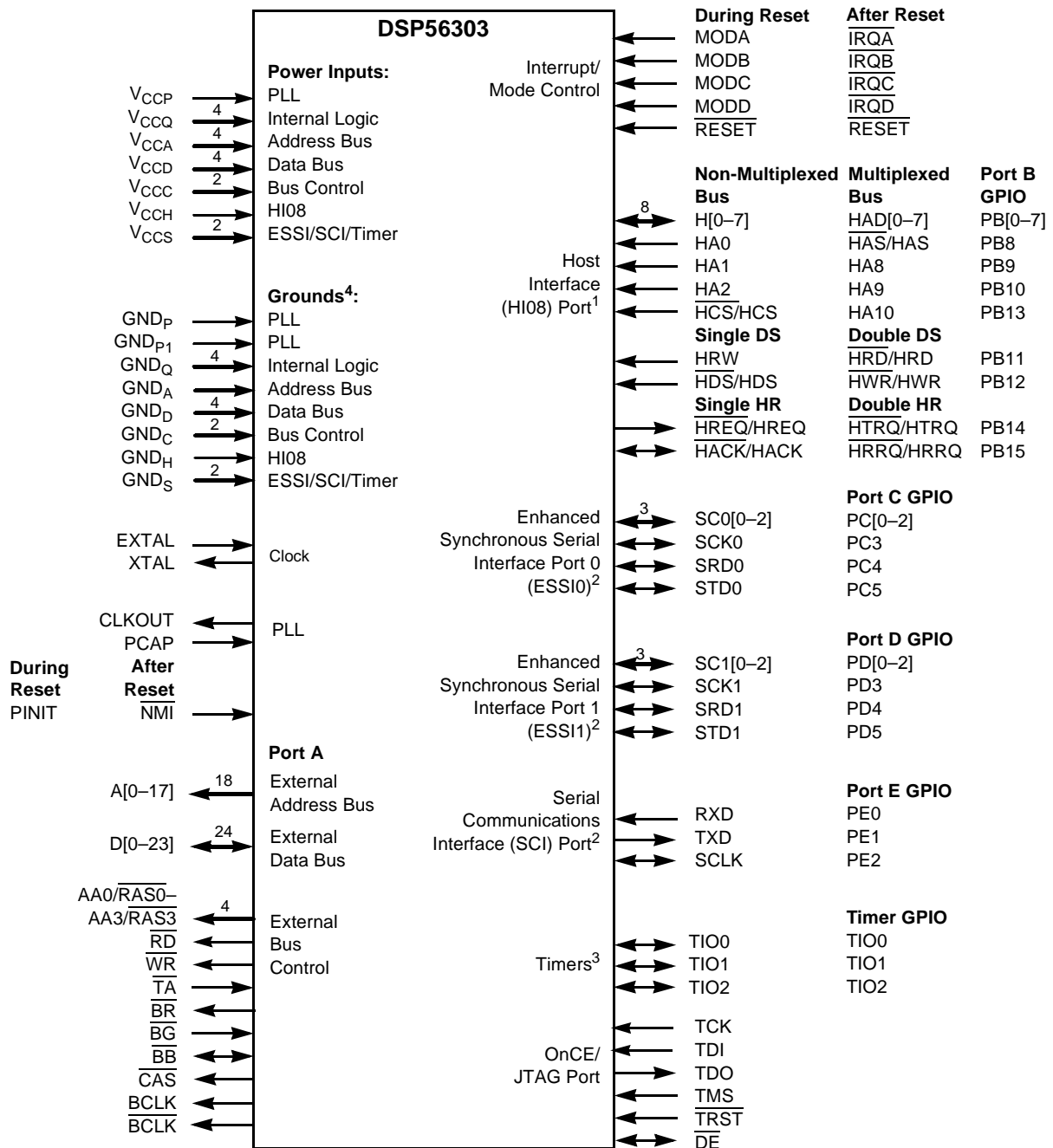
The DSP56303 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56303 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56303 Functional Signal Groupings

| Functional Group | | Number of Signals | |
|--|----------------------------|-------------------|---------|
| | | TQFP | MAP-BGA |
| Power (V_{CC}) | | 18 | 18 |
| Ground (GND) | | 19 | 66 |
| Clock | | 2 | 2 |
| PLL | | 3 | 3 |
| Address bus | Port A ¹ | 18 | 18 |
| Data bus | | 24 | 24 |
| Bus control | | 13 | 13 |
| Interrupt and mode control | | 5 | 5 |
| Host interface (HI08) | Port B ² | 16 | 16 |
| Enhanced synchronous serial interface (ESSI) | Ports C and D ³ | 12 | 12 |
| Serial communication interface (SCI) | Port E ⁴ | 3 | 3 |
| Timer | | 3 | 3 |
| OnCE/JTAG Port | | 6 | 6 |
| <p>Notes:</p> <ol style="list-style-type: none"> 1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals. 2. Port B signals are the HI08 port signals multiplexed with the GPIO signals. 3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals. 4. Port E signals are the SCI port signals multiplexed with the GPIO signals. 5. There are 2 signal connections in the TQFP package and 7 signal connections in the MAP-BGA package that are not used. These are designated as no connect (NC) in the package description (see Chapter 3). | | | |

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. Refer to the *DSP56303 User's Manual* for details on these configuration registers.

Signal Groupings



- Notes:**
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double Data Strobe (DS), and single or double Host Request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternatively as GPIO signals (PB[0-15]). Signals with dual designations (for example, HAS/HAS) have configurable polarity.
 2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0-5]), Port D GPIO signals (PD[0-5]), and Port E GPIO signals (PE[0-2]), respectively.
 3. TIO[0-2] can be configured as GPIO signals.
 4. Ground connections shown in this figure are for the TQFP package. In the MAP-BGA package, in addition to the GND_P and GND_{P1} connections, there are 64 GND connections to a common internal package ground plane.

Figure 1-1. Signals Identified by Functional Group

1.2 Power

Table 1-2. Power Inputs

| Power Name | Description |
|---|---|
| V_{CCP} | PLL Power — V_{CC} dedicated for PLL use. The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V_{CC} power rail. |
| V_{CCQ} | Quiet Power —An isolated power for the core processing logic. This input must be isolated externally from all other chip power inputs. |
| V_{CCA} | Address Bus Power —An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, <i>except</i> V_{CCQ} . |
| V_{CCD} | Data Bus Power —An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, <i>except</i> V_{CCQ} . |
| V_{CC} | Bus Control Power —An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs, <i>except</i> V_{CCQ} . |
| V_{CCH} | Host Power —An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs, <i>except</i> V_{CCQ} . |
| V_{CCS} | ESSI, SCI, and Timer Power —An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, <i>except</i> V_{CCQ} . |
| Note: The user must provide adequate external decoupling capacitors for all power connections. | |

1.3 Ground

Table 1-3. Grounds¹

| Ground Name | Description |
|---------------|--|
| GND_P | PLL Ground —Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. V_{CCP} should be bypassed to GND_P by a 0.47 μ F capacitor located as close as possible to the chip package. |
| GND_{P1} | PLL Ground 1 —Ground-dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. |
| GND_Q^2 | Quiet Ground —An isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections, <i>except</i> GND_P and GND_{P1} . The user must provide adequate external decoupling capacitors. |
| GND_A^2 | Address Bus Ground —An isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections, <i>except</i> GND_P and GND_{P1} . The user must provide adequate external decoupling capacitors. |
| GND_D^2 | Data Bus Ground —An isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections, <i>except</i> GND_P and GND_{P1} . The user must provide adequate external decoupling capacitors. |
| GND_C^2 | Bus Control Ground —An isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections, <i>except</i> GND_P and GND_{P1} . The user must provide adequate external decoupling capacitors. |
| GND_H^2 | Host Ground —An isolated ground for the HI08 I/O drivers. This connection must be tied externally to all other chip ground connections, <i>except</i> GND_P and GND_{P1} . The user must provide adequate external decoupling capacitors. |
| GND_S^2 | ESSI, SCI, and Timer Ground —An isolated ground for the ESSI, SCI, and timer I/O drivers. This connection must be tied externally to all other chip ground connections, <i>except</i> GND_P and GND_{P1} . The user must provide adequate external decoupling capacitors. |
| GND^3 | Ground —Connected to an internal device ground plane. |
| Notes: | <ol style="list-style-type: none"> 1. The user must provide adequate external decoupling capacitors for all GND connections. 2. These connections are only used on the TQFP package. 3. These connections are common grounds used on the MAP-BGA package. |

1.4 Clock

Table 1-4. Clock Signals

| Signal Name | Type | State During Reset | Signal Description |
|-------------|--------|--------------------|--|
| EXTAL | Input | Input | External Clock/Crystal Input —Interfaces the internal crystal oscillator input to an external crystal or an external clock. |
| XTAL | Output | Chip-driven | Crystal Output —Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected. |

1.5 PLL

Table 1-5. Phase-Locked Loop Signals

| Signal Name | Type | State During Reset | Signal Description |
|-------------------------|--------|--------------------|--|
| CLKOUT | Output | Chip-driven | <p>Clock Output—Provides an output clock synchronized to the internal core clock phase.</p> <p>If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL.</p> <p>If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.</p> |
| PCAP | Input | Input | <p>PLL Capacitor—An input connecting an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to V_{CCP}.</p> <p>If the PLL is not used, PCAP can be tied to V_{CC}, GND, or left floating.</p> |
| PINIT | Input | Input | <p>PLL Initial—During assertion of $\overline{\text{RESET}}$, the value of PINIT is written into the PLL enable (PEN) bit of the PLL control (PCTL) register, determining whether the PLL is enabled or disabled.</p> |
| $\overline{\text{NMI}}$ | Input | | <p>Nonmaskable Interrupt—After $\overline{\text{RESET}}$ deassertion and during normal instruction processing, this Schmitt-trigger input is the negative-edge-triggered NMI request internally synchronized to CLKOUT.</p> <p>Note: PINIT/$\overline{\text{NMI}}$ can tolerate 5 V.</p> |

1.6 External Memory Expansion Port (Port A)

Note: When the DSP56303 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant Port A signals: A[0–17], D[0–23], AA0/RAS0–AA3/RAS3, RD, WR, BB, CAS.

1.6.1 External Address Bus

Table 1-6. External Address Bus Signals

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|-------------|--------|-----------------------------------|---|
| A[0–17] | Output | Tri-stated | Address Bus —When the DSP is the bus master, A[0–17] are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–17] do not change state when external memory spaces are not being accessed. |

1.6.2 External Data Bus

Table 1-7. External Data Bus Signals

| Signal Name | Type | State During Reset | State During Stop or Wait | Signal Description |
|-------------|---------------|--------------------|---|---|
| D[0–23] | Input/ Output | Ignored Input | Last state: <i>Input:</i> Ignored <i>Output:</i> Tri-stated | Data Bus —When the DSP is the bus master, D[0–23] are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] are tri-stated. |

1.6.3 External Bus Control

Table 1-8. External Bus Control Signals

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|------------------------------|--------|---|---|
| AA[0–3] | Output | Tri-stated | Address Attribute —When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the Operating Mode Register, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals. |
| $\overline{\text{RAS}}[0–3]$ | Output | | Row Address Strobe —When defined as $\overline{\text{RAS}}$, these signals can be used as RAS for DRAM interface. These signals are tri-statable outputs with programmable polarity. |
| $\overline{\text{RD}}$ | Output | Tri-stated | Read Enable —When the DSP is the bus master, $\overline{\text{RD}}$ is an active-low output that is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{\text{RD}}$ is tri-stated. |
| $\overline{\text{WR}}$ | Output | Tri-stated | Write Enable —When the DSP is the bus master, $\overline{\text{WR}}$ is an active-low output that is asserted to write external memory on the data bus (D[0–23]). Otherwise, the signals are tri-stated. |
| $\overline{\text{TA}}$ | Input | Ignored Input | Transfer Acknowledge —If the DSP56303 is the bus master and there is no external bus activity, or the DSP56303 is not the bus master, the $\overline{\text{TA}}$ input is ignored. The $\overline{\text{TA}}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2, . . . infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{\text{TA}}$ deasserted. In typical operation, $\overline{\text{TA}}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{\text{TA}}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{\text{TA}}$ input or by the BCR, whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. To use the $\overline{\text{TA}}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{\text{TA}}$ deassertion; otherwise, improper operation may result. $\overline{\text{TA}}$ can operate synchronously or asynchronously depending on the setting of the TAS bit in the Operating Mode Register. $\overline{\text{TA}}$ functionality cannot be used during DRAM type accesses; otherwise improper operation may result. |
| $\overline{\text{BR}}$ | Output | Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted) | Bus Request —Asserted when the DSP requests bus mastership. $\overline{\text{BR}}$ is deasserted when the DSP no longer needs the bus. $\overline{\text{BR}}$ may be asserted or deasserted independently of whether the DSP56303 is a bus master or a bus slave. Bus “parking” allows $\overline{\text{BR}}$ to be deasserted even though the DSP56303 is the bus master. (See the description of bus “parking” in the $\overline{\text{BB}}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{\text{BR}}$ to be asserted under software control even though the DSP does not need the bus. $\overline{\text{BR}}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{\text{BR}}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{\text{BR}}$ is deasserted and the arbitration is reset to the bus slave state. |

Table 1-8. External Bus Control Signals (Continued)

| Signal Name | Type | State During Reset, Stop, or Wait | Signal Description |
|-------------------|--------------|-----------------------------------|--|
| \overline{BG} | Input | Ignored Input | <p>Bus Grant—Asserted by an external bus arbitration circuit when the DSP56303 becomes the next bus master. When \overline{BG} is asserted, the DSP56303 must wait until \overline{BB} is deasserted before taking bus mastership. When \overline{BG} is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution.</p> <p>The default operation of this bit requires a setup and hold time as specified in Table 2-14. An alternate mode can be invoked: set the asynchronous bus arbitration enable (ABE) bit (Bit 13) in the Operating Mode Register. When this bit is set, \overline{BG} and \overline{BB} are synchronized internally. This eliminates the respective setup and hold time requirements but adds a required delay between the deassertion of an initial \overline{BG} input and the assertion of a subsequent \overline{BG} input.</p> |
| \overline{BB} | Input/Output | Ignored Input | <p>Bus Busy—Indicates that the bus is active. Only after \overline{BB} is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep \overline{BB} asserted after ceasing bus activity regardless of whether \overline{BR} is asserted or deasserted. Called “bus parking,” this allows the current bus master to reuse the bus without re arbitration until another device requires the bus. \overline{BB} is deasserted by an “active pull-up” method (that is, \overline{BB} is driven high and then released and held high by an external pull-up resistor).</p> <p>The default operation of this signal requires a setup and hold time as specified in Table 2-14. An alternative mode can be invoked by setting the ABE bit (Bit 13) in the Operating Mode Register. When this bit is set, \overline{BG} and \overline{BB} are synchronized internally. See \overline{BG} for additional information.</p> <p>Note: \overline{BB} requires an external pull-up resistor.</p> |
| \overline{CAS} | Output | Tri-stated | <p>Column Address Strobe—When the DSP is the bus master, \overline{CAS} is an active-low output used by DRAM to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM control register is cleared, the signal is tri-stated.</p> |
| BCLK | Output | Tri-stated | <p>Bus Clock When the DSP is the bus master, BCLK is active when the Operating Mode Register Address Trace Enable bit is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle.</p> |
| \overline{BCLK} | Output | Tri-stated | <p>Bus Clock Not When the DSP is the bus master, \overline{BCLK} is the inverse of the BCLK signal. Otherwise, the signal is tri-stated.</p> |

1.7 Interrupt and Mode Control

The interrupt and mode control signals select the chip operating mode as it comes out of hardware reset. After $\overline{\text{RESET}}$ is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

| Signal Name | Type | State During Reset | Signal Description |
|--|-------|-----------------------|--|
| $\overline{\text{RESET}}$ | Input | Schmitt-trigger Input | Reset —Places the chip in the Reset state and resets the internal phase generator. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted after powerup. |
| MODA | Input | Schmitt-trigger Input | Mode Select A —MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. External Interrupt Request A —After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the STOP or WAIT standby state and $\overline{\text{IRQA}}$ is asserted, the processor exits the STOP or WAIT state. |
| $\overline{\text{IRQA}}$ | Input | | |
| MODB | Input | Schmitt-trigger Input | Mode Select B —MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. External Interrupt Request B —After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQB}}$ is asserted, the processor exits the WAIT state. |
| $\overline{\text{IRQB}}$ | Input | | |
| MODC | Input | Schmitt-trigger Input | Mode Select C —MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. External Interrupt Request C —After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQC}}$ is asserted, the processor exits the WAIT state. |
| $\overline{\text{IRQC}}$ | Input | | |
| MODD | Input | Schmitt-trigger Input | Mode Select D —MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the $\overline{\text{RESET}}$ signal is deasserted. External Interrupt Request D —After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and $\overline{\text{IRQD}}$ is asserted, the processor exits the WAIT state. |
| $\overline{\text{IRQD}}$ | Input | | |
| Note: These signals are all 5 V tolerant. | | | |

1.8 Host Interface (HI08)

The HI08 provides a fast, 8-bit, parallel data port that connects directly to the host bus. The HI08 supports a variety of standard buses and connects directly to a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.8.4 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

| Action | Description |
|---|--|
| Asynchronous read of receive byte registers | When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid. |
| Asynchronous write to transmit byte registers | The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register. |
| Asynchronous write to host vector | The host interface programmer must change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector. |

1.8.5 Host Port Configuration

HI08 signal functions vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register.

Table 1-11. Host Interface

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|-------------|-----------------|-----------------------------------|---|
| H[0–7] | Input/Output | Ignored Input | Host Data —When the HI08 is programmed to interface with a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus. |
| HAD[0–7] | Input/Output | | Host Address —When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional multiplexed Address/Data bus. |
| PB[0–7] | Input or Output | | Port B 0–7 —When the HI08 is configured as GPIO through the HI08 Port Control Register, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register. |

Table 1-11. Host Interface (Continued)

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|------------------------------|-----------------|-----------------------------------|---|
| HA0 | Input | Ignored Input | <p>Host Address Input 0—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 0 of the host address input bus.</p> <p>Host Address Strobe—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is the host address strobe (HAS) Schmitt-trigger input. The polarity of the address strobe is programmable but is configured active-low (HAS) following reset.</p> <p>Port B 8—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.</p> |
| $\overline{\text{HAS}}$ /HAS | Input | | |
| PB8 | Input or Output | | |
| HA1 | Input | Ignored Input | <p>Host Address Input 1—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 1 of the host address (HA1) input bus.</p> <p>Host Address 8—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 8 of the host address (HA8) input bus.</p> <p>Port B 9—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.</p> |
| HA8 | Input | | |
| PB9 | Input or Output | | |
| HA2 | Input | Ignored Input | <p>Host Address Input 2—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is line 2 of the host address (HA2) input bus.</p> <p>Host Address 9—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 9 of the host address (HA9) input bus.</p> <p>Port B 10—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.</p> |
| HA9 | Input | | |
| PB10 | Input or Output | | |
| $\overline{\text{HCS}}$ /HCS | Input | Ignored Input | <p>Host Chip Select—When the HI08 is programmed to interface with a nonmultiplexed host bus and the HI function is selected, this signal is the host chip select (HCS) input. The polarity of the chip select is programmable but is configured active-low (HCS) after reset.</p> <p>Host Address 10—When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, this signal is line 10 of the host address (HA10) input bus.</p> <p>Port B 13—When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register.</p> |
| HA10 | Input | | |
| PB13 | Input or Output | | |

Table 1-11. Host Interface (Continued)

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|--------------------------------|-----------------|-----------------------------------|---|
| HRW | Input | Ignored Input | Host Read/Write —When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the Host Read/Write (HRW) input. |
| $\overline{\text{HRD}}$ /HRD | Input | | Host Read Data —When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the HRD strobe Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low (HRD) after reset. |
| PB11 | Input or Output | | Port B 11 —When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register. |
| $\overline{\text{HDS}}$ /HDS | Input | Ignored Input | Host Data Strobe —When the HI08 is programmed to interface with a single-data-strobe host bus and the HI function is selected, this signal is the host data strobe (HDS) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HDS}}$) following reset. |
| $\overline{\text{HWR}}$ /HWR | Input | | Host Write Data —When the HI08 is programmed to interface with a double-data-strobe host bus and the HI function is selected, this signal is the host write data strobe (HWR) Schmitt-trigger input. The polarity of the data strobe is programmable but is configured as active-low ($\overline{\text{HWR}}$) following reset. |
| PB12 | Input or Output | | Port B 12 —When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register. |
| $\overline{\text{HREQ}}$ /HREQ | Output | Ignored Input | Host Request —When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host request (HREQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HREQ}}$) following reset. The host request may be programmed as a driven or open-drain output. |
| $\overline{\text{HTRQ}}$ /HTRQ | Output | | Transmit Host Request —When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the transmit host request (HTRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HTRQ}}$) following reset. The host request may be programmed as a driven or open-drain output. |
| PB14 | Input or Output | | Port B 14 —When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register. |

Table 1-11. Host Interface (Continued)

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|---|-----------------|-----------------------------------|---|
| $\overline{\text{HACK}}/\text{HACK}$ | Input | Ignored Input | Host Acknowledge —When the HI08 is programmed to interface with a single host request host bus and the HI function is selected, this signal is the host acknowledge (HACK) Schmitt-trigger input. The polarity of the host acknowledge is programmable but is configured as active-low ($\overline{\text{HACK}}$) after reset. |
| $\overline{\text{HRRQ}}/\text{HRRQ}$ | Output | | Receive Host Request —When the HI08 is programmed to interface with a double host request host bus and the HI function is selected, this signal is the receive host request (HRRQ) output. The polarity of the host request is programmable but is configured as active-low ($\overline{\text{HRRQ}}$) after reset. The host request may be programmed as a driven or open-drain output. |
| PB15 | Input or Output | | Port B 15 —When the HI08 is configured as GPIO through the HI08 Port Control Register, this signal is individually programmed as an input or output through the HI08 Data Direction Register. |
| <p>Notes:</p> <ol style="list-style-type: none"> In the Stop state, the signal maintains the last state as follows: <ul style="list-style-type: none"> If the last state is input, the signal is an ignored input. If the last state is output, the signal is tri-stated. The Wait processing state does not affect the signal state. All inputs are 5 V tolerant. | | | |

1.9 Enhanced Synchronous Serial Interface 0 (ESSIO)

Two synchronous serial interfaces (ESSIO and ESSIO1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Motorola serial peripheral interface (SPI).

Table 1-12. Enhanced Synchronous Serial Interface 0

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|-------------|-----------------|-----------------------------------|--|
| SC00 | Input or Output | Ignored Input | Serial Control 0 —For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0. |
| PC0 | Input or Output | | Port C 0 —The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register. |
| SC01 | Input/Output | Ignored Input | Serial Control 1 —For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1. |
| PC1 | Input or Output | | Port C 1 —The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register. |
| SC02 | Input/Output | Ignored Input | Serial Control Signal 2 —The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation). |
| PC2 | Input or Output | | Port C 2 —The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register. |
| SCK0 | Input/Output | Ignored Input | Serial Clock —Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. |
| PC3 | Input or Output | | Port C 3 —The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register. |

Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-12. Enhanced Synchronous Serial Interface 0 (Continued)

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|--|-----------------|-----------------------------------|--|
| SRD0 | Input | Ignored Input | Serial Receive Data —Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received. |
| PC4 | Input or Output | | Port C 4 —The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register. |
| STD0 | Output | Ignored Input | Serial Transmit Data —Transmits data from the Serial Transmit Shift Register. STD0 is an output when data is transmitted. |
| PC5 | Input or Output | | Port C 5 —The default configuration following reset is GPIO input PC5. When configured as PC5, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal STD0 through the Port C Control Register. |
| Notes: <ol style="list-style-type: none"> In the Stop state, the signal maintains the last state as follows: <ul style="list-style-type: none"> If the last state is input, the signal is an ignored input. If the last state is output, the signal is tri-stated. The Wait processing state does not affect the signal state. All inputs are 5 V tolerant. | | | |

1.10 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Serial Synchronous Interface 1

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|-------------|-----------------|-----------------------------------|--|
| SC10 | Input or Output | Ignored Input | Serial Control 0 —For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0. |
| PD0 | Input or Output | | Port D 0 —The default configuration following reset is GPIO input PD0. When configured as PD0, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC10 through the Port D Control Register. |
| SC11 | Input/Output | Ignored Input | Serial Control 1 —For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for Transmitter 2 output or for Serial I/O Flag 1. |
| PD1 | Input or Output | | Port D 1 —The default configuration following reset is GPIO input PD1. When configured as PD1, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC11 through the Port D Control Register. |

Table 1-13. Enhanced Serial Synchronous Interface 1 (Continued)

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|--|-----------------|-----------------------------------|---|
| SC12 | Input/Output | Ignored Input | Serial Control Signal 2 —The frame sync for both the transmitter and receiver in synchronous mode and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation). |
| PD2 | Input or Output | | Port D 2 —The default configuration following reset is GPIO input PD2. When configured as PD2, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SC12 through the Port D Control Register. |
| SCK1 | Input/Output | Ignored Input | Serial Clock —Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock. |
| PD3 | Input or Output | | Port D 3 —The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register. |
| SRD1 | Input | Ignored Input | Serial Receive Data —Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received. |
| PD4 | Input or Output | | Port D 4 —The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register. |
| STD1 | Output | Ignored Input | Serial Transmit Data —Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted. |
| PD5 | Input or Output | | Port D 5 —The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register. |
| Notes: <ol style="list-style-type: none"> In the Stop state, the signal maintains the last state as follows: <ul style="list-style-type: none"> If the last state is input, the signal is an ignored input. If the last state is output, the signal is tri-stated. The Wait processing state does not affect the signal state. All inputs are 5 V tolerant. | | | |

1.11 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|---|-----------------|-----------------------------------|---|
| RXD | Input | Ignored Input | Serial Receive Data —Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register. |
| PE0 | Input or Output | | Port E 0 —The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register. |
| TXD | Output | Ignored Input | Serial Transmit Data —Transmits data from the SCI Transmit Data Register. |
| PE1 | Input or Output | | Port E 1 —The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register. |
| SCLK | Input/Output | Ignored Input | Serial Clock —Provides the input or output clock used by the transmitter and/or the receiver. |
| PE2 | Input or Output | | Port E 2 —The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register. |
| <p>Notes:</p> <ol style="list-style-type: none"> In the Stop state, the signal maintains the last state as follows: <ul style="list-style-type: none"> If the last state is input, the signal is an ignored input. If the last state is output, the signal is tri-stated. The Wait processing state does not affect the signal state. All inputs are 5 V tolerant. | | | |

1.12 Timers

The DSP56303 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56303 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-15. Triple Timer Signals

| Signal Name | Type | State During Reset ^{1,2} | Signal Description |
|---|-----------------|-----------------------------------|--|
| TIO0 | Input or Output | Ignored Input | <p>Timer 0 Schmitt-Trigger Input/Output— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output.</p> <p>The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).</p> |
| TIO1 | Input or Output | Ignored Input | <p>Timer 1 Schmitt-Trigger Input/Output— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output.</p> <p>The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).</p> |
| TIO2 | Input or Output | Ignored Input | <p>Timer 2 Schmitt-Trigger Input/Output— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output.</p> <p>The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).</p> |
| <p>Notes:</p> <ol style="list-style-type: none"> In the Stop state, the signal maintains the last state as follows: <ul style="list-style-type: none"> If the last state is input, the signal is an ignored input. If the last state is output, the signal is tri-stated. The Wait processing state does not affect the signal state. All inputs are 5 V tolerant. | | | |

1.13 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56303 support circuit-board test strategies based on the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*, the industry standard developed under the sponsorship of the Test Technology Committee of IEEE and the JTAG.

The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals.

For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

Table 1-16. JTAG/OnCE Interface

| Signal Name | Type | State During Reset | Signal Description |
|------------------------------------|----------------------------|--------------------|--|
| TCK | Input | Input | Test Clock —A test clock input signal to synchronize the JTAG test logic. |
| TDI | Input | Input | Test Data Input —A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. |
| TDO | Output | Tri-stated | Test Data Output —A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK. |
| TMS | Input | Input | Test Mode Select —Sequences the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. |
| $\overline{\text{TRST}}$ | Input | Input | Test Reset —Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted after powerup. |
| $\overline{\text{DE}}$ | Input/ Output (open-drain) | Input | <p>Debug Event—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor.</p> <p>This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.</p> |
| Note: All inputs are 5 V tolerant. | | | |

2.1 Introduction

The DSP56303 is fabricated in high-density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

2.2 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Note: In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device that has a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

2.3 Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings¹

| Rating | Symbol | Value | Unit |
|---|-----------|-----------------------------|------|
| Supply Voltage | V_{CC} | -0.3 to +4.0 | V |
| All input voltages excluding "5 V tolerant" inputs | V_{IN} | GND - 0.3 to $V_{CC} + 0.3$ | V |
| All "5 V tolerant" input voltages ² | V_{IN5} | GND - 0.3 to 5.5 | V |
| Current drain per pin excluding V_{CC} and GND | I | 10 | mA |
| Operating temperature range | T_J | -40 to +100 | °C |
| Storage temperature | T_{STG} | -55 to +150 | °C |
| Notes: <ol style="list-style-type: none"> 1. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device. 2. At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V. | | | |

2.4 Thermal Characteristics

Table 2-2. Thermal Characteristics

| Characteristic | Symbol | TQFP Value | MAP-BGA ³ Value | MAP-BGA ⁴ Value | Unit |
|--|----------------------------------|------------|----------------------------|----------------------------|------|
| Junction-to-ambient thermal resistance ¹ | $R_{\theta JA}$ or θ_{JA} | 56 | 57 | 28 | °C/W |
| Junction-to-case thermal resistance ² | $R_{\theta JC}$ or θ_{JC} | 11 | 15 | — | °C/W |
| Thermal characterization parameter | Ψ_{JT} | 7 | 8 | — | °C/W |
| Notes: <ol style="list-style-type: none"> 1. Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per JEDEC Specification JESD51-3. 2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature. 3. These are simulated values. See note 1 for test board conditions. 4. These are simulated values. The test board has two 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board. | | | | | |

2.5 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics⁶

| Characteristics | Symbol | Min | Typ | Max | Unit |
|--|-----------|---------------------|-----|---------------------|---------|
| Supply voltage | V_{CC} | 3.0 | 3.3 | 3.6 | V |
| Input high voltage | V_{IH} | 2.0 | — | V_{CC} | V |
| • D[0–23], \overline{BG} , \overline{BB} , \overline{TA} | V_{IHP} | 2.0 | — | 5.25 | V |
| • MOD ¹ / \overline{IRQ}^1 , \overline{RESET} , $\overline{PINIT}/\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins | V_{IHx} | $0.8 \times V_{CC}$ | — | V_{CC} | V |
| • EXTAL ⁸ | | | | | |
| Input low voltage | V_{IL} | –0.3 | — | 0.8 | V |
| • D[0–23], \overline{BG} , \overline{BB} , \overline{TA} , MOD ¹ / \overline{IRQ}^1 , \overline{RESET} , \overline{PINIT} | V_{ILP} | –0.3 | — | 0.8 | V |
| • All JTAG/ESSI/SCI/Timer/HI08 pins | V_{ILx} | –0.3 | — | $0.2 \times V_{CC}$ | V |
| • EXTAL ⁸ | | | | | |
| Input leakage current | I_{IN} | –10 | — | 10 | μ A |
| High impedance (off-state) input current (@ 2.4 V / 0.4 V) | I_{TSI} | –10 | — | 10 | μ A |
| Output high voltage | V_{OH} | 2.4 | — | — | V |
| • TTL ($I_{OH} = -0.4$ mA) ^{5,7} | | $V_{CC} - 0.01$ | — | — | V |
| • CMOS ($I_{OH} = -10$ μ A) ⁵ | | | | | |
| Output low voltage | V_{OL} | — | — | 0.4 | V |
| • TTL ($I_{OL} = 1.6$ mA, open-drain pins $I_{OL} = 6.7$ mA) ^{5,7} | | — | — | 0.01 | V |
| • CMOS ($I_{OL} = 10$ μ A) ⁵ | | | | | |
| Internal supply current ² : | | | | | |
| • In Normal mode | I_{CCI} | — | 127 | — | mA |
| • In Wait mode ³ | I_{CCW} | — | 7.5 | — | mA |
| • In Stop mode ⁴ | I_{CCS} | — | 100 | — | μ A |
| PLL supply current | | — | 1 | 2.5 | mA |
| Input capacitance ⁵ | C_{IN} | — | — | 10 | pF |
| <p>Notes:</p> <ol style="list-style-type: none"> 1. Refers to $\overline{MODA}/\overline{IRQA}$, $\overline{MODB}/\overline{IRQB}$, $\overline{MODC}/\overline{IRQC}$, and $\overline{MODD}/\overline{IRQD}$ pins. 2. Power Consumption Considerations on page Section 4-3 provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see Appendix A). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with $V_{CC} = 3.3$ V at $T_J = 100^\circ\text{C}$. 3. In order to obtain these results, all inputs must be terminated (that is, not allowed to float). 4. In order to obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state. 5. Periodically sampled and not 100 percent tested. 6. $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50$ pF 7. This characteristic does not apply to XTAL and PCAP. 8. Driving EXTAL to the low V_{IHx} or the high V_{ILx} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHx} should be no lower than $0.9 \times V_{CC}$ and the maximum V_{ILx} should be no higher than $0.1 \times V_{CC}$. | | | | | |

2.6 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal transition. DSP56303 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

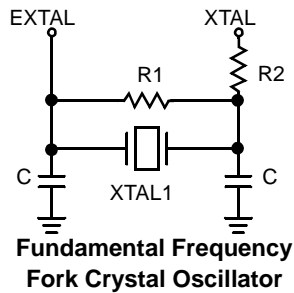
2.6.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

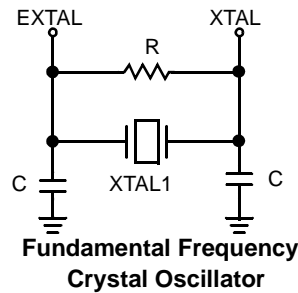
| Characteristics | Symbol | Expression ^{1,2} | | |
|---|-----------|---|------------------------------------|---|
| | | Min | Typ | Max |
| Internal operation frequency and CLKOUT with PLL enabled | f | — | $(Ef \times MF) / (PDF \times DF)$ | — |
| Internal operation frequency and CLKOUT with PLL disabled | f | — | $Ef/2$ | — |
| Internal clock and CLKOUT high period <ul style="list-style-type: none"> • With PLL disabled • With PLL enabled and $MF \leq 4$ • With PLL enabled and $MF > 4$ | T_H | — $0.49 \times ET_C \times PDF \times DF/MF$ $0.47 \times ET_C \times PDF \times DF/MF$ | ET_C — — | — $0.51 \times ET_C \times PDF \times DF/MF$ $0.53 \times ET_C \times PDF \times DF/MF$ |
| Internal clock and CLKOUT low period <ul style="list-style-type: none"> • With PLL disabled • With PLL enabled and $MF \leq 4$ • With PLL enabled and $MF > 4$ | T_L | — $0.49 \times ET_C \times PDF \times DF/MF$ $0.47 \times ET_C \times PDF \times DF/MF$ | ET_C — — | — $0.51 \times ET_C \times PDF \times DF/MF$ $0.53 \times ET_C \times PDF \times DF/MF$ |
| Internal clock and CLKOUT cycle time with PLL enabled | T_C | — | $ET_C \times PDF \times DF/MF$ | — |
| Internal clock and CLKOUT cycle time with PLL disabled | T_C | — | $2 \times ET_C$ | — |
| Instruction cycle time | I_{CYC} | — | T_C | — |
| Notes: <ol style="list-style-type: none"> 1. DF = Division Factor; Ef = External frequency; ET_C = External clock cycle; MF = Multiplication Factor; PDF = Predivision Factor; T_C = internal clock cycle 2. See the PLL and Clock Generation section in the <i>DSP56300 Family Manual</i> for a detailed discussion of the PLL. | | | | |

2.6.2 External Clock Operation

The DSP56303 system clock is derived from the on-chip oscillator or is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; examples are shown in **Figure 2-1**.



Note: Ensure that in the PCTL Register:
 ■ XTLD (bit 16) = 0
 ■ If $f_{OSC} \leq 200$ kHz, XTLR (bit 15) = 1



Note: Ensure that in the PCTL Register:
 ■ XTLD (bit 16) = 0
 ■ If $f_{OSC} > 200$ kHz, XTLR (bit 15) = 0

Suggested Component Values:

$f_{OSC} = 32.768$ kHz
 $R1 = 3.9$ M $\Omega \pm 10\%$
 $C = 22$ pF $\pm 20\%$
 $R2 = 200$ k $\Omega \pm 10\%$

Calculations are for a 32.768 kHz crystal with the following parameters:

- load capacitance (C_L) of 12.5 pF,
- shunt capacitance (C_0) of 1.8 pF,
- series resistance of 40 k Ω , and
- drive level of 1 μ W.

Suggested Component Values:

$f_{OSC} = 4$ MHz $f_{OSC} = 20$ MHz
 $R = 680$ k $\Omega \pm 10\%$ $R = 680$ k $\Omega \pm 10\%$
 $C = 56$ pF $\pm 20\%$ $C = 22$ pF $\pm 20\%$

Calculations are for a 4/20 MHz crystal with the following parameters:

- C_L of 30/20 pF,
- C_0 of 7/6 pF,
- series resistance of 100/20 Ω , and
- drive level of 2 mW.

Figure 2-1. Crystal Oscillator Circuits

If an externally-supplied square wave voltage source is used, disable the internal oscillator circuit during bootup by setting XTLD (PCTL Register bit 16 = 1—see the *DSP56303 User's Manual*). The external square wave source connects to EXTAL; XTAL is not physically connected to the board or socket. **Figure 2-2** shows the relationship between the EXTAL input and the internal clock and CLKOUT.

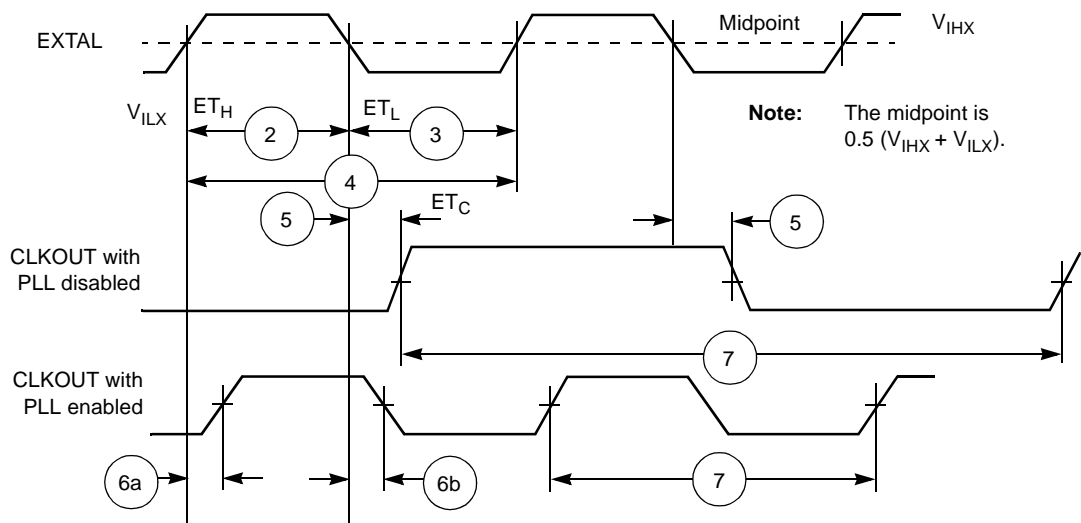


Figure 2-2. External Clock Timing

Table 2-5. Clock Operation

| No. | Characteristics | Symbol | 100 MHz | |
|---|--|-----------|----------------------|---------------------------|
| | | | Min | Max |
| 1 | Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum. | E_f | 0 | 100.0 |
| 2 | EXTAL input high ^{1, 2} • With PLL disabled (46.7%–53.3% duty cycle ⁶) • With PLL enabled (42.5%–57.5% duty cycle ⁶) | ET_H | 4.67 ns 4.25 ns | ∞ 157.0 μ s |
| 3 | EXTAL input low ^{1, 2} • With PLL disabled (46.7%–53.3% duty cycle ⁶) • With PLL enabled (42.5%–57.5% duty cycle ⁶) | ET_L | 4.67 ns 4.25 ns | ∞ 157.0 μ s |
| 4 | EXTAL cycle time ² • With PLL disabled • With PLL enabled | ET_C | 10.00 ns 10.00 ns | ∞ 273.1 μ s |
| 5 | Internal clock change from EXTAL fall with PLL disabled | | 4.3 ns | 11.0 ns |
| 6 | a. Internal clock rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, $E_f > 15$ MHz) ^{3,5} b. Internal clock falling edge from EXTAL falling edge with PLL enabled (MF \leq 4, PDF \neq 1, $E_f / PDF > 15$ MHz) ^{3,5} | | 0.0 ns 0.0 ns | 1.8 ns 1.8 ns |
| 7 | Instruction cycle time = $I_{CYC} = T_C^4$ (see Table 2-4) (46.7%–53.3% duty cycle) • With PLL disabled • With PLL enabled | I_{CYC} | 20.0 ns 10.00 ns | ∞ 8.53 μ s |
| Notes: <ol style="list-style-type: none"> 1. Measured at 50 percent of the input transition. 2. The maximum value for PLL enabled is given for minimum VCO frequency (see Table 2-4) and maximum MF. 3. Periodically sampled and not 100 percent tested. 4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF. 5. The skew is not guaranteed for any other MF value. 6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met. | | | | |

2.6.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

| Characteristics | 100 MHz | | Unit |
|---|--|---|----------|
| | Min | Max | |
| Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF $\times E_f \times 2 / PDF$) | 30 | 200 | MHz |
| PLL external capacitor (PCAP pin to V_{CCP}) (C_{PCAP}^1) • @ MF \leq 4 • @ MF $>$ 4 | (580 \times MF) – 100 830 \times MF | (780 \times MF) – 140 1470 \times MF | pF pF |
| Note: C_{PCAP} is the value of the PLL capacitor (connected between the PCAP pin and V_{CCP}) computed using the appropriate expression listed above. | | | |

2.6.4 Reset, Stop, Mode Select, and Interrupt Timing

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing⁶

| No. | Characteristics | Expression | 100 MHz | | Unit |
|-----|---|--|---|--------------------------------------|---------------------------------------|
| | | | Min | Max | |
| 8 | Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value ³ | — | — | 26.0 | ns |
| 9 | Required $\overline{\text{RESET}}$ duration ⁴ <ul style="list-style-type: none"> Power on, external clock generator, PLL disabled Power on, external clock generator, PLL enabled Power on, internal oscillator During STOP, XTAL disabled (PCTL Bit 16 = 0) During STOP, XTAL enabled (PCTL Bit 16 = 1) During normal operation | $50 \times ET_C$ $1000 \times ET_C$ $75000 \times ET_C$ $75000 \times ET_C$ $2.5 \times T_C$ $2.5 \times T_C$ | 500.0 10.0 0.75 0.75 25.0 25.0 | — — — — — — | ns μ s ms ms ns ns |
| 10 | Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion) ⁵ <ul style="list-style-type: none"> Minimum Maximum | $3.25 \times T_C + 2.0$ $20.25 \times T_C + 10$ | 34.5 — | — 212.5 | ns ns |
| 11 | Synchronous reset set-up time from $\overline{\text{RESET}}$ deassertion to CLKOUT Transition 1 <ul style="list-style-type: none"> Minimum Maximum | T_C | 5.9 — | — 10.0 | ns ns |
| 12 | Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output <ul style="list-style-type: none"> Minimum Maximum | $3.25 \times T_C + 1.0$ $20.25 \times T_C + 1.0$ | 33.5 — | — 203.5 | ns ns |
| 13 | Mode select setup time | | 30.0 | — | ns |
| 14 | Mode select hold time | | 0.0 | — | ns |
| 15 | Minimum edge-triggered interrupt request assertion width | | 6.6 | — | ns |
| 16 | Minimum edge-triggered interrupt request deassertion width | | 6.6 | — | ns |
| 17 | Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid <ul style="list-style-type: none"> Caused by first interrupt instruction fetch Caused by first interrupt instruction execution | $4.25 \times T_C + 2.0$ $7.25 \times T_C + 2.0$ | 44.5 74.5 | — — | ns ns |
| 18 | Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution | $10 \times T_C + 5.0$ | 105.0 | — | ns |
| 19 | Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts ^{1, 7, 8} | $(WS + 3.75) \times T_C - 10.94$ | — | Note 8 | ns |
| 20 | Delay from $\overline{\text{RD}}$ assertion to interrupt request deassertion for level sensitive fast interrupts ^{1, 7, 8} | $(WS + 3.25) \times T_C - 10.94$ | — | Note 8 | ns |
| 21 | Delay from $\overline{\text{WR}}$ assertion to interrupt request deassertion for level sensitive fast interrupts ^{1, 7, 8} <ul style="list-style-type: none"> DRAM for all WS SRAM WS = 1 SRAM WS = 2, 3 SRAM WS \geq 4 | $(WS + 3.5) \times T_C - 10.94$ $(WS + 3.5) \times T_C - 10.94$ $(WS + 3) \times T_C - 10.94$ $(WS + 2.5) \times T_C - 10.94$ | — — — — | Note 8 Note 8 Note 8 Note 8 | ns ns ns ns |
| 22 | Synchronous interrupt set-up time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to the CLKOUT Transition 2 | | 5.9 | T_C | ns |
| 23 | Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state <ul style="list-style-type: none"> Minimum Maximum | $8.25 \times T_C + 1.0$ $24.75 \times T_C + 5.0$ | 83.5 — | — 252.5 | ns ns |
| 24 | Duration for $\overline{\text{IRQA}}$ assertion to recover from Stop state | | 5.9 | — | ns |

AC Electrical Characteristics

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing⁶ (Continued)

| No. | Characteristics | Expression | 100 MHz | | Unit |
|-----|--|---|----------|---------|------|
| | | | Min | Max | |
| 25 | Delay from $\overline{\text{IRQA}}$ assertion to fetch of first instruction (when exiting Stop) ^{2, 3} <ul style="list-style-type: none"> • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay) | $\text{PLC} \times \text{ET}_C \times \text{PDF} + (128 \text{ K} - \text{PLC}/2) \times \text{T}_C$ $\text{PLC} \times \text{ET}_C \times \text{PDF} + (23.75 \pm 0.5) \times \text{T}_C$ $(8.25 \pm 0.5) \times \text{T}_C$ | 1.3 | 9.1 | ms |
| | | | 232.5 ns | 12.3 ms | |
| | | | 87.5 | 97.5 | ns |
| 26 | Duration of level sensitive $\overline{\text{IRQA}}$ assertion to ensure interrupt service (when exiting Stop) ^{2, 3} <ul style="list-style-type: none"> • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay) | $\text{PLC} \times \text{ET}_C \times \text{PDF} + (128\text{K} - \text{PLC}/2) \times \text{T}_C$ $\text{PLC} \times \text{ET}_C \times \text{PDF} + (20.5 \pm 0.5) \times \text{T}_C$ $5.5 \times \text{T}_C$ | 13.6 | — | ms |
| | | | 12.3 | — | ms |
| | | | 55.0 | — | ns |
| 27 | Interrupt Requests Rate <ul style="list-style-type: none"> • HI08, ESSI, SCI, Timer • DMA • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger) • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (level trigger) | Maximum: $12 \times \text{T}_C$ $8 \times \text{T}_C$ $8 \times \text{T}_C$ $12 \times \text{T}_C$ | — | 120.0 | ns |
| | | | — | 80.0 | ns |
| | | | — | 80.0 | ns |
| | | | — | 120.0 | ns |
| 28 | DMA Requests Rate <ul style="list-style-type: none"> • Data read from HI08, ESSI, SCI • Data write to HI08, ESSI, SCI • Timer • $\overline{\text{IRQ}}$, $\overline{\text{NMI}}$ (edge trigger) | Maximum: $6 \times \text{T}_C$ $7 \times \text{T}_C$ $2 \times \text{T}_C$ $3 \times \text{T}_C$ | — | 60.0 | ns |
| | | | — | 70.0 | ns |
| | | | — | 20.0 | ns |
| | | | — | 30.0 | ns |
| 29 | Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory (DMA source) access address out valid | Minimum: $4.25 \times \text{T}_C + 2.0$ | 30.3 | — | ns |

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing⁶ (Continued)

| No. | Characteristics | Expression | 100 MHz | | Unit |
|---------------|---|------------|---------|-----|------|
| | | | Min | Max | |
| Notes: | <ol style="list-style-type: none"> When fast interrupts are used and \overline{IRQA}, \overline{IRQB}, \overline{IRQC}, and \overline{IRQD} are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode. This timing depends on several settings: <ul style="list-style-type: none"> For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case. For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored). For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings. For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion. PLC value for PLL disable is 0. The maximum value for ET_C is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is $4096/66 \text{ MHz} = 62 \mu\text{s}$). During the stabilization period, T_C, T_H, and T_L is not constant, and their width may vary, so timing may vary as well. Periodically sampled and not 100 percent tested. Value depends on clock source: <ul style="list-style-type: none"> For an external clock generator, \overline{RESET} duration is measured while \overline{RESET} is asserted, V_{CC} is valid, and the EXTAL input is active and valid. For an internal oscillator, \overline{RESET} duration is measured while \overline{RESET} is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions. When the V_{CC} is valid, but the other "required RESET duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration. If PLL does not lose lock. $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$. WS = number of wait states (measured in clock cycles, number of T_C). Use the expression to compute a maximum value. | | | | |

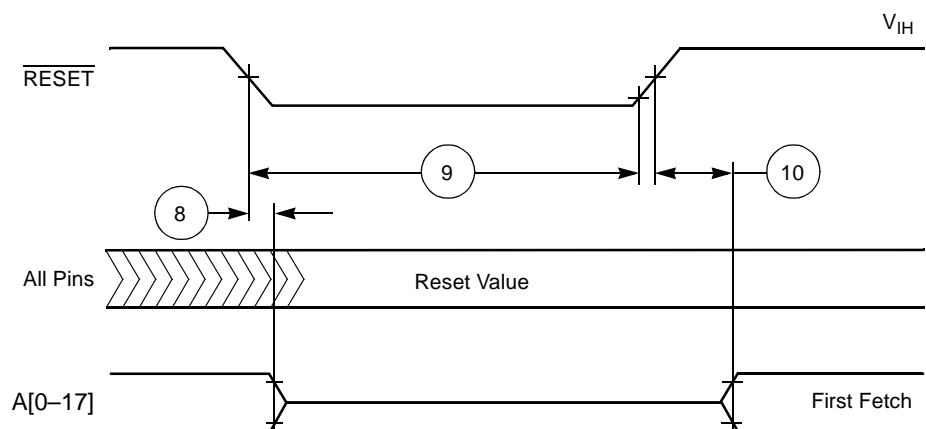


Figure 2-3. Reset Timing

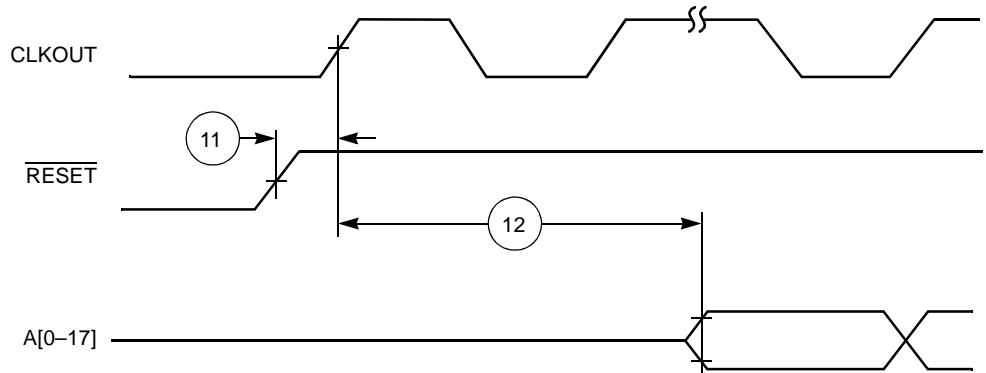
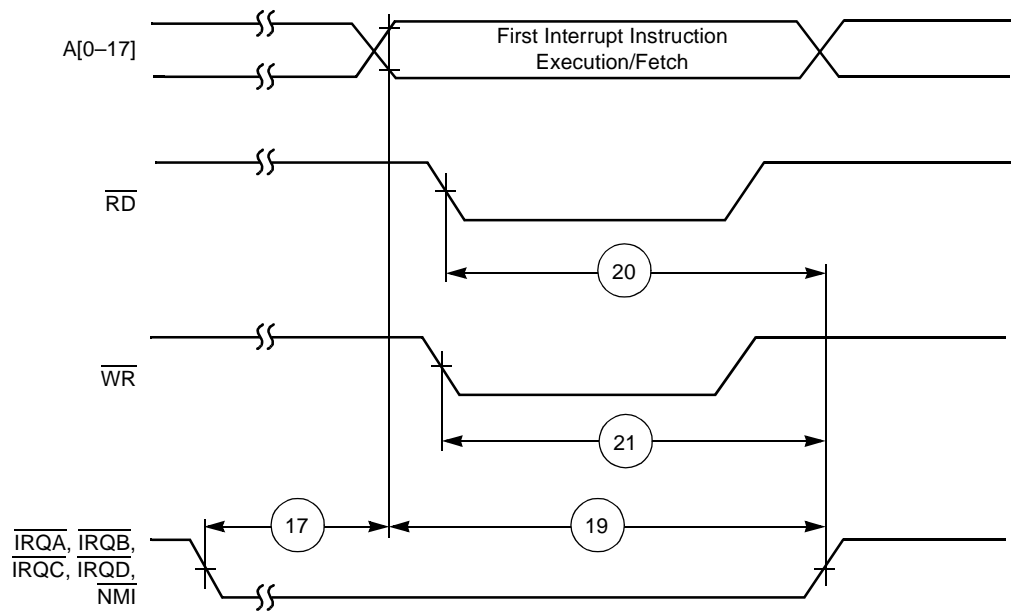
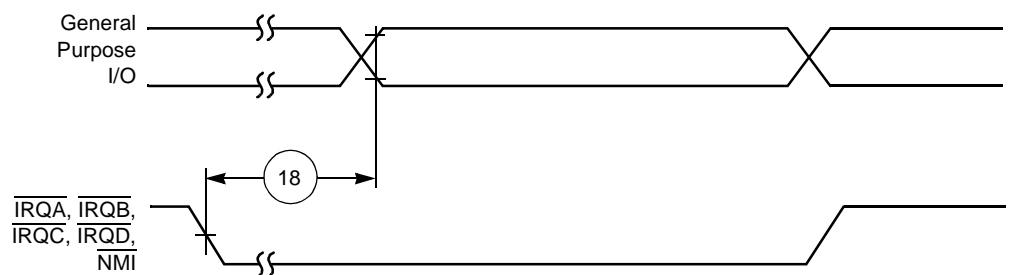


Figure 2-4. Synchronous Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-5. External Fast Interrupt Timing

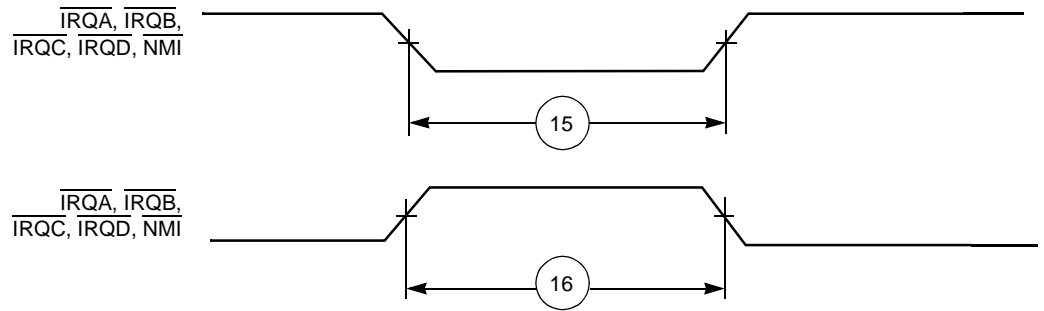


Figure 2-6. External Interrupt Timing (Negative Edge-Triggered)

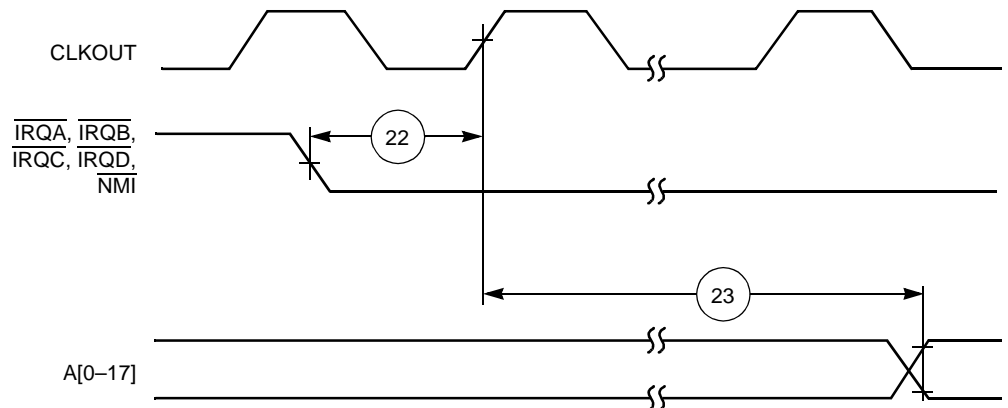


Figure 2-7. Synchronous Interrupt from Wait State Timing

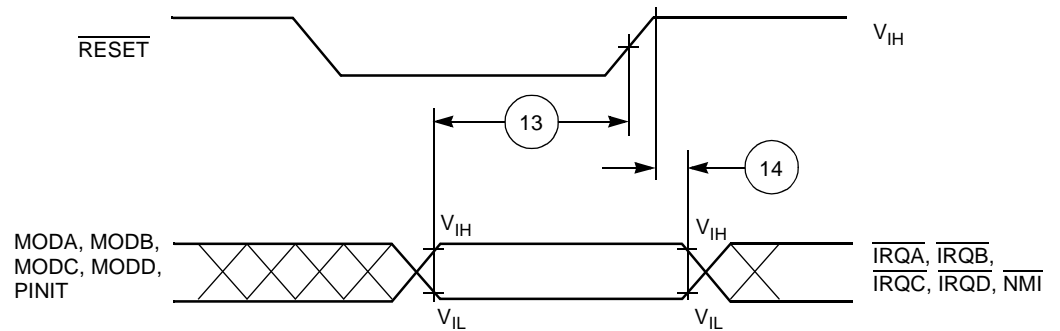


Figure 2-8. Operating Mode Select Timing

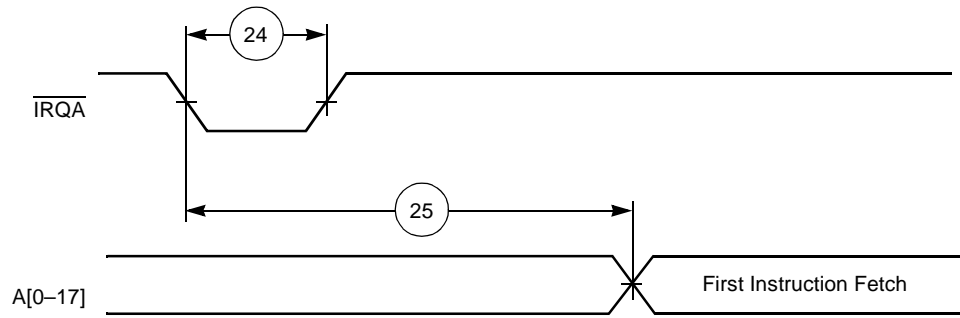


Figure 2-9. Recovery from Stop State Using $\overline{\text{IRQA}}$

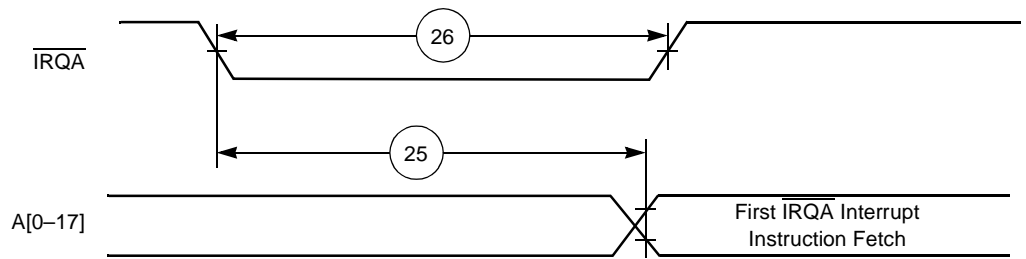


Figure 2-10. Recovery from Stop State Using $\overline{\text{IRQA}}$ Interrupt Service

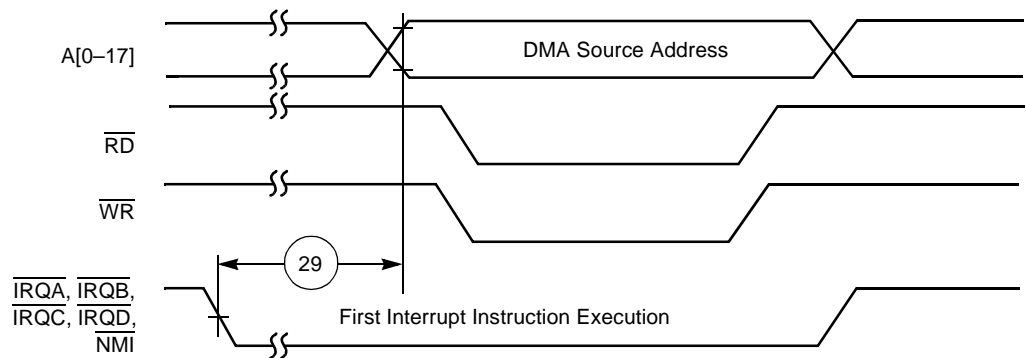


Figure 2-11. External Memory Access (DMA Source) Timing

2.6.5 External Memory Expansion Port (Port A)

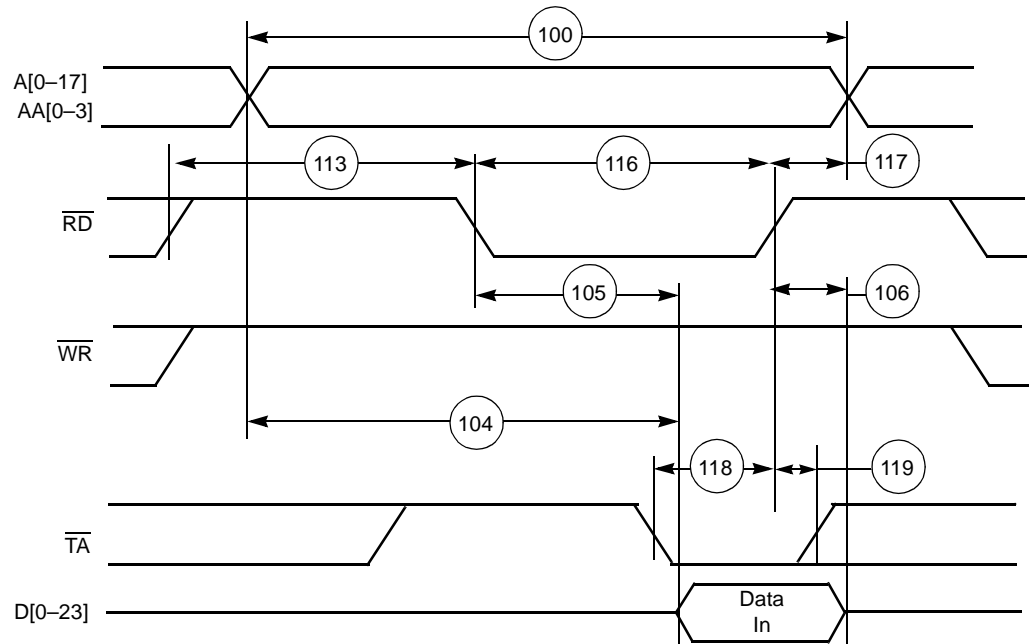
2.6.5.1 SRAM Timing

Table 2-8. SRAM Read and Write Accesses

| No. | Characteristics | Symbol | Expression ¹ | 100 MHz | | Unit |
|-----|--|-------------------|---|---------|------|------|
| | | | | Min | Max | |
| 100 | Address valid and AA assertion pulse width ² | t_{RC}, t_{WC} | $(WS + 1) \times T_C - 4.0$ [1 ≤ WS ≤ 3] | 16.0 | — | ns |
| | | | $(WS + 2) \times T_C - 4.0$ [4 ≤ WS ≤ 7] | 56.0 | — | ns |
| | | | $(WS + 3) \times T_C - 4.0$ [WS ≥ 8] | 106.0 | — | ns |
| 101 | Address and AA valid to \overline{WR} assertion | t_{AS} | $0.25 \times T_C - 2.0$ [WS = 1] | 0.5 | — | ns |
| | | | $0.75 \times T_C - 2.0$ [2 ≤ WS ≤ 3] | 5.5 | — | ns |
| | | | $1.25 \times T_C - 2.0$ [WS ≥ 4] | 10.5 | — | ns |
| 102 | \overline{WR} assertion pulse width | t_{WP} | $1.5 \times T_C - 4.0$ [WS = 1] | 11.0 | — | ns |
| | | | $WS \times T_C - 4.0$ [2 ≤ WS ≤ 3] | 16.0 | — | ns |
| | | | $(WS - 0.5) \times T_C - 4.0$ [WS ≥ 4] | 31.0 | — | ns |
| 103 | \overline{WR} deassertion to address not valid | t_{WR} | $0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3] | 0.5 | — | ns |
| | | | $1.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7] | 8.5 | — | ns |
| | | | $2.25 \times T_C - 4.0$ [WS ≥ 8] | 18.5 | — | ns |
| 104 | Address and AA valid to input data valid | t_{AA}, t_{AC} | $(WS + 0.75) \times T_C - 5.0$ [WS ≥ 1] | — | 12.5 | ns |
| 105 | \overline{RD} assertion to input data valid | t_{OE} | $(WS + 0.25) \times T_C - 5.0$ [WS ≥ 1] | — | 7.5 | ns |
| 106 | \overline{RD} deassertion to data not valid (data hold time) | t_{OHZ} | | 0.0 | — | ns |
| 107 | Address valid to \overline{WR} deassertion ² | t_{AW} | $(WS + 0.75) \times T_C - 4.0$ [WS ≥ 1] | 13.5 | — | ns |
| 108 | Data valid to \overline{WR} deassertion (data setup time) | $t_{DS} (t_{DW})$ | $(WS - 0.25) \times T_C - 3.0$ [WS ≥ 1] | 4.5 | — | ns |
| 109 | Data hold time from \overline{WR} deassertion | t_{DH} | $0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3] | 0.5 | — | ns |
| | | | $1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7] | 10.5 | — | ns |
| | | | $2.25 \times T_C - 2.0$ [WS ≥ 8] | 20.5 | — | ns |
| 110 | \overline{WR} assertion to data active | — | $0.75 \times T_C - 3.7$ [WS = 1] | 3.8 | — | ns |
| | | | $0.25 \times T_C - 3.7$ [2 ≤ WS ≤ 3] | -1.2 | — | ns |
| | | | $-0.25 \times T_C - 3.7$ [WS ≥ 4] | -6.2 | — | ns |

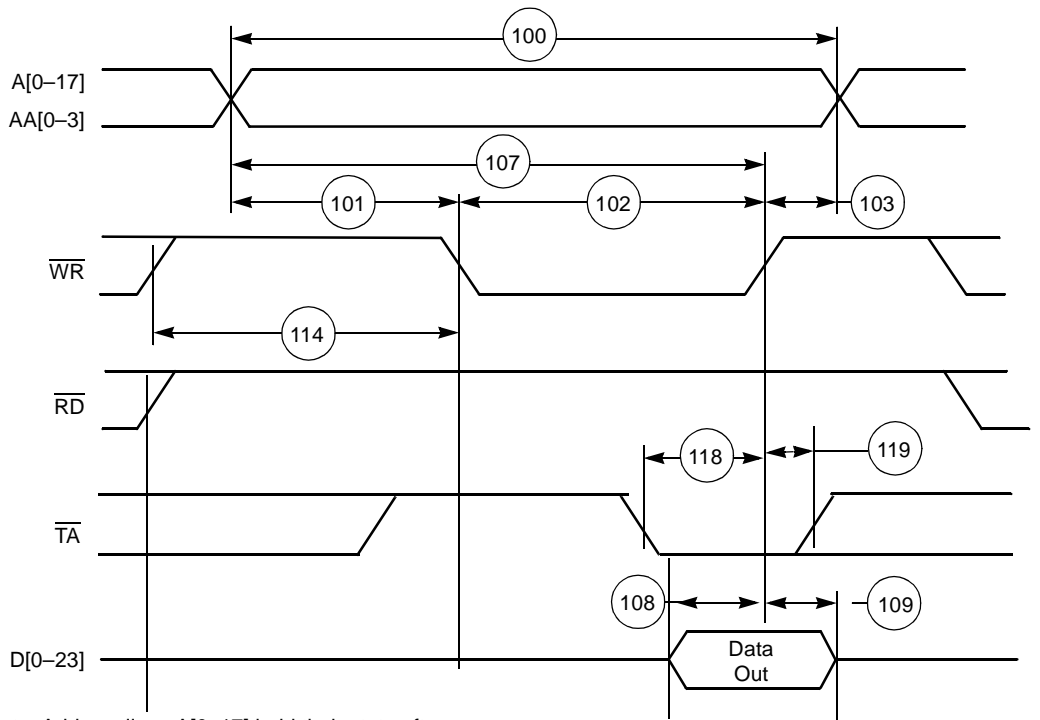
Table 2-8. SRAM Read and Write Accesses (Continued)

| No. | Characteristics | Symbol | Expression ¹ | 100 MHz | | Unit |
|---|--|--------|---|---------|------|------|
| | | | | Min | Max | |
| 111 | \overline{WR} deassertion to data high impedance | — | $0.25 \times T_C + 0.2$ [1 ≤ WS ≤ 3] | — | 2.7 | ns |
| | | | $1.25 \times T_C + 0.2$ [4 ≤ WS ≤ 7] | — | 12.7 | ns |
| | | | $2.25 \times T_C + 0.2$ [WS > 8] | — | 22.7 | ns |
| 112 | Previous \overline{RD} deassertion to data active (write) | — | $1.25 \times T_C - 4.0$ [1 ≤ WS ≤ 3] | 8.5 | — | ns |
| | | | $2.25 \times T_C - 4.0$ [4 ≤ WS ≤ 7] | 18.5 | — | ns |
| | | | $3.25 \times T_C - 4.0$ [WS > 8] | 28.5 | — | ns |
| 113 | \overline{RD} deassertion time | — | $0.75 \times T_C - 4.0$ [1 ≤ WS ≤ 3] | 3.5 | — | ns |
| | | | $1.75 \times T_C - 4.0$ [4 ≤ WS ≤ 7] | 13.5 | — | ns |
| | | | $2.75 \times T_C - 4.0$ [WS ≥ 8] | 23.5 | — | ns |
| 114 | \overline{WR} deassertion time | — | $0.5 \times T_C - 4.0$ [WS = 1] | 1.0 | — | ns |
| | | | $T_C - 4.0$ [2 ≤ WS ≤ 3] | 6.0 | — | ns |
| | | | $2.5 \times T_C - 4.0$ [4 ≤ WS ≤ 7] | 21.0 | — | ns |
| | | | $3.5 \times T_C - 4.0$ [WS ≥ 8] | 31.0 | — | ns |
| 115 | Address valid to \overline{RD} assertion | — | $0.5 \times T_C - 4.0$ | 1.0 | — | ns |
| 116 | \overline{RD} assertion pulse width | — | $(WS + 0.25) \times T_C - 4.0$ | 8.5 | — | ns |
| 117 | \overline{RD} deassertion to address not valid | — | $0.25 \times T_C - 2.0$ [1 ≤ WS ≤ 3] | 0.5 | — | ns |
| | | | $1.25 \times T_C - 2.0$ [4 ≤ WS ≤ 7] | 10.5 | — | ns |
| | | | $2.25 \times T_C - 2.0$ [WS ≥ 8] | 20.5 | — | ns |
| 118 | \overline{TA} setup before \overline{RD} or \overline{WR} deassertion ⁴ | — | $0.25 \times T_C + 2.0$ | 4.5 | — | ns |
| 119 | \overline{TA} hold after \overline{RD} or \overline{WR} deassertion | — | — | 0 | — | ns |
| Notes: <ol style="list-style-type: none"> WS is the number of wait states specified in the BCR. An expression is used to compute the number listed as the minimum or maximum value, as appropriate. Timings 100, 107 are guaranteed by design, not tested. All timings for 100 MHz are measured from $0.5 \times V_{CC}$ to $0.5 \times V_{CC}$. Timing 118 is relative to the deassertion edge of \overline{RD} or \overline{WR} even if \overline{TA} remains asserted. $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$ | | | | | | |



Note: Address lines A[0-17] hold their state after a read or write operation. AA[0-3] do not hold their state after a read or write operation.

Figure 2-12. SRAM Read Access



Note: Address lines A[0-17] hold their state after a read or write operation. AA[0-3] do not hold their state after a read or write operation.

Figure 2-13. SRAM Write Access

2.6.5.2 DRAM Timing

The selection guides in **Figure 2-14** and **Figure 2-17** are for primary selection only. Final selection should be based on the timing in the following tables. For example, the selection guide suggests that four wait states must be used for 100 MHz operation with Page Mode DRAM. However, consulting the appropriate table, a designer can evaluate whether fewer wait states might suffice by determining which timing prevents operation at 100 MHz, running the chip at a slightly lower frequency (for example, 95 MHz), using faster DRAM (if it becomes available), and manipulating control factors such as capacitive and resistive load to improve overall system performance.

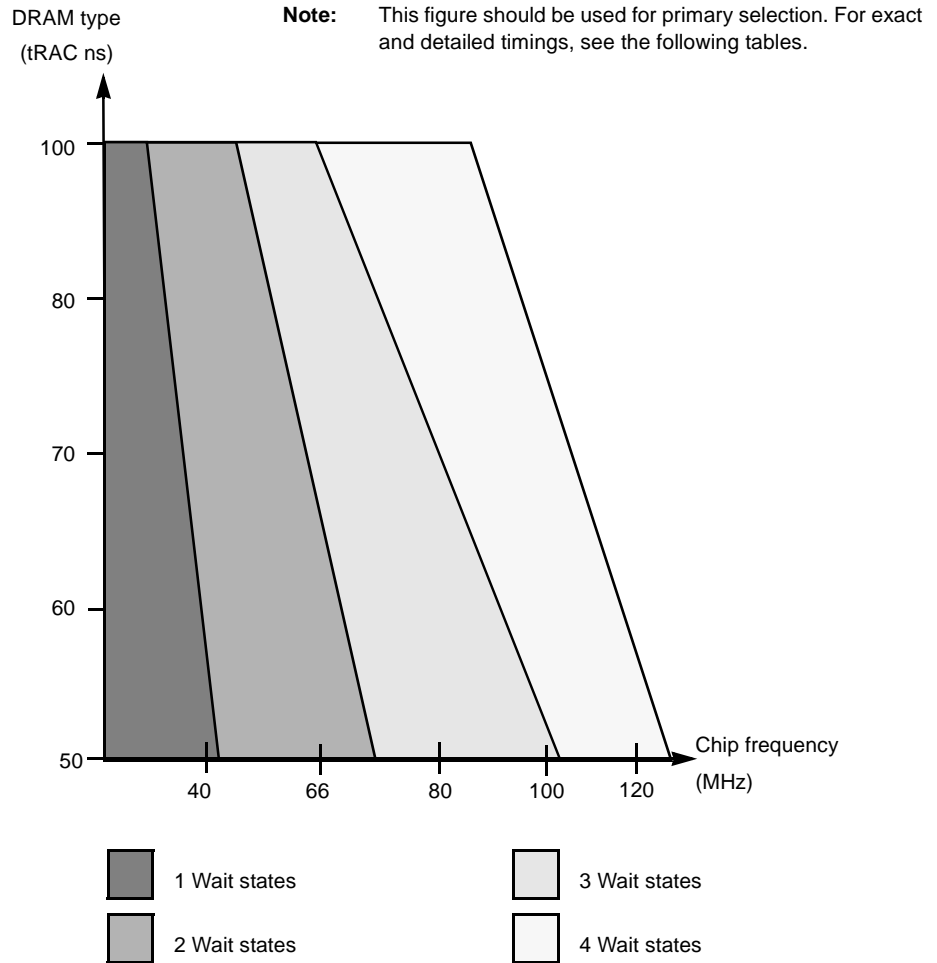


Figure 2-14. DRAM Page Mode Wait State Selection Guide

Table 2-9. DRAM Page Mode Timings, Three Wait States^{1,2,3}

| No. | Characteristics | Symbol | Expression ⁴ | 100 MHz | | Unit |
|--|--|------------|-------------------------|---------|------|------|
| | | | | Min | Max | |
| 131 | Page mode cycle time for two consecutive accesses of the same direction | | $4 \times T_C$ | 40.0 | — | ns |
| | Page mode cycle time for mixed (read and write) accesses | t_{PC} | $3.5 \times T_C$ | 35.0 | — | ns |
| 132 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $2 \times T_C - 5.7$ | — | 14.3 | ns |
| 133 | Column address valid to data valid (read) | t_{AA} | $3 \times T_C - 5.7$ | — | 24.3 | ns |
| 134 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | | 0.0 | — | ns |
| 135 | Last \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 136 | Previous \overline{CAS} deassertion to \overline{RAS} deassertion | t_{RHCP} | $4.5 \times T_C - 4.0$ | 41.0 | — | ns |
| 137 | \overline{CAS} assertion pulse width | t_{CAS} | $2 \times T_C - 4.0$ | 16.0 | — | ns |
| 138 | Last \overline{CAS} deassertion to \overline{RAS} assertion ⁵ <ul style="list-style-type: none"> • BRW[1–0] = 00, 01—not applicable • BRW[1–0] = 10 • BRW[1–0] = 11 | t_{CRP} | — | — | — | — |
| | | | $4.75 \times T_C - 6.0$ | 41.5 | — | ns |
| | | | $6.75 \times T_C - 6.0$ | 61.5 | — | ns |
| | | | | | | |
| 139 | \overline{CAS} deassertion pulse width | t_{CP} | $1.5 \times T_C - 4.0$ | 11.0 | — | ns |
| 140 | Column address valid to \overline{CAS} assertion | t_{ASC} | $T_C - 4.0$ | 6.0 | — | ns |
| 141 | \overline{CAS} assertion to column address not valid | t_{CAH} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 142 | Last column address valid to \overline{RAS} deassertion | t_{RAL} | $4 \times T_C - 4.0$ | 36.0 | — | ns |
| 143 | \overline{WR} deassertion to \overline{CAS} assertion | t_{RCS} | $1.25 \times T_C - 4.0$ | 8.5 | — | ns |
| 144 | \overline{CAS} deassertion to \overline{WR} assertion | t_{RCH} | $0.75 \times T_C - 4.0$ | 3.5 | — | ns |
| 145 | \overline{CAS} assertion to \overline{WR} deassertion | t_{WCH} | $2.25 \times T_C - 4.2$ | 18.3 | — | ns |
| 146 | \overline{WR} assertion pulse width | t_{WP} | $3.5 \times T_C - 4.5$ | 30.5 | — | ns |
| 147 | Last \overline{WR} assertion to \overline{RAS} deassertion | t_{RWL} | $3.75 \times T_C - 4.3$ | 33.2 | — | ns |
| 148 | \overline{WR} assertion to \overline{CAS} deassertion | t_{CWL} | $3.25 \times T_C - 4.3$ | 28.2 | — | ns |
| 149 | Data valid to \overline{CAS} assertion (write) | t_{DS} | $0.5 \times T_C - 4.5$ | 0.5 | — | ns |
| 150 | \overline{CAS} assertion to data not valid (write) | t_{DH} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 151 | \overline{WR} assertion to \overline{CAS} assertion | t_{WCS} | $1.25 \times T_C - 4.3$ | 8.2 | — | ns |
| 152 | Last \overline{RD} assertion to \overline{RAS} deassertion | t_{ROH} | $3.5 \times T_C - 4.0$ | 31.0 | — | ns |
| 153 | \overline{RD} assertion to data valid | t_{GA} | $2.5 \times T_C - 5.7$ | — | 19.3 | ns |
| 154 | \overline{RD} deassertion to data not valid ⁶ | t_{GZ} | | 0.0 | — | ns |
| 155 | \overline{WR} assertion to data active | | $0.75 \times T_C - 1.5$ | 6.0 | — | ns |
| 156 | \overline{WR} deassertion to data high impedance | | $0.25 \times T_C$ | — | 2.5 | ns |
| Notes: <ol style="list-style-type: none"> 1. The number of wait states for Page mode access is specified in the DRAM Control Register. 2. The refresh period is specified in the DRAM Control Register. 3. The asynchronous delays specified in the expressions are valid for the DSP56303. 4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $4 \times T_C$ for read-after-read or write-after-write sequences). An expression is used to compute the number listed as the minimum or maximum value listed, as appropriate. 5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page-access. 6. \overline{RD} deassertion always occurs after \overline{CAS} deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}. | | | | | | |

Table 2-10. DRAM Page Mode Timings, Four Wait States^{1,2,3}

| No. | Characteristics | Symbol | Expression ⁴ | 100 MHz | | Unit |
|-----|--|------------|-------------------------|---------|------|------|
| | | | | Min | Max | |
| 131 | Page mode cycle time for two consecutive accesses of the same direction | | $5 \times T_C$ | 50.0 | — | ns |
| | Page mode cycle time for mixed (read and write) accesses | t_{PC} | $4.5 \times T_C$ | 45.0 | — | ns |
| 132 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $2.75 \times T_C - 5.7$ | — | 21.8 | ns |
| 133 | Column address valid to data valid (read) | t_{AA} | $3.75 \times T_C - 5.7$ | — | 31.8 | ns |
| 134 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | | 0.0 | — | ns |
| 135 | Last \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $3.5 \times T_C - 4.0$ | 31.0 | — | ns |
| 136 | Previous \overline{CAS} deassertion to \overline{RAS} deassertion | t_{RHCP} | $6 \times T_C - 4.0$ | 56.0 | — | ns |
| 137 | \overline{CAS} assertion pulse width | t_{CAS} | $2.5 \times T_C - 4.0$ | 21.0 | — | ns |
| 138 | Last \overline{CAS} deassertion to \overline{RAS} assertion ⁵ <ul style="list-style-type: none"> • BRW[1-0] = 00, 01—Not applicable • BRW[1-0] = 10 • BRW[1-0] = 11 | t_{CRP} | — | — | — | — |
| | | | $5.25 \times T_C - 6.0$ | 46.5 | — | ns |
| | | | $7.25 \times T_C - 6.0$ | 66.5 | — | ns |
| | | | | | | |
| 139 | \overline{CAS} deassertion pulse width | t_{CP} | $2 \times T_C - 4.0$ | 16.0 | — | ns |
| 140 | Column address valid to \overline{CAS} assertion | t_{ASC} | $T_C - 4.0$ | 6.0 | — | ns |
| 141 | \overline{CAS} assertion to column address not valid | t_{CAH} | $3.5 \times T_C - 4.0$ | 31.0 | — | ns |
| 142 | Last column address valid to \overline{RAS} deassertion | t_{RAL} | $5 \times T_C - 4.0$ | 46.0 | — | ns |
| 143 | \overline{WR} deassertion to \overline{CAS} assertion | t_{RCS} | $1.25 \times T_C - 4.0$ | 8.5 | — | ns |
| 144 | \overline{CAS} deassertion to \overline{WR} assertion | t_{RCH} | $1.25 \times T_C - 3.7$ | 8.8 | — | ns |
| 145 | \overline{CAS} assertion to \overline{WR} deassertion | t_{WCH} | $3.25 \times T_C - 4.2$ | 28.3 | — | ns |
| 146 | \overline{WR} assertion pulse width | t_{WP} | $4.5 \times T_C - 4.5$ | 40.5 | — | ns |
| 147 | Last \overline{WR} assertion to \overline{RAS} deassertion | t_{RWL} | $4.75 \times T_C - 4.3$ | 43.2 | — | ns |
| 148 | \overline{WR} assertion to \overline{CAS} deassertion | t_{CWL} | $3.75 \times T_C - 4.3$ | 33.2 | — | ns |
| 149 | Data valid to \overline{CAS} assertion (write) | t_{DS} | $0.5 \times T_C - 4.5$ | 0.5 | — | ns |
| 150 | \overline{CAS} assertion to data not valid (write) | t_{DH} | $3.5 \times T_C - 4.0$ | 31.0 | — | ns |
| 151 | \overline{WR} assertion to \overline{CAS} assertion | t_{WCS} | $1.25 \times T_C - 4.3$ | 8.2 | — | ns |
| 152 | Last \overline{RD} assertion to \overline{RAS} deassertion | t_{ROH} | $4.5 \times T_C - 4.0$ | 41.0 | — | ns |
| 153 | \overline{RD} assertion to data valid | t_{GA} | $3.25 \times T_C - 5.7$ | — | 26.8 | ns |
| 154 | \overline{RD} deassertion to data not valid ⁶ | t_{GZ} | | 0.0 | — | ns |
| 155 | \overline{WR} assertion to data active | | $0.75 \times T_C - 1.5$ | 6.0 | — | ns |
| 156 | \overline{WR} deassertion to data high impedance | | $0.25 \times T_C$ | — | 2.5 | ns |

- Notes:**
1. The number of wait states for Page mode access is specified in the DRAM Control Register.
 2. The refresh period is specified in the DRAM Control Register.
 3. The asynchronous delays specified in the expressions are valid for the DSP56303.
 4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t_{PC} equals $3 \times T_C$ for read-after-read or write-after-write sequences). An expressions is used to calculate the maximum or minimum value listed, as appropriate.
 5. BRW[1-0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
 6. \overline{RD} deassertion always occurs after \overline{CAS} deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ} .

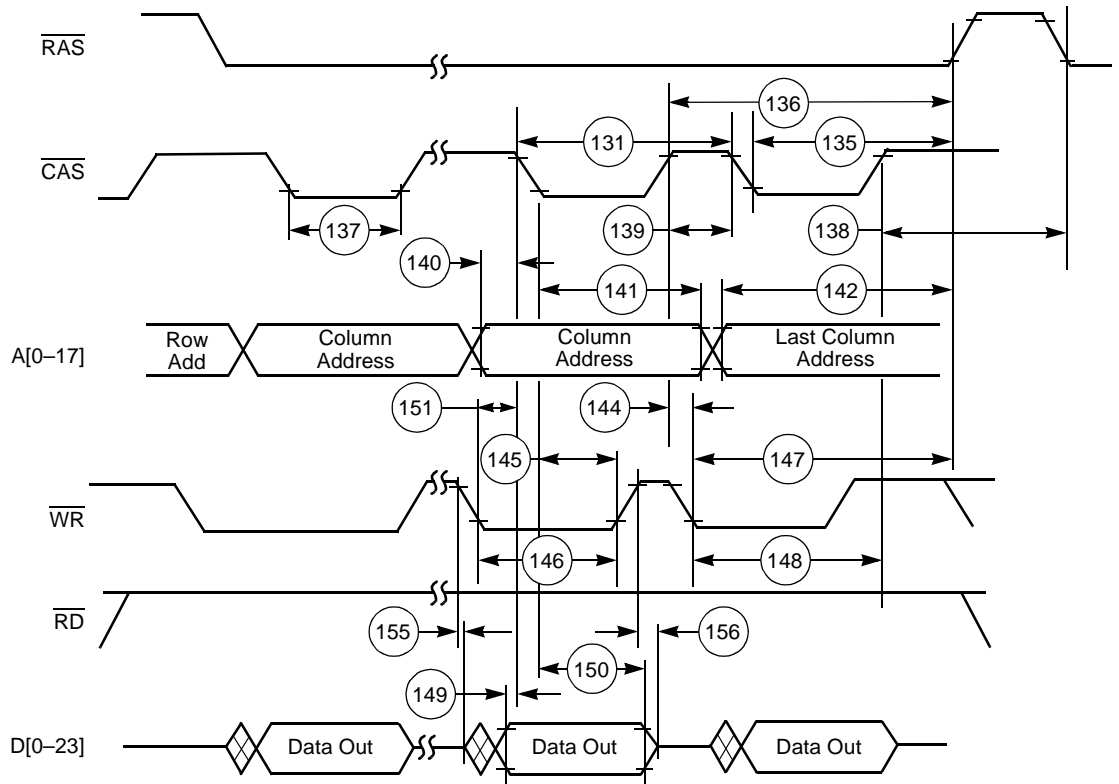


Figure 2-15. DRAM Page Mode Write Accesses

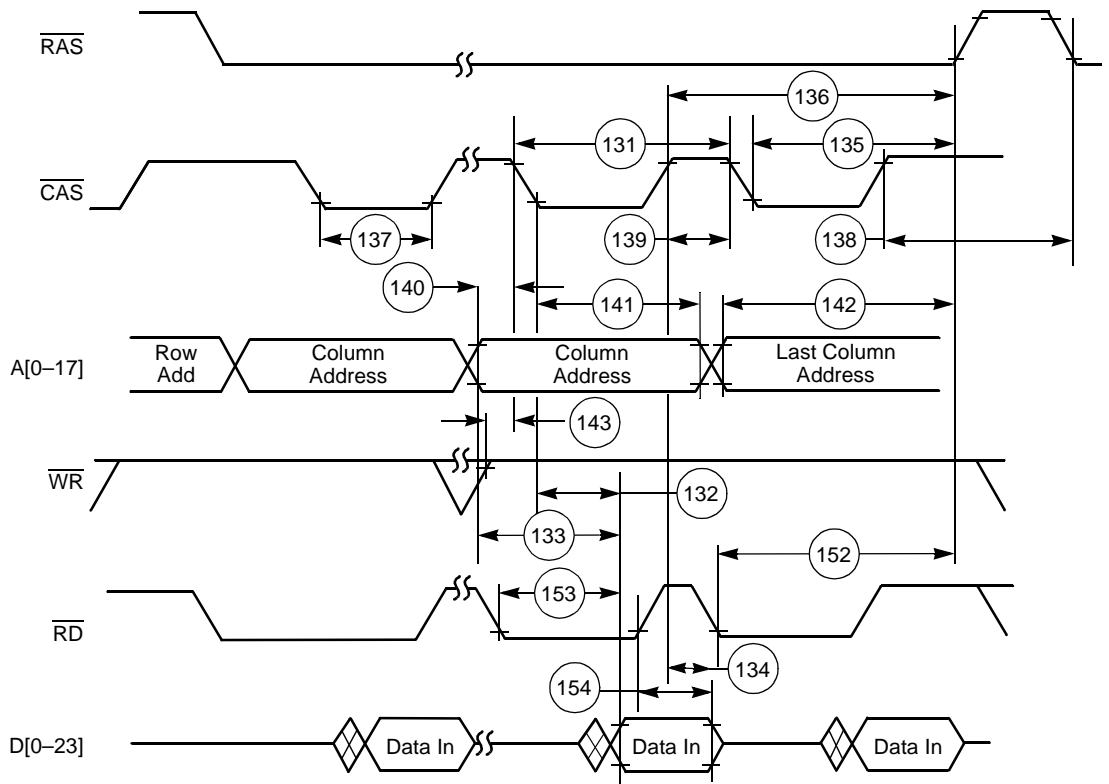


Figure 2-16. DRAM Page Mode Read Accesses

AC Electrical Characteristics

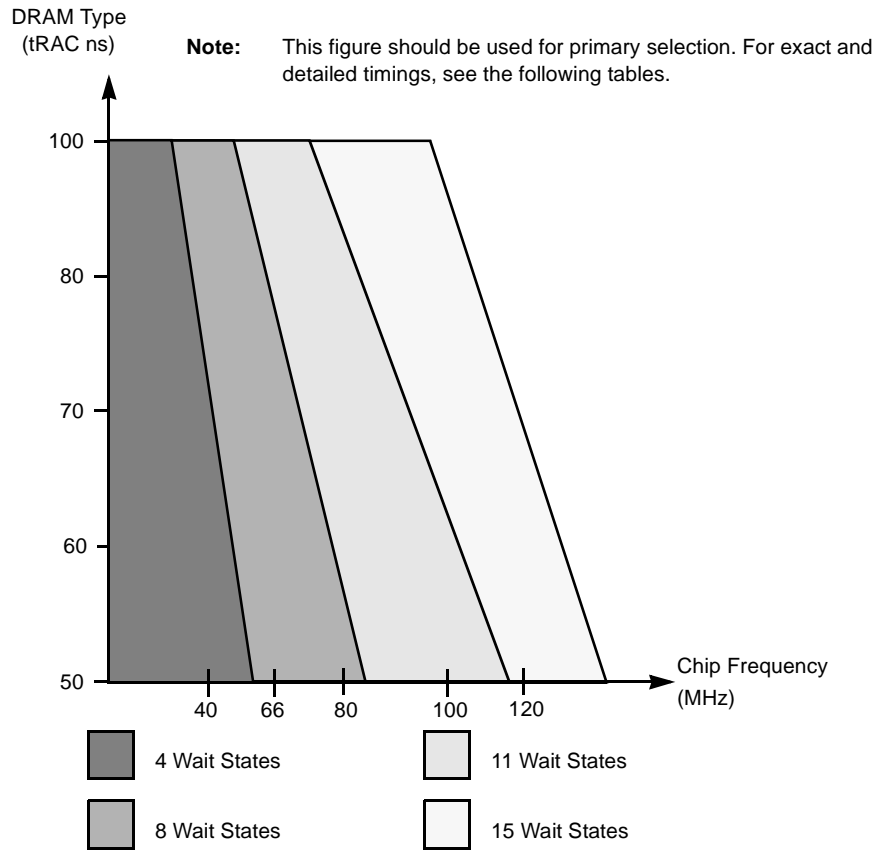


Figure 2-17. DRAM Out-of-Page Wait State Selection Guide

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States^{1,2}

| No. | Characteristics | Symbol | Expression ³ | 100 MHz | | Unit |
|-----|---|-----------|---------------------------|---------|------|------|
| | | | | Min | Max | |
| 157 | Random read or write cycle time | t_{RC} | $12 \times T_C$ | 120.0 | — | ns |
| 158 | \overline{RAS} assertion to data valid (read) | t_{RAC} | $6.25 \times T_C - 7.0$ | — | 55.5 | ns |
| 159 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $3.75 \times T_C - 7.0$ | — | 30.5 | ns |
| 160 | Column address valid to data valid (read) | t_{AA} | $4.5 \times T_C - 7.0$ | — | 38.0 | ns |
| 161 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | | 0.0 | — | ns |
| 162 | \overline{RAS} deassertion to \overline{RAS} assertion | t_{RP} | $4.25 \times T_C - 4.0$ | 38.5 | — | ns |
| 163 | \overline{RAS} assertion pulse width | t_{RAS} | $7.75 \times T_C - 4.0$ | 73.5 | — | ns |
| 164 | \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $5.25 \times T_C - 4.0$ | 48.5 | — | ns |
| 165 | \overline{RAS} assertion to \overline{CAS} deassertion | t_{CSH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 166 | \overline{CAS} assertion pulse width | t_{CAS} | $3.75 \times T_C - 4.0$ | 33.5 | — | ns |
| 167 | \overline{RAS} assertion to \overline{CAS} assertion | t_{RCD} | $2.5 \times T_C \pm 4.0$ | 21.0 | 29.0 | ns |
| 168 | \overline{RAS} assertion to column address valid | t_{RAD} | $1.75 \times T_C \pm 4.0$ | 13.5 | 21.5 | ns |
| 169 | \overline{CAS} deassertion to \overline{RAS} assertion | t_{CRP} | $5.75 \times T_C - 4.0$ | 53.5 | — | ns |
| 170 | \overline{CAS} deassertion pulse width | t_{CP} | $4.25 \times T_C - 6.0$ | 36.5 | — | ns |

Table 2-11. DRAM Out-of-Page and Refresh Timings, Eleven Wait States^{1,2} (Continued)

| No. | Characteristics | Symbol | Expression ³ | 100 MHz | | Unit |
|---|--|------------------|--------------------------|---------|------|------|
| | | | | Min | Max | |
| 171 | Row address valid to $\overline{\text{RAS}}$ assertion | t_{ASR} | $4.25 \times T_C - 4.0$ | 38.5 | — | ns |
| 172 | $\overline{\text{RAS}}$ assertion to row address not valid | t_{RAH} | $1.75 \times T_C - 4.0$ | 13.5 | — | ns |
| 173 | Column address valid to $\overline{\text{CAS}}$ assertion | t_{ASC} | $0.75 \times T_C - 4.0$ | 3.5 | — | ns |
| 174 | $\overline{\text{CAS}}$ assertion to column address not valid | t_{CAH} | $5.25 \times T_C - 4.0$ | 48.5 | — | ns |
| 175 | $\overline{\text{RAS}}$ assertion to column address not valid | t_{AR} | $7.75 \times T_C - 4.0$ | 73.5 | — | ns |
| 176 | Column address valid to $\overline{\text{RAS}}$ deassertion | t_{RAL} | $6 \times T_C - 4.0$ | 56.0 | — | ns |
| 177 | $\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion | t_{RCS} | $3.0 \times T_C - 4.0$ | 26.0 | — | ns |
| 178 | $\overline{\text{CAS}}$ deassertion to $\overline{\text{WR}}^4$ assertion | t_{RCH} | $1.75 \times T_C - 3.7$ | 13.8 | — | ns |
| 179 | $\overline{\text{RAS}}$ deassertion to $\overline{\text{WR}}^4$ assertion | t_{RRH} | $0.25 \times T_C - 2.0$ | 0.5 | — | ns |
| 180 | $\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion | t_{WCH} | $5 \times T_C - 4.2$ | 45.8 | — | ns |
| 181 | $\overline{\text{RAS}}$ assertion to $\overline{\text{WR}}$ deassertion | t_{WCR} | $7.5 \times T_C - 4.2$ | 70.8 | — | ns |
| 182 | $\overline{\text{WR}}$ assertion pulse width | t_{WP} | $11.5 \times T_C - 4.5$ | 110.5 | — | ns |
| 183 | $\overline{\text{WR}}$ assertion to $\overline{\text{RAS}}$ deassertion | t_{RWL} | $11.75 \times T_C - 4.3$ | 113.2 | — | ns |
| 184 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ deassertion | t_{CWL} | $10.25 \times T_C - 4.3$ | 98.2 | — | ns |
| 185 | Data valid to $\overline{\text{CAS}}$ assertion (write) | t_{DS} | $5.75 \times T_C - 4.0$ | 53.5 | — | ns |
| 186 | $\overline{\text{CAS}}$ assertion to data not valid (write) | t_{DH} | $5.25 \times T_C - 4.0$ | 48.5 | — | ns |
| 187 | $\overline{\text{RAS}}$ assertion to data not valid (write) | t_{DHR} | $7.75 \times T_C - 4.0$ | 73.5 | — | ns |
| 188 | $\overline{\text{WR}}$ assertion to $\overline{\text{CAS}}$ assertion | t_{WCS} | $6.5 \times T_C - 4.3$ | 60.7 | — | ns |
| 189 | $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ assertion (refresh) | t_{CSR} | $1.5 \times T_C - 4.0$ | 11.0 | — | ns |
| 190 | $\overline{\text{RAS}}$ deassertion to $\overline{\text{CAS}}$ assertion (refresh) | t_{RPC} | $2.75 \times T_C - 4.0$ | 23.5 | — | ns |
| 191 | $\overline{\text{RD}}$ assertion to $\overline{\text{RAS}}$ deassertion | t_{ROH} | $11.5 \times T_C - 4.0$ | 111.0 | — | ns |
| 192 | $\overline{\text{RD}}$ assertion to data valid | t_{GA} | $10 \times T_C - 7.0$ | — | 93.0 | ns |
| 193 | $\overline{\text{RD}}$ deassertion to data not valid ⁵ | t_{GZ} | | 0.0 | — | ns |
| 194 | $\overline{\text{WR}}$ assertion to data active | | $0.75 \times T_C - 1.5$ | 6.0 | — | ns |
| 195 | $\overline{\text{WR}}$ deassertion to data high impedance | | $0.25 \times T_C$ | — | 2.5 | ns |
| Notes: <ol style="list-style-type: none"> 1. The number of wait states for an out-of-page access is specified in the DRAM Control Register. 2. The refresh period is specified in the DRAM Control Register. 3. Use the expression to compute the maximum or minimum value listed (or both if the expression includes \pm). 4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles. 5. $\overline{\text{RD}}$ deassertion always occurs after $\overline{\text{CAS}}$ deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}. | | | | | | |

AC Electrical Characteristics

Table 2-12. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States^{1,2}

| No. | Characteristics | Symbol | Expression ³ | 100 MHz | | Unit |
|-----|--|-----------|--------------------------|---------|-------|------|
| | | | | Min | Max | |
| 157 | Random read or write cycle time | t_{RC} | $16 \times T_C$ | 160.0 | — | ns |
| 158 | \overline{RAS} assertion to data valid (read) | t_{RAC} | $8.25 \times T_C - 5.7$ | — | 76.8 | ns |
| 159 | \overline{CAS} assertion to data valid (read) | t_{CAC} | $4.75 \times T_C - 5.7$ | — | 41.8 | ns |
| 160 | Column address valid to data valid (read) | t_{AA} | $5.5 \times T_C - 5.7$ | — | 49.3 | ns |
| 161 | \overline{CAS} deassertion to data not valid (read hold time) | t_{OFF} | 0.0 | 0.0 | — | ns |
| 162 | \overline{RAS} deassertion to \overline{RAS} assertion | t_{RP} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 163 | \overline{RAS} assertion pulse width | t_{RAS} | $9.75 \times T_C - 4.0$ | 93.5 | — | ns |
| 164 | \overline{CAS} assertion to \overline{RAS} deassertion | t_{RSH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 165 | \overline{RAS} assertion to \overline{CAS} deassertion | t_{CSH} | $8.25 \times T_C - 4.0$ | 78.5 | — | ns |
| 166 | \overline{CAS} assertion pulse width | t_{CAS} | $4.75 \times T_C - 4.0$ | 43.5 | — | ns |
| 167 | \overline{RAS} assertion to \overline{CAS} assertion | t_{RCD} | $3.5 \times T_C \pm 2$ | 33.0 | 37.0 | ns |
| 168 | \overline{RAS} assertion to column address valid | t_{RAD} | $2.75 \times T_C \pm 2$ | 25.5 | 29.5 | ns |
| 169 | \overline{CAS} deassertion to \overline{RAS} assertion | t_{CRP} | $7.75 \times T_C - 4.0$ | 73.5 | — | ns |
| 170 | \overline{CAS} deassertion pulse width | t_{CP} | $6.25 \times T_C - 6.0$ | 56.5 | — | ns |
| 171 | Row address valid to \overline{RAS} assertion | t_{ASR} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 172 | \overline{RAS} assertion to row address not valid | t_{RAH} | $2.75 \times T_C - 4.0$ | 23.5 | — | ns |
| 173 | Column address valid to \overline{CAS} assertion | t_{ASC} | $0.75 \times T_C - 4.0$ | 3.5 | — | ns |
| 174 | \overline{CAS} assertion to column address not valid | t_{CAH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 175 | \overline{RAS} assertion to column address not valid | t_{AR} | $9.75 \times T_C - 4.0$ | 93.5 | — | ns |
| 176 | Column address valid to \overline{RAS} deassertion | t_{RAL} | $7 \times T_C - 4.0$ | 66.0 | — | ns |
| 177 | \overline{WR} deassertion to \overline{CAS} assertion | t_{RCS} | $5 \times T_C - 3.8$ | 46.2 | — | ns |
| 178 | \overline{CAS} deassertion to \overline{WR}^4 assertion | t_{RCH} | $1.75 \times T_C - 3.7$ | 13.8 | — | ns |
| 179 | \overline{RAS} deassertion to \overline{WR}^4 assertion | t_{RRH} | $0.25 \times T_C - 2.0$ | 0.5 | — | ns |
| 180 | \overline{CAS} assertion to \overline{WR} deassertion | t_{WCH} | $6 \times T_C - 4.2$ | 55.8 | — | ns |
| 181 | \overline{RAS} assertion to \overline{WR} deassertion | t_{WCR} | $9.5 \times T_C - 4.2$ | 90.8 | — | ns |
| 182 | \overline{WR} assertion pulse width | t_{WP} | $15.5 \times T_C - 4.5$ | 150.5 | — | ns |
| 183 | \overline{WR} assertion to \overline{RAS} deassertion | t_{RWL} | $15.75 \times T_C - 4.3$ | 153.2 | — | ns |
| 184 | \overline{WR} assertion to \overline{CAS} deassertion | t_{CWL} | $14.25 \times T_C - 4.3$ | 138.2 | — | ns |
| 185 | Data valid to \overline{CAS} assertion (write) | t_{DS} | $8.75 \times T_C - 4.0$ | 83.5 | — | ns |
| 186 | \overline{CAS} assertion to data not valid (write) | t_{DH} | $6.25 \times T_C - 4.0$ | 58.5 | — | ns |
| 187 | \overline{RAS} assertion to data not valid (write) | t_{DHR} | $9.75 \times T_C - 4.0$ | 93.5 | — | ns |
| 188 | \overline{WR} assertion to \overline{CAS} assertion | t_{WCS} | $9.5 \times T_C - 4.3$ | 90.7 | — | ns |
| 189 | \overline{CAS} assertion to \overline{RAS} assertion (refresh) | t_{CSR} | $1.5 \times T_C - 4.0$ | 11.0 | — | ns |
| 190 | \overline{RAS} deassertion to \overline{CAS} assertion (refresh) | t_{RPC} | $4.75 \times T_C - 4.0$ | 43.5 | — | ns |
| 191 | \overline{RD} assertion to \overline{RAS} deassertion | t_{ROH} | $15.5 \times T_C - 4.0$ | 151.0 | — | ns |
| 192 | \overline{RD} assertion to data valid | t_{GA} | $14 \times T_C - 5.7$ | — | 134.3 | ns |
| 193 | \overline{RD} deassertion to data not valid ⁵ | t_{GZ} | | 0.0 | — | ns |
| 194 | \overline{WR} assertion to data active | | $0.75 \times T_C - 1.5$ | 6.0 | — | ns |
| 195 | \overline{WR} deassertion to data high impedance | | $0.25 \times T_C$ | — | 2.5 | ns |

Table 2-12. DRAM Out-of-Page and Refresh Timings, Fifteen Wait States^{1,2} (Continued)

| No. | Characteristics | Symbol | Expression ³ | 100 MHz | | Unit |
|---|-----------------|--------|-------------------------|---------|-----|------|
| | | | | Min | Max | |
| Notes: <ol style="list-style-type: none"> 1. The number of wait states for an out-of-page access is specified in the DRAM Control Register. 2. The refresh period is specified in the DRAM Control Register. 3. Use the expression to compute the maximum or minimum value listed (or both if the expression includes \pm). 4. Either t_{RCH} or t_{RRH} must be satisfied for read cycles. 5. \overline{RD} deassertion always occurs after \overline{CAS} deassertion; therefore, the restricted timing is t_{OFF} and not t_{GZ}. | | | | | | |

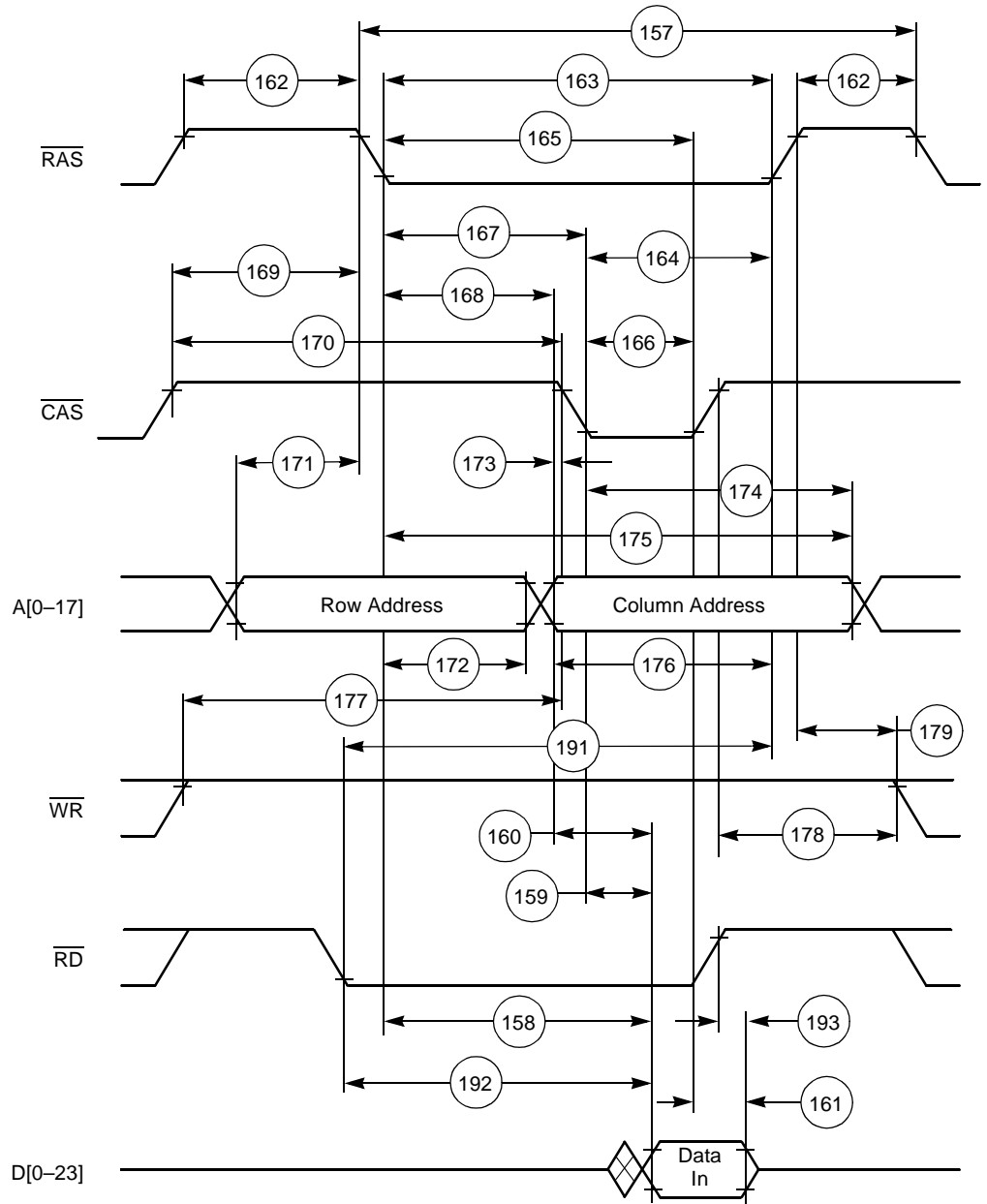


Figure 2-18. DRAM Out-of-Page Read Access

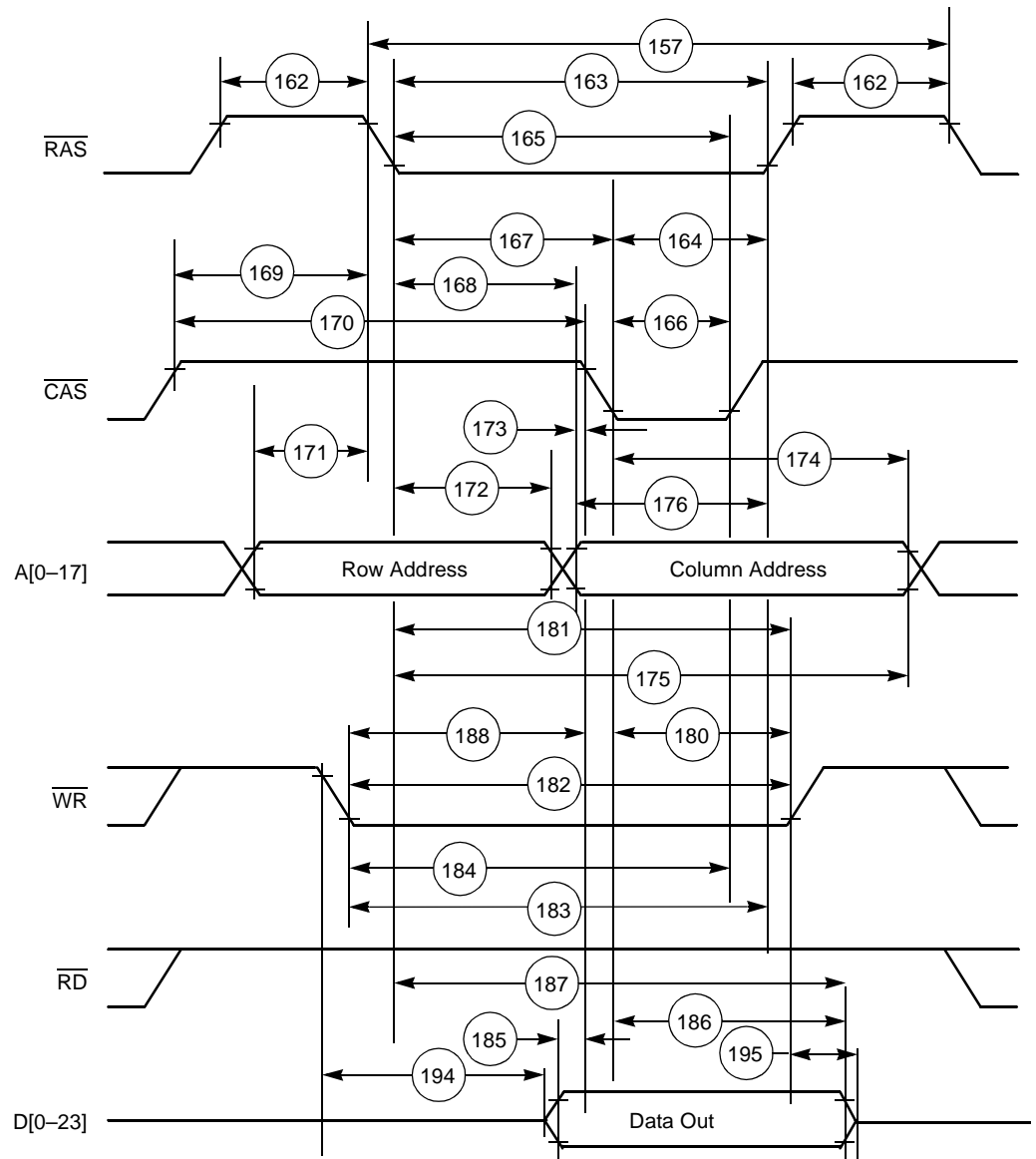


Figure 2-19. DRAM Out-of-Page Write Access

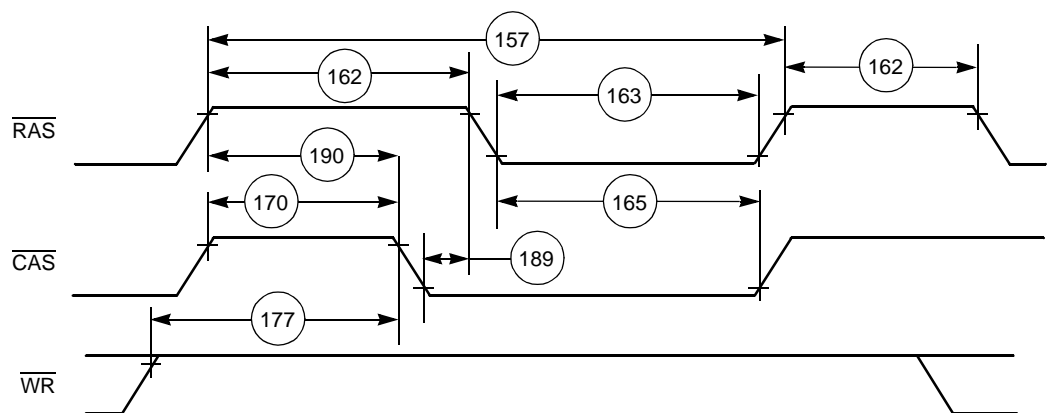


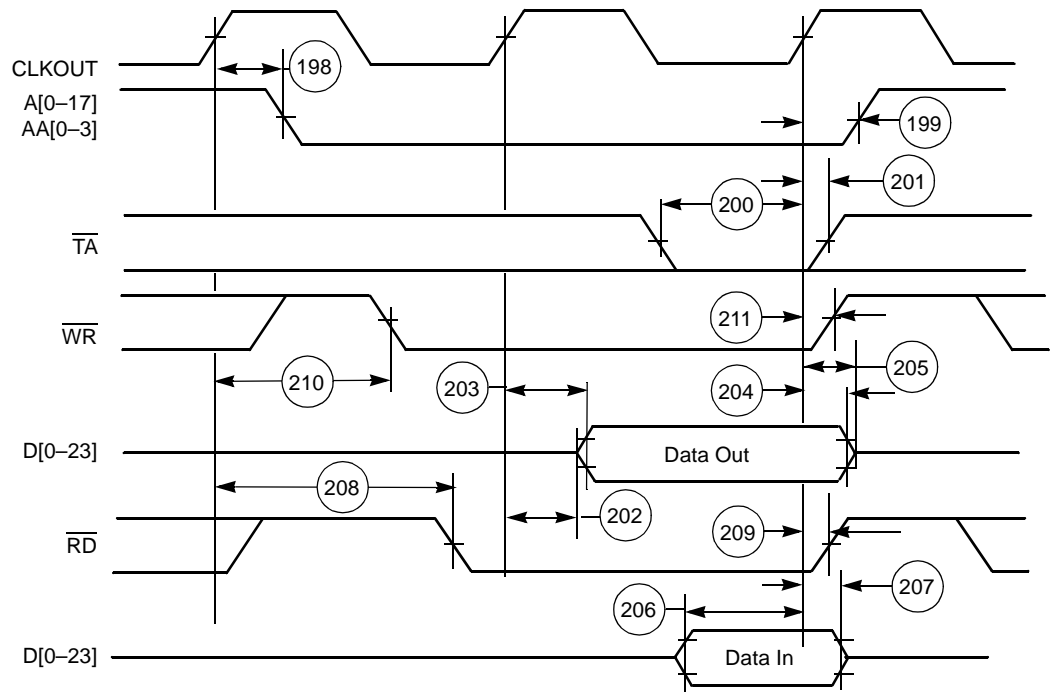
Figure 2-20. DRAM Refresh Access

2.6.5.3 Synchronous Timings

Table 2-13. External Bus Synchronous Timings^{1,2}

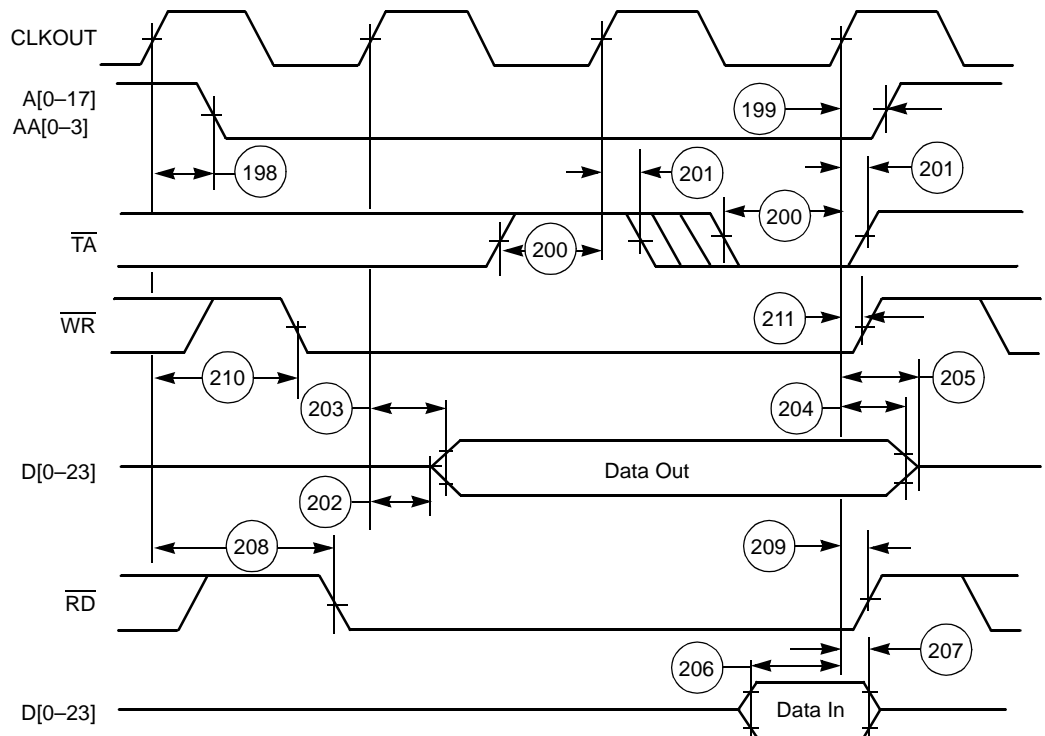
| No. | Characteristics | Expression ^{3,4,5} | 100 MHz | | Unit |
|---|---|--|---------|------|------|
| | | | Min | Max | |
| 198 | CLKOUT high to address, and AA valid ⁶ | $0.25 \times T_C + 4.0$ | — | 6.5 | ns |
| 199 | CLKOUT high to address, and AA invalid ⁶ | $0.25 \times T_C$ | 2.5 | — | ns |
| 200 | \overline{TA} valid to CLKOUT high (set-up time) | | 4.0 | — | ns |
| 201 | CLKOUT high to \overline{TA} invalid (hold time) | | 0.0 | — | ns |
| 202 | CLKOUT high to data out active | $0.25 \times T_C$ | 2.5 | — | ns |
| 203 | CLKOUT high to data out valid | $0.25 \times T_C + 4.0$ | — | 6.5 | ns |
| 204 | CLKOUT high to data out invalid | $0.25 \times T_C$ | 2.5 | — | ns |
| 205 | CLKOUT high to data out high impedance | $0.25 \times T_C$ | — | 2.5 | ns |
| 206 | Data in valid to CLKOUT high (set-up) | | 4.0 | — | ns |
| 207 | CLKOUT high to data in invalid (hold) | | 0.0 | — | ns |
| 208 | CLKOUT high to \overline{RD} assertion | maximum: $0.75 \times T_C + 2.5$ | 6.7 | 10.0 | ns |
| 209 | CLKOUT high to \overline{RD} deassertion | | 0.0 | 4.0 | ns |
| 210 | CLKOUT high to \overline{WR} assertion ² | maximum: $0.5 \times T_C + 4.3$ for $WS = 1$ or $WS \geq 4$ for $2 \leq WS \leq 3$ | 5.0 | 9.3 | ns |
| | | | 0.0 | 4.3 | ns |
| 211 | CLKOUT high to \overline{WR} deassertion | | 0.0 | 3.8 | ns |
| Notes: <ol style="list-style-type: none"> 1. Use external bus synchronous timings only for reference to the clock and <i>not</i> for relative timings. 2. Synchronous Bus Arbitration is not recommended. Use Asynchronous mode whenever possible. 3. WS is the number of wait states specified in the BCR. 4. If $WS > 1$, \overline{WR} assertion refers to the next rising edge of CLKOUT. 5. Use the expression to compute the maximum or minimum value listed, as appropriate. For timing 210, the minimum is an absolute value. 6. T198 and T199 are valid for Address Trace mode if the ATE bit in the Operating Mode Register is set. when this mode is enabled, use the status of BR (See T212) to determine whether the access referenced by A[0–17] is internal or external. | | | | | |

AC Electrical Characteristics



Note: Address lines A[0-17] hold their state after a read or write operation. AA[0-3] do not hold their state after a read or write operation.

Figure 2-21. Synchronous Bus Timings 1 WS (BCR Controlled)



Note: Address lines A[0-17] hold their state after a read or write operation. AA[0-3] do not hold their state after a read or write operation.

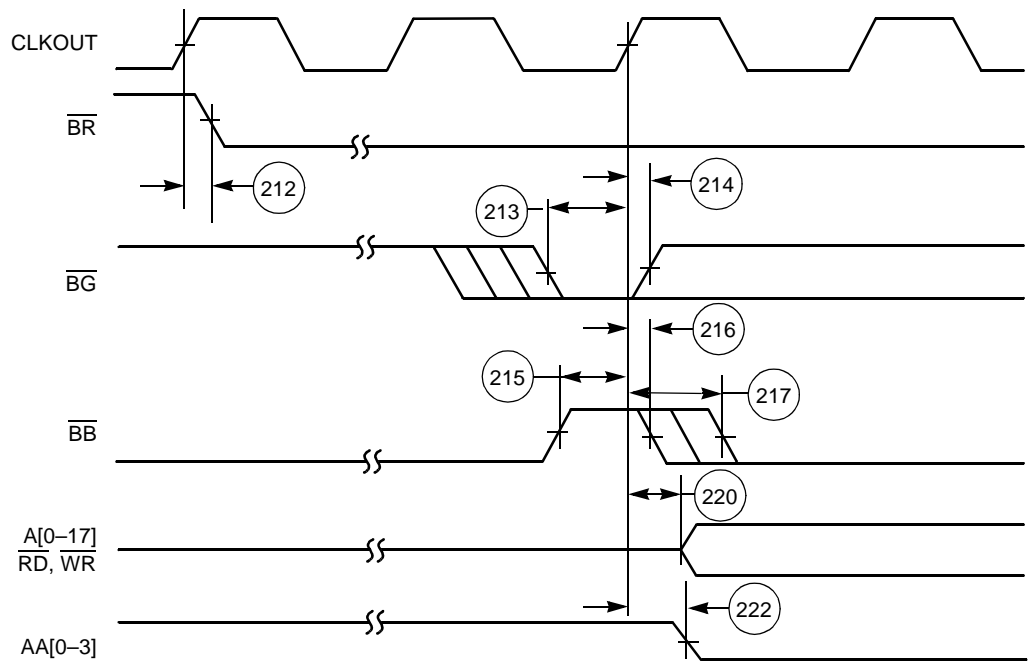
Figure 2-22. Synchronous Bus Timings 2 WS (\overline{TA} Controlled)

2.6.5.4 Arbitration Timings

Table 2-14. Arbitration Bus Timings¹

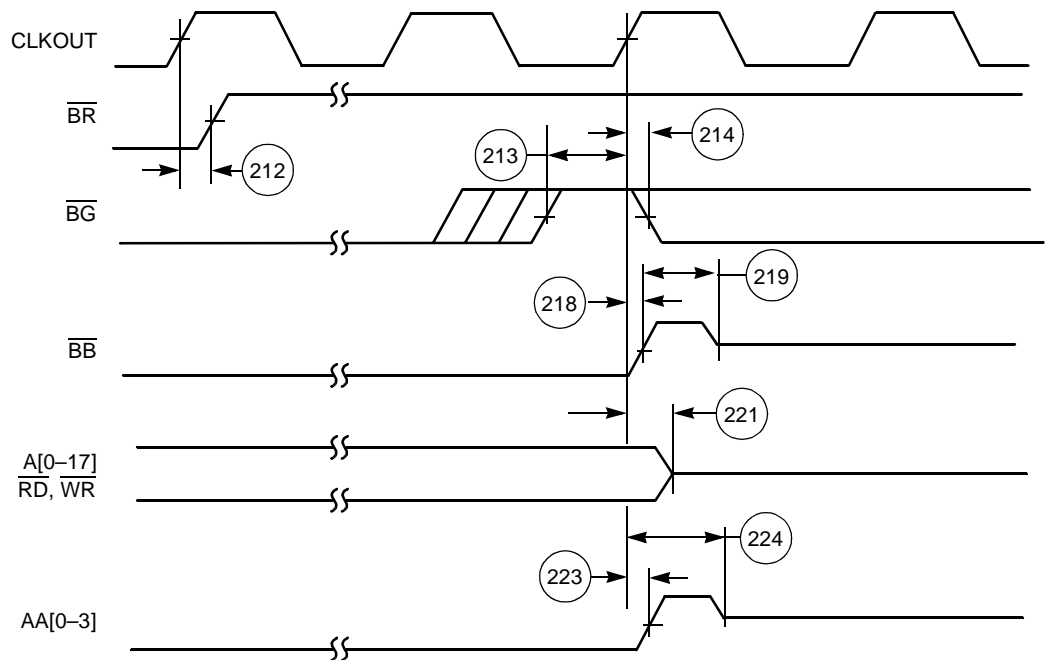
| No. | Characteristics | Expression ² | 100 MHz | | Unit |
|---|---|----------------------------------|---------|-----|------|
| | | | Min | Max | |
| 212 | CLKOUT high to \overline{BR} assertion/deassertion ³ | | 0.0 | 4.0 | ns |
| 213 | \overline{BG} asserted/deasserted to CLKOUT high (setup) | | 4.0 | — | ns |
| 214 | CLKOUT high to \overline{BG} deasserted/asserted (hold) | | 0.0 | — | ns |
| 215 | \overline{BB} deassertion to CLKOUT high (input set-up) | | 4.0 | — | ns |
| 216 | CLKOUT high to \overline{BB} assertion (input hold) | | 0.0 | — | ns |
| 217 | CLKOUT high to \overline{BB} assertion (output) | | 0.0 | 4.0 | ns |
| 218 | CLKOUT high to \overline{BB} deassertion (output) | | 0.0 | 4.0 | ns |
| 219 | \overline{BB} high to \overline{BB} high impedance (output) | | — | 4.5 | ns |
| 220 | CLKOUT high to address and controls active | $0.25 \times T_C$ | 2.5 | — | ns |
| 221 | CLKOUT high to address and controls high impedance | $0.75 \times T_C$ | — | 7.5 | ns |
| 222 | CLKOUT high to AA active | $0.25 \times T_C$ | 2.5 | — | ns |
| 223 | CLKOUT high to AA deassertion | maximum: $0.25 \times T_C + 4.0$ | 2.0 | 6.5 | ns |
| 224 | CLKOUT high to AA high impedance | $0.75 \times T_C$ | — | 7.5 | ns |
| Notes: <ol style="list-style-type: none"> 1. Synchronous Bus Arbitration is not recommended. Use Asynchronous mode whenever possible. 2. An expression is used to compute the maximum or minimum value listed, as appropriate. For timing 223, the minimum is an absolute value. 3. T212 is valid for Address Trace mode when the ATE bit in the Operating Mode Register is set. \overline{BR} is deasserted for internal accesses and asserted for external accesses. | | | | | |

AC Electrical Characteristics



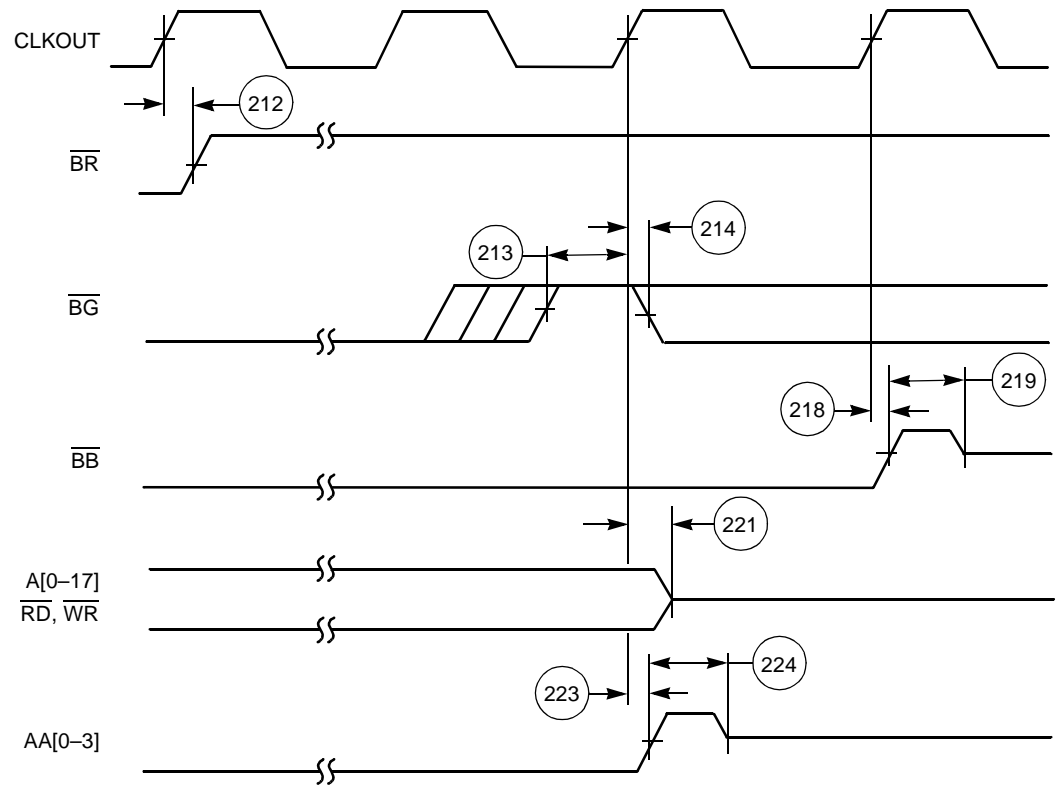
Note: Address lines $\text{A}[0-17]$ hold their state after a read or write operation. $\text{AA}[0-3]$ do not hold their state after a read or write operation.

Figure 2-23. Bus Acquisition Timings



Note: Address lines $\text{A}[0-17]$ hold their state after a read or write operation. $\text{AA}[0-3]$ do not hold their state after a read or write operation.

Figure 2-24. Bus Release Timings Case 1 (BRT Bit in Operating Mode Register Cleared)



Note: Address lines A[0-17] hold their state after a read or write operation. AA[0-3] do not hold their state after a read or write operation.

Figure 2-25. Bus Release Timings Case 2 (BRT Bit in Operating Mode Register Set)

2.6.5.5 Asynchronous Bus Arbitration Timings

Table 2-15. Asynchronous Bus Timings^{1, 2}

| No. | Characteristics | Expression ³ | 100 MHz ⁴ | | Unit |
|-----|--|-------------------------|----------------------|-----|------|
| | | | Min | Max | |
| 250 | $\overline{\text{BB}}$ assertion window from $\overline{\text{BG}}$ input deassertion ⁵ | $2.5 \times T_c + 5$ | — | 30 | ns |
| 251 | Delay from $\overline{\text{BB}}$ assertion to $\overline{\text{BG}}$ assertion ⁵ | $2 \times T_c + 5$ | 25 | — | ns |

Notes:

1. Bit 13 in the Operating Mode Register must be set to enter Asynchronous Arbitration mode.
2. If Asynchronous Arbitration mode is active, none of the timings in **Table 2-14** is required.
3. An expression is used to compute the maximum or minimum value listed, as appropriate.
4. Asynchronous Arbitration mode is recommended for operation at 100 MHz.
5. In order to guarantee timings 250, and 251, BG inputs must be asserted to different DSP56300 devices on the same bus in the non-overlap manner shown in **Figure 2-26**.

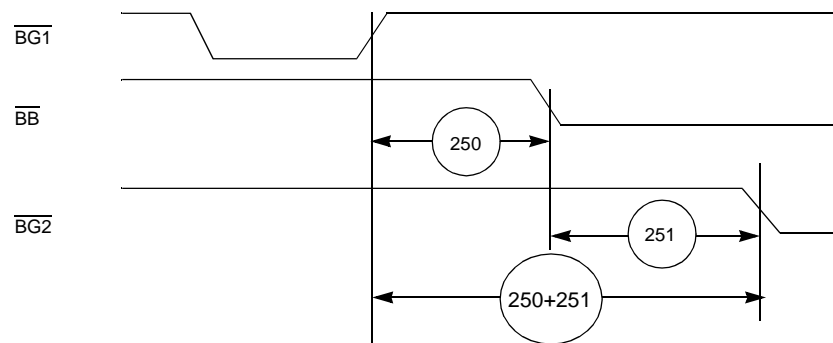


Figure 2-26. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{\text{BG}}$ and $\overline{\text{BB}}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{\text{BB}}$, for some time after $\overline{\text{BG}}$ is deasserted. This is the reason for timing 250.

Once $\overline{\text{BB}}$ is asserted, there is a synchronization delay from $\overline{\text{BB}}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{\text{BG}}$ input is asserted before that time, and $\overline{\text{BG}}$ is asserted and $\overline{\text{BB}}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{\text{BG}}$ input active to another $\overline{\text{BG}}$ input active is required. Timing 251 ensures that overlaps are avoided.

2.6.6 Host Interface Timing

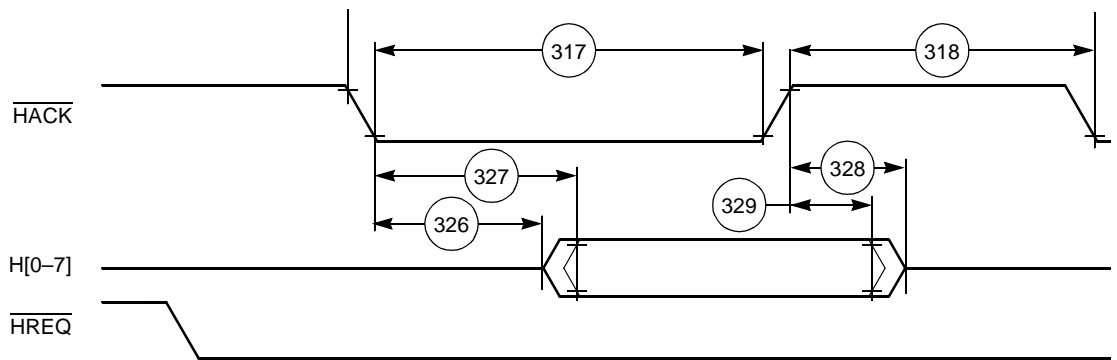
Table 2-16. Host Interface Timings^{1,2,12}

| No. | Characteristic ¹⁰ | Expression | 100 MHz | | Unit |
|-----|--|------------------------|--------------|--------|----------|
| | | | Min | Max | |
| 317 | Read data strobe assertion width ⁵ HACK assertion width | $T_C + 9.9$ | 19.9 | — | ns |
| 318 | Read data strobe deassertion width ⁵ HACK deassertion width | | 9.9 | — | ns |
| 319 | Read data strobe deassertion width ⁵ after “Last Data Register” reads ^{8,11} , or between two consecutive CVR, ICR, or ISR reads ³ HACK deassertion width after “Last Data Register” reads ^{8,11} | $2.5 \times T_C + 6.6$ | 31.6 | — | ns |
| 320 | Write data strobe assertion width ⁶ | | 13.2 | — | ns |
| 321 | Write data strobe deassertion width ⁸ HACK write deassertion width <ul style="list-style-type: none"> • after ICR, CVR and “Last Data Register” writes • after IVR writes, or after TXH:TXM:TXL writes (with HLEND= 0), or after TXL:TXM:TXH writes (with HLEND = 1) | $2.5 \times T_C + 6.6$ | 31.8 16.5 | — — | ns ns |
| 322 | \overline{HAS} assertion width | | 9.9 | — | ns |
| 323 | \overline{HAS} deassertion to data strobe assertion ⁴ | | 0.0 | — | ns |
| 324 | Host data input setup time before write data strobe deassertion ⁶ | | 9.9 | — | ns |
| 325 | Host data input hold time after write data strobe deassertion ⁶ | | 3.3 | — | ns |
| 326 | Read data strobe assertion to output data active from high impedance ⁵ HACK assertion to output data active from high impedance | | 3.3 | — | ns |
| 327 | Read data strobe assertion to output data valid ⁵ HACK assertion to output data valid | | — | 24.5 | ns |
| 328 | Read data strobe deassertion to output data high impedance ⁵ HACK deassertion to output data high impedance | | — | 9.9 | ns |
| 329 | Output data hold time after read data strobe deassertion ⁵ Output data hold time after HACK deassertion | | 3.3 | — | ns |
| 330 | \overline{HCS} assertion to read data strobe deassertion ⁵ | $T_C + 9.9$ | 19.9 | — | ns |
| 331 | \overline{HCS} assertion to write data strobe deassertion ⁶ | | 9.9 | — | ns |
| 332 | \overline{HCS} assertion to output data valid | | — | 19.3 | ns |
| 333 | \overline{HCS} hold time after data strobe deassertion ⁴ | | 0.0 | — | ns |
| 334 | Address (HAD[0–7]) setup time before \overline{HAS} deassertion (HMUX=1) | | 4.6 | — | ns |
| 335 | Address (HAD[0–7]) hold time after \overline{HAS} deassertion (HMUX=1) | | 3.3 | — | ns |
| 336 | HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), $\overline{HR/\overline{W}}$ setup time before data strobe assertion ⁴ <ul style="list-style-type: none"> • Read • Write | | 0 4.6 | — — | ns ns |
| 337 | HA[8–10] (HMUX=1), HA[0–2] (HMUX=0), $\overline{HR/\overline{W}}$ hold time after data strobe deassertion ⁴ | | 3.3 | — | ns |

Table 2-16. Host Interface Timings^{1,2,12} (Continued)

| No. | Characteristic ¹⁰ | Expression | 100 MHz | | Unit |
|-----|---|------------------------|---------|-------|------|
| | | | Min | Max | |
| 338 | Delay from read data strobe deassertion to host request assertion for "Last Data Register" read ^{5, 7, 8} | $T_C + 5.3$ | 15.3 | — | ns |
| 339 | Delay from write data strobe deassertion to host request assertion for "Last Data Register" write ^{6, 7, 8} | $1.5 \times T_C + 5.3$ | 20.3 | — | ns |
| 340 | Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=0) ^{4, 7, 8} | | — | 19.3 | ns |
| 341 | Delay from data strobe assertion to host request deassertion for "Last Data Register" read or write (HROD=1, open drain host request) ^{4, 7, 8, 9} | | — | 300.0 | ns |

- Notes:**
1. See the Programmer's Model section in the chapter on the HI08 in the *DSP56303 User's Manual*.
 2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
 3. This timing is applicable only if two consecutive reads from one of these registers are executed.
 4. The data strobe is Host Read (HRD) or Host Write (HWR) in the Dual Data Strobe mode and Host Data Strobe (HDS) in the Single Data Strobe mode.
 5. The read data strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
 6. The write data strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
 7. The host request is HREQ in the Single Host Request mode and HRRQ and HTRQ in the Double Host Request mode.
 8. The "Last Data Register" is the register at address \$7, which is the last location to be read or written in data transfers. This is RXL/TXL in the Big Endian mode (HLEND = 0; HLEND is the Interface Control Register bit 7—ICR[7]), or RXH/TXH in the Little Endian mode (HLEND = 1).
 9. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open-drain mode.
 10. $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$
 11. This timing is applicable only if a read from the "Last Data Register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ signal.
 12. After the external host writes a new value to the ICR, the HI08 is ready for operation after three DSP clock cycles ($3 \times T_C$).



Note: The IVR is only read by an MC680xx host processor using non-multiplexed mode.

Figure 2-27. Host Interrupt Vector Register (IVR) Read Timing Diagram

Figure 2-28. Read Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

Figure 2-29. Read Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

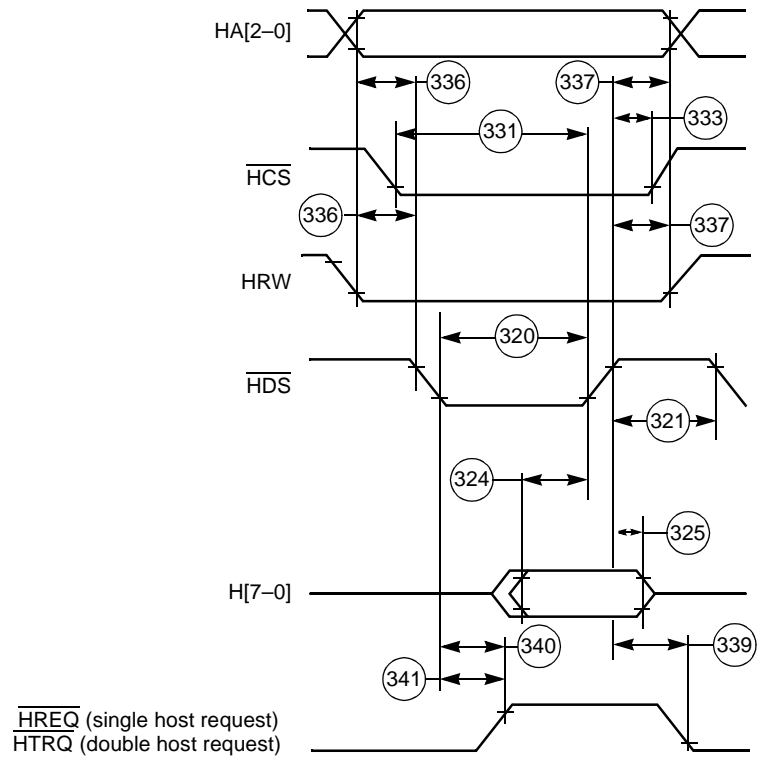


Figure 2-30. Write Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

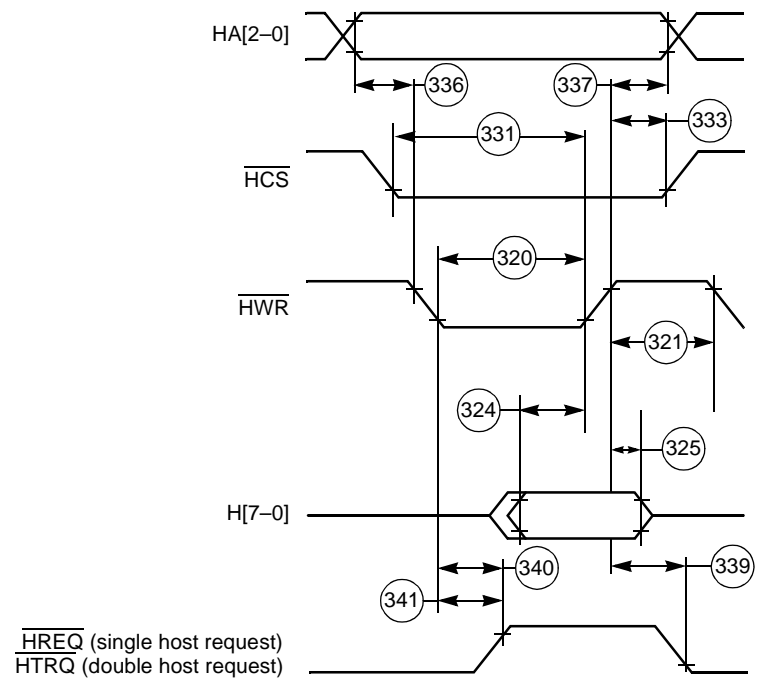


Figure 2-31. Write Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

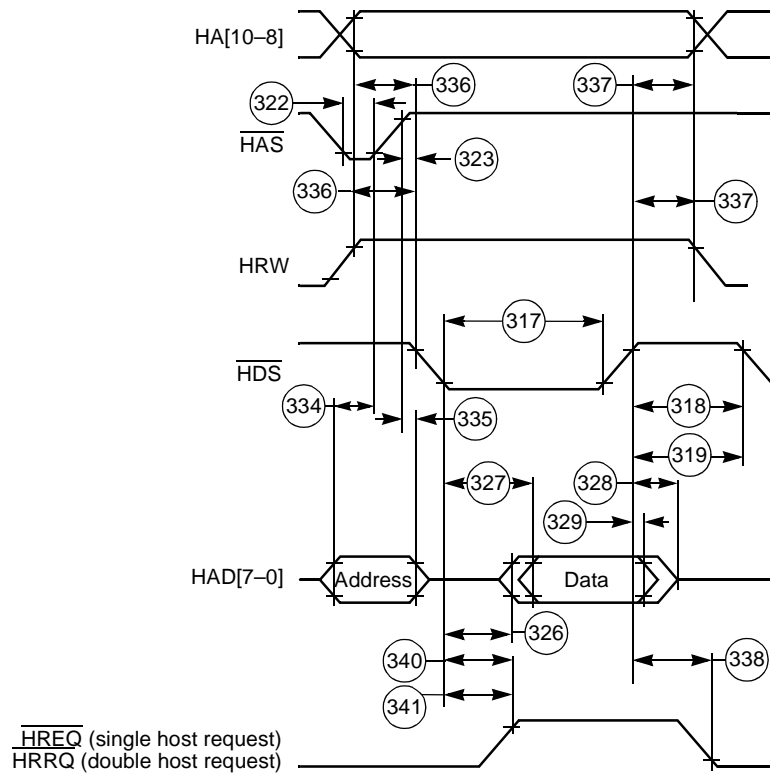


Figure 2-32. Read Timing Diagram, Multiplexed Bus, Single Data Strobe

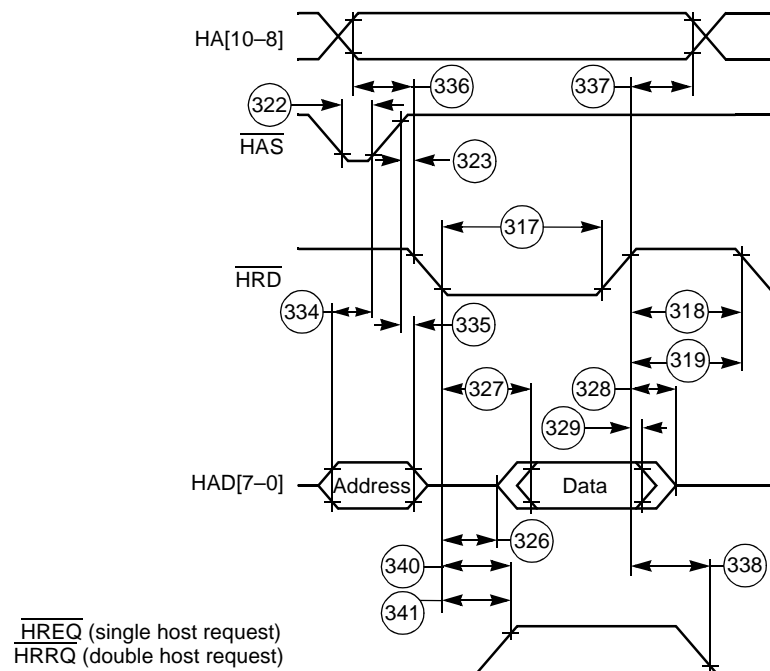


Figure 2-33. Read Timing Diagram, Multiplexed Bus, Double Data Strobe

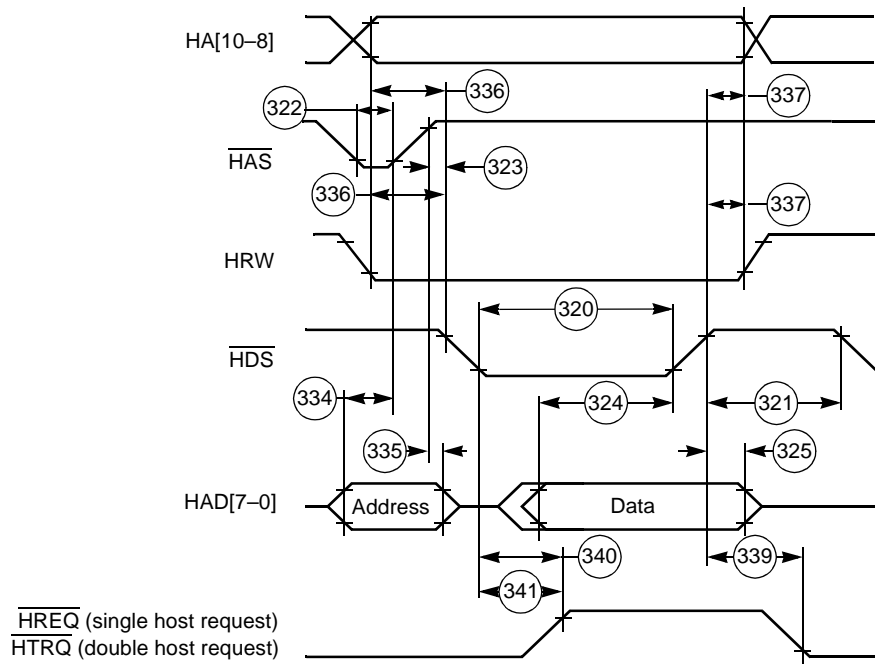


Figure 2-34. Write Timing Diagram, Multiplexed Bus, Single Data Strobe

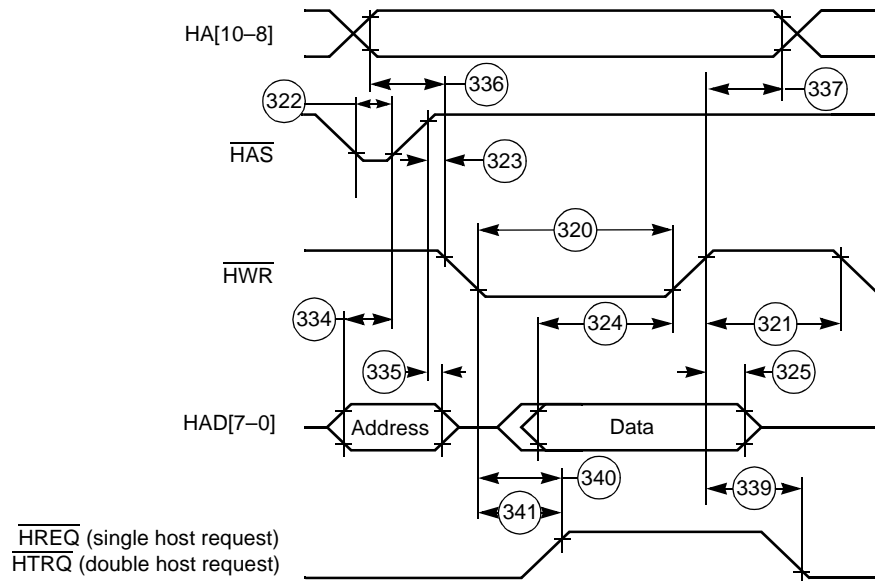
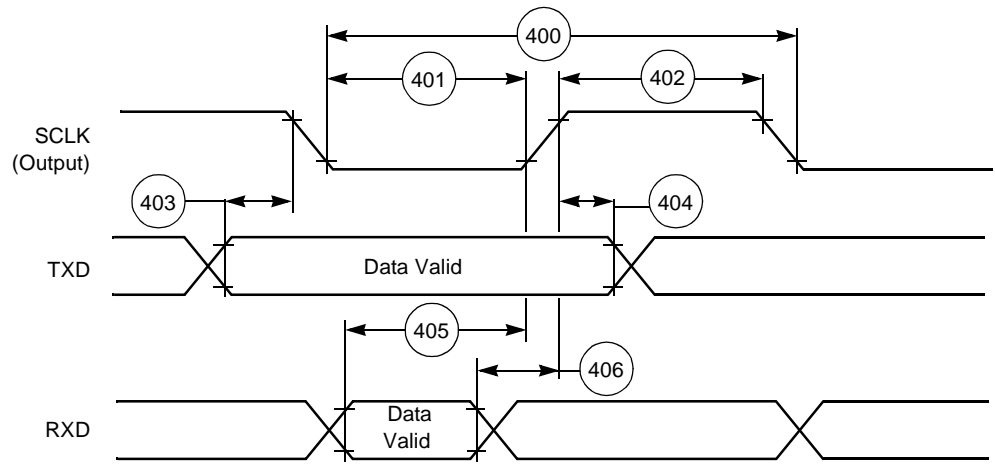


Figure 2-35. Write Timing Diagram, Multiplexed Bus, Double Data Strobe

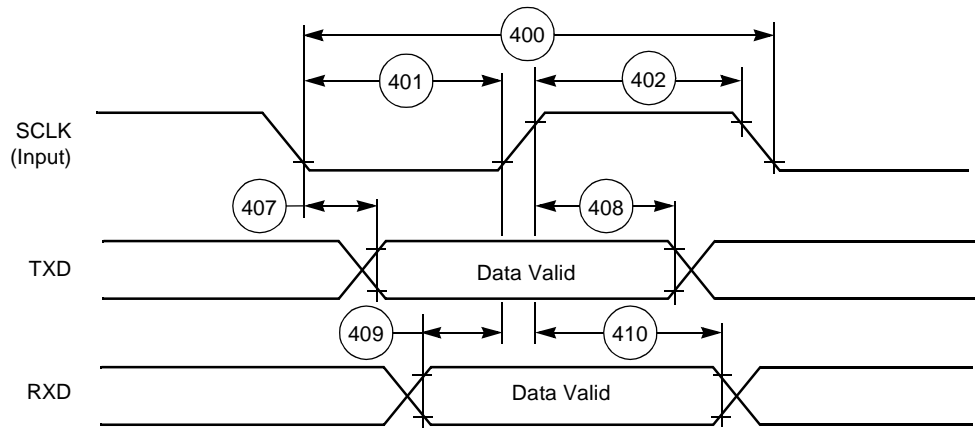
2.6.7 SCI Timing

Table 2-17. SCI Timings

| No. | Characteristics ¹ | Symbol | Expression | 100 MHz | | Unit |
|---|---|-------------|-------------------------------------|---------|------|------|
| | | | | Min | Max | |
| 400 | Synchronous clock cycle | t_{SCC}^2 | $8 \times T_C$ | 53.3 | — | ns |
| 401 | Clock low period | | $t_{SCC}/2 - 10.0$ | 16.7 | — | ns |
| 402 | Clock high period | | $t_{SCC}/2 - 10.0$ | 16.7 | — | ns |
| 403 | Output data setup to clock falling edge (internal clock) | | $t_{SCC}/4 + 0.5 \times T_C - 17.0$ | 8.0 | — | ns |
| 404 | Output data hold after clock rising edge (internal clock) | | $t_{SCC}/4 - 0.5 \times T_C$ | 15.0 | — | ns |
| 405 | Input data setup time before clock rising edge (internal clock) | | $t_{SCC}/4 + 0.5 \times T_C + 25.0$ | 50.0 | — | ns |
| 406 | Input data not valid before clock rising edge (internal clock) | | $t_{SCC}/4 + 0.5 \times T_C - 5.5$ | — | 19.5 | ns |
| 407 | Clock falling edge to output data valid (external clock) | | | — | 32.0 | ns |
| 408 | Output data hold after clock rising edge (external clock) | | $T_C + 8.0$ | 18.0 | — | ns |
| 409 | Input data setup time before clock rising edge (external clock) | | | 0.0 | — | ns |
| 410 | Input data hold time after clock rising edge (external clock) | | | 9.0 | — | ns |
| 411 | Asynchronous clock cycle | t_{ACC}^3 | $64 \times T_C$ | 640.0 | — | ns |
| 412 | Clock low period | | $t_{ACC}/2 - 10.0$ | 310.0 | — | ns |
| 413 | Clock high period | | $t_{ACC}/2 - 10.0$ | 310.0 | — | ns |
| 414 | Output data setup to clock rising edge (internal clock) | | $t_{ACC}/2 - 30.0$ | 290.0 | — | ns |
| 415 | Output data hold after clock rising edge (internal clock) | | $t_{ACC}/2 - 30.0$ | 290.0 | — | ns |
| Notes: <ol style="list-style-type: none"> $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$. t_{SCC} = synchronous clock cycle time (for internal clock, t_{SCC} is determined by the SCI clock control register and T_C). t_{ACC} = asynchronous clock cycle time; value given for 1X Clock mode (for internal clock, t_{ACC} is determined by the SCI clock control register and T_C). An expression is used to compute the number listed as the minimum or maximum value as appropriate. | | | | | | |



a) Internal Clock



b) External Clock

Figure 2-36. SCI Synchronous Mode Timing

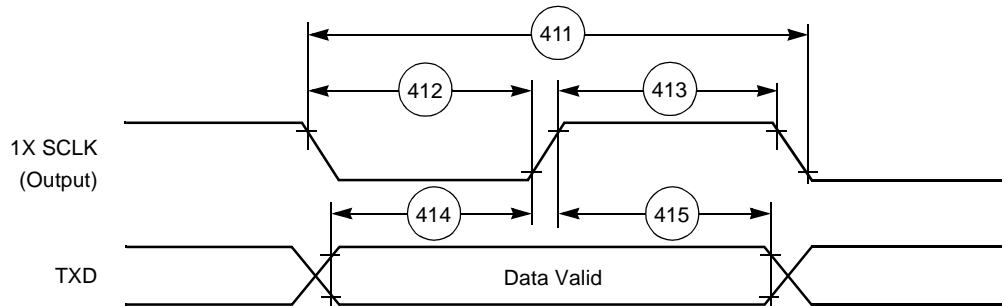


Figure 2-37. SCI Asynchronous Mode Timing

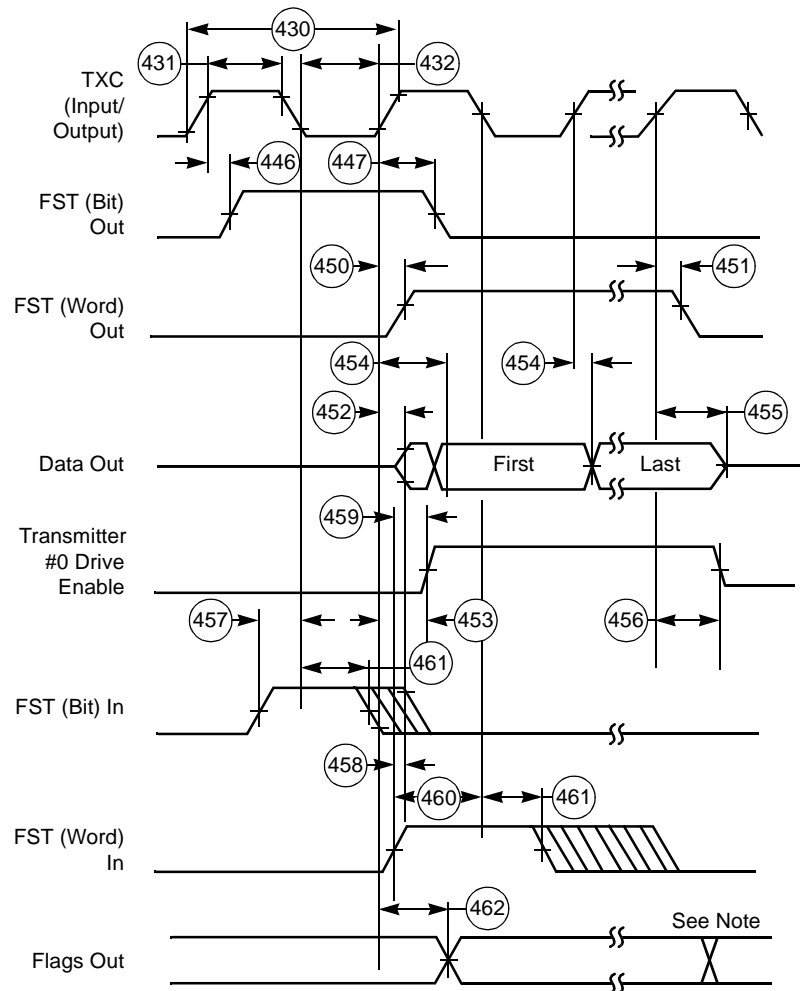
2.6.8 ESSI0/ESSI1 Timing

Table 2-18. ESSI Timings

| No. | Characteristics ^{4, 5, 7} | Symbol | Expression ⁹ | 100 MHz | | Condition ⁵ | Unit |
|-----|--|-------------|---|--------------|--------------|------------------------|----------|
| | | | | Min | Max | | |
| 430 | Clock cycle ¹ | t_{SSICC} | $3 \times T_C$ $4 \times T_C$ | 30.0 40.0 | — — | x ck i ck | ns |
| 431 | Clock high period • For internal clock • For external clock | | $2 \times T_C - 10.0$ $1.5 \times T_C$ | 10.0 15.0 | — — | | ns ns |
| 432 | Clock low period • For internal clock • For external clock | | $2 \times T_C - 10.0$ $1.5 \times T_C$ | 10.0 15.0 | — — | | ns ns |
| 433 | RXC rising edge to FSR out (bit-length) high | | | — — | 37.0 22.0 | x ck i ck a | ns |
| 434 | RXC rising edge to FSR out (bit-length) low | | | — — | 37.0 22.0 | x ck i ck a | ns |
| 435 | RXC rising edge to FSR out (word-length-relative) high ² | | | — — | 39.0 37.0 | x ck i ck a | ns |
| 436 | RXC rising edge to FSR out (word-length-relative) low ² | | | — — | 39.0 37.0 | x ck i ck a | ns |
| 437 | RXC rising edge to FSR out (word-length) high | | | — — | 36.0 21.0 | x ck i ck a | ns |
| 438 | RXC rising edge to FSR out (word-length) low | | | — — | 37.0 22.0 | x ck i ck a | ns |
| 439 | Data in setup time before RXC (SCK in Synchronous mode) falling edge | | | 10.0 19.0 | — — | x ck i ck | ns |
| 440 | Data in hold time after RXC falling edge | | | 5.0 3.0 | — — | x ck i ck | ns |
| 441 | FSR input (bl, wr) high before RXC falling edge ² | | | 1.0 23.0 | — — | x ck i ck a | ns |
| 442 | FSR input (wl) high before RXC falling edge | | | 3.5 23.0 | — — | x ck i ck a | ns |
| 443 | FSR input hold time after RXC falling edge | | | 3.0 0.0 | — — | x ck i ck a | ns |
| 444 | Flags input setup before RXC falling edge | | | 5.5 19.0 | — — | x ck i ck s | ns |
| 445 | Flags input hold time after RXC falling edge | | | 6.0 0.0 | — — | x ck i ck s | ns |
| 446 | TXC rising edge to FST out (bit-length) high | | | — — | 29.0 15.0 | x ck i ck | ns |
| 447 | TXC rising edge to FST out (bit-length) low | | | — — | 31.0 17.0 | x ck i ck | ns |
| 448 | TXC rising edge to FST out (word-length-relative) high ² | | | — — | 31.0 17.0 | x ck i ck | ns |
| 449 | TXC rising edge to FST out (word-length-relative) low ² | | | — — | 33.0 19.0 | x ck i ck | ns |

Table 2-18. ESSI Timings (Continued)

| No. | Characteristics ^{4, 5, 7} | Symbol | Expression ⁹ | 100 MHz | | Condition ⁵ | Unit |
|---|---|--------|-------------------------|-------------|---------------------------|------------------------|------|
| | | | | Min | Max | | |
| 450 | TXC rising edge to FST out (word-length) high | | | — — | 30.0 16.0 | x ck i ck | ns |
| 451 | TXC rising edge to FST out (word-length) low | | | — — | 31.0 17.0 | x ck i ck | ns |
| 452 | TXC rising edge to data out enable from high impedance | | | — — | 31.0 17.0 | x ck i ck | ns |
| 453 | TXC rising edge to Transmitter #0 drive enable assertion | | | — — | 34.0 20.0 | x ck i ck | ns |
| 454 | TXC rising edge to data out valid | | | — — | 20.0 ⁸ 10.0 | x ck i ck | ns |
| 455 | TXC rising edge to data out high impedance ³ | | | — — | 31.0 16.0 | x ck i ck | ns |
| 456 | TXC rising edge to Transmitter #0 drive enable deassertion ³ | | | — — | 34.0 20.0 | x ck i ck | ns |
| 457 | FST input (bl, wr) setup time before TXC falling edge ² | | | 2.0 21.0 | — — | x ck i ck | ns |
| 458 | FST input (wl) to data out enable from high impedance | | | — | 27.0 | — | ns |
| 459 | FST input (wl) to Transmitter #0 drive enable assertion | | | — | 31.0 | — | ns |
| 460 | FST input (wl) setup time before TXC falling edge | | | 2.5 21.0 | — — | x ck i ck | ns |
| 461 | FST input hold time after TXC falling edge | | | 4.0 0.0 | — — | x ck i ck | ns |
| 462 | Flag output valid after TXC rising edge | | | — — | 32.0 18.0 | x ck i ck | ns |
| <p>Notes:</p> <ol style="list-style-type: none"> For the internal clock, the external clock cycle is defined by I_{cyc} (see Timing 7) and the ESSI Control Register. The word-length-relative frame sync signal waveform operates the same way as the bit-length frame sync signal waveform, but spreads from one serial clock before the first bit clock (same as the Bit Length Frame Sync signal) until the one before last bit clock of the first word in the frame. Periodically sampled and not 100 percent tested $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$ TXC (SCK Pin) = Transmit Clock RXC (SC0 or SCK Pin) = Receive Clock FST (SC2 Pin) = Transmit Frame Sync FSR (SC1 or SC2 Pin) Receive Frame Sync i ck = Internal Clock x ck = External Clock i ck a = Internal Clock, Asynchronous Mode (asynchronous implies that TXC and RXC are two different clocks) i ck s = Internal Clock, Synchronous Mode (synchronous implies that TXC and RXC are the same clock) bl = bit length; wl = word length; wr = word length relative If the DSP core writes to the transmit register during the last cycle before causing an underrun error, the delay is $20 \text{ ns} + (0.5 \times T_C)$. An expression is used to compute the number listed as the minimum or maximum value as appropriate. | | | | | | | |



Note: In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

Figure 2-38. ESSI Transmitter Timing

AC Electrical Characteristics

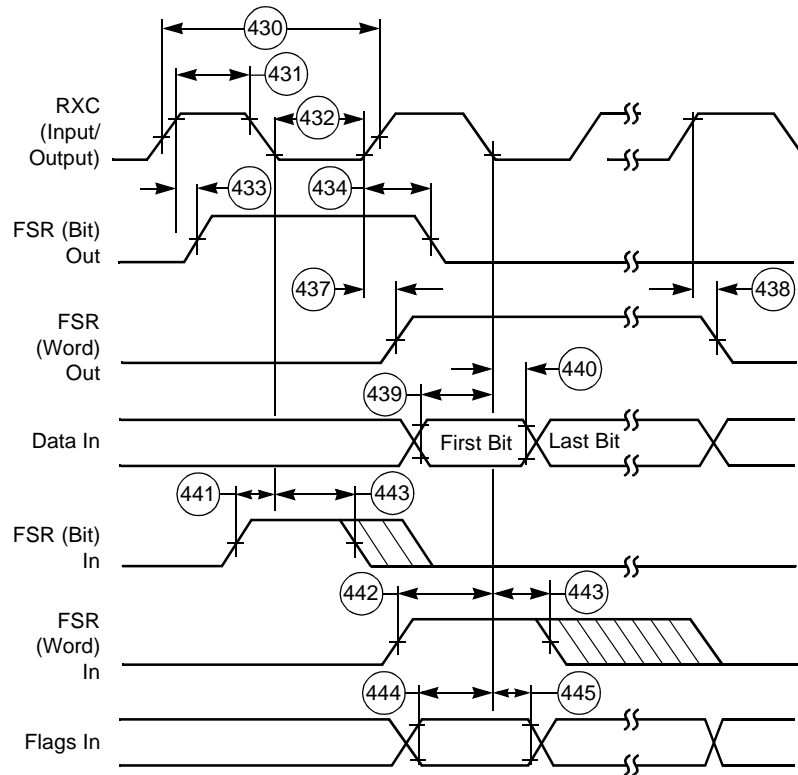


Figure 2-39. ESSI Receiver Timing

2.6.9 Timer Timing

Table 2-19. Timer Timing¹

| No. | Characteristics | Expression ² | 100 MHz | | Unit |
|-----|--|--------------------------|---------|------|------|
| | | | Min | Max | |
| 480 | TIO Low | $2 \times T_C + 2.0$ | 22.0 | — | ns |
| 481 | TIO High | $2 \times T_C + 2.0$ | 22.0 | — | ns |
| 482 | Timer set-up time from TIO (Input) assertion to CLKOUT rising edge | | 9.0 | 10.0 | ns |
| 483 | Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution | $10.25 \times T_C + 1.0$ | 103.5 | — | ns |
| 484 | CLKOUT rising edge to TIO (Output) assertion • Minimum • Maximum | $0.5 \times T_C + 0.5$ | 5.5 | — | ns |
| | | $0.5 \times T_C + 19.8$ | — | 24.8 | ns |
| 485 | CLKOUT rising edge to TIO (Output) deassertion • Minimum • Maximum | $0.5 \times T_C + 0.5$ | 5.5 | — | ns |
| | | $0.5 \times T_C + 19.8$ | — | 24.8 | ns |

Notes:

- $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$
- An expression is used to compute the number listed as the minimum or maximum value as appropriate.

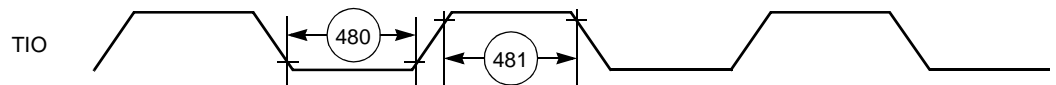


Figure 2-40. TIO Timer Event Input Restrictions

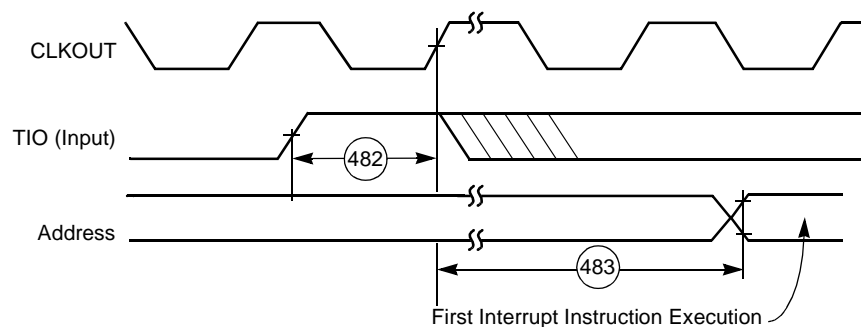


Figure 2-41. Timer Interrupt Generation

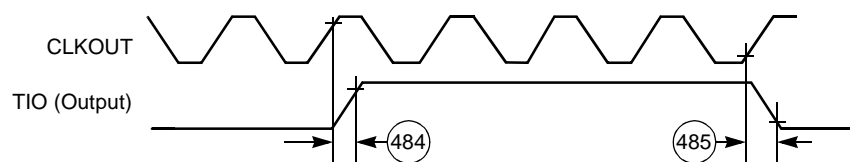


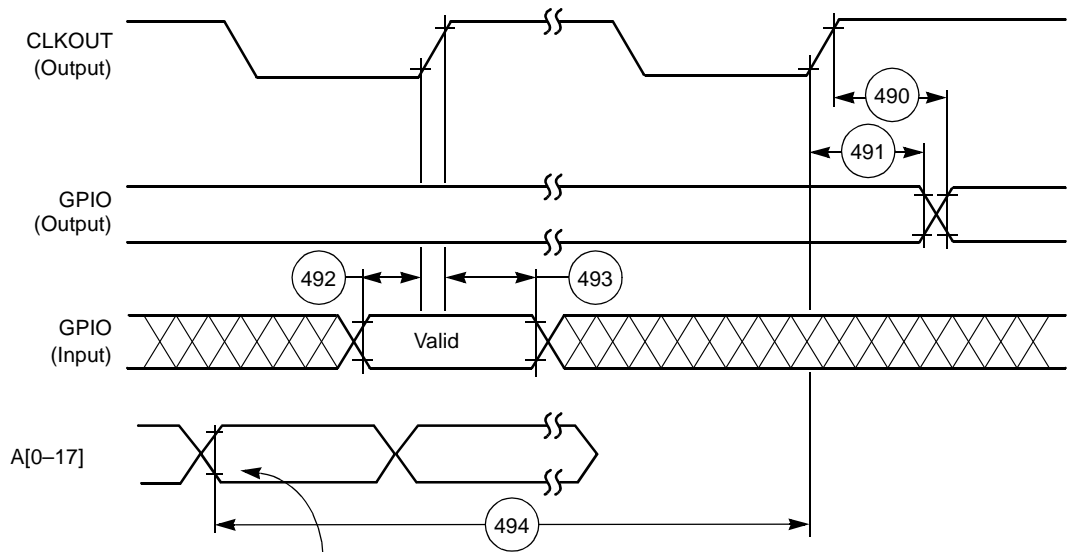
Figure 2-42. External Pulse Generation

2.6.10 GPIO Timing

Table 2-20. GPIO Timing

| No. | Characteristics | Expression | 100 MHz | | Unit |
|-----|--|----------------------------|---------|-----|------|
| | | | Min | Max | |
| 490 | CLKOUT edge to GPIO out valid (GPIO out delay time) | | — | 8.5 | ns |
| 491 | CLKOUT edge to GPIO out not valid (GPIO out hold time) | | 0.0 | — | ns |
| 492 | GPIO In valid to CLKOUT edge (GPIO in set-up time) | | 8.5 | — | ns |
| 493 | CLKOUT edge to GPIO in not valid (GPIO in hold time) | | 0.0 | — | ns |
| 494 | Fetch to CLKOUT edge before GPIO change | Minimum: $6.75 \times T_C$ | 67.5 | — | ns |

Note: $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$



Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of the GPIO data register.

Figure 2-43. GPIO Timing

2.6.11 JTAG Timing

Table 2-21. JTAG Timing

| No. | Characteristics | All frequencies | | Unit |
|-----|--|-----------------|------|------|
| | | Min | Max | |
| 500 | TCK frequency of operation | 0.0 | 22.0 | MHz |
| 501 | TCK cycle time in Crystal mode | 45.0 | — | ns |
| 502 | TCK clock pulse width measured at 1.5 V | 20.0 | — | ns |
| 503 | TCK rise and fall times | 0.0 | 3.0 | ns |
| 504 | Boundary scan input data setup time | 5.0 | — | ns |
| 505 | Boundary scan input data hold time | 24.0 | — | ns |
| 506 | TCK low to output data valid | 0.0 | 40.0 | ns |
| 507 | TCK low to output high impedance | 0.0 | 40.0 | ns |
| 508 | TMS, TDI data setup time | 5.0 | — | ns |
| 509 | TMS, TDI data hold time | 25.0 | — | ns |
| 510 | TCK low to TDO data valid | 0.0 | 44.0 | ns |
| 511 | TCK low to TDO high impedance | 0.0 | 44.0 | ns |
| 512 | $\overline{\text{TRST}}$ assert time | 100.0 | — | ns |
| 513 | $\overline{\text{TRST}}$ setup time to TCK low | 40.0 | — | ns |

Notes:

- $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$
- All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

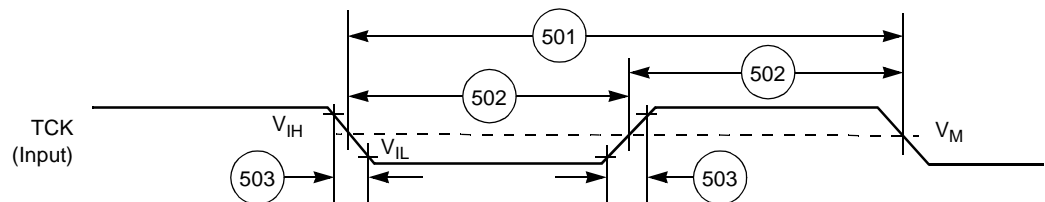


Figure 2-44. Test Clock Input Timing Diagram

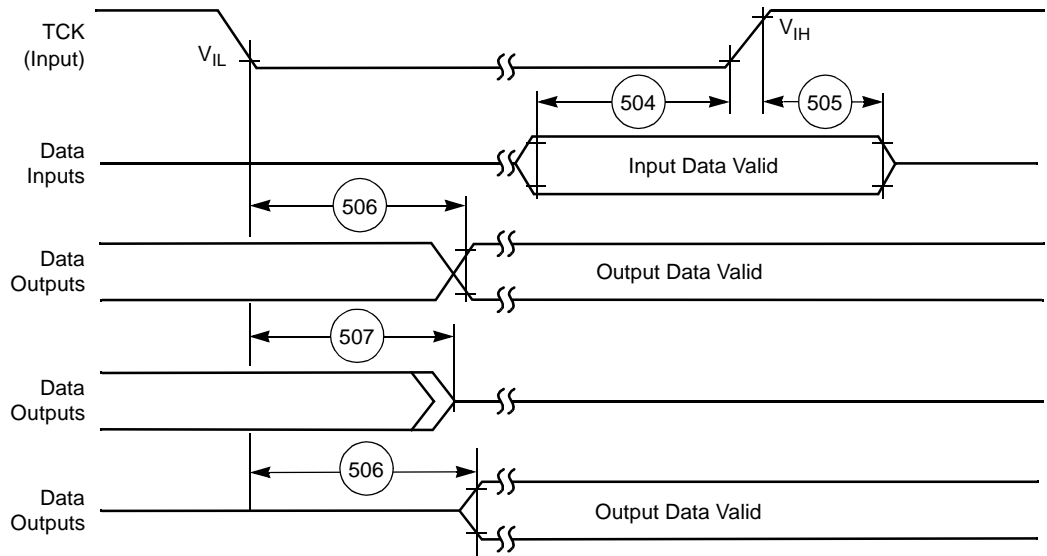


Figure 2-45. Boundary Scan (JTAG) Timing Diagram

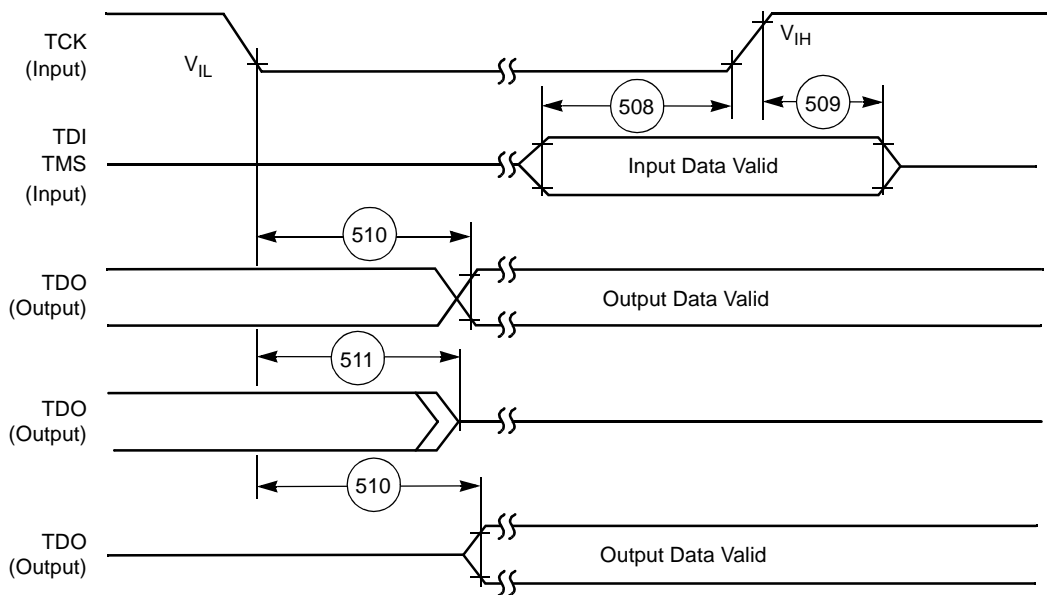


Figure 2-46. Test Access Port Timing Diagram

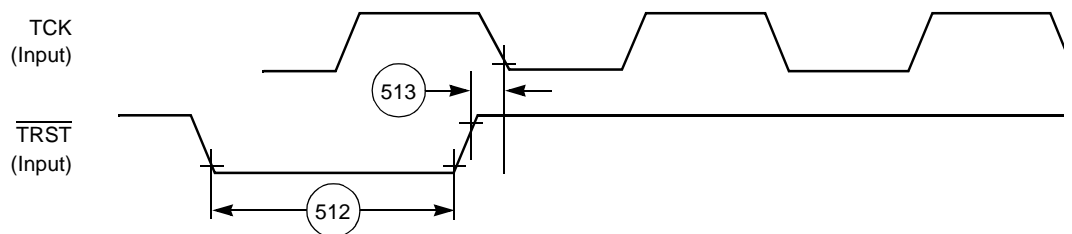


Figure 2-47. $\overline{\text{TRST}}$ Timing Diagram

2.6.12 OnCE Module Timing

Table 2-22. OnCE Module Timing

| No. | Characteristics | Expression | Min | Max | Unit |
|-----|--|-------------------------|------|------|------|
| 500 | TCK frequency of operation | Max 22.0 MHz | 0.0 | 22.0 | MHz |
| 514 | \overline{DE} assertion time in order to enter Debug mode | $1.5 \times T_C + 10.0$ | 20.0 | — | ns |
| 515 | Response time when DSP56303 is executing NOP instructions from internal memory | $5.5 \times T_C + 30.0$ | — | 67.0 | ns |
| 516 | Debug acknowledge assertion time | $3 \times T_C + 5.0$ | 25.0 | — | ns |

Note: $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$, $V_{CC} = 1.8 \text{ V} \pm 0.1 \text{ V}$; $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $C_L = 50 \text{ pF}$

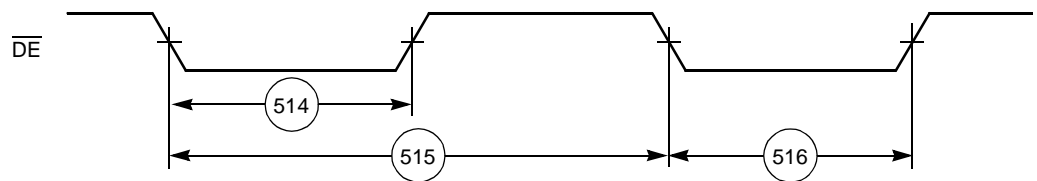


Figure 2-48. OnCE—Debug Request

AC Electrical Characteristics

3.1 Pin-Out and Package Information

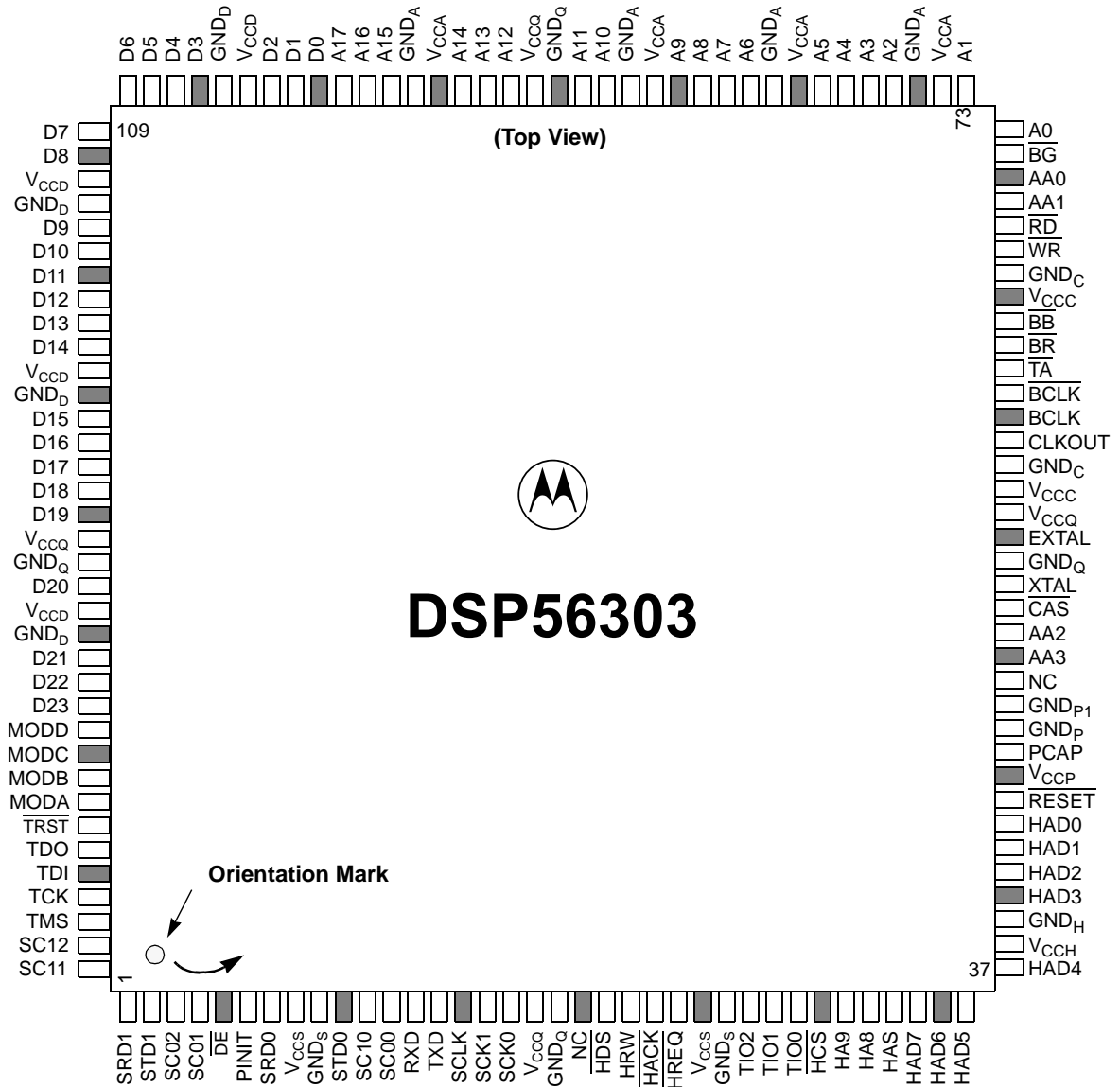
This section includes diagrams of the DSP56303 package pin-outs and tables showing how the signals described in **Chapter 1** are allocated for each package.

The DSP56303 is available in two package types:

- 144-pin Thin Quad Flat Pack (TQFP)
- 196-pin Molded Array Process-Ball Grid Array (MAP-BGA)

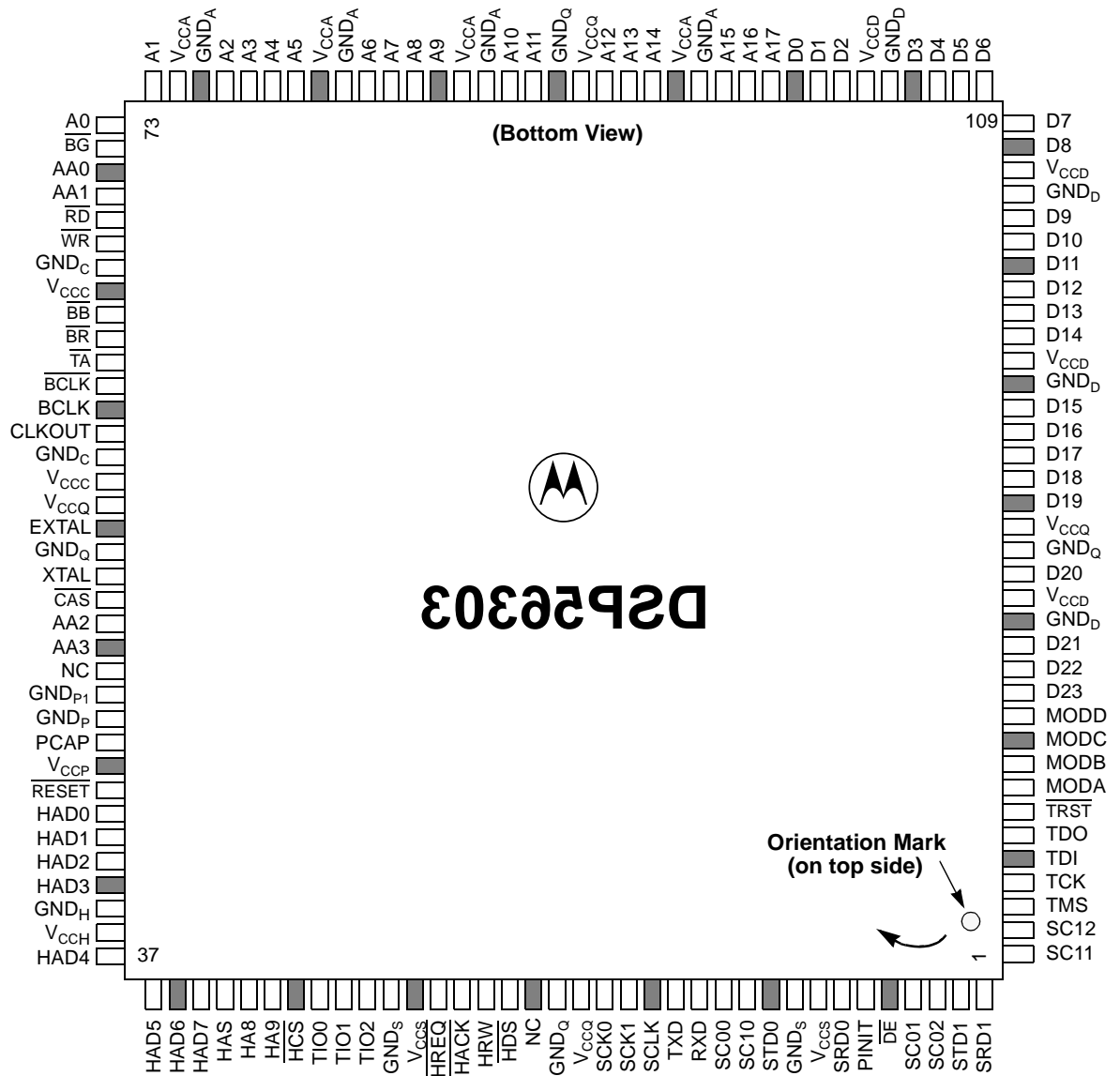
3.2 TQFP Package Description

Top and bottom views of the TQFP package are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.



Notes: Because of size constraints in this figure, only one name is shown for multiplexed pins. Refer to **Table 3-1** and **Table 3-2** for detailed information about pin functions and signal names.

Figure 3-1. DSP56303 Thin Quad Flat Pack (TQFP), Top View



Notes: Because of size constraints in this figure, only one name is shown for multiplexed pins. Refer to **Table 3-1** and **Table 3-2** for detailed information about pin functions and signal names.

Figure 3-2. DSP56303 Thin Quad Flat Pack (TQFP), Bottom View

Table 3-1. DSP56303 TQFP Signal Identification by Pin Number

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|---|---------|------------------------------------|---------|-------------------|
| 1 | SRD1 or PD4 | 26 | GND _S | 51 | AA2/RAS2 |
| 2 | STD1 or PD5 | 27 | TIO2 | 52 | CAS |
| 3 | SC02 or PC2 | 28 | TIO1 | 53 | XTAL |
| 4 | SC01 or PC1 | 29 | TIO0 | 54 | GND _Q |
| 5 | \overline{DE} | 30 | HCS/HCS, HA10, or PB13 | 55 | EXTAL |
| 6 | PINIT/ \overline{NMI} | 31 | HA2, HA9, or PB10 | 56 | V _{CCQ} |
| 7 | SRD0 or PC4 | 32 | HA1, HA8, or PB9 | 57 | V _{CC} |
| 8 | V _{CCS} | 33 | HA0, \overline{HAS}/HAS , or PB8 | 58 | GND _C |
| 9 | GND _S | 34 | H7, HAD7, or PB7 | 59 | CLKOUT |
| 10 | STD0 or PC5 | 35 | H6, HAD6, or PB6 | 60 | BCLK |
| 11 | SC10 or PD0 | 36 | H5, HAD5, or PB5 | 61 | \overline{BCLK} |
| 12 | SC00 or PC0 | 37 | H4, HAD4, or PB4 | 62 | \overline{TA} |
| 13 | RXD or PE0 | 38 | V _{CCH} | 63 | \overline{BR} |
| 14 | TXD or PE1 | 39 | GND _H | 64 | \overline{BB} |
| 15 | SCLK or PE2 | 40 | H3, HAD3, or PB3 | 65 | V _{CC} |
| 16 | SCK1 or PD3 | 41 | H2, HAD2, or PB2 | 66 | GND _C |
| 17 | SCK0 or PC3 | 42 | H1, HAD1, or PB1 | 67 | \overline{WR} |
| 18 | V _{CCQ} | 43 | H0, HAD0, or PB0 | 68 | \overline{RD} |
| 19 | GND _Q | 44 | \overline{RESET} | 69 | AA1/RAS1 |
| 20 | Not Connected (NC), reserved | 45 | V _{CCP} | 70 | AA0/RAS0 |
| 21 | \overline{HDS}/HDS , \overline{HWR}/HWR , or PB12 | 46 | PCAP | 71 | \overline{BG} |
| 22 | HRW, \overline{HRD}/HRD , or PB11 | 47 | GND _P | 72 | A0 |
| 23 | $\overline{HACK}/HACK$, $\overline{HRRQ}/HRRQ$, or PB15 | 48 | GND _{P1} | 73 | A1 |
| 24 | $\overline{HREQ}/HREQ$, $\overline{HTRQ}/HTRQ$, or PB14 | 49 | Not Connected (NC), reserved | 74 | V _{CCA} |
| 25 | V _{CCS} | 50 | AA3/RAS3 | 75 | GND _A |

Table 3-1. DSP56303 TQFP Signal Identification by Pin Number (Continued)

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---|------------------|---------|------------------|---------|--------------------------------|
| 76 | A2 | 99 | A17 | 122 | D16 |
| 77 | A3 | 100 | D0 | 123 | D17 |
| 78 | A4 | 101 | D1 | 124 | D18 |
| 79 | A5 | 102 | D2 | 125 | D19 |
| 80 | V _{CCA} | 103 | V _{CCD} | 126 | V _{CCQ} |
| 81 | GND _A | 104 | GND _D | 127 | GND _Q |
| 82 | A6 | 105 | D3 | 128 | D20 |
| 83 | A7 | 106 | D4 | 129 | V _{CCD} |
| 84 | A8 | 107 | D5 | 130 | GND _D |
| 85 | A9 | 108 | D6 | 131 | D21 |
| 86 | V _{CCA} | 109 | D7 | 132 | D22 |
| 87 | GND _A | 110 | D8 | 133 | D23 |
| 88 | A10 | 111 | V _{CCD} | 134 | MODD/ $\overline{\text{IRQD}}$ |
| 89 | A11 | 112 | GND _D | 135 | MODC/ $\overline{\text{IRQC}}$ |
| 90 | GND _Q | 113 | D9 | 136 | MODB/ $\overline{\text{IRQB}}$ |
| 91 | V _{CCQ} | 114 | D10 | 137 | MODA/ $\overline{\text{IRQA}}$ |
| 92 | A12 | 115 | D11 | 138 | $\overline{\text{TRST}}$ |
| 93 | A13 | 116 | D12 | 139 | TDO |
| 94 | A14 | 117 | D13 | 140 | TDI |
| 95 | V _{CCA} | 118 | D14 | 141 | TCK |
| 96 | GND _A | 119 | V _{CCD} | 142 | TMS |
| 97 | A15 | 120 | GND _D | 143 | SC12 or PD2 |
| 98 | A16 | 121 | D15 | 144 | SC11 or PD1 |
| <p>Notes: Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/IRQx pins that select an operating mode after $\overline{\text{RESET}}$ is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as $\overline{\text{HAS}}$/HAS. Some pins have two or more configurable functions; names assigned to these pins indicate the function for a specific configuration. For example, Pin 34 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin.</p> | | | | | |

Table 3-2. DSP56303 TQFP Signal Identification by Name

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|-------------------|---------|------------------|---------|-------------------|---------|
| A0 | 72 | \overline{BG} | 71 | D7 | 109 |
| A1 | 73 | \overline{BR} | 63 | D8 | 110 |
| A10 | 88 | \overline{CAS} | 52 | D9 | 113 |
| A11 | 89 | CLKOUT | 59 | \overline{DE} | 5 |
| A12 | 92 | D0 | 100 | EXTAL | 55 |
| A13 | 93 | D1 | 101 | GND _A | 75 |
| A14 | 94 | D10 | 114 | GND _A | 81 |
| A15 | 97 | D11 | 115 | GND _A | 87 |
| A16 | 98 | D12 | 116 | GND _A | 96 |
| A17 | 99 | D13 | 117 | GND _C | 58 |
| A2 | 76 | D14 | 118 | GND _C | 66 |
| A3 | 77 | D15 | 121 | GND _D | 104 |
| A4 | 78 | D16 | 122 | GND _D | 112 |
| A5 | 79 | D17 | 123 | GND _D | 120 |
| A6 | 82 | D18 | 124 | GND _D | 130 |
| A7 | 83 | D19 | 125 | GND _H | 39 |
| A8 | 84 | D2 | 102 | GND _P | 47 |
| A9 | 85 | D20 | 128 | GND _{P1} | 48 |
| AA0 | 70 | D21 | 131 | GND _Q | 19 |
| AA1 | 69 | D22 | 132 | GND _Q | 54 |
| AA2 | 51 | D23 | 133 | GND _Q | 90 |
| AA3 | 50 | D3 | 105 | GND _Q | 127 |
| \overline{BB} | 64 | D4 | 106 | GND _S | 9 |
| BCLK | 60 | D5 | 107 | GND _S | 26 |
| \overline{BCLK} | 61 | D6 | 108 | H0 | 43 |

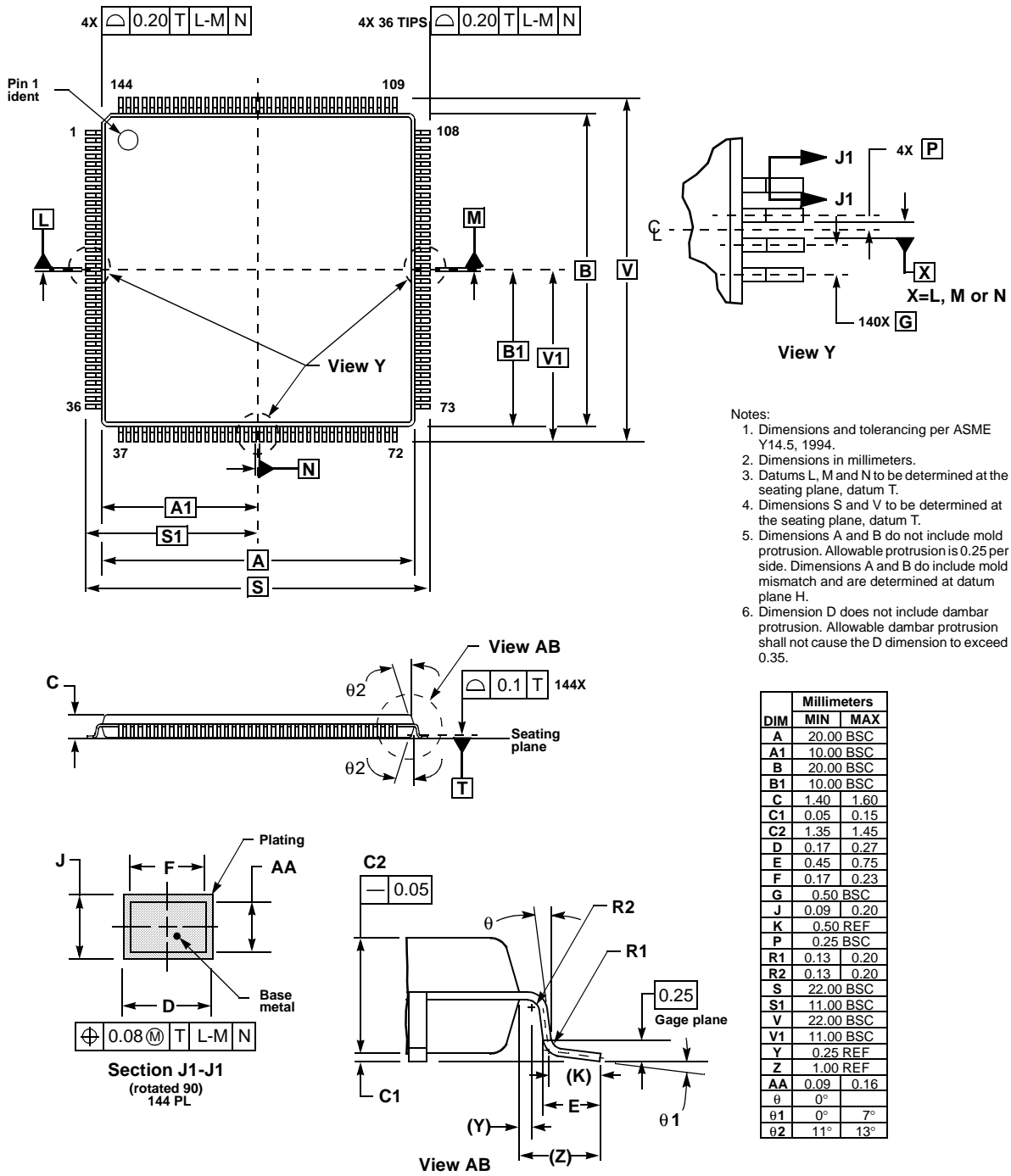
Table 3-2. DSP56303 TQFP Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|--------------------------------------|---------|--------------------------------------|---------|-------------|---------|
| H1 | 42 | $\overline{\text{HRD}}/\text{HRD}$ | 22 | PB2 | 41 |
| H2 | 41 | $\overline{\text{HREQ}}/\text{HREQ}$ | 24 | PB3 | 40 |
| H3 | 40 | $\overline{\text{HRRQ}}/\text{HRRQ}$ | 23 | PB4 | 37 |
| H4 | 37 | HRW | 22 | PB5 | 36 |
| H5 | 36 | $\overline{\text{HTRQ}}/\text{HTRQ}$ | 24 | PB6 | 35 |
| H6 | 35 | $\overline{\text{HWR}}/\text{HWR}$ | 21 | PB7 | 34 |
| H7 | 34 | $\overline{\text{IRQA}}$ | 137 | PB8 | 33 |
| HA0 | 33 | $\overline{\text{IRQB}}$ | 136 | PB9 | 32 |
| HA1 | 32 | $\overline{\text{IRQC}}$ | 135 | PC0 | 12 |
| HA10 | 30 | $\overline{\text{IRQD}}$ | 134 | PC1 | 4 |
| HA2 | 31 | MODA | 137 | PC2 | 3 |
| HA8 | 32 | MODB | 136 | PC3 | 17 |
| HA9 | 31 | MODC | 135 | PC4 | 7 |
| $\overline{\text{HACK}}/\text{HACK}$ | 23 | MODD | 134 | PC5 | 10 |
| HAD0 | 43 | NC | 20 | PCAP | 46 |
| HAD1 | 42 | NMI | 6 | PD0 | 11 |
| HAD2 | 41 | NC | 49 | PD1 | 144 |
| HAD3 | 40 | PB0 | 43 | PD2 | 143 |
| HAD4 | 37 | PB1 | 42 | PD3 | 16 |
| HAD5 | 36 | PB10 | 31 | PD4 | 1 |
| HAD6 | 35 | PB11 | 22 | PD5 | 2 |
| HAD7 | 34 | PB12 | 21 | PE0 | 13 |
| $\overline{\text{HAS}}/\text{HAS}$ | 33 | PB13 | 30 | PE1 | 14 |
| $\overline{\text{HCS}}/\text{HCS}$ | 30 | PB14 | 24 | PE2 | 15 |
| $\overline{\text{HDS}}/\text{HDS}$ | 21 | PB15 | 23 | PINIT | 6 |

Table 3-2. DSP56303 TQFP Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|---------------------------|---------|--------------------------|---------|------------------------|---------|
| $\overline{\text{RAS0}}$ | 70 | SRD1 | 1 | V_{CCC} | 57 |
| $\overline{\text{RAS1}}$ | 69 | STD0 | 10 | V_{CCC} | 65 |
| $\overline{\text{RAS2}}$ | 51 | STD1 | 2 | V_{CCD} | 103 |
| $\overline{\text{RAS3}}$ | 50 | $\overline{\text{TA}}$ | 62 | V_{CCD} | 111 |
| $\overline{\text{RD}}$ | 68 | TCK | 141 | V_{CCD} | 119 |
| $\overline{\text{RESET}}$ | 44 | TDI | 140 | V_{CCD} | 129 |
| RXD | 13 | TDO | 139 | V_{CCH} | 38 |
| SC00 | 12 | TIO0 | 29 | V_{CCP} | 45 |
| SC01 | 4 | TIO1 | 28 | V_{CCQ} | 18 |
| SC02 | 3 | TIO2 | 27 | V_{CCQ} | 56 |
| SC10 | 11 | TMS | 142 | V_{CCQ} | 91 |
| SC11 | 144 | $\overline{\text{TRST}}$ | 138 | V_{CCQ} | 126 |
| SC12 | 143 | TXD | 14 | V_{CCS} | 8 |
| SCK0 | 17 | V_{CCA} | 74 | V_{CCS} | 25 |
| SCK1 | 16 | V_{CCA} | 80 | $\overline{\text{WR}}$ | 67 |
| SCLK | 15 | V_{CCA} | 86 | XTAL | 53 |
| SRD0 | 7 | V_{CCA} | 95 | | |

3.3 TQFP Package Mechanical Drawing



- Notes:
1. Dimensions and tolerancing per ASME Y14.5, 1994.
 2. Dimensions in millimeters.
 3. Datums L, M and N to be determined at the seating plane, datum T.
 4. Dimensions S and V to be determined at the seating plane, datum T.
 5. Dimensions A and B do not include mold protrusion. Allowable protrusion is 0.25 per side. Dimensions A and B do include mold mismatch and are determined at datum plane H.
 6. Dimension D does not include dambar protrusion. Allowable dambar protrusion shall not cause the D dimension to exceed 0.35.

CASE 918-03
ISSUE C

Figure 3-3. DSP56303 Mechanical Information, 144-pin TQFP Package

3.4 MAP-BGA Package Description

Top and bottom views of the MAP-BGA package are shown in **Figure 3-4** and **Figure 3-5** with their pin-outs.

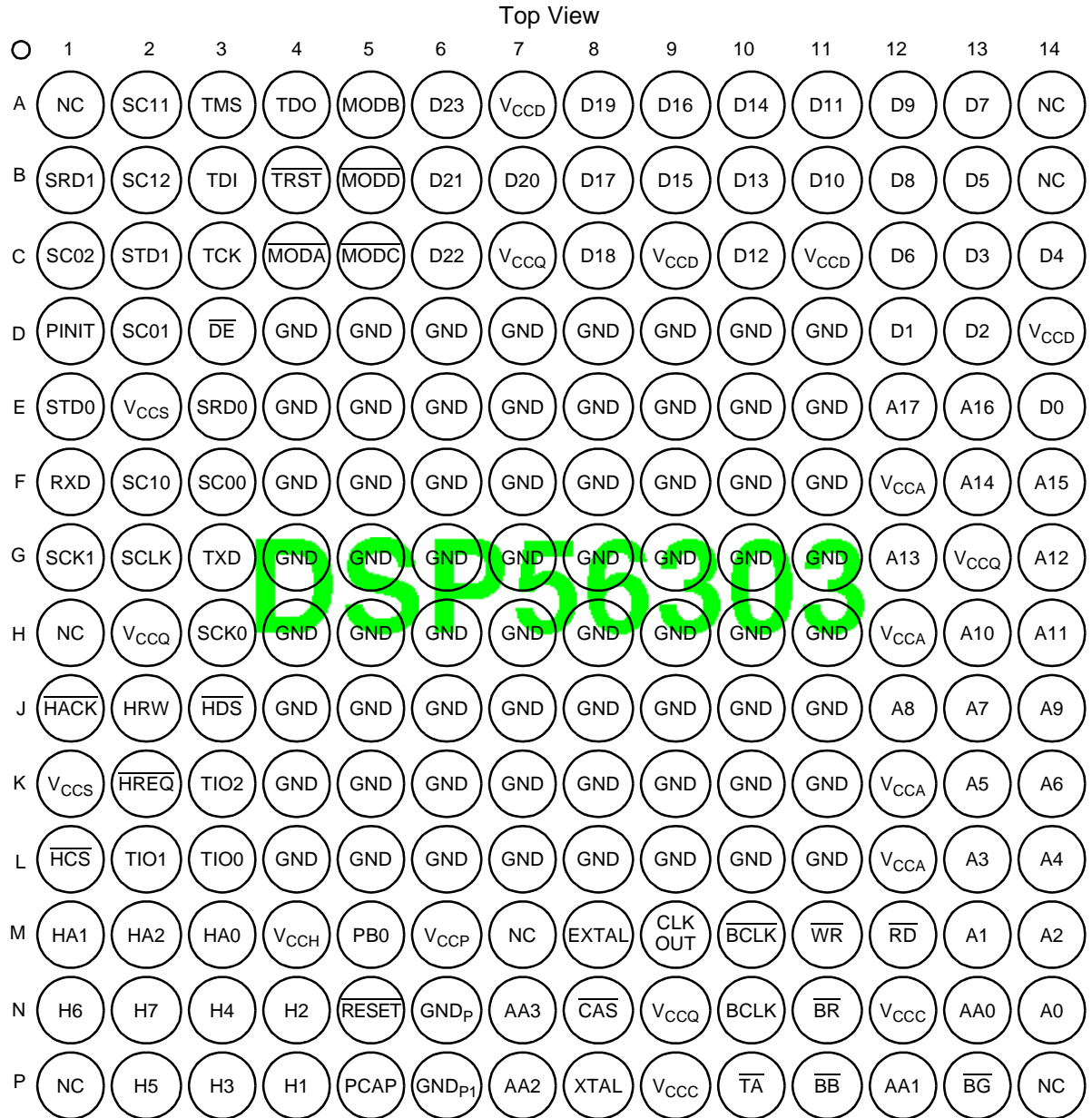


Figure 3-4. DSP56303 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

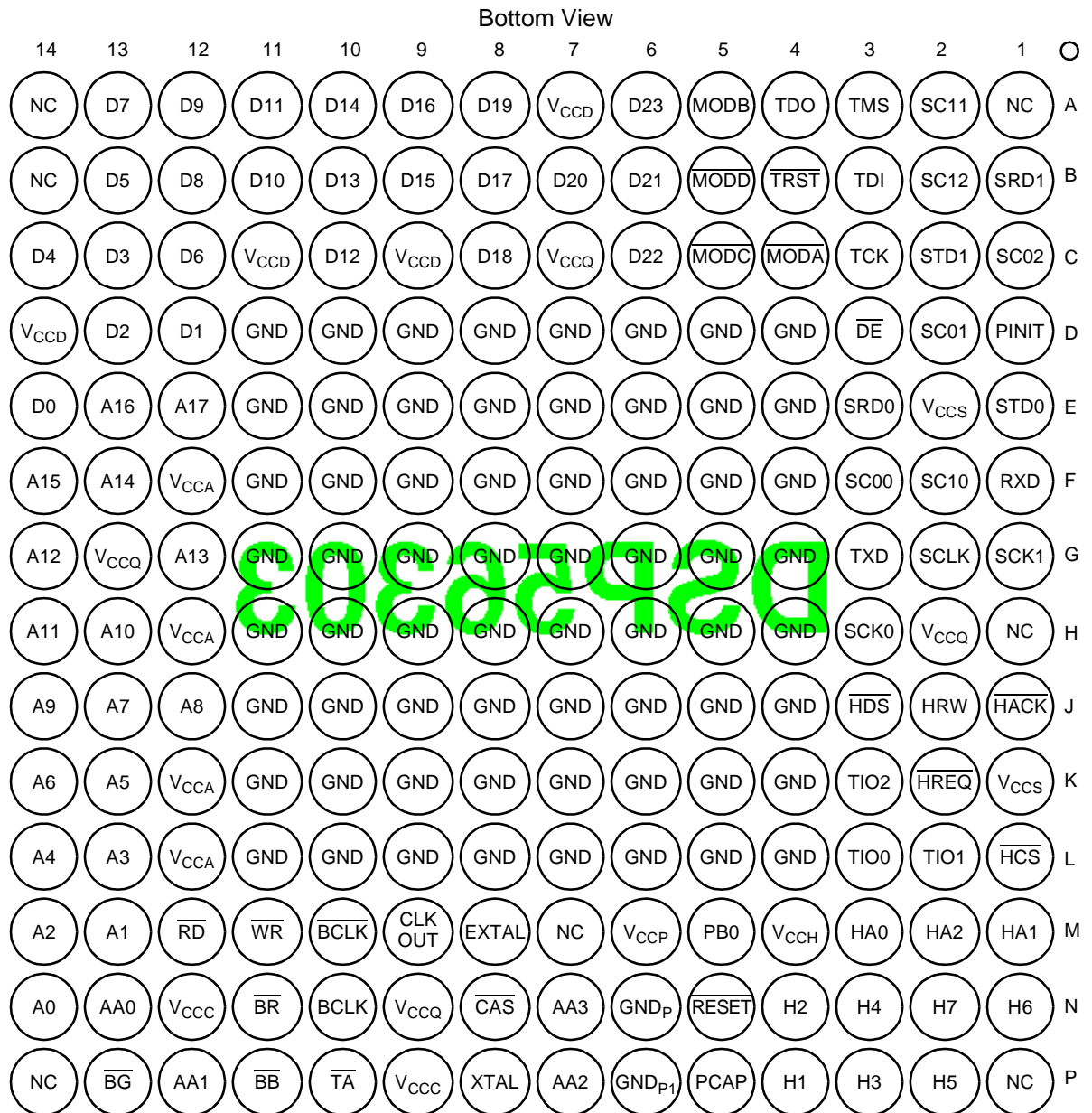


Figure 3-5. DSP56303 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|--------------------------------|---------|--------------------------------|---------|------------------|
| A1 | Not Connected (NC), reserved | B12 | D8 | D9 | GND |
| A2 | SC11 or PD1 | B13 | D5 | D10 | GND |
| A3 | TMS | B14 | NC | D11 | GND |
| A4 | TDO | C1 | SC02 or PC2 | D12 | D1 |
| A5 | MODB/ $\overline{\text{IRQB}}$ | C2 | STD1 or PD5 | D13 | D2 |
| A6 | D23 | C3 | TCK | D14 | V _{CCD} |
| A7 | V _{CCD} | C4 | MODA/ $\overline{\text{IRQA}}$ | E1 | STD0 or PC5 |
| A8 | D19 | C5 | MODC/ $\overline{\text{IRQC}}$ | E2 | V _{CCS} |
| A9 | D16 | C6 | D22 | E3 | SRD0 or PC4 |
| A10 | D14 | C7 | V _{CCQ} | E4 | GND |
| A11 | D11 | C8 | D18 | E5 | GND |
| A12 | D9 | C9 | V _{CCD} | E6 | GND |
| A13 | D7 | C10 | D12 | E7 | GND |
| A14 | NC | C11 | V _{CCD} | E8 | GND |
| B1 | SRD1 or PD4 | C12 | D6 | E9 | GND |
| B2 | SC12 or PD2 | C13 | D3 | E10 | GND |
| B3 | TDI | C14 | D4 | E11 | GND |
| B4 | $\overline{\text{TRST}}$ | D1 | PINIT/ $\overline{\text{NMI}}$ | E12 | A17 |
| B5 | MODD/ $\overline{\text{IRQD}}$ | D2 | SC01 or PC1 | E13 | A16 |
| B6 | D21 | D3 | $\overline{\text{DE}}$ | E14 | D0 |
| B7 | D20 | D4 | GND | F1 | RXD or PE0 |
| B8 | D17 | D5 | GND | F2 | SC10 or PD0 |
| B9 | D15 | D6 | GND | F3 | SC00 or PC0 |
| B10 | D13 | D7 | GND | F4 | GND |
| B11 | D10 | D8 | GND | F5 | GND |

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number (Continued)

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---------|------------------|---------|--|---------|--|
| F6 | GND | H3 | SCK0 or PC3 | J14 | A9 |
| F7 | GND | H4 | GND | K1 | V _{CCS} |
| F8 | GND | H5 | GND | K2 | $\overline{\text{HREQ}}/\overline{\text{HREQ}}$, $\overline{\text{HTRQ}}/\overline{\text{HTRQ}}$, or PB14 |
| F9 | GND | H6 | GND | K3 | TIO2 |
| F10 | GND | H7 | GND | K4 | GND |
| F11 | GND | H8 | GND | K5 | GND |
| F12 | V _{CCA} | H9 | GND | K6 | GND |
| F13 | A14 | H10 | GND | K7 | GND |
| F14 | A15 | H11 | GND | K8 | GND |
| G1 | SCK1 or PD3 | H12 | V _{CCA} | K9 | GND |
| G2 | SCLK or PE2 | H13 | A10 | K10 | GND |
| G3 | TXD or PE1 | H14 | A11 | K11 | GND |
| G4 | GND | J1 | $\overline{\text{HACK}}/\overline{\text{HACK}}$, $\overline{\text{HRRQ}}/\overline{\text{HRRQ}}$, or PB15 | K12 | V _{CCA} |
| G5 | GND | J2 | HRW, $\overline{\text{HRD}}/\overline{\text{HRD}}$, or PB11 | K13 | A5 |
| G6 | GND | J3 | $\overline{\text{HDS}}/\overline{\text{HDS}}$, $\overline{\text{HWR}}/\overline{\text{HWR}}$, or PB12 | K14 | A6 |
| G7 | GND | J4 | GND | L1 | $\overline{\text{HCS}}/\overline{\text{HCS}}$, HA10, or PB13 |
| G8 | GND | J5 | GND | L2 | TIO1 |
| G9 | GND | J6 | GND | L3 | TIO0 |
| G10 | GND | J7 | GND | L4 | GND |
| G11 | GND | J8 | GND | L5 | GND |
| G12 | A13 | J9 | GND | L6 | GND |
| G13 | V _{CCQ} | J10 | GND | L7 | GND |
| G14 | A12 | J11 | GND | L8 | GND |
| H1 | NC | J12 | A8 | L9 | GND |
| H2 | V _{CCQ} | J13 | A7 | L10 | GND |
| L11 | GND | M13 | A1 | P1 | NC |
| L12 | V _{CCA} | M14 | A2 | P2 | H5, HAD5, or PB5 |
| L13 | A3 | N1 | H6, HAD6, or PB6 | P3 | H3, HAD3, or PB3 |

Table 3-3. DSP56303 MAP-BGA Signal Identification by Pin Number (Continued)

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|--|---|---------|-------------------------------|---------|-------------------------------|
| L14 | A4 | N2 | H7, HAD7, or PB7 | P4 | H1, HAD1, or PB1 |
| M1 | HA1, HA8, or PB9 | N3 | H4, HAD4, or PB4 | P5 | PCAP |
| M2 | HA2, HA9, or PB10 | N4 | H2, HAD2, or PB2 | P6 | GND _{P1} |
| M3 | HA0, $\overline{\text{HAS}}$ /HAS, or PB8 | N5 | $\overline{\text{RESET}}$ | P7 | AA2/ $\overline{\text{RAS2}}$ |
| M4 | V _{CCH} | N6 | GND _P | P8 | XTAL |
| M5 | H0, HAD0, or PB0 | N7 | AA3/ $\overline{\text{RAS3}}$ | P9 | V _{CCC} |
| M6 | V _{CCP} | N8 | $\overline{\text{CAS}}$ | P10 | $\overline{\text{TA}}$ |
| M7 | NC | N9 | V _{CCQ} | P11 | $\overline{\text{BB}}$ |
| M8 | EXTAL | N10 | BCLK | P12 | AA1/ $\overline{\text{RAS1}}$ |
| M9 | CLKOUT | N11 | $\overline{\text{BR}}$ | P13 | $\overline{\text{BG}}$ |
| M10 | $\overline{\text{BCLK}}$ | N12 | V _{CCC} | P14 | NC |
| M11 | $\overline{\text{WR}}$ | N13 | AA0/ $\overline{\text{RAS0}}$ | | |
| M12 | $\overline{\text{RD}}$ | N14 | A0 | | |
| <p>Notes: Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/IRQx pins that select an operating mode after RESET is deasserted but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as HAS/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike in the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND_P and GND_{P1} that support the PLL, other GND signals do not support individual subsystems in the chip.</p> | | | | | |

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|-------------------|---------|------------------|---------|-----------------|---------|
| A0 | N14 | \overline{BG} | P13 | D7 | A13 |
| A1 | M13 | \overline{BR} | N11 | D8 | B12 |
| A10 | H13 | \overline{CAS} | N8 | D9 | A12 |
| A11 | H14 | CLKOUT | M9 | \overline{DE} | D3 |
| A12 | G14 | D0 | E14 | EXTAL | M8 |
| A13 | G12 | D1 | D12 | GND | D4 |
| A14 | F13 | D10 | B11 | GND | D5 |
| A15 | F14 | D11 | A11 | GND | D6 |
| A16 | E13 | D12 | C10 | GND | D7 |
| A17 | E12 | D13 | B10 | GND | D8 |
| A2 | M14 | D14 | A10 | GND | D9 |
| A3 | L13 | D15 | B9 | GND | D10 |
| A4 | L14 | D16 | A9 | GND | D11 |
| A5 | K13 | D17 | B8 | GND | E4 |
| A6 | K14 | D18 | C8 | GND | E5 |
| A7 | J13 | D19 | A8 | GND | E6 |
| A8 | J12 | D2 | D13 | GND | E7 |
| A9 | J14 | D20 | B7 | GND | E8 |
| AA0 | N13 | D21 | B6 | GND | E9 |
| AA1 | P12 | D22 | C6 | GND | E10 |
| AA2 | P7 | D23 | A6 | GND | E11 |
| AA3 | N7 | D3 | C13 | GND | F4 |
| \overline{BB} | P11 | D4 | C14 | GND | F5 |
| \overline{BCLK} | M10 | D5 | B13 | GND | F6 |
| BCLK | N10 | D6 | C12 | GND | F7 |

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|-------------|---------|-------------------|---------|--------------------------------------|---------|
| GND | F8 | GND | J9 | H4 | N3 |
| GND | F9 | GND | J10 | H5 | P2 |
| GND | F10 | GND | J11 | H6 | N1 |
| GND | F11 | GND | K4 | H7 | N2 |
| GND | G4 | GND | K5 | HA0 | M3 |
| GND | G5 | GND | K6 | HA1 | M1 |
| GND | G6 | GND | K7 | HA10 | L1 |
| GND | G7 | GND | K8 | HA2 | M2 |
| GND | G8 | GND | K9 | HA8 | M1 |
| GND | G9 | GND | K10 | HA9 | M2 |
| GND | G10 | GND | K11 | $\overline{\text{HACK}}/\text{HACK}$ | J1 |
| GND | G11 | GND | L4 | HAD0 | M5 |
| GND | H4 | GND | L5 | HAD1 | P4 |
| GND | H5 | GND | L6 | HAD2 | N4 |
| GND | H6 | GND | L7 | HAD3 | P3 |
| GND | H7 | GND | L8 | HAD4 | N3 |
| GND | H8 | GND | L9 | HAD5 | P2 |
| GND | H9 | GND | L10 | HAD6 | N1 |
| GND | H10 | GND | L11 | HAD7 | N2 |
| GND | H11 | GND _P | N6 | $\overline{\text{HAS}}/\text{HAS}$ | M3 |
| GND | J4 | GND _{P1} | P6 | $\overline{\text{HCS}}/\text{HCS}$ | L1 |
| GND | J5 | H0 | M5 | $\overline{\text{HDS}}/\text{HDS}$ | J3 |
| GND | J6 | H1 | P4 | $\overline{\text{HRD}}/\text{HRD}$ | J2 |
| GND | J7 | H2 | N4 | $\overline{\text{HREQ}}/\text{HREQ}$ | K2 |
| GND | J8 | H3 | P3 | $\overline{\text{HRRQ}}/\text{HRRQ}$ | J1 |

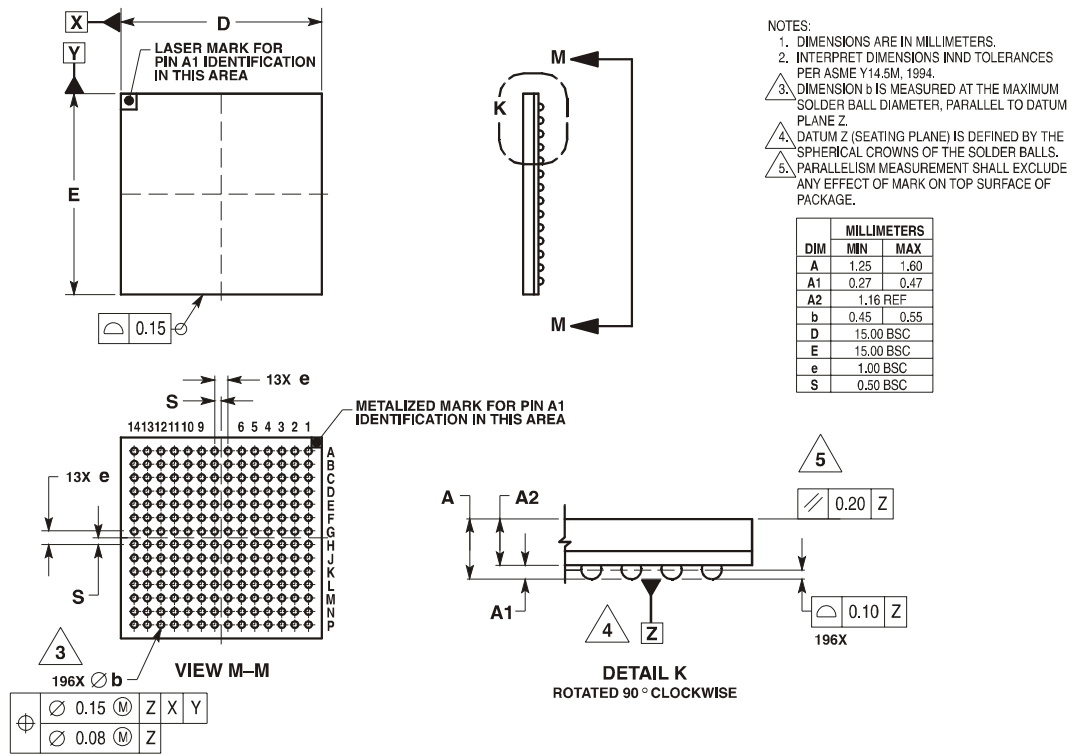
Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|--------------------------------------|---------|-------------|---------|---------------------------|---------|
| HRW | J2 | PB14 | K2 | PE2 | G2 |
| $\overline{\text{HTRQ}}/\text{HTRQ}$ | K2 | PB15 | J1 | PINIT | D1 |
| $\overline{\text{HWR}}/\text{HWR}$ | J3 | PB2 | N4 | $\overline{\text{RAS0}}$ | N13 |
| $\overline{\text{IRQA}}$ | C4 | PB3 | P3 | $\overline{\text{RAS1}}$ | P12 |
| $\overline{\text{IRQB}}$ | A5 | PB4 | N3 | $\overline{\text{RAS2}}$ | P7 |
| $\overline{\text{IRQC}}$ | C5 | PB5 | P2 | $\overline{\text{RAS3}}$ | N7 |
| $\overline{\text{IRQD}}$ | B5 | PB6 | N1 | $\overline{\text{RD}}$ | M12 |
| MODA | C4 | PB7 | N2 | $\overline{\text{RESET}}$ | N5 |
| MODB | A5 | PB8 | M3 | RXD | F1 |
| MODC | C5 | PB9 | M1 | SC00 | F3 |
| MODD | B5 | PC0 | F3 | SC01 | D2 |
| NC | A1 | PC1 | D2 | SC02 | C1 |
| NC | A14 | PC2 | C1 | SC10 | F2 |
| NC | B14 | PC3 | H3 | SC11 | A2 |
| NC | H1 | PC4 | E3 | SC12 | B2 |
| NC | M7 | PC5 | E1 | SCK0 | H3 |
| NC | P1 | PCAP | P5 | SCK1 | G1 |
| NC | P14 | PD0 | F2 | SCLK | G2 |
| NMI | D1 | PD1 | A2 | SRD0 | E3 |
| PB0 | M5 | PD2 | B2 | SRD1 | B1 |
| PB1 | P4 | PD3 | G1 | STD0 | E1 |
| PB10 | M2 | PD4 | B1 | STD1 | C2 |
| PB11 | J2 | PD5 | C2 | $\overline{\text{TA}}$ | P10 |
| PB12 | J3 | PE0 | F1 | TCK | C3 |
| PB13 | L1 | PE1 | G3 | TDI | B3 |

Table 3-4. DSP56303 MAP-BGA Signal Identification by Name (Continued)

| Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. |
|--------------------------|---------|------------------|---------|------------------------|---------|
| TDO | A4 | V _{CCA} | K12 | V _{CCP} | M6 |
| TIO0 | L3 | V _{CCA} | L12 | V _{CCQ} | C7 |
| TIO1 | L2 | V _{CC} | N12 | V _{CCQ} | G13 |
| TIO2 | K3 | V _{CC} | P9 | V _{CCQ} | H2 |
| TMS | A3 | V _{CCD} | A7 | V _{CCQ} | N9 |
| $\overline{\text{TRST}}$ | B4 | V _{CCD} | C9 | V _{CCS} | E2 |
| TXD | G3 | V _{CCD} | C11 | V _{CCS} | K1 |
| V _{CCA} | F12 | V _{CCD} | D14 | $\overline{\text{WR}}$ | M11 |
| V _{CCA} | H12 | V _{CCH} | M4 | XTAL | P8 |

3.5 MAP-BGA Package Mechanical Drawing



CASE 1128C-01
ISSUE O

DATE 07/28/98

Figure 3-6. DSP56303 Mechanical Information, 196-pin MAP-BGA Package

MAP-BGA Package Mechanical Drawing

4.1 Thermal Design Considerations

An estimate of the chip junction temperature, T_J , in °C can be obtained from this equation:

$$\text{Equation 1: } T_J = T_A + (P_D \times R_{\theta JA})$$

Where:

- T_A = ambient temperature °C
- $R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
- P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance, as in this equation:

$$\text{Equation 2: } R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

- $R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
- $R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
- $R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB) or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90 percent of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system-level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimates obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system-level model may be appropriate.

Electrical Design Considerations

A complicating factor is the existence of three common ways to determine the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to the point at which the leads attach to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation $(T_J - T_T)/P_D$.

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT} , has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

4.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Use the following list of recommendations to ensure correct DSP operation.

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 μF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{TA}}$, and $\overline{\text{BG}}$ pins. Maximum PCB trace lengths on the order of 6 inches are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- Take special care to minimize noise levels on the V_{CCP} , GND_P , and GND_{P1} pins.
- The following pins must be asserted after power-up: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$.
- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- $\overline{\text{RESET}}$ must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of $\overline{\text{RESET}}$.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip V_{CC} never exceeds 3.5 V.

4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

Equation 3: $I = C \times V \times f$

Where:

| | | |
|---|---|------------------------------|
| C | = | node/pin capacitance |
| V | = | voltage swing |
| f | = | frequency of node/pin toggle |

Example 4-1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^6 = 5.48 \text{ mA}$

The maximum internal current (I_{CC1max}) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CC1typ}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.
6. Disable unused peripherals.
7. Disable unused pin activity (for example, CLKOUT, XTAL).

One way to evaluate power consumption is to use a current-per-MIPS measurement methodology to minimize specific board effects (that is, to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current-per-MIPS value.

Equation 5: $I/\text{MIPS} = I/\text{MHz} = (I_{\text{typF2}} - I_{\text{typF1}}) / (F2 - F1)$

Where:

| | | |
|--------------------|---|---|
| I_{typF2} | = | current at F2 |
| I_{typF1} | = | current at F1 |
| F2 | = | high frequency (any specified operating frequency) |
| F1 | = | low frequency (any specified operating frequency lower than F2) |

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

4.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no test that replicates these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

4.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2, External Clock Timing**, on page 2-5 for input frequencies greater than 15 MHz and the $MF \leq 4$, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for $MF < 10$ and input frequencies greater than 10 MHz, this skew is between -1.4 ns and $+3.2$ ns.

4.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and $MF \leq 4$, this jitter is less than ± 0.6 ns; otherwise, this jitter is not guaranteed. However, for $MF < 10$ and input frequencies greater than 10 MHz, this jitter is less than ± 2 ns.

4.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF ($MF < 10$) this jitter is smaller than 0.5 percent. For mid-range MF ($10 < MF < 500$) this jitter is between 0.5 percent and approximately 2 percent. For large MF ($MF > 500$), the frequency jitter is 2–3 percent.

4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

Input (EXTAL) Jitter Requirements

Appendix A

Power Consumption Benchmark

The following benchmark program evaluates DSP56303 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
*****
*****
;*
;* CHECKS    Typical Power Consumption          *
;*          *                                  *
*****

        page    200,55,0,0,0
        nolist

I_VEC EQU $000000; Interrupt vectors for program debug only
START EQU $8000; MAIN (external) program starting address
INT_PROG EQU $100 ; INTERNAL program memory starting address
INT_XDAT EQU $0; INTERNAL X-data memory starting address
INT_YDAT EQU $0; INTERNAL Y-data memory starting address

        INCLUDE "ioequ.asm"
        INCLUDE "integu.asm"

        list

        org     P:START
;
        movep  #$0243FF,x:M_BCR ;; BCR: Area 3 = 2 w.s (SRAM)
; Default: 2w.s (SRAM)
;
        movep  #$0d0000,x:M_PCTL      ; XTAL disable
;                                       ; PLL enable
;                                       ; CLKOUT disable
;
; Load the program
;
        move   #INT_PROG,r0
        move   #PROG_START,r1
        do     #(PROG_END-PROG_START),PLOAD_LOOP
        move   p:(r1)+,x0
        move   x0,p:(r0)+
        nop
PLOAD_LOOP
;
; Load the X-data
;
        move   #INT_XDAT,r0
        move   #XDAT_START,r1
        do     #(XDAT_END-XDAT_START),XLOAD_LOOP
        move   p:(r1)+,x0
        move   x0,x:(r0)+
XLOAD_LOOP
;
; Load the Y-data
;
        move   #INT_YDAT,r0
        move   #YDAT_START,r1
        do     #(YDAT_END-YDAT_START),YLOAD_LOOP
        move   p:(r1)+,x0
        move   x0,y:(r0)+
YLOAD_LOOP
;

        jmp    INT_PROG

PROG_START
        move   #$0,r0
        move   #$0,r4
        move   #$3f,m0
        move   #$3f,m4
;
        clr   a
```

Power Consumption Benchmark

```
        clr     b
        move   #$0,x0
        move   #$0,x1
        move   #$0,y0
        move   #$0,y1
        bset   #4,omr           ; ebd
;
sbr     dor     #60,_end
        mac    x0,y0,a x:(r0)+,x1   y:(r4)+,y1
        mac    x1,y1,a x:(r0)+,x0   y:(r4)+,y0
        add    a,b
        mac    x0,y0,a x:(r0)+,x1   y:(r4)+,y0
        mac    x1,y1,a               y:(r4)+,y0
        move   b1,x:$ff
_end
        bra    sbr
        nop
        nop
        nop
        nop
PROG_END
        nop
        nop

XDAT_START
;     org     x:0
        dc    $262EB9
        dc    $86F2FE
        dc    $E56A5F
        dc    $616CAC
        dc    $8FFD75
        dc    $9210A
        dc    $A06D7B
        dc    $CEA798
        dc    $8DFBF1
        dc    $A063D6
        dc    $6C6657
        dc    $C2A544
        dc    $A3662D
        dc    $A4E762
        dc    $84F0F3
        dc    $E6F1B0
        dc    $B3829
        dc    $8BF7AE
        dc    $63A94F
        dc    $EF78DC
        dc    $242DE5
        dc    $A3E0BA
        dc    $EBAB6B
        dc    $8726C8
        dc    $CA361
        dc    $2F6E86
        dc    $A57347
        dc    $4BE774
        dc    $8F349D
        dc    $A1ED12
        dc    $4BFCE3
        dc    $EA26E0
        dc    $CD7D99
        dc    $4BA85E
        dc    $27A43F
        dc    $A8B10C
        dc    $D3A55
        dc    $25EC6A
        dc    $2A255B
        dc    $A5F1F8
        dc    $2426D1
        dc    $AE6536
        dc    $CBBC37
        dc    $6235A4
        dc    $37F0D
        dc    $63BEC2
        dc    $A5E4D3
        dc    $8CE810
        dc    $3FF09
        dc    $60E50E
        dc    $CFFB2F
        dc    $40753C
        dc    $8262C5
        dc    $CA641A
```

```

dc      $EB3B4B
dc      $2DA928
dc      $AB6641
dc      $28A7E6
dc      $4E2127
dc      $482FD4
dc      $7257D
dc      $E53C72
dc      $1A8C3
dc      $E27540
XDAT_END

```

```

YDAT_START
;      org      y:0
dc      $5B6DA
dc      $C3F70B
dc      $6A39E8
dc      $81E801
dc      $C666A6
dc      $46F8E7
dc      $AAEC94
dc      $24233D
dc      $802732
dc      $2E3C83
dc      $A43E00
dc      $C2B639
dc      $85A47E
dc      $ABFDDF
dc      $F3A2C
dc      $2D7CF5
dc      $E16A8A
dc      $ECB8FB
dc      $4BED18
dc      $43F371
dc      $83A556
dc      $E1E9D7
dc      $ACA2C4
dc      $8135AD
dc      $2CE0E2
dc      $8F2C73
dc      $432730
dc      $A87FA9
dc      $4A292E
dc      $A63CCF
dc      $6BA65C
dc      $E06D65
dc      $1AA3A
dc      $A1B6EB
dc      $48AC48
dc      $EF7AE1
dc      $6E3006
dc      $62F6C7
dc      $6064F4
dc      $87E41D
dc      $CB2692
dc      $2C3863
dc      $C6BC60
dc      $43A519
dc      $6139DE
dc      $ADF7BF
dc      $4B3E8C
dc      $6079D5
dc      $E0F5EA
dc      $8230DB
dc      $A3B778
dc      $2BFE51
dc      $E0A6B6
dc      $68FFB7
dc      $28F324
dc      $8F2E8D
dc      $667842
dc      $83E053
dc      $A1FD90
dc      $6B2689
dc      $85B68E
dc      $622EAF
dc      $6162BC
dc      $E4A245
YDAT_END

```

```

;*****

```

Power Consumption Benchmark

```
;
;   EQUATES for DSP56303 I/O registers and ports
;
;   Last update: June 11 1995
;
;*****
;
;   page   132,55,0,0,0
;   opt    mex
;
ioequ   ident   1,0
;-----
;
;   EQUATES for I/O Port Programming
;
;-----
;
;   Register Addresses
;
M_HDR EQU $FFFFC9      ; Host port GPIO data Register
M_HDDR EQU $FFFFC8    ; Host port GPIO direction Register
M_PCRC EQU $FFFFBF    ; Port C Control Register
M_PRRC EQU $FFFFBE    ; Port C Direction Register
M_PDRC EQU $FFFFBD    ; Port C GPIO Data Register
M_PCRD EQU $FFFFAF    ; Port D Control register
M_PRRD EQU $FFFFAE    ; Port D Direction Data Register
M_PDRD EQU $FFFFAD    ; Port D GPIO Data Register
M_PCRE EQU $FFFF9F    ; Port E Control register
M_PPRE EQU $FFFF9E    ; Port E Direction Register
M_PDRE EQU $FFFF9D    ; Port E Data Register
M_OGDB EQU $FFFFFC    ; OnCE GDB Register
;-----
;
;   EQUATES for Host Interface
;
;-----
;
;   Register Addresses
;
M_HCR EQU $FFFFC2      ; Host Control Register
M_HSR EQU $FFFFC3      ; Host Status Register
M_HPCR EQU $FFFFC4     ; Host Polarity Control Register
M_HBAR EQU $FFFFC5     ; Host Base Address Register
M_HRX EQU $FFFFC6      ; Host Receive Register
M_HTX EQU $FFFFC7      ; Host Transmit Register
;
;   HCR bits definition
M_HRIE EQU $0          ; Host Receive interrupts Enable
M_HTIE EQU $1          ; Host Transmit Interrupt Enable
M_HCIE EQU $2          ; Host Command Interrupt Enable
M_HF2 EQU $3           ; Host Flag 2
M_HF3 EQU $4           ; Host Flag 3
;
;   HSR bits definition
M_HRDF EQU $0          ; Host Receive Data Full
M_HTDE EQU $1          ; Host Receive Data Empty
M_HCP EQU $2           ; Host Command Pending
M_HF0 EQU $3           ; Host Flag 0
M_HF1 EQU $4           ; Host Flag 1
;
;   HPCR bits definition
M_HGEN EQU $0          ; Host Port GPIO Enable
M_HA8EN EQU $1         ; Host Address 8 Enable
M_HA9EN EQU $2         ; Host Address 9 Enable
M_HCSEN EQU $3         ; Host Chip Select Enable
M_HREN EQU $4          ; Host Request Enable
M_HAEN EQU $5          ; Host Acknowledge Enable
M_HEN EQU $6           ; Host Enable
M_HOD EQU $8           ; Host Request Open Drain mode
M_HDSP EQU $9          ; Host Data Strobe Polarity
M_HASP EQU $A          ; Host Address Strobe Polarity
M_HMUX EQU $B          ; Host Multiplexed bus select
M_HD_HS EQU $C         ; Host Double/Single Strobe select
M_HCSP EQU $D          ; Host Chip Select Polarity
M_HRP EQU $E           ; Host Request Polarity
M_HAP EQU $F           ; Host Acknowledge Polarity
```

```

;-----
;
;      EQUATES for Serial Communications Interface (SCI)
;
;-----

;      Register Addresses

M_STXH EQU $FFFF97      ; SCI Transmit Data Register (high)
M_STXM EQU $FFFF96      ; SCI Transmit Data Register (middle)
M_STXL EQU $FFFF95      ; SCI Transmit Data Register (low)
M_SRXH EQU $FFFF9A      ; SCI Receive Data Register (high)
M_SRXM EQU $FFFF99      ; SCI Receive Data Register (middle)
M_SRXL EQU $FFFF98      ; SCI Receive Data Register (low)
M_STXA EQU $FFFF94      ; SCI Transmit Address Register
M_SCR EQU $FFFF9C       ; SCI Control Register
M_SSR EQU $FFFF93       ; SCI Status Register
M_SCCR EQU $FFFF9B      ; SCI Clock Control Register

;      SCI Control Register Bit Flags

M_WDS EQU $7            ; Word Select Mask (WDS0-WDS3)
M_WDS0 EQU 0            ; Word Select 0
M_WDS1 EQU 1            ; Word Select 1
M_WDS2 EQU 2            ; Word Select 2
M_SSFTD EQU 3          ; SCI Shift Direction
M_SBK EQU 4             ; Send Break
M_WAKE EQU 5            ; Wakeup Mode Select
M_RWU EQU 6             ; Receiver Wakeup Enable
M_WOMS EQU 7            ; Wired-OR Mode Select
M_SCRE EQU 8            ; SCI Receiver Enable
M_SCTE EQU 9            ; SCI Transmitter Enable
M_ILIE EQU 10           ; Idle Line Interrupt Enable
M_SCRIE EQU 11          ; SCI Receive Interrupt Enable
M_SCTIE EQU 12          ; SCI Transmit Interrupt Enable
M_TMIE EQU 13           ; Timer Interrupt Enable
M_TIR EQU 14            ; Timer Interrupt Rate
M_SCKP EQU 15           ; SCI Clock Polarity
M_REIE EQU 16           ; SCI Error Interrupt Enable (REIE)

;      SCI Status Register Bit Flags

M_TRNE EQU 0            ; Transmitter Empty
M_TDRE EQU 1            ; Transmit Data Register Empty
M_RDRF EQU 2            ; Receive Data Register Full
M_IDLE EQU 3            ; Idle Line Flag
M_OR EQU 4              ; Overrun Error Flag
M_PE EQU 5              ; Parity Error
M_FE EQU 6              ; Framing Error Flag
M_R8 EQU 7              ; Received Bit 8 (R8) Address

;      SCI Clock Control Register

M_CD EQU $FFF           ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12            ; Clock Out Divider
M_SCP EQU 13            ; Clock Prescaler
M_RCM EQU 14            ; Receive Clock Mode Source Bit
M_TCM EQU 15            ; Transmit Clock Source Bit

;-----
;
;      EQUATES for Synchronous Serial Interface (SSI)
;
;-----

;
;      Register Addresses Of SSI0

M_TX00 EQU $FFFFBC      ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFB8      ; SSI0 Transmit Data Register 1
M_TX02 EQU $FFFFB4      ; SSI0 Transmit Data Register 2
M_TSRO EQU $FFFFB9      ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8       ; SSI0 Receive Data Register
M_SISR0 EQU $FFFFB7     ; SSI0 Status Register
M_CRB0 EQU $FFFFB6      ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5      ; SSI0 Control Register A
M_TSMAB EQU $FFFFB4     ; SSI0 Transmit Slot Mask Register A
M_TSMAB EQU $FFFFB3     ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2     ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1     ; SSI0 Receive Slot Mask Register B

```

Power Consumption Benchmark

```
; Register Addresses Of SSI1
M_TX10 EQU $FFFFAC      ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB      ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA      ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9      ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8       ; SSI1 Receive Data Register
M_SISR1 EQU $FFFFA7     ; SSI1 Status Register
M_CRB1 EQU $FFFFA6      ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5      ; SSI1 Control Register A
M_TSM1 EQU $FFFFA4      ; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3     ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2     ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1     ; SSI1 Receive Slot Mask Register B

; SSI Control Register A Bit Flags
M_PM EQU $FF            ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11           ; Prescaler Range
M_DC EQU $1F000        ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18           ; Alignment Control (ALC)
M_WL EQU $380000       ; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22          ; Select SC1 as TR #0 drive enable (SSC1)

; SSI Control Register B Bit Flags
M_OF EQU $3            ; Serial Output Flag Mask
M_OF0 EQU 0            ; Serial Output Flag 0
M_OF1 EQU 1            ; Serial Output Flag 1
M_SCD EQU $1C          ; Serial Control Direction Mask
M_SCD0 EQU 2           ; Serial Control 0 Direction
M_SCD1 EQU 3           ; Serial Control 1 Direction
M_SCD2 EQU 4           ; Serial Control 2 Direction
M_SCKD EQU 5           ; Clock Source Direction
M_SHFD EQU 6           ; Shift Direction
M_FSL EQU $180         ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7           ; Frame Sync Length 0
M_FSL1 EQU 8           ; Frame Sync Length 1
M_FSR EQU 9            ; Frame Sync Relative Timing
M_FSP EQU 10           ; Frame Sync Polarity
M_CKP EQU 11           ; Clock Polarity
M_SYN EQU 12           ; Sync/Async Control
M_MOD EQU 13           ; SSI Mode Select
M_SSTE EQU $1C000      ; SSI Transmit enable Mask
M_SSTE2 EQU 14         ; SSI Transmit #2 Enable
M_SSTE1 EQU 15         ; SSI Transmit #1 Enable
M_SSTE0 EQU 16         ; SSI Transmit #0 Enable
M_SSRE EQU 17          ; SSI Receive Enable
M_SSTIE EQU 18         ; SSI Transmit Interrupt Enable
M_SSRIE EQU 19         ; SSI Receive Interrupt Enable
M_STLIE EQU 20         ; SSI Transmit Last Slot Interrupt Enable
M_SRLIE EQU 21         ; SSI Receive Last Slot Interrupt Enable
M_STEIE EQU 22         ; SSI Transmit Error Interrupt Enable
M_SREIE EQU 23        ; SI Receive Error Interrupt Enable

; SSI Status Register Bit Flags
M_IF EQU $3            ; Serial Input Flag Mask
M_IF0 EQU 0            ; Serial Input Flag 0
M_IF1 EQU 1            ; Serial Input Flag 1
M_TFS EQU 2            ; Transmit Frame Sync Flag
M_RFS EQU 3            ; Receive Frame Sync Flag
M_TUE EQU 4            ; Transmitter Underrun Error Flag
M_ROE EQU 5            ; Receiver Overrun Error Flag
M_TDE EQU 6            ; Transmit Data Register Empty
M_RDF EQU 7            ; Receive Data Register Full

; SSI Transmit Slot Mask Register A
M_SSTSA EQU $FFFF      ; SSI Transmit Slot Bits Mask A (TS0-TS15)

; SSI Transmit Slot Mask Register B
M_SSTSB EQU $FFFF      ; SSI Transmit Slot Bits Mask B (TS16-TS31)

; SSI Receive Slot Mask Register A
M_SSRSA EQU $FFFF      ; SSI Receive Slot Bits Mask A (RS0-RS15)

; SSI Receive Slot Mask Register B
M_SSRSB EQU $FFFF      ; SSI Receive Slot Bits Mask B (RS16-RS31)
```

```

;-----
;
;      EQUATES for Exception Processing
;-----

;      Register Addresses

M_IPRC EQU $FFFFFF      ; Interrupt Priority Register Core
M_IPRP EQU $FFFFFFE    ; Interrupt Priority Register Peripheral

;      Interrupt Priority Register Core (IPRC)

M_IAL EQU $7           ; IRQA Mode Mask
M_IAL0 EQU 0           ; IRQA Mode Interrupt Priority Level (low)
M_IAL1 EQU 1           ; IRQA Mode Interrupt Priority Level (high)
M_IAL2 EQU 2           ; IRQA Mode Trigger Mode
M_IBL EQU $38          ; IRQB Mode Mask
M_IBL0 EQU 3           ; IRQB Mode Interrupt Priority Level (low)
M_IBL1 EQU 4           ; IRQB Mode Interrupt Priority Level (high)
M_IBL2 EQU 5           ; IRQB Mode Trigger Mode
M_ICL EQU $1C0         ; IRQC Mode Mask
M_ICL0 EQU 6           ; IRQC Mode Interrupt Priority Level (low)
M_ICL1 EQU 7           ; IRQC Mode Interrupt Priority Level (high)
M_ICL2 EQU 8           ; IRQC Mode Trigger Mode
M_IDL EQU $E00         ; IRQD Mode Mask
M_IDL0 EQU 9           ; IRQD Mode Interrupt Priority Level (low)
M_IDL1 EQU 10          ; IRQD Mode Interrupt Priority Level (high)
M_IDL2 EQU 11          ; IRQD Mode Trigger Mode
M_D0L EQU $3000        ; DMA0 Interrupt priority Level Mask
M_D0L0 EQU 12          ; DMA0 Interrupt Priority Level (low)
M_D0L1 EQU 13          ; DMA0 Interrupt Priority Level (high)
M_D1L EQU $C000        ; DMA1 Interrupt Priority Level Mask
M_D1L0 EQU 14          ; DMA1 Interrupt Priority Level (low)
M_D1L1 EQU 15          ; DMA1 Interrupt Priority Level (high)
M_D2L EQU $30000       ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16          ; DMA2 Interrupt Priority Level (low)
M_D2L1 EQU 17          ; DMA2 Interrupt Priority Level (high)
M_D3L EQU $C0000       ; DMA3 Interrupt Priority Level Mask
M_D3L0 EQU 18          ; DMA3 Interrupt Priority Level (low)
M_D3L1 EQU 19          ; DMA3 Interrupt Priority Level (high)
M_D4L EQU $300000      ; DMA4 Interrupt priority Level Mask
M_D4L0 EQU 20          ; DMA4 Interrupt Priority Level (low)
M_D4L1 EQU 21          ; DMA4 Interrupt Priority Level (high)
M_D5L EQU $C00000      ; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22          ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23          ; DMA5 Interrupt Priority Level (high)

;      Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3           ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0           ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1           ; Host Interrupt Priority Level (high)
M_S0L EQU $C           ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2           ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3           ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30          ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4           ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5           ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0          ; SCI Interrupt Priority Level Mask
M_SCL0 EQU 6           ; SCI Interrupt Priority Level (low)
M_SCL1 EQU 7           ; SCI Interrupt Priority Level (high)
M_T0L EQU $300         ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8           ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9           ; TIMER Interrupt Priority Level (high)

;-----
;
;      EQUATES for TIMER
;-----

;      Register Addresses Of TIMER0

M_TCSR0 EQU $FFFF8F    ; Timer 0 Control/Status Register

```

Power Consumption Benchmark

```
M_TLR0 EQU $FFFF8E ; TIMER0 Load Reg
M_TLCPRO EQU $FFFF8D ; TIMER0 Compare Register
M_TCR0 EQU $FFFF8C ; TIMER0 Count Register

; Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B ; TIMER1 Control/Status Register
M_TLR1 EQU $FFFF8A ; TIMER1 Load Reg
M_TLCPR1 EQU $FFFF89 ; TIMER1 Compare Register
M_TCR1 EQU $FFFF88 ; TIMER1 Count Register

; Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87 ; TIMER2 Control/Status Register
M_TLR2 EQU $FFFF86 ; TIMER2 Load Reg
M_TLCPR2 EQU $FFFF85 ; TIMER2 Compare Register
M_TCR2 EQU $FFFF84 ; TIMER2 Count Register
M_TPLR EQU $FFFF83 ; TIMER Prescaler Load Register
M_TPCR EQU $FFFF82 ; TIMER Prescaler Count Register

; Timer Control/Status Register Bit Flags

M_TE EQU 0 ; Timer Enable
M_TOIE EQU 1 ; Timer Overflow Interrupt Enable
M_TCIE EQU 2 ; Timer Compare Interrupt Enable
M_TC EQU $F0 ; Timer Control Mask (TC0-TC3)
M_INV EQU 8 ; Inverter Bit
M_TRM EQU 9 ; Timer Restart Mode
M_DIR EQU 11 ; Direction Bit
M_DI EQU 12 ; Data Input
M_DO EQU 13 ; Data Output
M_PCE EQU 15 ; Prescaled Clock Enable
M_TOF EQU 20 ; Timer Overflow Flag
M_TCF EQU 21 ; Timer Compare Flag

; Timer Prescaler Register Bit Flags

M_PS EQU $600000 ; Prescaler Source Mask
M_PS0 EQU 21
M_PS1 EQU 22

; Timer Control Bits

M_TC0 EQU 4 ; Timer Control 0
M_TC1 EQU 5 ; Timer Control 1
M_TC2 EQU 6 ; Timer Control 2
M_TC3 EQU 7 ; Timer Control 3

;-----
;
; EQUATES for Direct Memory Access (DMA)
;-----

; Register Addresses Of DMA
M_DSTR EQU $FFFFF4 ; DMA Status Register
M_DOR0 EQU $FFFFF3 ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2 ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1 ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0 ; DMA Offset Register 3

; Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED ; DMA0 Counter
M_DCR0 EQU $FFFFEC ; DMA0 Control Register

; Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9 ; DMA1 Counter
M_DCR1 EQU $FFFFE8 ; DMA1 Control Register

; Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7 ; DMA2 Source Address Register
```



```

M_DDR2 EQU $FFFFE6 ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5 ; DMA2 Counter
M_DCR2 EQU $FFFFE4 ; DMA2 Control Register

;      Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3 ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2 ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1 ; DMA3 Counter
M_DCR3 EQU $FFFFE0 ; DMA3 Control Register

;      Register Addresses Of DMA4

M_DSR4 EQU $FFFFDF ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD ; DMA4 Counter
M_DCR4 EQU $FFFFDC ; DMA4 Control Register

;      Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9 ; DMA5 Counter
M_DCR5 EQU $FFFFD8 ; DMA5 Control Register

;      DMA Control Register

M_DSS EQU $3      ; DMA Source Space Mask (DSS0-DSS1)
M_DSS0 EQU 0      ; DMA Source Memory space 0
M_DSS1 EQU 1      ; DMA Source Memory space 1
M_DDS EQU $C      ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2      ; DMA Destination Memory Space 0
M_DDS1 EQU 3      ; DMA Destination Memory Space 1
M_DAM EQU $3f0    ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0 EQU 4      ; DMA Address Mode 0
M_DAM1 EQU 5      ; DMA Address Mode 1
M_DAM2 EQU 6      ; DMA Address Mode 2
M_DAM3 EQU 7      ; DMA Address Mode 3
M_DAM4 EQU 8      ; DMA Address Mode 4
M_DAM5 EQU 9      ; DMA Address Mode 5
M_D3D EQU 10     ; DMA Three Dimensional Mode
M_DRS EQU $F800 ; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16    ; DMA Continuous Mode
M_DPR EQU $60000 ; DMA Channel Priority
M_DPR0 EQU 17   ; DMA Channel Priority Level (low)
M_DPR1 EQU 18   ; DMA Channel Priority Level (high)
M_DTM EQU $380000 ; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19   ; DMA Transfer Mode 0
M_DTM1 EQU 20   ; DMA Transfer Mode 1
M_DTM2 EQU 21   ; DMA Transfer Mode 2
M_DIE EQU 22    ; DMA Interrupt Enable bit
M_DE EQU 23     ; DMA Channel Enable bit

;      DMA Status Register

M_DTD EQU $3F    ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0    ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1    ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2    ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3    ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4    ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5    ; DMA Channel Transfer Done Status 5
M_DACT EQU 8     ; DMA Active State
M_DCH EQU $E00   ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU 9    ; DMA Active Channel 0
M_DCH1 EQU 10   ; DMA Active Channel 1
M_DCH2 EQU 11   ; DMA Active Channel 2

;-----
;
;      EQUATES for Enhanced Filter Co-Processor (EFCOP)
;-----
M_FDIR EQU $FFFFB0 ; EFCOP Data Input Register
M_FDOR EQU $FFFFB1 ; EFCOP Data Output Register
M_FKIR EQU $FFFFB2 ; EFCOP K-Constant Register
M_FCNT EQU $FFFFB3 ; EFCOP Filter Counter
M_FCSR EQU $FFFFB4 ; EFCOP Control Status Register
M_FACR EQU $FFFFB5 ; EFCOP ALU Control Register

```

Power Consumption Benchmark

```
M_FDBA EQU $FFFFB6 ; EFCOP Data Base Address
M_FCBA EQU $FFFFB7 ; EFCOP Coefficient Base Address
M_FDCH EQU $FFFFB8 ; EFCOP Decimation/Channel Register

;-----
;
; EQUATES for Phase Locked Loop (PLL)
;-----
;
; Register Addresses Of PLL
M_PCTL EQU $FFFFFFD ; PLL Control Register
;
; PLL Control Register
M_MF EQU $FFF ; Multiplication Factor Bits Mask (MF0-MF11)
M_DF EQU $7000 ; Division Factor Bits Mask (DF0-DF2)
M_XTLR EQU 15 ; XTAL Range select bit
M_XTLD EQU 16 ; XTAL Disable Bit
M_PSTP EQU 17 ; STOP Processing State Bit
M_PEN EQU 18 ; PLL Enable Bit
M_PCOD EQU 19 ; PLL Clock Output Disable Bit
M_PD EQU $F00000; PreDivider Factor Bits Mask (PD0-PD3)

;-----
;
; EQUATES for BIU
;-----
;
; Register Addresses Of BIU
M_BCR EQU $FFFFFFB; Bus Control Register
M_DCR EQU $FFFFFFA; DRAM Control Register
M_AAR0 EQU $FFFFFF9; Address Attribute Register 0
M_AAR1 EQU $FFFFFF8; Address Attribute Register 1
M_AAR2 EQU $FFFFFF7; Address Attribute Register 2
M_AAR3 EQU $FFFFFF6; Address Attribute Register 3
M_IDR EQU $FFFFFF5 ; ID Register
;
; Bus Control Register
M_BA0W EQU $1F ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0; Area 1 Wait Control Mask (BA1W0-BA14)
M_BA2W EQU $1C00; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000 ; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21 ; Bus State
M_BLH EQU 22 ; Bus Lock Hold
M_BRH EQU 23 ; Bus Request Hold
;
; DRAM Control Register
M_BCW EQU $3 ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300 ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11 ; Page Logic Enable
M_BME EQU 12 ; Mastership Enable
M_BRE EQU 13 ; Refresh Enable
M_BSTR EQU 14 ; Software Triggered Refresh
M_BRF EQU $7F8000; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23 ; Refresh prescaler
;
; Address Attribute Registers
M_BAT EQU $3 ; Ext. Access Type and Pin Def. Bits Mask (BAT0-BAT1)
M_BAAP EQU 2 ; Address Attribute Pin Polarity
M_BPEN EQU 3 ; Program Space Enable
M_BXEN EQU 4 ; X Data Space Enable
M_BYEN EQU 5 ; Y Data Space Enable
M_BAM EQU 6 ; Address Muxing
M_BPAC EQU 7 ; Packing Enable
M_BNC EQU $F00 ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000; Address to Compare Bits Mask (BAC0-BAC11)
```

```

;          control and status bits in SR
M_CP EQU $c00000; mask for CORE-DMA priority bits in SR
M_CA EQU 0      ; Carry
M_V EQU 1      ; Overflow
M_Z EQU 2      ; Zero
M_N EQU 3      ; Negative
M_U EQU 4      ; Unnormalized
M_E EQU 5      ; Extension
M_L EQU 6      ; Limit
M_S EQU 7      ; Scaling Bit
M_I0 EQU 8     ; Interupt Mask Bit 0
M_I1 EQU 9     ; Interupt Mask Bit 1
M_S0 EQU 10    ; Scaling Mode Bit 0
M_S1 EQU 11    ; Scaling Mode Bit 1
M_SC EQU 13    ; Sixteen_Bit Compatibility
M_DM EQU 14    ; Double Precision Multiply
M_LF EQU 15    ; DO-Loop Flag
M_FV EQU 16    ; DO-Forever Flag
M_SA EQU 17    ; Sixteen-Bit Arithmetic
M_CE EQU 19    ; Instruction Cache Enable
M_SM EQU 20    ; Arithmetic Saturation
M_RM EQU 21    ; Rounding Mode
M_CP0 EQU 22   ; bit 0 of priority bits in SR
M_CP1 EQU 23   ; bit 1 of priority bits in SR

;          control and status bits in OMR
M_CDP EQU $300 ; mask for CORE-DMA priority bits in OMR
M_MA EQU 0     ; Operating Mode A
M_MB EQU 1     ; Operating Mode B
M_MC EQU 2     ; Operating Mode C
M_MD EQU 3     ; Operating Mode D
M_EBD EQU 4    ; External Bus Disable bit in OMR
M_SD EQU 6     ; Stop Delay
M_MS EQU 7     ; Memory Switch bit in OMR
M_CDP0 EQU 8   ; bit 0 of priority bits in OMR
M_CDP1 EQU 9   ; bit 1 of priority bits in OMR
M_BEN EQU 10   ; Burst Enable
M_TAS EQU 11   ; TA Synchronize Select
M_BRT EQU 12   ; Bus Release Timing
M_ATE EQU 15   ; Address Tracing Enable bit in OMR.
M_XYS EQU 16   ; Stack Extension space select bit in OMR.
M_EUN EQU 17   ; Extended stack UNDERflow flag in OMR.
M_EOV EQU 18   ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19   ; Extended WRAP flag in OMR.
M_SEN EQU 20   ; Stack Extension Enable bit in OMR.

;*****
;
;          EQUATES for DSP56303 interrupts
;
;          Last update: June 11 1995
;*****

        page    132,55,0,0,0
        opt     mex

intequ  ident    1,0

        if      @DEF(I_VEC)
        ;leave user definition as is.
        else
I_VEC EQU $0
        endif

;-----
; Non-Maskable interrupts
;-----
I_RESET EQU I_VEC+$00 ; Hardware RESET
I_STACK EQU I_VEC+$02 ; Stack Error
I_ILL EQU I_VEC+$04   ; Illegal Instruction
I_DBG EQU I_VEC+$06   ; Debug Request

```

Power Consumption Benchmark

```
I_TRAP EQU I_VEC+$08 ; Trap
I_NMI EQU I_VEC+$0A ; Non Maskable Interrupt

;-----
; Interrupt Request Pins
;-----
I_IRQA EQU I_VEC+$10 ; IRQA
I_IRQB EQU I_VEC+$12 ; IRQB
I_IRQC EQU I_VEC+$14 ; IRQC
I_IRQD EQU I_VEC+$16 ; IRQD

;-----
; DMA Interrupts
;-----
I_DMA0 EQU I_VEC+$18 ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E ; DMA Channel 3
I_DMA4 EQU I_VEC+$20 ; DMA Channel 4
I_DMA5 EQU I_VEC+$22 ; DMA Channel 5

;-----
; Timer Interrupts
;-----
I_TIMER0 EQU I_VEC+$24 ; TIMER 0 compare
I_TIMER0OF EQU I_VEC+$26 ; TIMER 0 overflow
I_TIMER1 EQU I_VEC+$28 ; TIMER 1 compare
I_TIMER1OF EQU I_VEC+$2A ; TIMER 1 overflow
I_TIMER2 EQU I_VEC+$2C ; TIMER 2 compare
I_TIMER2OF EQU I_VEC+$2E ; TIMER 2 overflow

;-----
; ESSI Interrupts
;-----
I_SSI0RD EQU I_VEC+$30 ; ESSI0 Receive Data
I_SSI0RDE EQU I_VEC+$32 ; ESSI0 Receive Data w/ exception Status
I_SSI0RLS EQU I_VEC+$34 ; ESSI0 Receive last slot
I_SSI0TD EQU I_VEC+$36 ; ESSI0 Transmit data
I_SSI0TDE EQU I_VEC+$38 ; ESSI0 Transmit Data w/ exception Status
I_SSI0TLS EQU I_VEC+$3A ; ESSI0 Transmit last slot
I_SSI1RD EQU I_VEC+$40 ; ESSI1 Receive Data
I_SSI1RDE EQU I_VEC+$42 ; ESSI1 Receive Data w/ exception Status
I_SSI1RLS EQU I_VEC+$44 ; ESSI1 Receive last slot
I_SSI1TD EQU I_VEC+$46 ; ESSI1 Transmit data
I_SSI1TDE EQU I_VEC+$48 ; ESSI1 Transmit Data w/ exception Status
I_SSI1TLS EQU I_VEC+$4A ; ESSI1 Transmit last slot

;-----
; SCI Interrupts
;-----
I_SCIRD EQU I_VEC+$50 ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52 ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54 ; SCI Transmit Data
I_SCIIL EQU I_VEC+$56 ; SCI Idle Line
I_SCITM EQU I_VEC+$58 ; SCI Timer

;-----
; HOST Interrupts
;-----
I_HRDF EQU I_VEC+$60 ; Host Receive Data Full
I_HTDE EQU I_VEC+$62 ; Host Transmit Data Empty
I_HC EQU I_VEC+$64 ; Default Host Command

;-----
; EFCOP Filter Interrupts
;-----
I_FDIIE EQU I_VEC+$68 ; EFilter input buffer empty
I_FDOIIE EQU I_VEC+$6A ; EFilter output buffer full

;-----
; INTERRUPT ENDING ADDRESS
;-----
I_INTEND EQU I_VEC+$FF ; last address of interrupt vector space
```

Index

A

- ac electrical characteristics 2-4
- address bus 1-1
- Address Trace mode 2-25, 2-27
- applications iv
- arbitration bus timings 2-27

B

- benchmark test algorithm A-1
- block diagram i
- bootstrap ROM iii
- Boundary Scan (JTAG Port) timing diagram 2-46
- bus
 - acquisition timings 2-28
 - address 1-2
 - control 1-1
 - data 1-2
 - external address 1-5
 - external data 1-5
 - multiplexed 1-2
 - non-multiplexed 1-2
 - release timings 2-28, 2-29

C

- clock 1-1, 1-4
 - external 2-4
- clocks
 - internal 2-4
- crystal oscillator circuits 2-5

D

- data bus 1-1
- data memory expansion iv
- Data Strobe (DS) 1-2
- dc electrical characteristics 2-3
- \overline{DE} signal 1-18
- Debug Event signal (\overline{DE} signal) 1-18
- Debug mode
 - entering 1-18
 - external indication 1-18
- Debug support iii
- design considerations
 - electrical 4-2, 4-3
 - PLL 4-5
 - power consumption 4-4
 - thermal 4-1
- documentation list iv
- Double Data Strobe 1-2
- DRAM
 - controller iv

- out of page
 - read access 2-23
 - wait states selection guide 2-20
 - write access 2-24
- Page mode
 - read accesses 2-19
 - wait states selection guide 2-16
 - write accesses 2-19
- refresh access 2-24

DSP56300

- Family Manual iv

DSP56303

- block diagram i
- Technical Data iv
- User's Manual iv

E

EFCOP

- interrupts A-12

electrical

- design considerations 4-2, 4-3

Enhanced Synchronous Serial Interface (ESSI) iii,

- 1-1, 1-2, 1-13, 1-14

- receiver timing 2-42

- transmitter timing 2-41

- external address bus 1-5

- external bus control 1-5, 1-6, 1-7

- external bus synchronous timings (SRAM access) 2-25

- external clock operation 2-4

- external data bus 1-5

- external interrupt timing (negative edge-triggered) 2-11

- external level-sensitive fast interrupt timing 2-10

- external memory access (DMA Source) timing 2-12

- External Memory Expansion Port 2-13

- external memory expansion port 1-5

F

- functional groups 1-2

- functional signal groups 1-1

G

- General-Purpose Input/Output (GPIO) iii, 1-2

- ground 1-1, 1-3

- PLL 1-3

H

Host Interface (HI08) iii, 1-1, 1-2, 1-9, 1-10, 1-11, 1-12
 Host Port Control Register (HPCR) 1-10, 1-12
 host port
 configuration 1-9
 usage considerations 1-9
 Host Port Control Register (HPCR) 1-10, 1-12
 Host Request
 Double 1-2
 Single 1-2
 Host Request (HR) 1-2

I

information sources iv
 instruction cache iii
 internal clocks 2-4
 interrupt and mode control 1-1, 1-8
 interrupt control 1-8
 interrupt timing 2-7
 external level-sensitive fast 2-10
 external negative edge-triggered 2-11
 synchronous from Wait state 2-11
 interrupts
 EFCOP A-12

J

Joint Test Action Group (JTAG)
 interface 1-18
 JTAG iii
 JTAG Port
 reset timing diagram 2-46
 timing 2-46
 JTAG/OnCE Interface signals
 Debug Event signal (DE signal) 1-18
 JTAG/OnCE port 1-1, 1-2

M

MAP-BGA 3-1
 ball list by name 3-15
 ball list by number 3-12
 mechanical drawing 3-19
 molded array process-ball grid drawing (bottom) 3-11
 molded array process-ball grid drawing (top) 3-10
 maximum ratings 2-1, 2-2
 memory expansion port iii
 mode control 1-8

Mode select timing 2-7
 multiplexed bus 1-2
 multiplexed bus timings
 read 2-35
 write 2-36

N

non-multiplexed bus 1-2
 non-multiplexed bus timings
 read 2-33
 write 2-34

O

off-chip memory iii
 OnCE module iii
 Debug request 2-47
 on-chip DRAM controller iv
 On-Chip Emulation (OnCE) module
 interface 1-18
 On-Chip Emulation module iii
 on-chip memory iii
 operating mode select timing 2-11

P

package
 144-pin TQFP 3-1
 196-pin MAP-BGA 3-1
 MAP-BGA description 3-10, 3-11, 3-12, 3-15, 3-19
 TQFP description 3-2, 3-3, 3-4, 3-6, 3-9
 Phase-Lock Loop (PLL) 1-1, 2-6
 design considerations 4-5
 performance issues 4-5
 PLL 1-4
 Port A 1-1, 1-5, 2-13
 Port B 1-1, 1-2, 1-11
 Port C 1-1, 1-2, 1-13
 Port D 1-1, 1-2, 1-14
 Port E 1-1
 power 1-1, 1-2, 1-3
 power consumption
 design considerations 4-4
 power consumption benchmark test A-1
 power management iv
 program memory expansion iv
 program RAM iii

R

recovery from Stop state using IRQA 2-12
 reset
 clock signals 1-4

- interrupt signals 1-8
- JTAG signals 1-18
- mode control 1-8
- OnCE signals 1-18
- PLL signals 1-4
- Reset timing 2-7, 2-9
 - synchronous 2-10
- ROM, bootstrap iii

S

- Serial Communication Interface (SCI) iii, 1-1, 1-2, 1-16
 - Asynchronous mode timing 2-38
 - Synchronous mode timing 2-38
- signal groupings 1-1
- signals 1-1
 - functional grouping 1-2
- Single Data Strobe 1-2
- SRAM
 - read access 2-15
 - support iv
 - write access 2-15
- Stop mode iv
- Stop state
 - recovery from 2-12
- Stop timing 2-7
- supply voltage 2-2
- Switch mode iii
- synchronous bus timings
 - SRAM
 - 2 wait states 2-26
 - SRAM 1 wait state (BCR controlled) 2-26
- synchronous interrupt from Wait state timing 2-11
- synchronous Reset timing 2-10

T

- target applications iv
- Test Access Port (TAP) iii
 - timing diagram 2-46
- Test Clock (TCLK) input timing diagram 2-45
- thermal
 - design considerations 4-1
- Timer
 - event input restrictions 2-43
- Timers 1-1, 1-2, 1-17
 - interrupt generation 2-43
- TQFP 3-1
 - mechanical drawing 3-9
 - pin list by name 3-6
 - pin list by number 3-4
 - pin-out drawing (bottom) 3-3
 - pin-out drawing (top) 3-2

W

- Wait mode iv
- World Wide Web iv

X

- X-data RAM iii

Y

- Y-data RAM iii

Ordering Information

Consult a Motorola Semiconductor sales office or authorized distributor to determine product availability and place an order.

| Part | Supply Voltage | Package Type | Pin Count | Core Frequency (MHz) | Order Number |
|----------|----------------|--|-----------|----------------------|---------------|
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