Freescale Semiconductor
Data Sheet: Technical Data

DSP56371
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DSP56371 Data Sheet

1 Introduction

The DSP56371 is a high density CMOS device with 5.0-V compatible inputs and outputs.

NOTE

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Finalized specifications may be published after further characterization and device qualifications are completed.

For software or simulation models (for example, IBIS files), contact sales or go to www.freescale.com.

2 DSP56371 Overview

2.1 Introduction

This manual describes the DSP56371 24-bit digital signal processor (DSP), its memory, operating modes and peripheral modules. The DSP56371 is a member of

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the DSP56300 family of programmable CMOS DSPs. The DSP56371 is targeted to applications that require digital audio compression/decompression, sound field processing, acoustic equalization and other digital audio algorithms. Changes in core functionality specific to the DSP56371 are also described in this manual. See Figure 1. for the block diagram of the DSP56371.

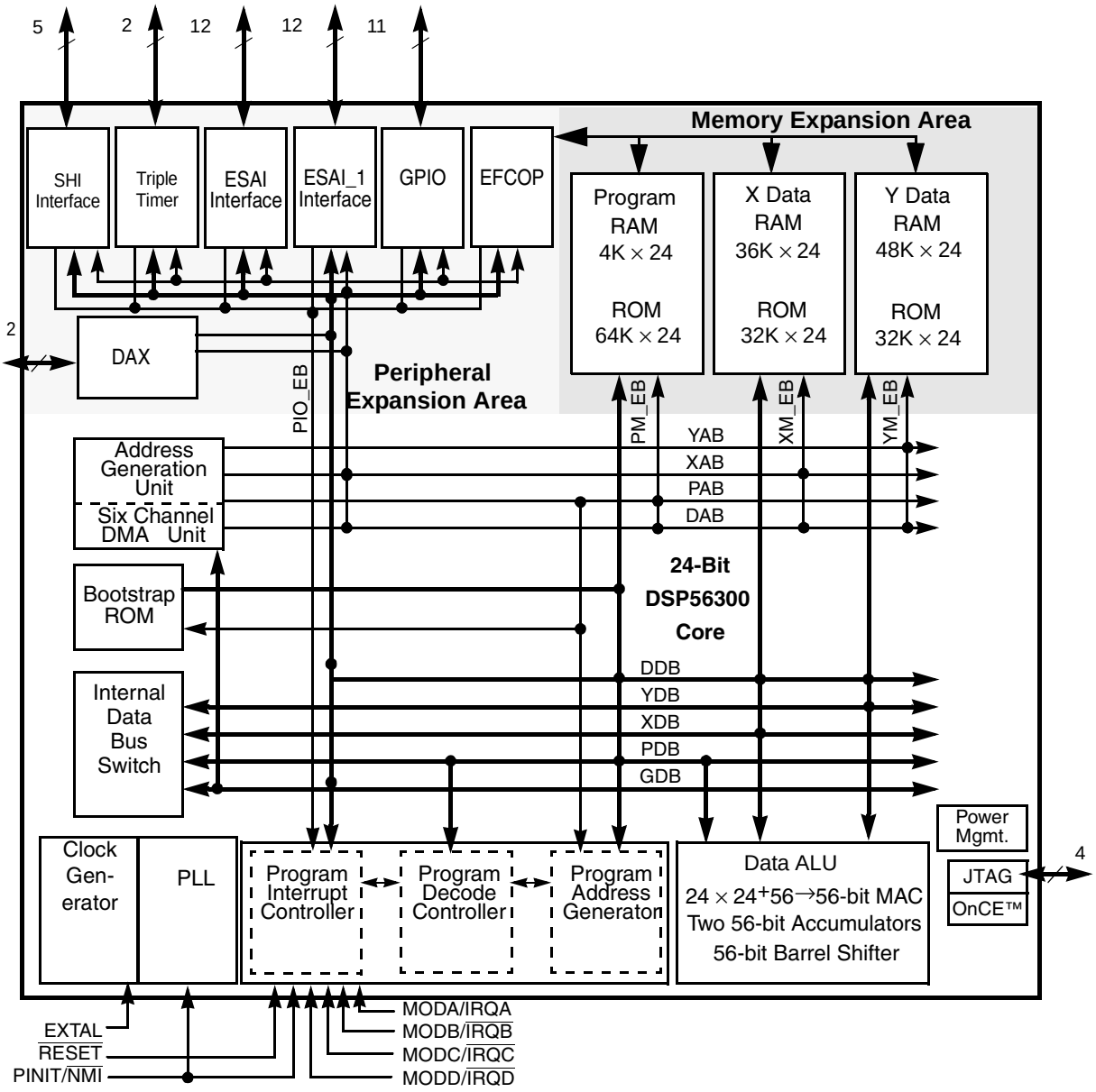


Figure 1. DSP56371 Block Diagram

2.2 DSP56300 Core Description

The DSP56371 uses the DSP56300 core, a high-performance, single clock cycle per instruction engine that provides up to twice the performance of Motorola's popular DSP56000 core family while retaining code compatibility with it.

The DSP56300 core family offers a new level of performance in speed and power, provided by its rich instruction set and low power dissipation, thus enabling a new generation of wireless, telecommunications and multimedia products. For a description of the DSP56300 core, see *Section 2.4 DSP56300 Core Functional Blocks*. Significant architectural enhancements to the DSP56300 core family include a barrel shifter, 24-bit addressing, an instruction patch module and direct memory access (DMA).

The DSP56300 core family members contain the DSP56300 core and additional modules. The modules are chosen from a library of standard pre-designed elements such as memories and peripherals. New modules may be added to the library to meet customer specifications. A standard interface between the DSP56300 core and the on-chip memory and peripherals supports a wide variety of memory and peripheral configurations. Refer to DSP56371 User's Manual, *Memory Configuration* section.

Core features are described fully in the *DSP56300 Family Manual*. Pinout, memory and peripheral features are described in this manual.

- DSP56300 modular chassis
  - 181 Million Instructions Per Second (MIPS) with a 181 MHz clock at an internal logic supply (QVDDL) of 1.25 V
  - Object Code Compatible with the 56K core
  - Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support
  - Program Control with position independent code support and instruction patch support
  - EFCOP running concurrently with the core, capable of executing 181 million filter taps per second at peak performance
  - Six-channel DMA controller
  - Low jitter, PLL based clocking with a wide range of frequency multiplications (1 to 255), predivider factors (1 to 31) and power saving clock divider (2^i: i=0 to 7). Reduces clock noise.
  - Internal address tracing support and OnCE for Hardware/Software debugging
  - JTAG port
  - Very low-power CMOS design, fully static design with operating frequencies down to DC
  - STOP and WAIT low-power standby modes
- On-chip Memory Configuration
  - 48Kx24 Bit Y-Data RAM and 32Kx24 Bit Y-Data ROM
  - 36Kx24 Bit X-Data RAM and 32Kx24 Bit X-Data ROM
  - 64Kx24 Bit Program and Bootstrap ROM
  - 4Kx24 Bit Program RAM.
  - PROM patching mechanism
  - Up to 32Kx24 Bit from Y Data RAM and 8Kx24 Bit from X Data RAM can be switched to Program RAM resulting in up to 44Kx24 Bit of Program RAM.
- Peripheral modules
  - Enhanced Serial Audio Interface (ESAI): up to 4 receivers and up to 6 transmitters, master or

slave. I^2S, left justified, right justified, Sony, AC97, network and other programmable protocols

— Enhanced Serial Audio Interface I (ESAI_1): up to 4 receivers and up to 6 transmitters, master or slave. I^2S, left justified, right justified, Sony, AC97, network and other programmable protocols

— Serial Host Interface (SHI): SPI and I^2C protocols, multi master capability in I^2C mode, 10-word receive FIFO, support for 8, 16 and 24-bit words

— Triple Timer module (TEC).

— 11 dedicated GPIO pins

— Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats

— Pins of unused peripherals (except SHI) may be programmed as GPIO lines

2.3 DSP56371 Audio Processor Architecture

This section defines the DSP56371 audio processor architecture. The audio processor is composed of the following units:

- The DSP56300 core is composed of the Data ALU, Address Generation Unit, Program Controller, DMA Controller, Memory Module Interface, Peripheral Module Interface and the On-Chip Emulator (OnCE). The DSP56300 core is described in the document *<st-blue>DSP56300 24-Bit Digital Signal Processor Family Manual, Motorola publication DSP56300FM/AD.*
- Phased Lock Loop and Clock Generator
- Memory modules
- Peripheral modules. The peripheral modules are defined in the following sections.

Memory sizes in the block diagram are defaults. Memory may be differently partitioned, according to the memory mode of the chip. See Section 2.4.7 *On-Chip Memory* for more details about memory size.

2.4 DSP56300 Core Functional Blocks

The DSP56300 core provides the following functional blocks:

- Data arithmetic logic unit (Data ALU)
- Address generation unit (AGU)
- Program control unit (PCU)
- DMA controller (with six channels)
- Instruction patch controller
- PLL-based clock oscillator
- OnCE module
- Memory

In addition, the DSP56371 provides a set of on-chip peripherals, described in Section 2.5 *Peripheral Overview*.

2.4.1 Data ALU

The Data ALU performs all the arithmetic and logical operations on data operands in the DSP56300 core. The components of the Data ALU are as follows:

- Fully pipelined 24-bit × 24-bit parallel multiplier-accumulator (MAC)
- Bit field unit, comprising a 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing)
- Conditional ALU instructions
- 24-bit or 16-bit arithmetic support under software control
- Four 24-bit input general purpose registers: X1, X0, Y1, and Y0
- Six Data ALU registers (A2, A1, A0, B2, B1 and B0) that are concatenated into two general purpose, 56-bit accumulators (A and B), accumulator shifters
- Two data bus shifter/limiter circuits

2.4.1.1 Data ALU Registers

The Data ALU registers can be read or written over the X memory data bus (XDB) and the Y memory data bus (YDB) as 24- or 48-bit operands (or as 16- or 32-bit operands in 16-bit arithmetic mode). The source operands for the Data ALU, which can be 24, 48, or 56 bits (16, 32, or 40 bits in 16-bit arithmetic mode), always originate from Data ALU registers. The results of all Data ALU operations are stored in an accumulator.

All the Data ALU operations are performed in two clock cycles in pipeline fashion so that a new instruction can be initiated in every clock, yielding an effective execution rate of one instruction per clock cycle. The destination of every arithmetic operation can be used as a source operand for the immediately following arithmetic operation without a time penalty (for example, without a pipeline stall).

2.4.1.2 Multiplier-Accumulator (MAC)

The MAC unit comprises the main arithmetic processing unit of the DSP56300 core and performs all of the calculations on data operands. In the case of arithmetic instructions, the unit accepts as many as three input operands and outputs one 56-bit result of the following form- Extension:Most Significant Product:Least Significant Product (EXT:MSP:LSP).

The multiplier executes 24-bit × 24-bit, parallel, fractional multiplies, between two's-complement signed, unsigned, or mixed operands. The 48-bit product is right-justified and added to the 56-bit contents of either the A or B accumulator. A 56-bit result can be stored as a 24-bit operand. The LSP can either be truncated or rounded into the MSP. Rounding is performed if specified.

2.4.2 Address Generation Unit (AGU)

The AGU performs the effective address calculations using integer arithmetic necessary to address data operands in memory and contains the registers used to generate the addresses. It implements four types of arithmetic: linear, modulo, multiple wrap-around modulo and reverse-carry. The AGU operates in parallel with other chip resources to minimize address-generation overhead.

The AGU is divided into two halves, each with its own Address ALU. Each Address ALU has four sets of register triplets, and each register triplet is composed of an address register, an offset register and a modifier register. The two Address ALUs are identical. Each contains a 24-bit full adder (called an offset adder).

A second full adder (called a modulo adder) adds the summed result of the first full adder to a modulo value that is stored in its respective modifier register. A third full adder (called a reverse-carry adder) is also provided.

The offset adder and the reverse-carry adder are in parallel and share common inputs. The only difference between them is that the carry propagates in opposite directions. Test logic determines which of the three summed results of the full adders is output.

Each Address ALU can update one address register from its respective address register file during one instruction cycle. The contents of the associated modifier register specifies the type of arithmetic to be used in the address register update calculation. The modifier value is decoded in the Address ALU.

2.4.3 Program Control Unit (PCU)

The PCU performs instruction prefetch, instruction decoding, hardware DO loop control and exception processing. The PCU implements a seven-stage pipeline and controls the different processing states of the DSP56300 core. The PCU consists of the following three hardware blocks:

- Program decode controller (PDC)
- Program address generator (PAG)
- Program interrupt controller

The PDC decodes the 24-bit instruction loaded into the instruction latch and generates all signals necessary for pipeline control. The PAG contains all the hardware needed for program address generation, system stack and loop control. The Program interrupt controller arbitrates among all interrupt requests (internal interrupts, as well as the five external requests: $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$ and $\overline{\text{NMI}}$) and generates the appropriate interrupt vector address.

PCU features include the following:

- Position independent code support
- Addressing modes optimized for DSP applications (including immediate offsets)
- On-chip instruction cache controller
- On-chip memory-expandable hardware stack
- Nested hardware DO loops
- Fast auto-return interrupts

The PCU implements its functions using the following registers:

- PC—program counter register
- SR—Status register
- LA—loop address register
- LC—loop counter register
- VBA—vector base address register
- SZ—stack size register
- SP—stack pointer
- OMR—operating mode register
- SC—stack counter register

The PCU also includes a hardware system stack (SS).

2.4.4 Internal Buses

To provide data exchange between blocks, the following buses are implemented:

- Peripheral input/output expansion bus (PIO_EB) to peripherals
- Program memory expansion bus (PM_EB) to program memory
- X memory expansion bus (XM_EB) to X memory
- Y memory expansion bus (YM_EB) to Y memory
- Global data bus (GDB) between registers in the DMA, AGU, OnCE, PLL, BIU and PCU, as well as the memory-mapped registers in the peripherals
- DMA data bus (DDB) for carrying DMA data between memories and/or peripherals
- DMA address bus (DAB) for carrying DMA addresses to memories and peripherals
- Program Data Bus (PDB) for carrying program data throughout the core
- X memory Data Bus (XDB) for carrying X data throughout the core
- Y memory Data Bus (YDB) for carrying Y data throughout the core
- Program address bus (PAB) for carrying program memory addresses throughout the core
- X memory address bus (XAB) for carrying X memory addresses throughout the core
- Y memory address bus (YAB) for carrying Y memory addresses throughout the core

All internal buses on the DSP56300 family members are 24-bit buses. See Figure 1.

2.4.5 Direct Memory Access (DMA)

The DMA block has the following features:

- Six DMA channels supporting internal and external accesses
- One-, two- and three-dimensional transfers (including circular buffering)
- End-of-block-transfer interrupts

- Triggering from interrupt lines and all peripherals

2.4.6 PLL-based Clock Oscillator

The clock generator in the DSP56300 core is composed of two main blocks: the PLL, which performs clock input division, frequency multiplication, skew elimination and the clock generator (CLKGEN), which performs low-power division and clock pulse generation. PLL-based clocking:

- Allows change of low-power divide factor (DF) without loss of lock
- Provides output clock with skew elimination
- Provides a wide range of frequency multiplications (1 to 255), predivider factors (1 to 31), PLL feedback multiplier (2 or 4), output divide factor (1, 2 or 4), and a power-saving clock divider (2^i: i = 0 to 7) to reduce clock noise

The PLL allows the processor to operate at a high internal clock frequency using a low frequency clock input. This feature offers two immediate benefits:

- A lower frequency clock input reduces the overall electromagnetic interference generated by a system.
- The ability to oscillate at different frequencies reduces costs by eliminating the need to add additional oscillators to a system.

NOTE

The PLL will momentarily overshoot the target frequency when the PLL is first enabled or when the VCO frequency is modified. It is important that when modifying the PLL frequency or enabling the PLL that the two-step procedure defined in Section 3, *DSP56371 Overview* be followed.

2.4.7 On-Chip Memory

The memory space of the DSP56300 core is partitioned into program memory space, X data memory space and Y data memory space. The data memory space is divided into X and Y data memory in order to work with the two Address ALUs and to feed two operands simultaneously to the Data ALU. Memory space includes internal RAM and ROM and can not be expanded off-chip.

There is an instruction patch module. The patch module is used to patch program ROM. The memory switch mode is used to increase the size of program RAM as needed (switch from X data RAM and/or Y data RAM).

There are on-chip ROMs for program and bootstrap memory (64K x 24-bit), X ROM (32K x 24-bit) and Y ROM (32K x 24-bit).

More information on the internal memory is provided in the DSP56371 User's Manual, *Memory* section.

2.4.8 Off-Chip Memory Expansion

Memory cannot be expanded off-chip. There is no external memory bus.

2.5 Peripheral Overview

The DSP56371 is designed to perform a wide variety of fixed-point digital signal processing functions. In addition to the core features previously discussed, the DSP56371 provides the following peripherals:

- As many as 39 dedicate or user-configurable general purpose input/output (GPIO) signals
- Timer/event counter (TEC) module, containing three independent timers
- Memory switch mode in on-chip memory
- Four external interrupt/mode control lines and one external non-maskable interrupt line
- Enhanced serial audio interface (ESAI) with up to four receivers and up to six transmitters, master or slave, using the I^2S, Sony, AC97, network and other programmable protocols
- A second enhanced serial audio interface (ESAI_1) with up to four receivers and up to six transmitters, master or slave, using the I^2S, Sony, AC97, network and other programmable protocols.
- Serial host interface (SHI) using SPI and I^2C protocols, with multi-master capability, 10-word receive FIFO and support for 8-, 16- and 24-bit words
- A Digital audio transmitter (DAX): a serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats

2.5.1 General Purpose Input/Output (GPIO)

The DSP56371 provides 11 dedicated GPIO and 28 programmable signals that can operate either as GPIO pins or peripheral pins (ESAI, ESAI_1, DAX, and TEC). The signals are configured as GPIO after hardware reset. Register programming techniques for all GPIO functionality among these interfaces are very similar and are described in the following sections.

2.5.2 Triple Timer (TEC)

This section describes a peripheral module composed of a common 21-bit prescaler and three independent and identical general purpose 24-bit timer/event counters, each one having its own register set.

Each timer can use internal or external clocking and can interrupt the DSP after a specified number of events (clocks). Two of the three timers can signal an external device after counting internal events. Each timer can also be used to trigger DMA transfers after a specified number of events (clocks) occurred. Two of the three timers connect to the external world through bidirectional pins (TIO0, TIO1). When a TIO pin is configured as input, the timer functions as an external event counter or can measure external pulse width/signal period. When a TIO pin is used as output the timer is functioning as either a timer, a watchdog or a Pulse Width Modulator. When a TIO pin is not used by the timer it can be used as a General Purpose Input/Output Pin. Refer to DSP56371 User's Manual, *Triple Timer Module* section.

2.5.3 Enhanced Serial Audio Interface (ESAI)

The ESAI provides a full-duplex serial port for serial communication with a variety of serial devices including one or more industry-standard codecs, other DSPs, microprocessors and peripherals that

implement the Motorola SPI serial protocol. The ESAI consists of independent transmitter and receiver sections, each with its own clock generator. It is a superset of the DSP56300 family ESSI peripheral and of the DSP56000 family SAI peripheral. For more information on the ESAI, refer to DSP56371 User's Manual, *Enhanced Serial Audio Interface (ESAI)* section.

2.5.4 Enhanced Serial Audio Interface 1 (ESAI_1)

The ESAI_1 is a second ESAI interface. The ESAI_1 is functionally identical to ESAI. For more information on the ESAI_1, refer to DSP56371 User's Manual, *Enhanced Serial Audio Interface (ESAI_1)* section.

2.5.5 Serial Host Interface (SHI)

The SHI is a serial input/output interface providing a path for communication and program/coefficient data transfers between the DSP and an external host processor. The SHI can also communicate with other serial peripheral devices. The SHI can interface directly to either of two well-known and widely used synchronous serial buses: the Motorola serial peripheral interface (SPI) bus and the Philips inter-integrated-circuit control (I^2C) bus. The SHI supports either the SPI or I^2C bus protocol, as required, from a slave or a single-master device. To minimize DSP overhead, the SHI supports single-, double- and triple-byte data transfers. The SHI has a 10-word receive FIFO that permits receiving up to 30 bytes before generating a receive interrupt, reducing the overhead for data reception. For more information on the SHI, refer to DSP56371 User's Manual, *Serial Host Interface* section.

2.5.6 Digital Audio Transmitter (DAX)

The DAX is a serial audio interface module that outputs digital audio data in the AES/EBU, CP-340 and IEC958 formats. For more information on the DAX, refer to DSP56371 User's Manual, *Digital Audio* section.

3 Signal/Connection Descriptions

3.1 Signal Groupings

The input and output signals of the DSP56374 are organized into functional groups, which are listed in Table 1. and illustrated in Figure 2.

The DSP56374 is operated from a 1.25 V and 3.3 V supply; however, some of the inputs can tolerate 5.0 V. A special notice for this feature is added to the signal descriptions of those inputs.

Table 1. DSP56374 Functional Signal Groupings

Functional Group		Number of Signals	Detailed Description
Power (V_{DD})		12	Table 2
Ground (GND)		12	Table 3
Scan Pins		1	Table 4
Clock and PLL		2	Table 5
Interrupt and mode control		5	Table 6
SHI		5	Table 7
ESAI	Port C[1]	12	Table 8
ESAI_1	Port E[2]	12	Table 9
SPDIF Transmitter (DAX)	Port D[3]	2	Table 10
Dedicated GPIO	Port F[4]	11	Table 11
Timer		2	Table 12
JTAG/OnCE Port		4	Table 13

Note:

1. Port C signals are the GPIO port signals which are multiplexed with the ESAI signals.
2. Port E signals are the GPIO port signals which are multiplexed with the ESAI_1 signals.
3. Port D signals are the GPIO port signals which are multiplexed with the DAX signals.
4. Port F signals are the dedicated GPIO port signals.

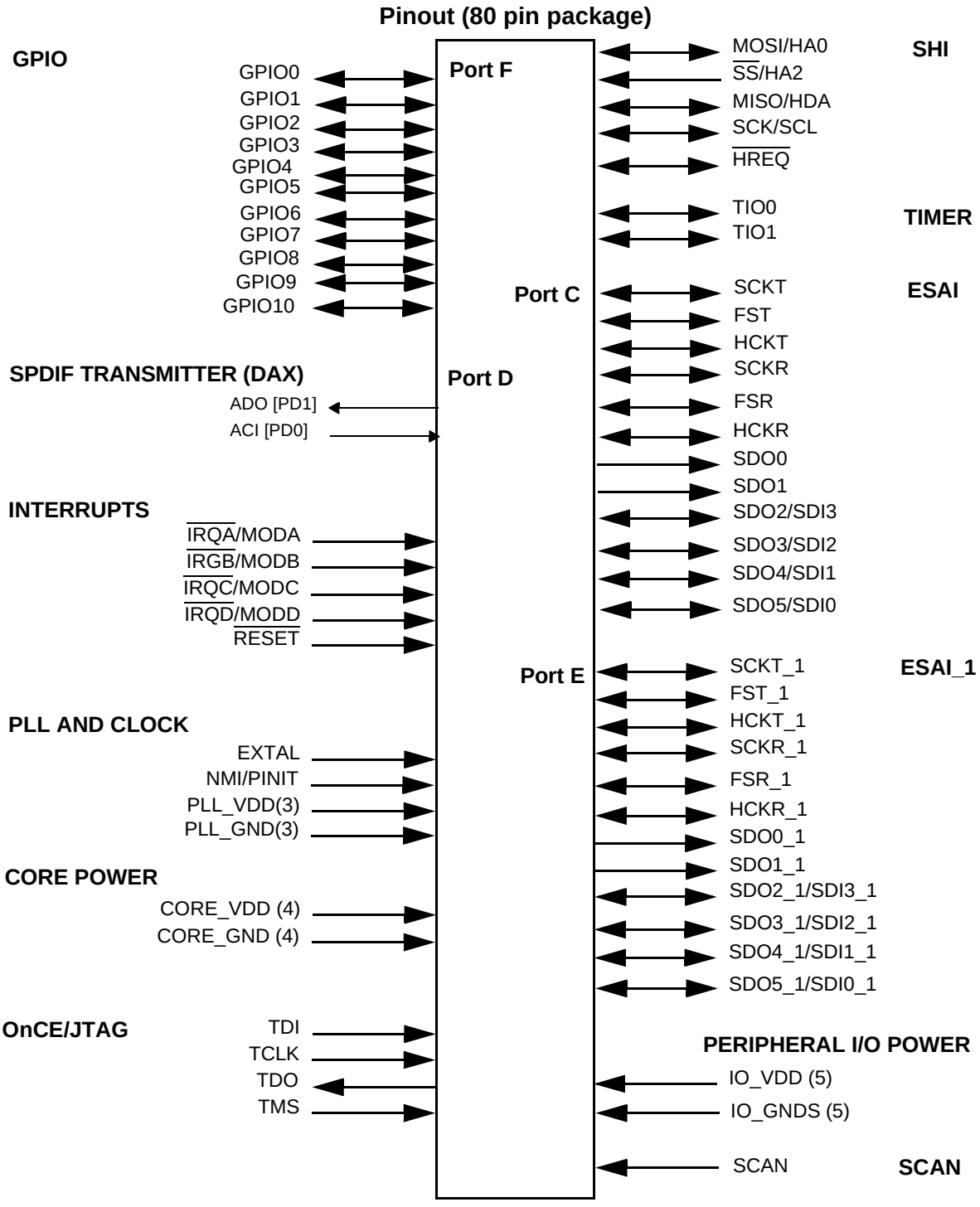


Figure 2. Signals Identified by Functional Group

3.2 Power

Table 2. Power Inputs

Power Name	Description
PLLA_VDD (1) PLLP_VDD(1)	**PLL Power**— The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. The user must provide adequate external decoupling capacitors.
PLLD_VDD (1)	**PLL Power—** The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate external decoupling capacitors.
CORE_VDD (4)	**Core Power**—The voltage (1.25 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 1.25 V_{DD} power rail. The user must provide adequate decoupling capacitors.
IO_VDD (5)	**SHI, ESAI, ESAI_1, DAX and Timer I/O Power** —The voltage (3.3 V) should be well-regulated and the input should be provided with an extremely low impedance path to the 3.3 V_{DD} power rail. This is an isolated power for the SHI, ESAI, ESAI_1, DAX and Timer I/O. The user must provide adequate external decoupling capacitors.

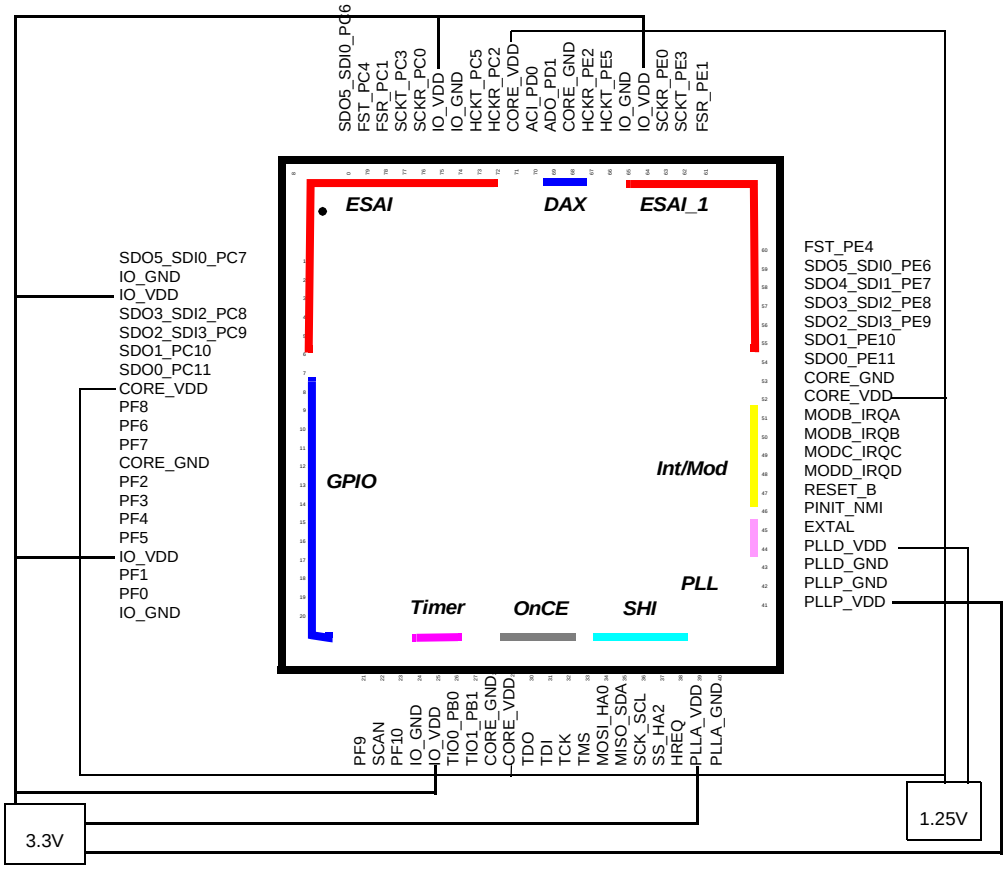


Figure 3. VDD Connections

3.3 Ground

Table 3. Grounds

Ground Name	Description
PLLA_GND(1) PLLP_GND(1)	**PLL Ground**—The PLL ground should be provided with an extremely low-impedance path to ground. The user must provide adequate external decoupling capacitors.
PLLD_GND(1)	**PLL Ground**—The PLL ground should be provided with an extremely low-impedance path to ground. The user must provide adequate external decoupling capacitors.
CORE_GND (4)	**Core Ground**—The Core ground should be provided with an extremely low-impedance path to ground. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.
IO_GND (5)	**SHI, ESAI, ESAI_1, DAX and Timer I/O Ground**—IO_GND is an isolated ground for the SHI, ESAI, ESAI_1, DAX and Timer I/O. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.

3.4 SCAN

Table 4. SCAN Signals

Signal Name	Type	State During Reset	Signal Description
SCAN	Input	Input	**SCAN**—Manufacturing test pin. This pin should be pulled low. Internal Pull down resistor.

3.5 Clock and PLL

Table 5. Clock and PLL Signals

Signal Name	Type	State during Reset	Signal Description
EXTAL	Input	Input	**External Clock Input**—An external clock source must be connected to EXTAL in order to supply the clock to the internal clock generator and PLL. *This input is 5 V tolerant.*
PINIT/$\overline{\text{NMI}}$	Input	Input	**PLL Initial/Nonmaskable Interrupt**—During assertion of $\overline{\text{RESET}}$, the value of PINIT/$\overline{\text{NMI}}$ is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After $\overline{\text{RESET}}$ de assertion and during normal instruction processing, the PINIT/$\overline{\text{NMI}}$ Schmitt-trigger input is a negative-edge-triggered nonmaskable interrupt (NMI) request internally synchronized to internal system clock. Internal Pull up resistor. This input is 5 V tolerant.

3.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 6. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA/IRQA	Input	Input	**Mode Select A/External Interrupt Request A—**MODA/IRQA is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODA/IRQA selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into the OMR when the RESET signal is deasserted. If the processor is in the stop standby state and the MODA/IRQA pin is pulled to GND, the processor will exit the stop state. Internal Pull up resistor. This input is 5 V tolerant.

Table 6. Interrupt and Mode Control (continued)

Signal Name	Type	State During Reset	Signal Description
MODB/$\overline{\text{IRQB}}$	Input	Input	**Mode Select B/External Interrupt Request B—**MODB/$\overline{\text{IRQB}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODB/$\overline{\text{IRQB}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. Internal Pull up resistor. This input is 5 V tolerant.
MODC/$\overline{\text{IRQC}}$	Input	Input	**Mode Select C/External Interrupt Request C—**MODC/$\overline{\text{IRQC}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODC/$\overline{\text{IRQC}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. Internal Pull up resistor. This input is 5 V tolerant.
MODD/$\overline{\text{IRQD}}$	Input	Input	**Mode Select D/External Interrupt Request D**—MODD/$\overline{\text{IRQD}}$ is an active-low Schmitt-trigger input, internally synchronized to the DSP clock. MODD/$\overline{\text{IRQD}}$ selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. MODA, MODB, MODC and MODD select one of 16 initial chip operating modes, latched into OMR when the $\overline{\text{RESET}}$ signal is deasserted. Internal Pull up resistor. This input is 5 V tolerant.
$\overline{\text{RESET}}$	Input	Input	**Reset—**$\overline{\text{RESET}}$ is an active-low, Schmitt-trigger input. When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the $\overline{\text{RESET}}$ signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC and MODD inputs. The $\overline{\text{RESET}}$ signal must be asserted during power up. A stable EXTAL signal must be supplied while $\overline{\text{RESET}}$ is being asserted. Internal Pull up resistor. This input is 5 V tolerant.

3.7 Serial Host Interface

The SHI has five I/O signals that can be configured to allow the SHI to operate in either SPI or I^2C mode.

Table 7. Serial Host Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCK	Input or output	Tri-stated	**SPI Serial Clock**—The SCK signal is an output when the SPI is configured as a master and a Schmitt-trigger input when the SPI is configured as a slave. When the SPI is configured as a master, the SCK signal is derived from the internal SHI clock generator. When the SPI is configured as a slave, the SCK signal is an input, and the clock signal from the external master synchronizes the data transfer. The SCK signal is ignored by the SPI if it is defined as a slave and the slave select ($\overline{SS}$) signal is not asserted. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.
SCL	Input or output		**I^2C Serial Clock**—SCL carries the clock for I^2C bus transactions in the I^2C mode. SCL is a Schmitt-trigger input when configured as a slave and an open-drain output when configured as a master. SCL should be connected to V_{DD} through a pull-up resistor. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. Internal Pull up resistor. This input is 5 V tolerant.
MISO	Input or output	Tri-stated	**SPI Master-In-Slave-Out**—When the SPI is configured as a master, MISO is the master data input line. The MISO signal is used in conjunction with the MOSI signal for transmitting and receiving serial data. This signal is a Schmitt-trigger input when configured for the SPI Master mode, an output when configured for the SPI Slave mode, and tri-stated if configured for the SPI Slave mode when $\overline{SS}$ is deasserted. An external pull-up resistor is not required for SPI operation.
SDA	Input or open-drain output		**I^2C Data and Acknowledge**—In I^2C mode, SDA is a Schmitt-trigger input when receiving and an open-drain output when transmitting. SDA should be connected to V_{DD} through a pull-up resistor. SDA carries the data for I^2C transactions. The data in SDA must be stable during the high period of SCL. The data in SDA is only allowed to change when SCL is low. When the bus is free, SDA is high. The SDA line is only allowed to change during the time SCL is high in the case of start and stop events. A high-to-low transition of the SDA line while SCL is high is a unique situation, and it is defined as the start event. A low-to-high transition of SDA while SCL is high is a unique situation defined as the stop event. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. Internal Pull up resistor. This input is 5 V tolerant.

Table 7. Serial Host Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
MOSI	Input or output	Tri-stated	**SPI Master-Out-Slave-In**—When the SPI is configured as a master, MOSI is the master data output line. The MOSI signal is used in conjunction with the MISO signal for transmitting and receiving serial data. MOSI is the slave data input line when the SPI is configured as a slave. This signal is a Schmitt-trigger input when configured for the SPI Slave mode.
HA0	Input		**I^2C Slave Address 0**—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for I^2C slave mode, the HA0 signal is used to form the slave device address. HA0 is ignored when configured for the I^2C master mode. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. Internal Pull up resistor. This input is 5 V tolerant.
SS	Input	Tri-stated	**SPI Slave Select**—This signal is an active low Schmitt-trigger input when configured for the SPI mode. When configured for the SPI Slave mode, this signal is used to enable the SPI slave for transfer. When configured for the SPI master mode, this signal should be kept deasserted (pulled high). If it is asserted while configured as SPI master, a bus error condition is flagged. If $\overline{SS}$ is deasserted, the SHI ignores SCK clocks and keeps the MISO output signal in the high-impedance state.
HA2	Input		**I^2C Slave Address 2**—This signal uses a Schmitt-trigger input when configured for the I^2C mode. When configured for the I^2C Slave mode, the HA2 signal is used to form the slave device address. HA2 is ignored in the I^2C master mode. This signal is tri-stated during hardware, software and individual reset. Thus, there is no need for an external pull-up in this state. Internal Pull up resistor. This input is 5 V tolerant.
HREQ	Input or Output	Tri-stated	**Host Request**—This signal is an active low Schmitt-trigger input when configured for the master mode but an active low output when configured for the slave mode. When configured for the slave mode, $\overline{HREQ}$ is asserted to indicate that the SHI is ready for the next data word transfer and deasserted at the first clock pulse of the new data word transfer. When configured for the master mode, $\overline{HREQ}$ is an input. When asserted by the external slave device, it will trigger the start of the data word transfer by the master. After finishing the data word transfer, the master will await the next assertion of $\overline{HREQ}$ to proceed to the next transfer. This signal is tri-stated during hardware, software, personal reset, or when the HREQ1–HREQ0 bits in the HCSR are cleared. There is no need for an external pull-up in this state. Internal Pull up resistor. This input is 5 V tolerant.

3.8 Enhanced Serial Audio Interface

Table 8. Enhanced Serial Audio Interface Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR	Input or output	GPIO disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (for example, for external digital to analog converters [DACs]) or as an additional system clock.
PC2	Input, output, or disconnected		**Port C2**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
HCKT	Input or output	GPIO disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (for example, for external DACs) or as an additional system clock.
PC5	Input, output, or disconnected		**Port C5**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 8. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
FSR	Input or output	GPIO disconnected	**Frame Sync for Receiver**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC1	Input, output, or disconnected		**Port C1**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
FST	Input or output	GPIO disconnected	**Frame Sync for Transmitter**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI transmit clock control register (TCCR).
PC4	Input, output, or disconnected		**Port C4**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 8. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SCKR	Input or output	GPIO disconnected	**Receiver Serial Clock**—SCKR provides the receiver serial bit clock for the ESAI. The SCKR operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PC0	Input, output, or disconnected		**Port C0**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SCKT	Input or output	GPIO disconnected	**Transmitter Serial Clock**—This signal provides the serial bit rate clock for the ESAI. SCKT is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PC3	Input, output, or disconnected		**Port C3**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO5	Output	GPIO disconnected	**Serial Data Output 5**—When programmed as a transmitter, SDO5 is used to transmit data from the TX5 serial transmit shift register.
SDI0	Input		**Serial Data Input 0**—When programmed as a receiver, SDI0 is used to receive serial data into the RX0 serial receive shift register.
PC6	Input, output, or disconnected		**Port C6**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 8. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO4	Output	GPIO disconnected	**Serial Data Output 4**—When programmed as a transmitter, SDO4 is used to transmit data from the TX4 serial transmit shift register.
SDI1	Input		**Serial Data Input 1**—When programmed as a receiver, SDI1 is used to receive serial data into the RX1 serial receive shift register.
PC7	Input, output, or disconnected		**Port C7**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3 is used to transmit data from the TX3 serial transmit shift register.
SDI2	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2 is used to receive serial data into the RX2 serial receive shift register.
PC8	Input, output, or disconnected		**Port C8**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO2	Output	GPIO disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2 is used to transmit data from the TX2 serial transmit shift register
SDI3	Input		**Serial Data Input 3**—When programmed as a receiver, SDI3 is used to receive serial data into the RX3 serial receive shift register.
PC9	Input, output, or disconnected		**Port C9**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 8. Enhanced Serial Audio Interface Signals (continued)

Signal Name	Signal Type	State during Reset	Signal Description
SDO1	Output	GPIO disconnected	**Serial Data Output 1**—SDO1 is used to transmit data from the TX1 serial transmit shift register.
PC10	Input, output, or disconnected		**Port C10**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0	Output	GPIO disconnected	**Serial Data Output 0**—SDO0 is used to transmit data from the TX0 serial transmit shift register.
PC11	Input, output, or disconnected		**Port C11**—When the ESAI is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

3.9 Enhanced Serial Audio Interface_1

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
HCKR_1	Input or output	GPIO disconnected	**High Frequency Clock for Receiver**—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 receiver as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high-frequency sample clock (for example, for external digital to analog converters [DACs]) or as an additional system clock.
PE2	Input, output, or disconnected		**Port E2**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
HCKT_1	Input or output	GPIO disconnected	**High Frequency Clock for Transmitter**—When programmed as an input, this signal provides a high frequency clock source for the ESAI_1 transmitter as an alternate to the DSP core clock. When programmed as an output, this signal can serve as a high frequency sample clock (for example, for external DACs) or as an additional system clock.
PE5	Input, output, or disconnected		**Port E5**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
FSR_1	Input or output	GPIO disconnected	**Frame Sync for Receiver_1**—This is the receiver frame sync input/output signal. In the asynchronous mode (SYN=0), the FSR_1 pin operates as the frame sync input or output used by all the enabled receivers. In the synchronous mode (SYN=1), it operates as either the serial flag 1 pin (TEBE=0), or as the transmitter external buffer enable control (TEBE=1, RFSD=1). When this pin is configured as serial flag pin, its direction is determined by the RFSD bit in the RCCR_1 register. When configured as the output flag OF1, this pin will reflect the value of the OF1 bit in the SAICR_1 register, and the data in the OF1 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF1, the data value at the pin will be stored in the IF1 bit in the SAISR register, synchronized by the frame sync in normal mode or the slot in network mode.
PE1	Input, output, or disconnected		**Port E1**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
FST_1	Input or output	GPIO disconnected	**Frame Sync for Transmitter_1**—This is the transmitter frame sync input/output signal. For synchronous mode, this signal is the frame sync for both transmitters and receivers. For asynchronous mode, FST_1 is the frame sync for the transmitters only. The direction is determined by the transmitter frame sync direction (TFSD) bit in the ESAI_1 transmit clock control register (TCCR_1).
PE4	Input, output, or disconnected		**Port E4**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SCKR_1	Input or output	GPIO disconnected	**Receiver Serial Clock_1**—SCKR_1 provides the receiver serial bit clock for the ESAI_1. The SCKR_1 operates as a clock input or output used by all the enabled receivers in the asynchronous mode (SYN=0), or as serial flag 0 pin in the synchronous mode (SYN=1). When this pin is configured as serial flag pin, its direction is determined by the RCKD bit in the RCCR_1 register. When configured as the output flag OF0, this pin will reflect the value of the OF0 bit in the SAICR_1 register, and the data in the OF0 bit will show up at the pin synchronized to the frame sync in normal mode or the slot in network mode. When configured as the input flag IF0, the data value at the pin will be stored in the IF0 bit in the SAISR_1 register, synchronized by the frame sync in normal mode or the slot in network mode.
PE0	Input, output, or disconnected		**Port E0**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SCKT_1	Input or output	GPIO disconnected	**Transmitter Serial Clock_1**—This signal provides the serial bit rate clock for the ESAI_1. SCKT_1 is a clock input or output used by all enabled transmitters and receivers in synchronous mode, or by all enabled transmitters in asynchronous mode.
PE3	Input, output, or disconnected		**Port E3**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO5_1	Output	GPIO disconnected	**Serial Data Output 5_1**—When programmed as a transmitter, SDO5_1 is used to transmit data from the TX5 serial transmit shift register.
SDI0_1	Input		**Serial Data Input 0_1**—When programmed as a receiver, SDI0_1 is used to receive serial data into the RX0 serial receive shift register.
PE6	Input, output, or disconnected		**Port E6**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SDO4_1	Output	GPIO disconnected	**Serial Data Output 4_1**—When programmed as a transmitter, SDO4_1 is used to transmit data from the TX4 serial transmit shift register.
SDI1_1	Input		**Serial Data Input 1_1**—When programmed as a receiver, SDI1_1 is used to receive serial data into the RX1 serial receive shift register.
PE7	Input, output, or disconnected		**Port E7**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO3_1	Output	GPIO disconnected	**Serial Data Output 3**—When programmed as a transmitter, SDO3_1 is used to transmit data from the TX3 serial transmit shift register.
SDI2_1	Input		**Serial Data Input 2**—When programmed as a receiver, SDI2_1 is used to receive serial data into the RX2 serial receive shift register.
PE8	Input, output, or disconnected		**Port E8**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO2_1	Output	GPIO disconnected	**Serial Data Output 2**—When programmed as a transmitter, SDO2_1 is used to transmit data from the TX2 serial transmit shift register.
SDI3_1	Input		**Serial Data Input 3**—When programmed as a receiver, SDI3_1 is used to receive serial data into the RX3 serial receive shift register.
PE9	Input, output, or disconnected		**Port E9**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 9. Enhanced Serial Audio Interface_1 Signals

Signal Name	Signal Type	State during Reset	Signal Description
SDO1_1 PE10	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 1**—SDO1_1 is used to transmit data from the TX1 serial transmit shift register. **Port E10**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
SDO0_1 PE11	Output Input, output, or disconnected	GPIO disconnected	**Serial Data Output 0**—SDO0_1 is used to transmit data from the TX0 serial transmit shift register. **Port E11**—When the ESAI_1 is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

3.10 SPDIF Transmitter Digital Audio Interface

Table 10. Digital Audio Interface (DAX) Signals

Signal Name	Type	State During Reset	Signal Description
ACI	Input	GPIO Disconnected	**Audio Clock Input**—This is the DAX clock input. When programmed to use an external clock, this input supplies the DAX clock. The external clock frequency must be 256, 384, or 512 times the audio sampling frequency (256 × Fs, 384 × Fs or 512 × Fs, respectively).
PD0	Input, output, or disconnected		**Port D0**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
ADO	Output	GPIO Disconnected	**Digital Audio Data Output**—This signal is an audio and non-audio output in the form of AES/SPDIF, CP340 and IEC958 data in a biphase mark format.
PD1	Input, output, or disconnected		**Port D1**—When the DAX is configured as GPIO, this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

3.11 Dedicated GPIO Interface

Table 11. Dedicated GPIO Signals

Signal Name	Type	State During Reset	Signal Description
PF0	Input, output, or disconnected	GPIO disconnected	**Port F0**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF1	Input, output, or disconnected	GPIO disconnected	**Port F1**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF2	Input, output, or disconnected	GPIO disconnected	**Port F2**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF3	Input, output, or disconnected	GPIO disconnected	**Port F3**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF4	Input, output, or disconnected	GPIO disconnected	**Port F4**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF5	Input, output, or disconnected	GPIO disconnected	**Port F5**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF6	Input, output, or disconnected	GPIO disconnected	**Port F6**—this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

Table 11. Dedicated GPIO Signals (continued)

Signal Name	Type	State During Reset	Signal Description
PF7	Input, output, or disconnected	GPIO disconnected	**Port F7**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF8	Input, output, or disconnected	GPIO disconnected	**Port F8**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF9	Input, output, or disconnected	GPIO disconnected	**Port F9**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.
PF10	Input, output, or disconnected	GPIO disconnected	**Port F10**— this signal is individually programmable as input, output, or internally disconnected. The default state after reset is GPIO disconnected. Internal Pull down resistor. This input is 5 V tolerant.

3.12 Timer

Table 12. Timer Signal

Signal Name	Type	State during Reset	Signal Description
TIO0	Input or Output	GPIO Input	**Timer 0 Schmitt-Trigger Input/Output**—When timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 0 control/status register (TCSR0). If TIO0 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected to VDD through a pull-up resistor in order to ensure a stable logic level at this input. Internal Pull down resistor. This input is 5 V tolerant.
TIO1	Input or Output	GPIO Input	**Timer 1 Schmitt-Trigger Input/Output**—When timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. This can be changed to output or configured as a timer input/output through the timer 1 control/status register (TCSR1). If TIO1 is not being used, it is recommended to either define it as GPIO output immediately at the beginning of operation or leave it defined as GPIO input but connected to Vdd through a pull-up resistor in order to ensure a stable logic level at this input. Internal Pull down resistor. This input is 5 V tolerant.

3.13 JTAG/OnCE Interface

Table 13. JTAG/OnCE Interface

Signal Name	Signal Type	State during Reset	Signal Description
TCK	Input	Input	**Test Clock**—TCK is a test clock input signal used to synchronize the JTAG test logic. It has an internal pull-up resistor. Internal Pull up resistor. This input is 5 V tolerant.
TDI	Input	Input	**Test Data Input**—TDI is a test data serial input signal used for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor. Internal Pull up resistor. This input is 5 V tolerant.
TDO	Output	Tri-state	**Test Data Output**—TDO is a test data serial output signal used for test instructions and data. TDO is tri-statable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—TMS is an input signal used to sequence the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor. Internal Pull up resistor. This input is 5 V tolerant.

4 Maximum Ratings

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are pulled to an appropriate logic voltage level (for example, either GND or V_{DD}). The suggested value for a pull-up or pull-down resistor is 4.7 kΩ.

NOTE

In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification will never occur in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

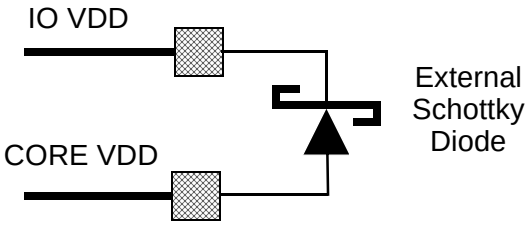
Table 14. Maximum Ratings

Rating[1]	Symbol	Value[1, 2]	Unit
Supply Voltage	V_{CORE_VDD}, V_{PLLD_VDD}	–0.3 to + 1.6	V
	V_{PLLP_VDD}, V_{IO_VDD}, V_{PLLA_VDD},	–0.3 to + 4.0	V
All “5.0V tolerant” input voltages	V_{IN}	GND – 0.3 to 5.5V	V
Current drain per pin excluding V_{DD} and GND (Except for pads listed below)	I	12	mA
SCK_SCL	I_{SCK}	16	mA
ACI_PD0,ADO_PD1	I_{DAX}	24	mA
TDO	Ijtag	24	mA
Operating temperature range[3]	T_J	–40 to +115	°C
Storage temperature	T_{STG}	–55 to +125	°C

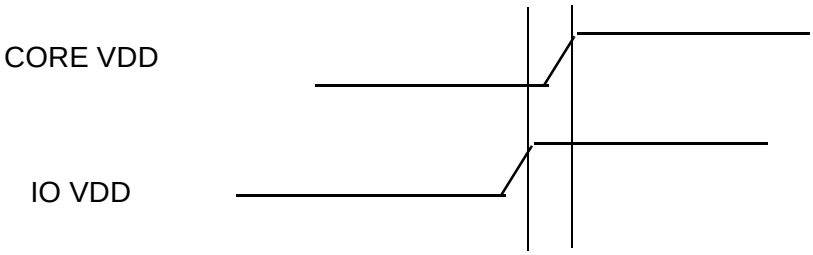
Note:
1. GND = 0 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; CL = 50PF
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
3. Operating temperature qualified for automotive applications.

5 Power Requirements

To prevent high current conditions due to possible improper sequencing of the power supplies, the connection shown below is recommended to be made between the DSP56371 IO_VDD and CORE_VDD power pins.



To prevent a high current condition upon power up, the IOVDD must be applied ahead of the CORE VDD as shown below if the external Schottky is not used.



6 Thermal Characteristics

Table 15. Thermal Characteristics

Characteristic	Symbol	TQFP Value	Unit
Natural Convection, Junction-to-ambient thermal resistance[1,2]	$R_{\theta JA}$ or θ_{JA}	39	°C/W
Junction-to-case thermal resistance[3]	$R_{\theta JC}$ or θ_{JC}	18.25	°C/W

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

7 DC Electrical Characteristics

Table 16. DC ELECTRICAL CHARACTERISTICS[4]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltages • Core (core_vdd) • PLL (plld_vdd)	V_{DD}	1.2	1.25	1.3[1]	V
Supply voltages • Vio_vdd • PLL (pllp_vdd) • PLL (plla_vdd)	V_{DDIO}	3.14	3.3	3.46[1]	V
Input high voltage • All pins	V_{IH}	2.0	—	V_{IO_VDD+2V}	V
Note: All 3.3 V supplies must rise prior to the rise of the 1.25 V supplies to avoid a high current condition and possible system damage.					
Input low voltage • All pins	V_{IL}	–0.3	—	0.8	V
Input leakage current (All pins)	I_{IN}	—	—	84	µA
Clock pin Input Capacitance (EXTAL)	C_{IN}		3.749		pF
High impedance (off-state) input current (@ 3.46 V)	I_{TSI}	–84	—	84	µA
Output high voltage I_{OH} = -5 mA	V_{OH}	2.4	—	—	V
Output low voltage I_{OL} = 5 mA	V_{OL}	—	—	0.4	V
Internal supply current[1] at internal clock of 181MHz • In Normal mode	I_{CCI}	—	99	200	mA

Table 16. DC ELECTRICAL CHARACTERISTICS[4]

Characteristics	Symbol	Min	Typ	Max	Unit
• In Wait mode	I_{CCW}	—	48	150	mA
• In Stop mode[3]	I_{CCS}	—	2.5	82	mA
Input capacitance[4]	C_{IN}	—	—	10	pF

Note:

1. Section 3, *Power Consumption Considerations* provides a formula to compute the estimated current requirements in Normal mode. In order to obtain these results, all inputs must be terminated (for example, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks. The power consumption numbers in this specification are 90% of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V_{CORE_VDD} = 1.25V, V_{DD_IO} = 3.3V at T_J = 25°C. Maximum internal supply current is measured with V_{CORE_VDD} = 1.30 V, $V_{IO\_VDD)}$ = 3.46V at T_J = 115°C.
2. In order to obtain these results, all inputs, which are not disconnected at Stop mode, must be terminated (for example, not allowed to float).
3. Periodically sampled and not 100% tested
4. T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; CL=50pF

8 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.8V and a V_{IH} minimum of 2.0V for all pins. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50% point of the respective input signal's transition. DSP56371 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 1.0V and 1.8V, respectively.

NOTE

Although the minimum value for the frequency of EXTAL is 0 MHz (PLL bypassed), the device AC test conditions are 5 MHz and rated speed.

9 Internal Clocks

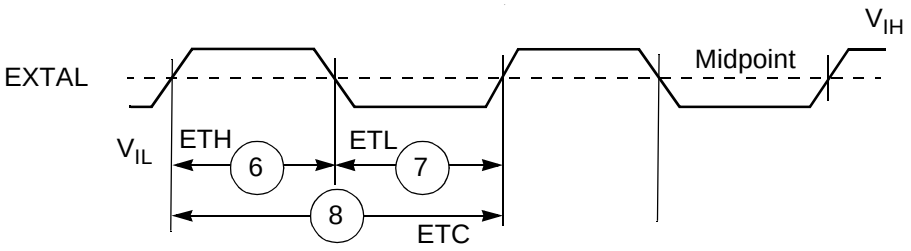
Table 17. INTERNAL CLOCKS

No.	Characteristics	Symbol	Min	Typ	Max	UNIT	Condition
1	Comparison Frequency	Fref[1]	5	—	20	MHZ	Fref = FN/NR
2	Input Clock Frequency	FIN	Fref*NR				NR is input divider value
3	Output clock Frequency (with PLL enabled)[2,3]	FOUT Tc	75 13.3	(1000/Etc × MF x FM)/ (PDF × DF x OD)	—	MHZ ns	FOUT = FVCO/NO where NO is output divider value
4	Output clock Frequency (with PLL disabled)[2,3]	FOUT Tc	—	1000/Etc	—	MHZ	—
5	Duty Cycle	—	40	50	60	%	FVCO=300MHZ ~600MHZ

Note:
1 See users manual for definition.
2 DF = Division Factor
Ef = External frequency
MF = Multiplication Factor
PDF = Predivision Factor
FM= Feedback Multiplier
OD = Output Divider
Tc = internal clock period
3 Maximum frequency will vary depending on the ordered part number.

10 External Clock Operation

The DSP56371 system clock is an externally supplied square wave voltage source connected to EXTAL (see Figure 4.).



Note: The midpoint is 0.5 (V_{IH} + V_{IL}).

Figure 4. External Clock Timing

Table 18. Clock Operation 150 and 181 MHz Values

No.	Characteristics	Symbol	150 MHz		181 MHz	
			Min	Max	Min	Max
6	EXTAL input high [1,2] (40% to 60% duty cycle)	Eth	3.33ns	100ns	2.75ns	100ns
7	EXTAL input low[1,2] (40% to 60% duty cycle)	Etl	3.33ns	100ns	2.75ns	100ns
8	EXTAL cycle time[2] • With PLL disabled • With PLL enabled	Etc	 6.66ns 6.66ns	 inf 200ns	 5.52ns 5.52ns	 inf 200ns
9	Instruction cycle time= I_{CYC} = T_C[3] • With PLL disabled • With PLL enabled	Icyc	 6.66ns 6.66ns	 inf 13.0ns	 5.52ns 5.52ns	 inf 13.0ns

Note:

1. Measured at 50% of the input transition
2. The maximum value for PLL enabled is given for minimum V_{CO} and maximum MF.
3. The maximum value for PLL enabled is given for minimum V_{CO} and maximum DF.
4. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correct operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

11 Reset, Stop, Mode Select, and Interrupt Timing

Table 19. Reset, Stop, Mode Select, and Interrupt Timing

No.	Characteristics	Expression	Min	Max	Unit
10	Delay from $\overline{\text{RESET}}$ assertion to all output pins at reset value[3]	—	—	11	ns
11	Required $\overline{\text{RESET}}$ duration[4] • Power on, external clock generator, PLL disabled • Power on, external clock generator, PLL enabled	 2 x T_C 2 x T_C	 11.1 11.1	 — --	 ns ns
12	Syn reset setup time from RESET • Maximum	T_C	—	5.5	ns
13	Syn reset de assert delay time • Minimum • Maximum(PLL enabled)	 2× T_C (2xT_C)+T_{LOCK}	 11.1 5.0	 —	 ns ms
14	Mode select setup time		10.0	—	ns
15	Mode select hold time		10.0	—	ns
16	Minimum edge-triggered interrupt request assertion width	2 xT_C	11.1	—	ns
17	Minimum edge-triggered interrupt request deassertion width	2 xT_C	11.1	—	ns

Table 19. Reset, Stop, Mode Select, and Interrupt Timing (continued)

No.	Characteristics	Expression	Min	Max	Unit
18	Delay from interrupt trigger to interrupt code execution.	10 xT_C + 5	60.0		ns
19	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] • PLL is active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	9+(128K× T_C)	704	—	us
	• PLL is active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	25× T_C	138	—	ns
	• PLL is not active during Stop and Stop delay is enabled (OMR Bit 6 = 0)	9+(128KxT_C)+T_{lock}	5.7		ms
	• PLL is not active during Stop and Stop delay is not enabled (OMR Bit 6 = 1)	(25 x T_C)+T_{lock}	5		ms
20	• Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	10 x T_C + 3.0		59.0	ns
21	Interrupt Requests Rate • ESAI, ESAI_1, SHI, DAX, Timer	12 x T_C	—	—	ns
	• DMA	8 x T_C	—	—	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	8 x T_C	—	—	ns
	• $\overline{IRQ}$ (level trigger)	12 c T_C	—	—	ns
22	DMA Requests Rate • Data read from ESAI, ESAI_1, SHI, DAX	6 x T_C	—	—	ns
	• Data write to ESAI, ESAI_1, SHI, DAX	7 x T_C	—	—	ns
	• Timer	2 x T_C	—	—	ns
	• $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	3 x T_C	—	—	ns

Note:

1. When using fast interrupts and $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, and $\overline{IRQD}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
2. For PLL disable, using external clock (PCTL Bit 13 = 0), no stabilization delay is required and recovery time will be defined by the OMR Bit 6 settings.

   For PLL enable, (if bit 12 of the PCTL register is 0), the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0.5 ms.
3. Periodically sampled and not 100% tested
4. $\overline{RESET}$ duration is measured during the time in which $\overline{RESET}$ is asserted, V_{DD} is valid, and the EXTAL input is active and valid. When the V_{DD} is valid, but the other “required $\overline{RESET}$ duration” conditions (as specified above) have not been yet met, the device circuitry will be in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

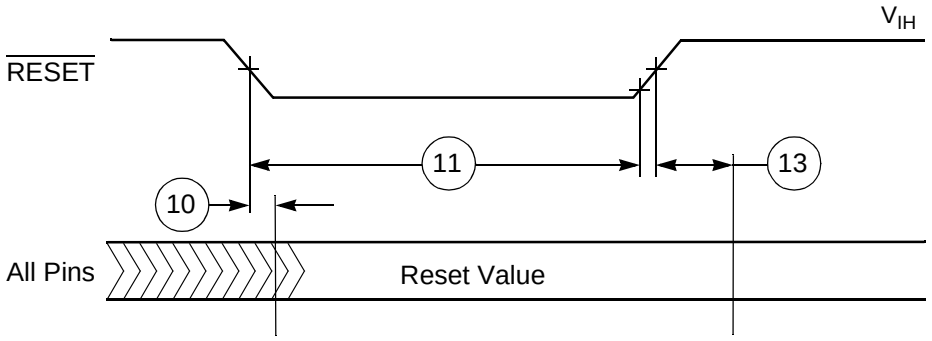


Figure 5. Reset Timing

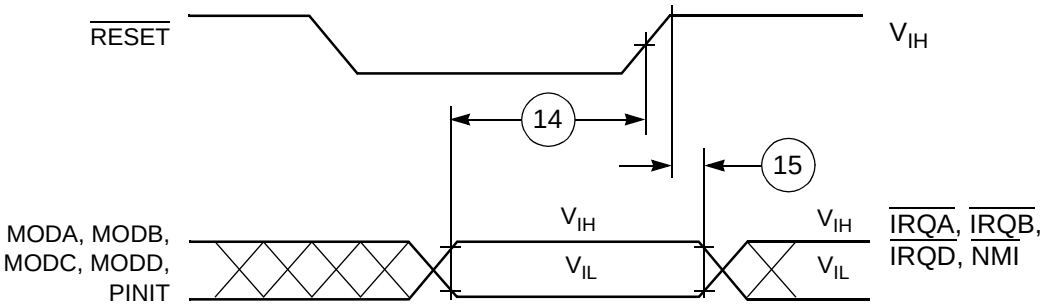


Figure 6. Recovery from Stop State Using $\overline{IRQA}$ Interrupt Service

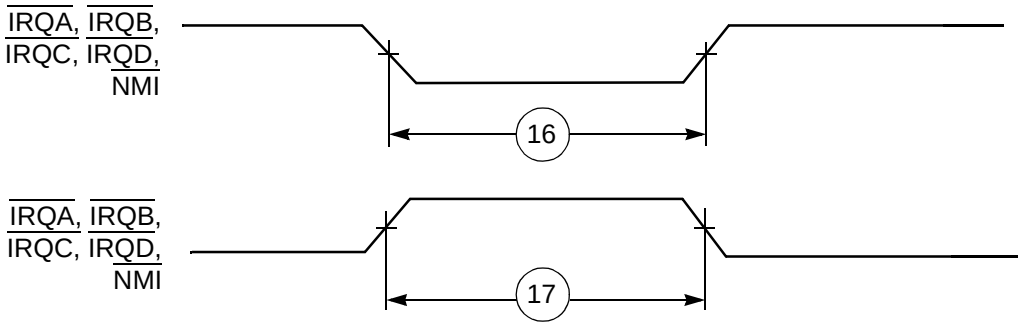


Figure 7. External Interrupt Timing (Negative Edge-Triggered)

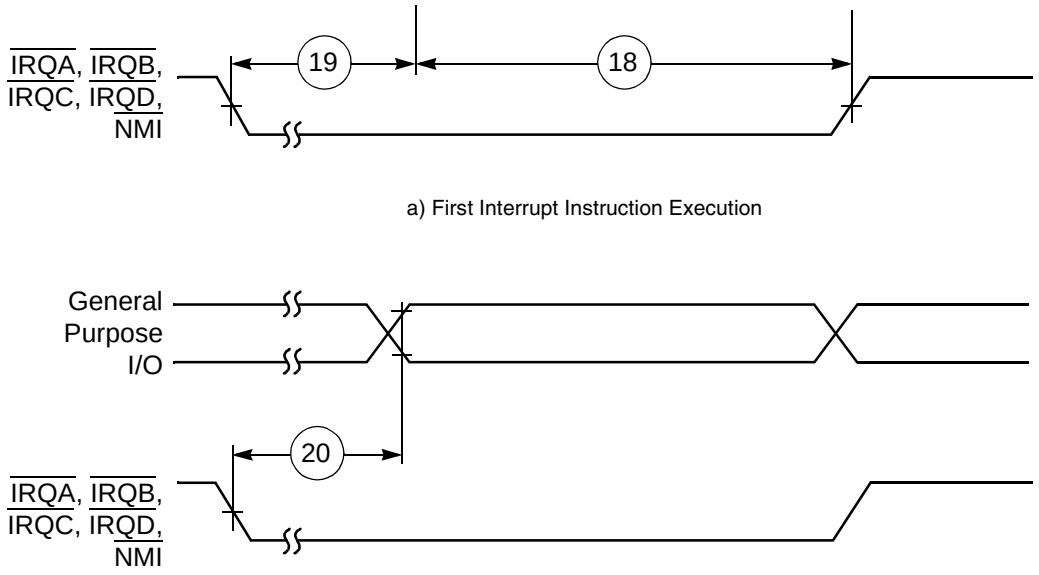


Figure 8. External Fast Interrupt Timing

12 Serial Host Interface SPI Protocol Timing

Table 20. Serial Host Interface SPI Protocol Timing

No.	Characteristics[1,3,4]	Mode	Expressions	Min	Max	Unit
23	Minimum serial clock cycle = t_{SPICC}(min)	Master	10.0 x T_C + 9	64.0	—	ns
24	Serial clock high period	Master	—	29.5	—	ns
		Slave	2.0 x T_C + 19.6	27.5	—	ns
25	Serial clock low period	Master	—	29.5	—	ns
		Slave	2.0 x T_C + 19.6	27.5	—	ns
26	Serial clock rise/fall time	Master	—	—	10	ns
		Slave	—	—	10	ns
27	$\overline{SS}$ assertion to first SCK edge CPHA = 0	Slave	2.0 x T_C + 12.6	34.4	—	ns
	CPHA = 1	Slave	—	10.0	—	ns
28	Last SCK edge to $\overline{SS}$ not asserted	Slave	—	12.0	—	ns
29	Data input valid to SCK edge (data input set-up time)	Master/Slave	—	0	—	ns
30	SCK last sampling edge to data input not valid	Master/Slave	3.0 x T_C	22.4	—	ns
31	$\overline{SS}$ assertion to data out active	Slave	—	5	—	ns
32	$\overline{SS}$ deassertion to data high impedance[2]	Slave	—	—	9	ns
33	SCK edge to data out valid (data out delay time)	Master/Slave	3.0 x T_C + 26.1	50.0	100	ns

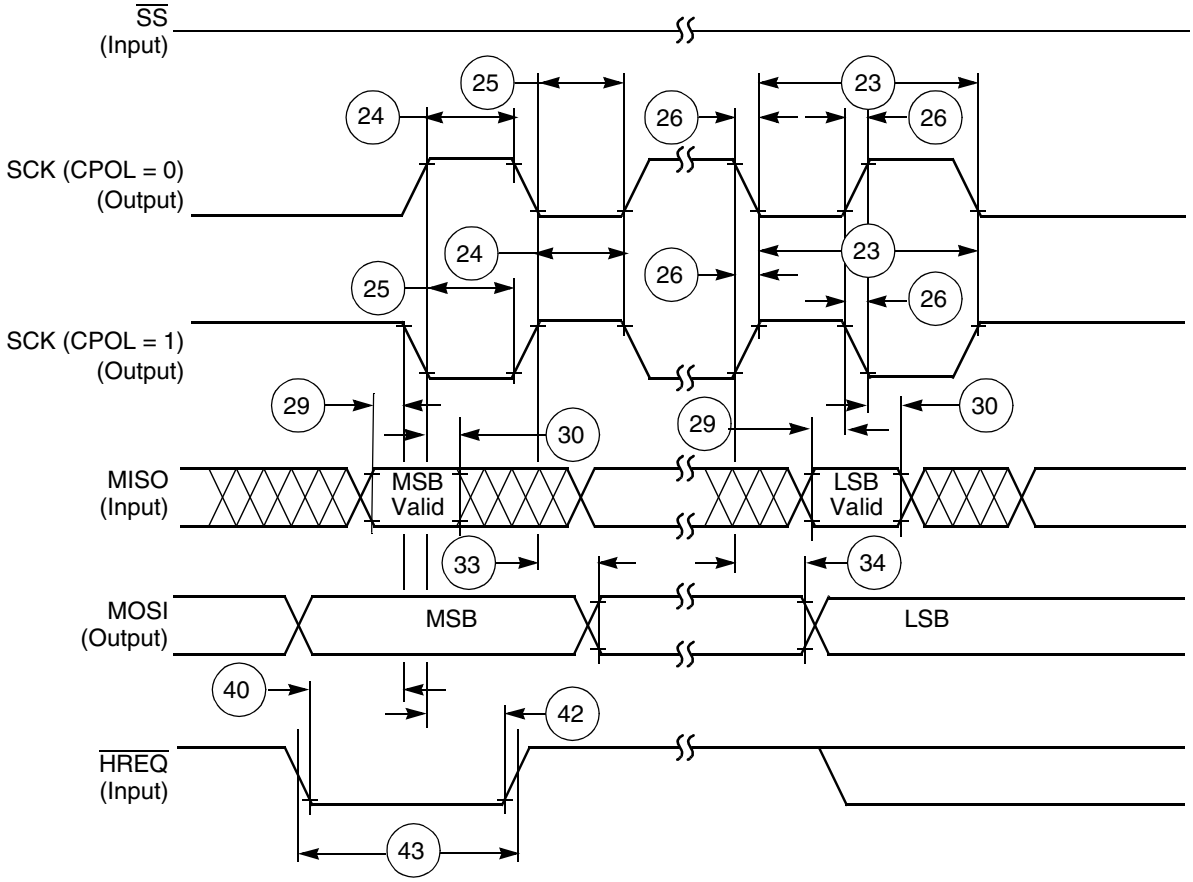
Table 20. Serial Host Interface SPI Protocol Timing (continued)

No.	Characteristics[1,3,4]	Mode	Expressions	Min	Max	Unit
34	SCK edge to data out not valid (data out hold time)	Master/Slave	2.0 x T_C	12.0	—	ns
35	$\overline{SS}$ assertion to data out valid (CPHA = 0)	Slave	—	—	15.0	ns
36	First SCK sampling edge to HREQ output deassertion	Slave	3.0 x T_C + 30	50	—	ns
37	Last SCK sampling edge to HREQ output not deasserted (CPHA = 1)	Slave	4.0 x T_C	52.2	—	ns
38	SS deassertion to HREQ output not deasserted (CPHA = 0)	Slave	3.0 x T_C + 30	46.6	—	ns
39	SS deassertion pulse width (CPHA = 0)	Slave	2.0 x T_C	12.7	—	ns
40	HREQ in assertion to first SCK edge	Master	0.5 x T_{SPICC} + 3.0 x T_C + 5	63.0	—	ns
41	HREQ in deassertion to last SCK sampling edge (HREQ in set-up time) (CPHA = 1)	Master	—	0	—	ns
42	First SCK edge to HREQ in not asserted (HREQ in hold time)	Master	—	0	—	ns
43	HREQ assertion width	Master	3.0 x T_C	20.0		ns

Note:

1. V_{CORE_VDD} = 1.2 5 ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
2. Periodically sampled, not 100% tested
3. All times assume noise free inputs
4. All times assume internal clock frequency of 150 MHz
5. Equation applies when the result is positive T_C

Figure 9. SPI Master Timing (CPHA = 0)



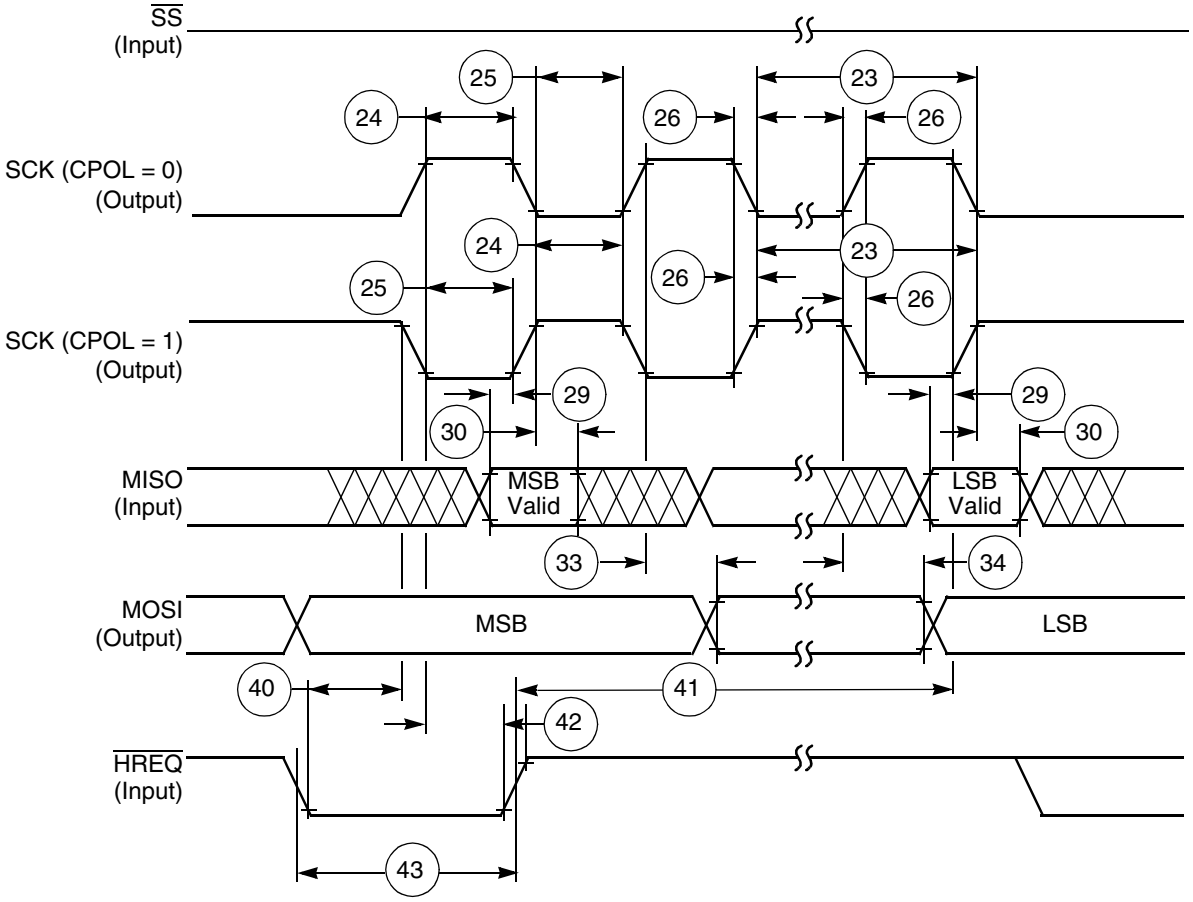


Figure 10. SPI Master Timing (CPHA = 1)

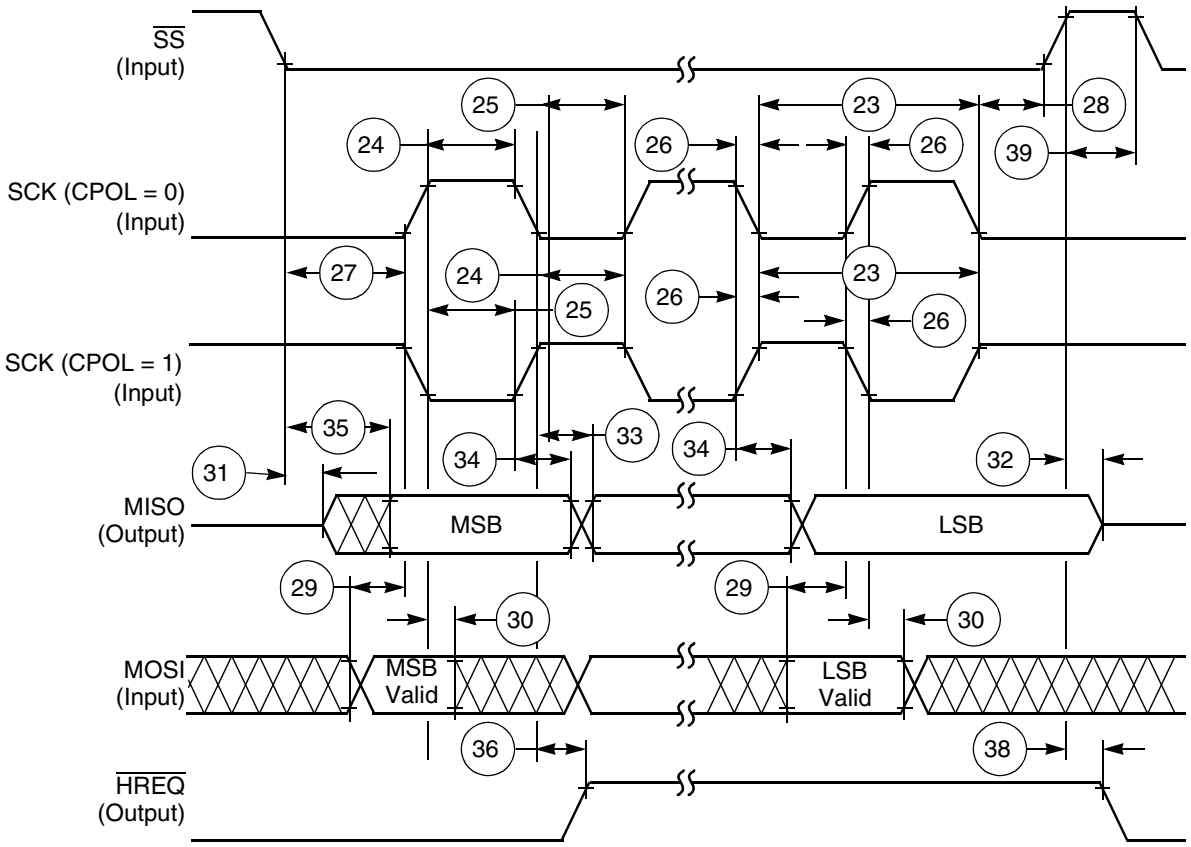


Figure 11. SPI Slave Timing (CPHA = 0)

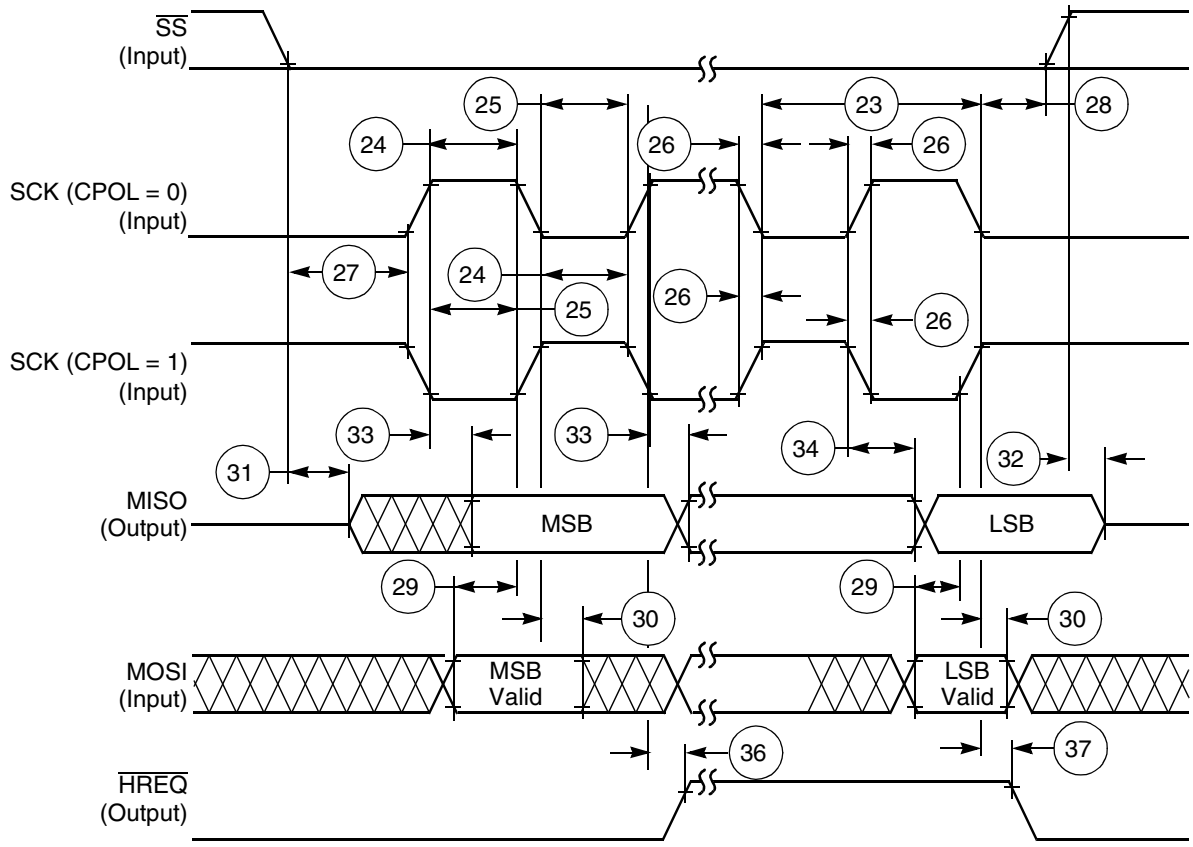


Figure 12. SPI Slave Timing (CPHA = 1)

13 Serial Host Interface (SHI) I2C Protocol Timing

Table 21. SHI I2C Protocol Timing

Standard I2C*							
No.	Characteristics[1]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
44	SCL clock frequency	F_{SCL}	—	100	—	400	kHz
44	SCL clock cycle	T_{SCL}	10	—	2.5	—	µs
45	Bus free time	T_{BUF}	4.7	—	1.3	—	µs
46	Start condition set-up time	T_{SUSTA}	4.7	—	0.6	—	µs
47	Start condition hold time	$T_{HD;STA}$	4.0	—	0.6	—	µs
48	SCL low period	T_{LOW}	4.7	—	1.3	—	µs
49	SCL high period	T_{HIGH}	4.0	—	1.3	—	µs
50	SCL and SDA rise time	T_R	—	5	—	5	ns
51	SCL and SDA fall time	T_F	—	5	—	5	ns

Table 21. SHI I2C Protocol Timing (continued)

Standard I2C*							
No.	Characteristics[1]	Symbol/ Expression	Standard		Fast-Mode		Unit
			Min	Max	Min	Max	
52	Data set-up time	$T_{SU;DAT}$	250	—	100	—	ns
53	Data hold time	$T_{HD;DAT}$	0.0	—	0.0	0.9	µs
54	DSP clock frequency	F_{OSC}	10.6	—	28.5	—	MHz
55	SCL low to data out valid	$T_{VD;DAT}$	—	3.4	—	0.9	µs
56	Stop condition setup time	$T_{SU;STO}$	4.0	—	0.6	—	µs
57	$\overline{\text{HREQ}}$ in deassertion to last SCL edge ($\overline{\text{HREQ}}$ in set-up time)	$t_{SU;RQI}$	0.0	—	0.0	—	ns
58	First SCL sampling edge to $\overline{\text{HREQ}}$ output deassertion	$T_{NG;RQO}$ $4 \times T_C + 30$	—	52	—	52	ns
59	Last SCL edge to HREQ output not deasserted	$T_{AS;RQO}$ $2 \times T_C + 30$	52	—	52	—	ns
60	HREQ in assertion to first SCL edge	$T_{AS;RQI}$ $0.5 \times T_I2_{CCP}$ $-0.5 \times T_C - 21$	4327	—	927	—	ns
61	First SCL edge to $\overline{\text{HREQ}}$ in not asserted ($\overline{\text{HREQ}}$ in hold time.)	$t_{HO;RQI}$	0.0	—	0.0	—	ns

Note:
1. VCORE_VDD = 1.2 5 ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; CL = 50 pF
2. Pull-up resistor: R_P (min) = 1.5 kOhm
3. Capacitive load: C_b (max) = 50 pF
4. All times assume noise free inputs
5. All times assume internal clock frequency of 180MHz

13.1 Programming the Serial Clock

The programmed serial clock cycle, T_{I^2CCP}, is specified by the value of the HDM[7:0] and HRS bits of the HCKR (SHI clock control register).

The expression for T_{I^2CCP} is

$$T_{I^2CCP} = [T_C \times 2 \times (HDM[7:0] + 1) \times (7 \times (1 - HRS) + 1)] \quad \textit{Eqn. 1}$$

where

— HRS is the pre-scaler rate select bit. When HRS is cleared, the fixed divide-by-eight pre-scaler is operational. When HRS is set, the pre-scaler is bypassed.

— HDM[7:0] are the divider modulus select bits. A divide ratio from 1 to 256 (HDM[7:0] = $00 to $FF) may be selected.

In I^2C mode, the user may select a value for the programmed serial clock cycle from

$$6 \times T_C \text{ (if HDM[7:0] = \$02 and HRS = 1)} \qquad \textit{Eqn. 2}$$

to

$$4096 \times T_C \text{ (if HDM[7:0] = \$FF and HRS = 0)} \qquad \textit{Eqn. 3}$$

The programmed serial clock cycle (T_{I^2CCP}), SCL rise time (T_R), should be chosen in order to achieve the desired SCL serial clock cycle (T_{SCL}), as shown in Table 22.

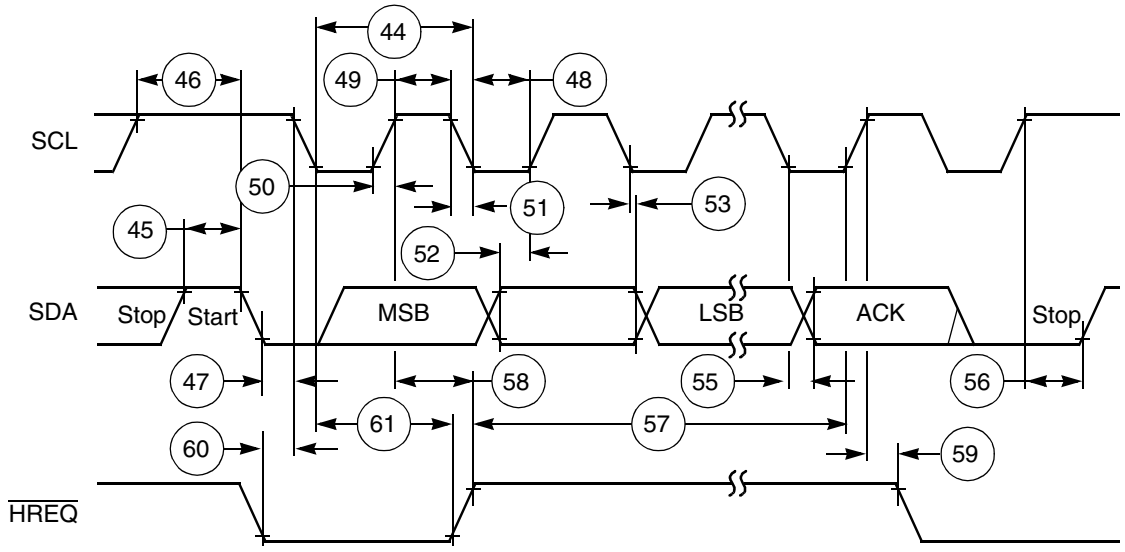


Figure 13. I^2C Timing

14 Enhanced Serial Audio Interface Timing

Table 22. Enhanced Serial Audio Interface Timing

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
62	Clock cycle[5]	t_{SSICC}	$4 \times T_C$ $4 \times T_C$	22.3 22.3	— —	x ck i ck	ns
63	Clock high period • For internal clock • For external clock	t_{SSICCH}	 $2 \times T_C$ $2 \times T_C$	 12.0 12.0	 — —		ns
64	Clock low period • For internal clock • For external clock	t_{SSICCL}	 $2 \times T_C$ $2 \times T_C$	 12.0 12.0	 — —		ns
65	SCKR edge to FSR out (bl) high	—	—	— —	37.0 22.0	x ck i ck a	ns
66	SCKR edge to FSR out (bl) low	—	—	— —	37.0 22.0	x ck i ck a	ns

Table 22. Enhanced Serial Audio Interface Timing (continued)

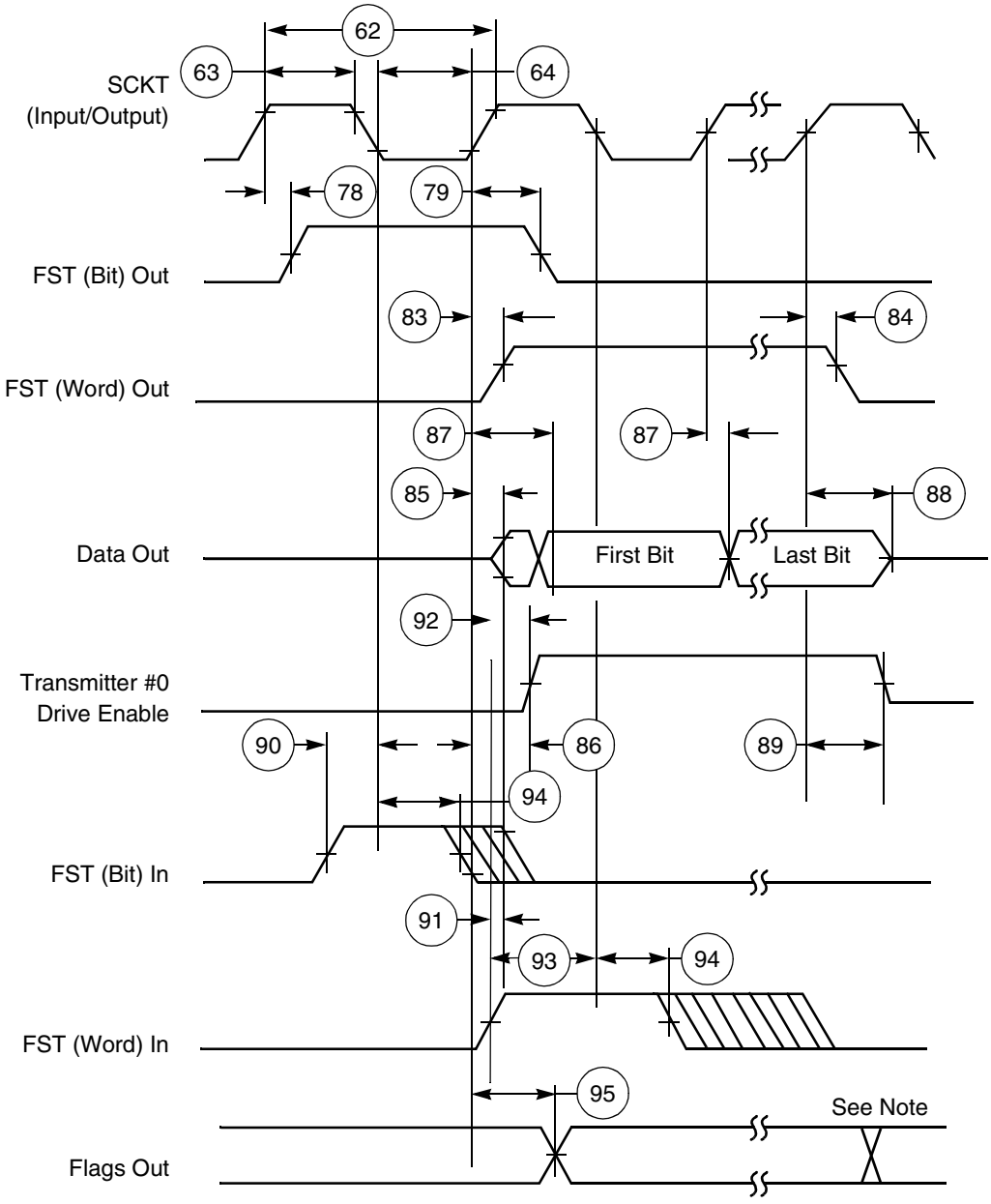
No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
67	SCKR edge to FSR out (wr) high[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
68	SCKR edge to FSR out (wr) low[6]	—	—	— —	39.0 24.0	x ck i ck a	ns
69	SCKR edge to FSR out (wl) high	—	—	— —	36.0 21.0	x ck i ck a	ns
70	SCKR edge to FSR out (wl) low	—	—	— —	37.0 22.0	x ck i ck a	ns
71	Data in setup time before SCKR (SCK in synchronous mode) edge	—	—	12.0 19.0	— —	x ck i ck	ns
72	Data in hold time after SCKR edge	—	—	5.0 3.0	— —	x ck i ck	ns
73	FSR input (bl, wr) high before SCKR edge [6]	—	—	2.0 23.0	— —	x ck i ck a	ns
74	FSR input (wl) high before SCKR edge	—	—	2.0 23.0	— —	x ck i ck a	ns
75	FSR input hold time after SCKR edge	—	—	3.0 0.0	— —	x ck i ck a	ns
76	Flags input setup before SCKR edge	—	—	0.0 19.0	— —	x ck i ck s	ns
77	Flags input hold time after SCKR edge	—	—	6.0 0.0	— —	x ck i ck s	ns
78	SCKT edge to FST out (bl) high	—	—	— —	29.0 15.0	x ck i ck	ns
79	SCKT edge to FST out (bl) low	—	—	— —	31.0 17.0	x ck i ck	ns
80	SCKT edge to FST out (wr) high[6]	—	—	— —	31.0 17.0	x ck i ck	ns
81	SCKT edge to FST out (wr) low[6]	—	—	— —	33.0 19.0	x ck i ck	ns
82	SCKT edge to FST out (wl) high	—	—	— —	30.0 16.0	x ck i ck	ns
83	SCKT edge to FST out (wl) low	—	—	— —	31.0 17.0	x ck i ck	ns
84	SCKT edge to data out enable from high impedance	—	—	— —	31.0 17.0	x ck i ck	ns
85	SCKT edge to transmitter #0 drive enable assertion	—	—	— —	34.0 20.0	x ck i ck	ns
86	SCKT edge to data out valid	—	—	— —	26.5 21.0	x ck i ck	ns
87	SCKT edge to data out high impedance[7]	—	—	— —	31.0 16.0	x ck i ck	ns

Table 22. Enhanced Serial Audio Interface Timing (continued)

No.	Characteristics[1, 2, 3]	Symbol	Expression	Min	Max	Condition[4]	Unit
88	SCKT edge to transmitter #0 drive enable deassertion[7]	—	—	— —	34.0 20.0	x ck i ck	ns
89	FST input (bl, wr) setup time before SCKT edge[6]	—	—	2.0 21.0	— —	x ck i ck	ns
90	FST input (wl) setup time before SCKT edge	—	—	2.0 21.0	— —	x ck i ck	ns
91	FST input hold time after SCKT edge	—	—	4.0 0.0	— —	x ck i ck	ns
92	FST input (wl) to data out enable from high impedance	—	—	—	27.0	—	ns
93	FST input (wl) to transmitter #0 drive enable assertion	—	—	—	31.0	—	ns
94	Flag output valid after SCKT edge	—	—	— —	32.0 18.0	x ck i ck	ns
95	HCKR/HCKT clock cycle	—	2 x T_C	13.4	—		ns
96	HCKT input edge to SCKT output	—	—	—	18.0		ns
97	HCKR input edge to SCKR output	—	—	—	18.0		ns

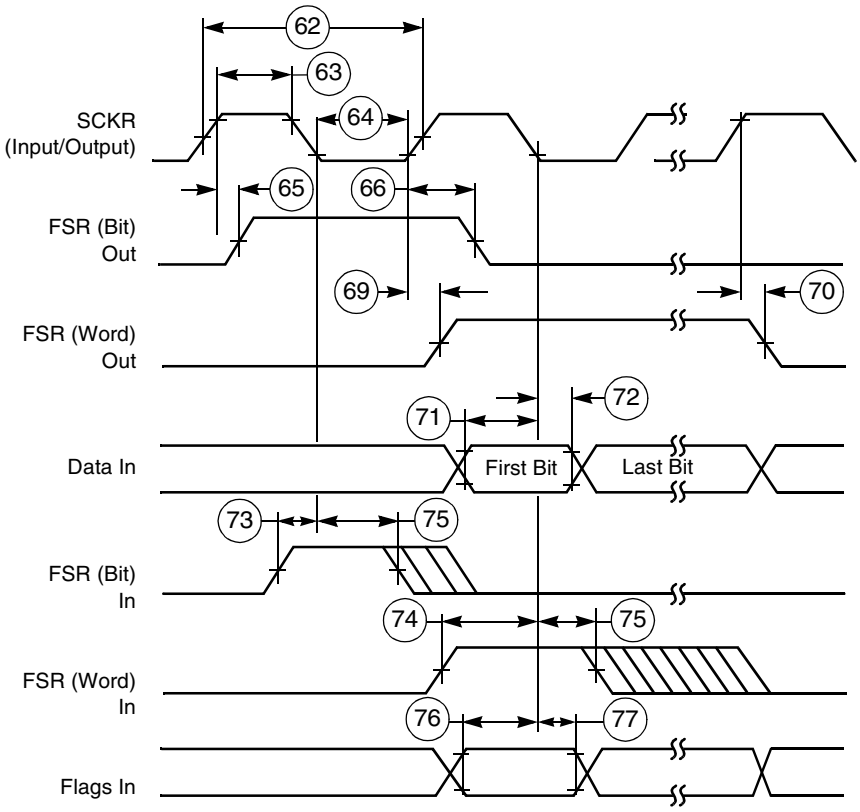
Note:

1. V_{CORE_VDD} = 1.25 ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
2. SCKT(SCKT pin) = transmit clock
   SCKR(SCKR pin) = receive clock
   FST(FST pin) = transmit frame sync
   FSR(FSR pin) = receive frame sync
   HCKT(HCKT pin) = transmit high frequency clock
   HCKR(HCKR pin) = receive high frequency clock
3. bl = bit length
   wl = word length
   wr = word length relative
4. i ck = internal clock
   x ck = external clock
   i ck a = internal clock, asynchronous mode
   (asynchronous implies that SCKT and SCKR are two different clocks)
   i ck s = internal clock, synchronous mode
   (synchronous implies that SCKT and SCKR are the same clock)
5. For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.
6. The word-relative frame sync signal waveform relative to the clock operates in the same manner as the bit-length frame sync signal waveform, but spreads from one serial clock before first bit clock (same as bit length frame sync signal), until the one before last bit clock of the first word in frame.
7. Periodically sampled and not 100% tested
8. ESAI_1 specs match those of ESAI_0



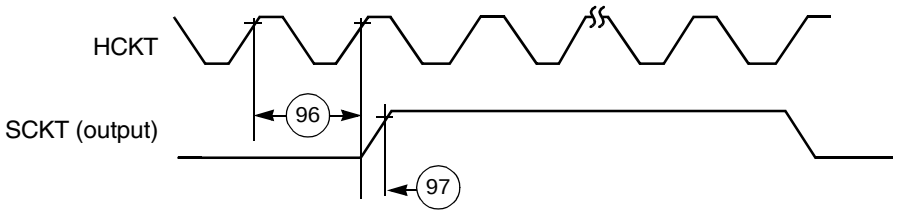
Note: In network mode, output flag transitions can occur at the start of each time slot within the frame. In normal mode, the output flag state is asserted for the entire frame period. Figure 14 is drawn assuming positive polarity bit clock (TCKP=0) and positive frame sync polarity (TFSP=0).

Figure 14. ESAI Transmitter Timing



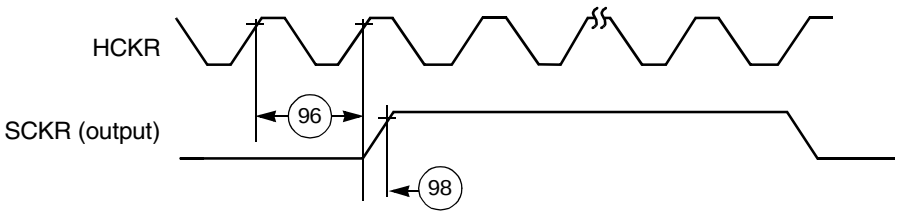
Note: Figure 15 is drawn assuming positive polarity bit clock (RCKP=0) and positive frame sync polarity (RFSP=0).

Figure 15. ESAI Receiver Timing



Note: Figure 16 is drawn assuming positive polarity high frequency clock (THCKP=0) and positive bit clock polarity (TCKP=0).

Figure 16. ESAI HCKT Timing



Note: Figure 17 is drawn assuming positive polarity high frequency clock (RHCKP=0) and positive bit clock polarity (RCKP=0).

Figure 17. ESAI HCKR Timing

15 Digital Audio Transmitter Timing

Table 23. Digital Audio Transmitter Timing

No.	Characteristic	Expression	181 MHz		Unit
			Min	Max	
99	ACI frequency (see note)	1 / (2 x T_C)	—	90	MHz
100	ACI period	$2 \times T_C$	11.1	—	ns
101	ACI high duration	$0.5 \times T_C$	2.8	—	ns
102	ACI low duration	$0.5 \times T_C$	2.8	—	ns
103	ACI rising edge to ADO valid	$1.5 \times T_C$	—	8.3	ns

Note:

1. In order to assure proper operation of the DAX, the ACI frequency should be less than 1/2 of theDSP56371 internal clock frequency. For example, if the DSP56371 is running at 181 MHz internally, the ACI frequency should be less than 90MHz.

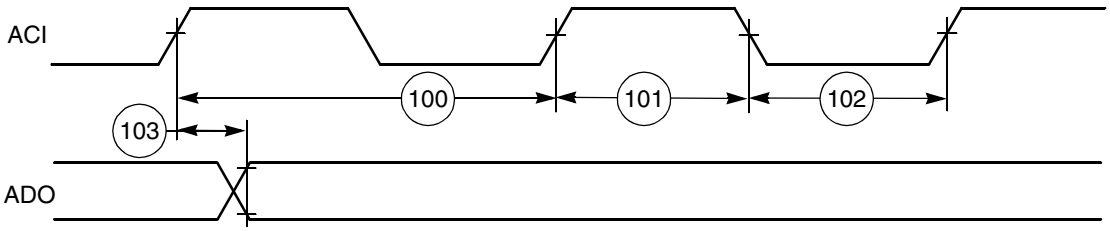


Figure 18. Digital Audio Transmitter Timing

16 Timer Timing

Table 24. Timer Timing

No.	Characteristics	Expression	181 MHz		Unit
			Min	Max	
104	TIO Low	$2 \times T_C + 2.0$	13	—	ns
105	TIO High	$2 \times T_C + 2.0$	13	—	ns

Note:
1. V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF

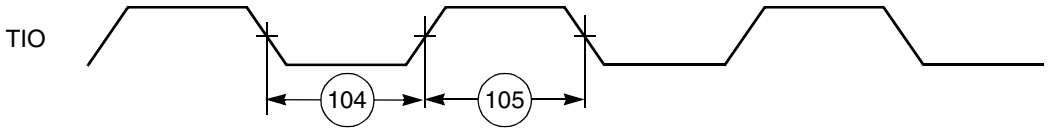


Figure 19. TIO Timer Event Input Restrictions

17 GPIO Timing

Table 25. GPIO Timing

No.	Characteristics[1]	Expression	Min	Max	Unit
106	FOSC edge to GPIO out valid (GPIO out delay time)		—	7	ns
107	FOSC edge to GPIO out not valid (GPIO out hold time)		—	7	ns
108	FOSC In valid to EXTAL edge (GPIO in set-up time)		2	—	ns
109	FOSC edge to GPIO in not valid (GPIO in hold time)		0	—	ns
110	Minimum GPIO pulse high width (except Port F)	$T_C + 13$	19	—	ns
111	Minimum GPIO pulse low width (except Port F)	$T_C + 13$	19		ns
112	Minimum GPIO pulse low width (Port F)	$6 \times T_C$	33.3		ns
113	Minimum GPIO pulse high width (Port F)	$6 \times T_C$	33.3		ns
114	GPIO out rise time	—	—	13	ns
115	GPIO out fall time	—	—	13	ns

Note:
1. V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
2. PLL Disabled, EXTAL driven by a square wave

Figure 20. GPIO Timing

18 JTAG Timing

Table 26. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
116	TCK frequency of operation (1/($T_C \times 6$); maximum 22 MHz)	0.0	22.0	MHz
117	TCK cycle time	45.0	—	ns
118	TCK clock pulse width	20.0	—	ns
119	TCK rise and fall times	0.0	10.0	ns
120	TCK low to output data valid	0.0	40.0	ns
121	TCK low to output high impedance	0.0	40.0	ns
122	TMS, TDI data setup time	5.0	—	ns
123	TMS, TDI data hold time	25.0	—	ns
124	TCK low to TDO data valid	0.0	44.0	ns
125	TCK low to TDO high impedance	0.0	44.0	ns

Note:
V_{CORE_VDD} = 1.25 V ± 0.05 V; T_J = –40°C to 115°C for 150 MHz; T_J = 0°C to 100°C for 181 MHz; C_L = 50 pF
All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

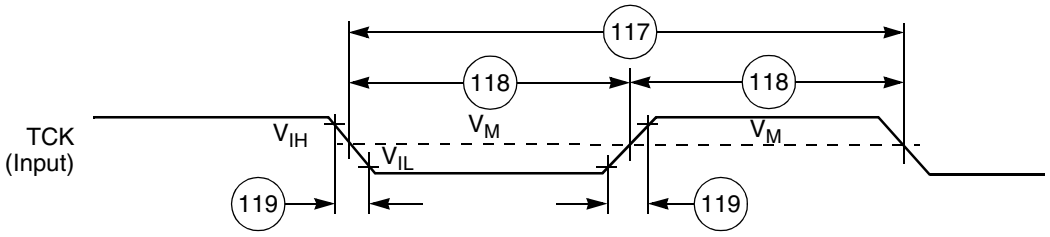


Figure 21. Test Clock Input Timing Diagram

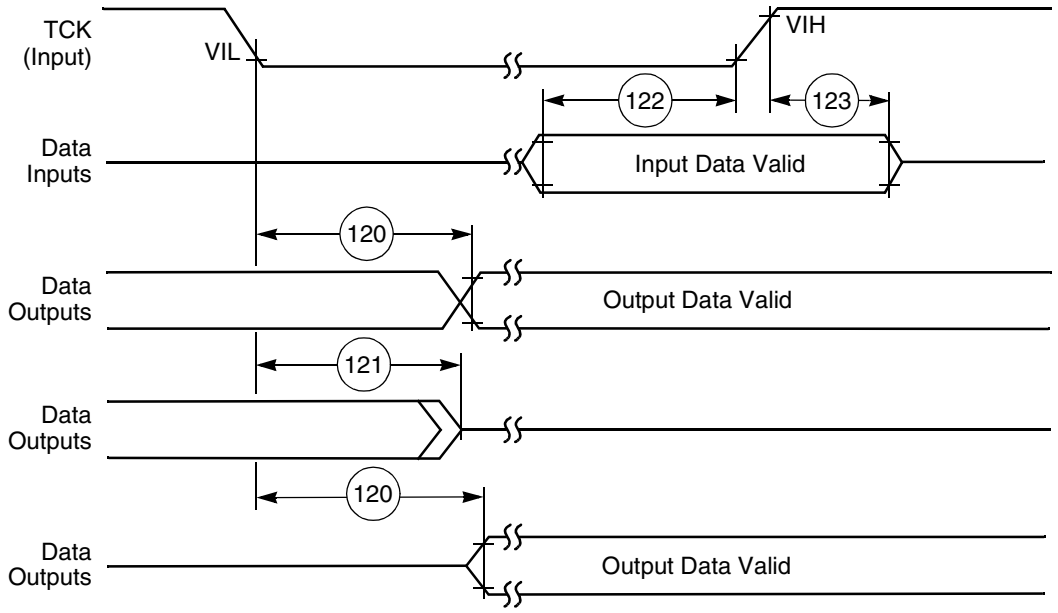


Figure 22. Debugger Port Timing Diagram

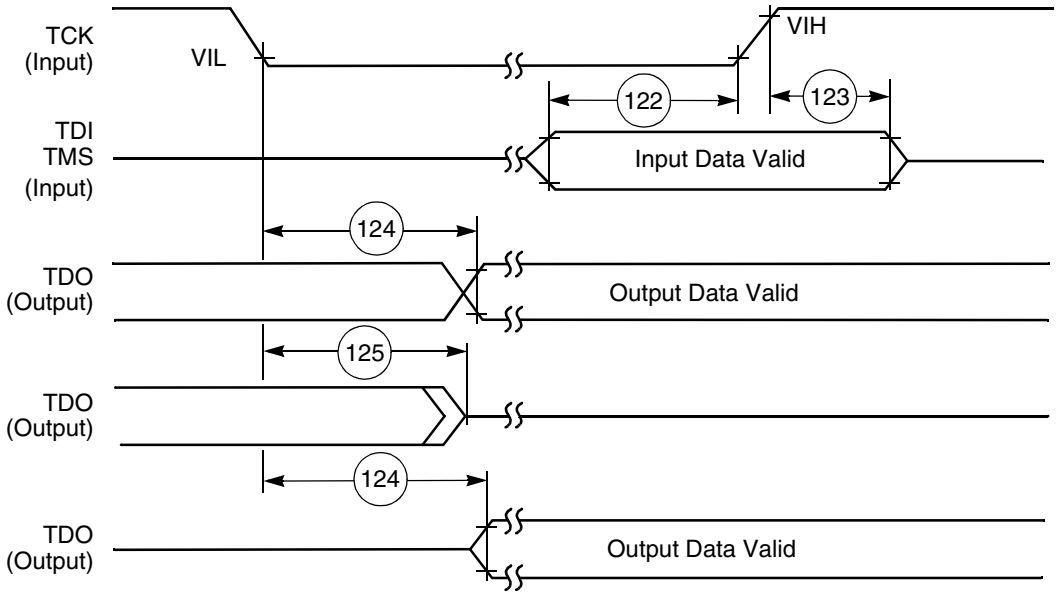


Figure 23. Test Access Port Timing Diagram

19 Package Information

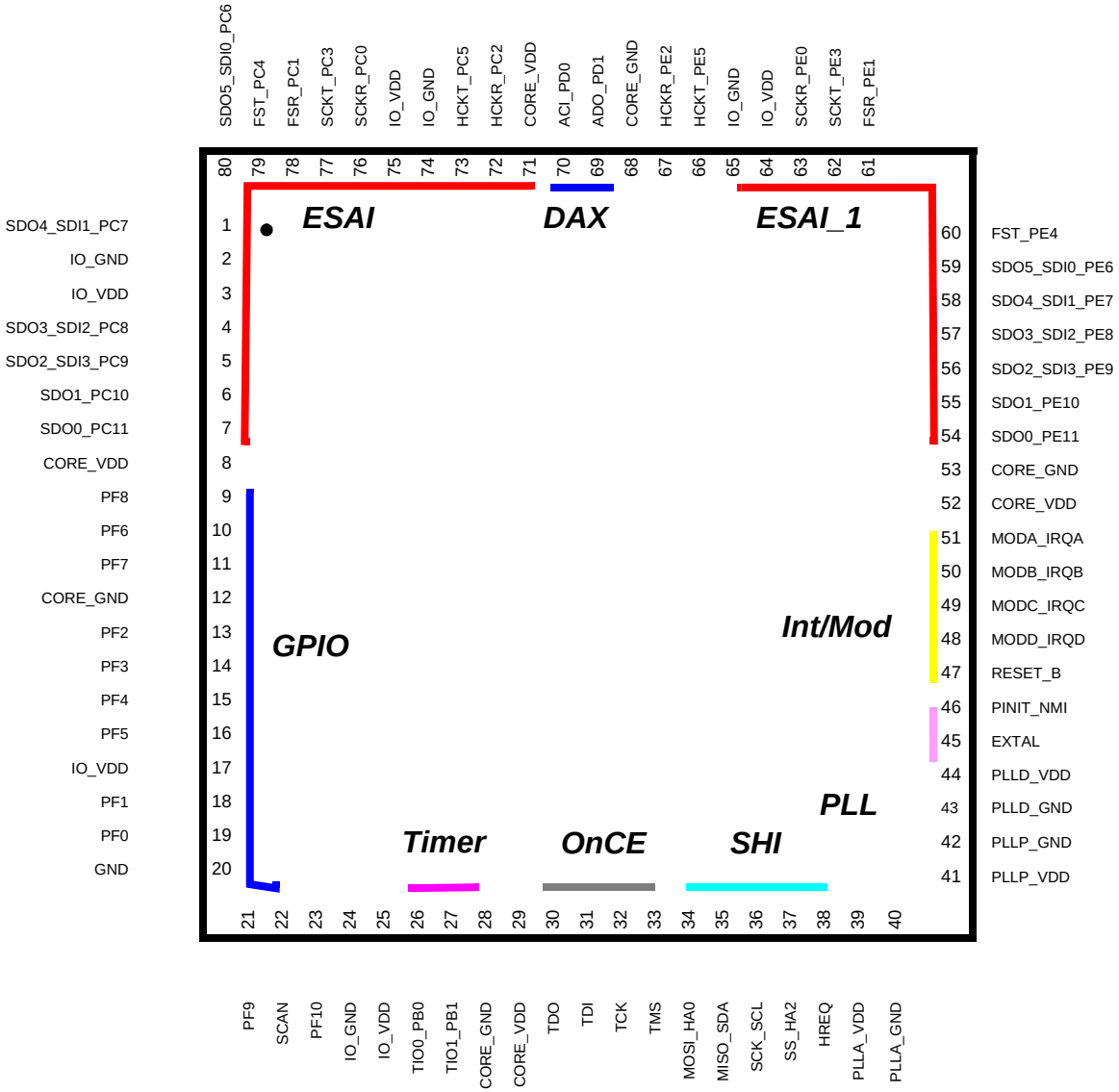
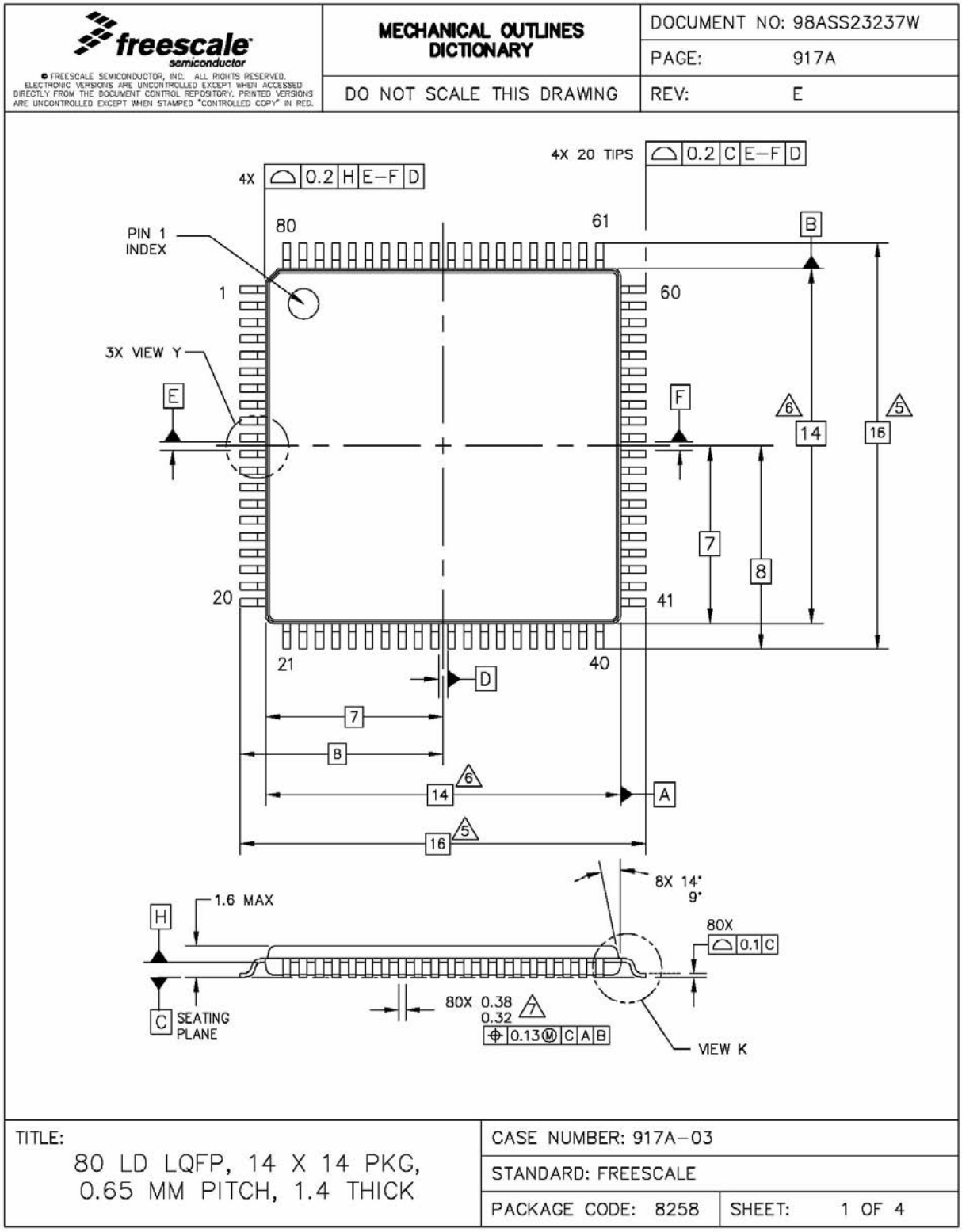


Figure 24. DSP56371 Pinout

Table 27. Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	SDO4_SDI1_PC7	21	PF9	41	PLLP_VDD	61	FSR_PE1
2	IO_GND	22	SCAN	42	PLLP_GND	62	SCKT_PE3
3	IO_VDD	23	PF10	43	PLLD_GND	63	SCKR_PE0
4	SDO3_SDI2_PC8	24	IO_GND	44	PLLD_VDD	64	IO_VDD
5	SDO2_SDI3_PC9	25	IO_VDD	45	EXTAL	65	IO_GND
6	SDO1_PC10	26	TI0_PB0	46	PINIT_NMI	66	HCKT_PE5
7	SDO0_PC11	27	TI0_PB1	47	RESET_B	67	HCKR_PE2
8	CORE_VDD	28	CORE_GND	48	MODD_IRQD	68	CORE_GND
9	PF8	29	CORE_VDD	49	MODC_IRQC	69	ADO_PD1
10	PF6	30	TDO	50	MODB_IRQB	70	ADI_PD0
11	PF7	31	TDI	51	MODA_IRQA	71	CORE_VDD
12	CORE_GND	32	TCK	52	CORE_VDD	72	HCKR_PC2
13	PF2	33	TMS	53	CORE_GND	73	HCKT2_PC5
14	PF3	34	MOSI_HA0	54	SDO0_PE11	74	IO_GND
15	PF4	35	MISO_SDA	55	SDO1_PE10	75	IO_VDD
16	PF5	36	SCK_SCL	56	SDO2_SDI3_PE9	76	SCKR_PC0
17	IO_VDD	37	SS_HA2	57	SDO3_SDI2_PE8	77	SCKT_PC3
18	PF1	38	HREQ	58	SDO4_SDI1_PE7	78	FSR_PC1
19	PF0	39	PLLA_VDD	59	SDO5_SD10_PE6	79	FST_PC4
20	GND	40	PLLA_GND	60	FST_PE4	80	SDO5_SDI10_PC6



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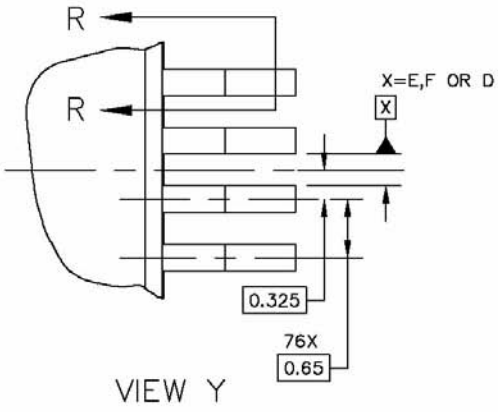

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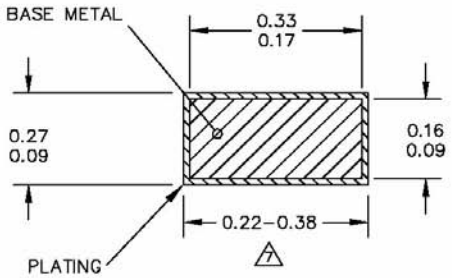

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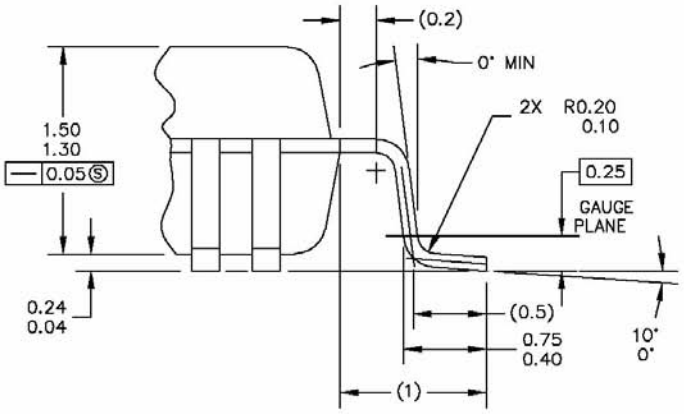
ROTATED 90° CW



VIEW K

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A–03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 2 OF 4

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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE:	CASE NUMBER: 917A–03	
80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 4

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REVISION HISTORY

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D	GARY JOHNSON	REFORMAT DOCUMENT. DELETED DUAL DIMENSIONS (INCH). CHANGED DOCUMENT TITLE FROM TQFP TO LQFP.	AZHAR A.	11 MAR 2004
E	PATRICE L.	UPDATED DRAWINGS PER FREESCALE FORMAT.	KL CHIN	7 OCT 2004

TITLE:
80 LQFP, 14 X 14 PKG,
0.65 MM PITCH, 1.4 THICK

CASE NUMBER: 917A-03
STANDARD: FREESCALE
PACKAGE CODE: 8258
SHEET: 4 OF 4

20 Design Considerations

20.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the following equation:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \textit{Eqn. 4}$$

Where: T_A=ambient temperature °C
R_{qJA}=package junction-to-ambient thermal resistance °C/W
P_D=power dissipation in package W

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 5}$$

Where: $R_{\theta JA}$=package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$=package junction-to-case thermal resistance °C/W
$R_{\theta CA}$=package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

A complicating factor is the existence of three common ways for determining the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to where the leads are attached to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, the thermal resistance is computed using the value obtained by the equation $(T_J - T_T)/P_D$.

As noted above, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable for determining the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, using the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will estimate a junction temperature slightly hotter than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when using the surface temperature of the package. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

21 Electrical Design Considerations

CAUTION

This device contains circuitry protecting against damage due to high static voltage or electrical fields. However, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}). The suggested value for a pull-up or pull-down resistor is 10 k ohm.

Use the following list of recommendations to assure correct DSP operation:

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01–0.1 µF bypass capacitors positioned as close as possible to the four sides of the package to connect the V_{CC} power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 1.2 cm (0.5 inch) per capacitor lead.
- Route the DVDD pin carefully to minimize noise.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ pins. Maximum PCB trace lengths on the order of 15 cm (6 inches) are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- Take special care to minimize noise levels on the V_{CCP} and GND_P pins.
- If multiple DSP56371 devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal must be supplied before deassertion of RESET.

- At power-up, ensure that the voltage difference between the 3.3 V tolerant pins and the chip V_{CC} never exceeds a 3.00 V.

21.1 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors which affect current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by the following formula:

$$I = C \times V \times f \qquad \textit{Eqn. 6}$$

where C=node/pin capacitance
V=voltage swing
f=frequency of node/pin toggle

Power Consumption Example

For a GPIO address pin loaded with 50 pF capacitance, operating at 3.3 V, and with a 150 MHz clock, toggling at its maximum possible rate (75 MHz), the current consumption is

$$I = 50x10^{-12}x3.3x75x10^{6} = 12.375mA \qquad \textit{Eqn. 7}$$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions, which is not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

For applications that require very low current consumption, do the following:

- Minimize the number of pins that are switching.
- Minimize the capacitive load on the pins.

One way to evaluate power consumption is to use a current per MIPS measurement methodology to minimize specific board effects (for example, to compensate for measured board current not caused by the DSP). Use the test algorithm, specific test current measurements, and the following equation to derive the current per MIPS value.

$$\text{I/MIPS} = \text{I/MHz} = (I_{typF2} - I_{typF1})/(F2 - F1) \qquad \textit{Eqn. 8}$$

where : I_{typF2}=current at F2
I_{typF1}=current at F1
F2=high frequency (any specified operating frequency)
F1=low frequency (any specified operating frequency lower than F2)

NOTE

F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

22 Power Consumption Benchmark

The following benchmark program permits evaluation of DSP power usage in a test situation.

```
;*********************************;*******************************

;* ;* CHECKS Typical Power Consumption

;*************************************************************************

ORG P:$000800
move #$000000,r1
move #$000000,r0
do #1024,ldmem
move r1,p:(r0)
move r1,y:(r0)+
ldmem nop



move #0,b1

;jmp $FF2AE0

;org P:$FF2AE0
move b1,y:>$100
move #$FF,B
move #>$AF080,X0
move #>$FF2AD6,r0
move #$0,r1

dor #6,loop1

move p:(r0)+,x1
move x0,p:(r1)+
move x1,p:(r1)+
nop
loop1

move #$0,vba
move #$0,sp
move #$0,sc
reset
move #$FFFFFF,m0
move m0,m1
move m0,m2
move m0,m3
move m0,m4
move m0,m5
move m0,m6
move m0,m7
move #>$102,ep
move #>$18,sz
move #>$110000,omr
```

```
move #$300,sr
movep #>$F02000,X:$FFFFFF
movep #$187,X:$FFFFFE

;then sets up BCR and AAR registers

;then sets up PORTB and HDI08 PORT

andi #$FC,mr

;start running ROM intialisation stage
;jsr $FF1C7E

; Set green HLX zone table
jsr $FF1D64

; Run GPIONil function
jsr $FF2F82

; Initialise Green HLX
jsr $FF1FA1

; Disable DAX
move #>$15F,x1
move x1,P:$FF0D7F

; Run Green HLX
jmp $FF1FDB


nop
nop
nop
nop
nop
nop
dor forever,endprog
nop
nop
endprog nop
```

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