Commercial Grade SHARC® Family DSP Microcomputer

ADSP-21061/ADSP-21061L

SUMMARY

High performance signal processor for communications, graphics, and imaging applications

Super Harvard Architecture

- **Four independent buses for dual data fetch, instruction fetch, and nonintrusive I/O**

32-bit IEEE floating-point computation units—multiplier, ALU, and shifter

Dual-ported on-chip SRAM and integrated I/O peripherals—a complete system-on-a-chip

Integrated multiprocessing features

Dual data address generators with modulo and bit-reverse addressing

Efficient program sequencing with zero-overhead looping: single-cycle loop setup

IEEE JTAG Standard 1149.1 test access port and on-chip emulation

32-bit single-precision and 40-bit extended-precision IEEE floating-point data formats or 32-bit fixed-point data format

240-lead MQFP package, thermally enhanced MQFP, 225-ball plastic ball grid array (PBGA)

Lead (Pb) free packages. **For more information, see Ordering Guide on Page 53.**

KEY FEATURES—PROCESSOR CORE

50 MIPS, 20 ns instruction rate, single-cycle instruction execution

120 MFLOPS peak, 80 MFLOPS sustained performance

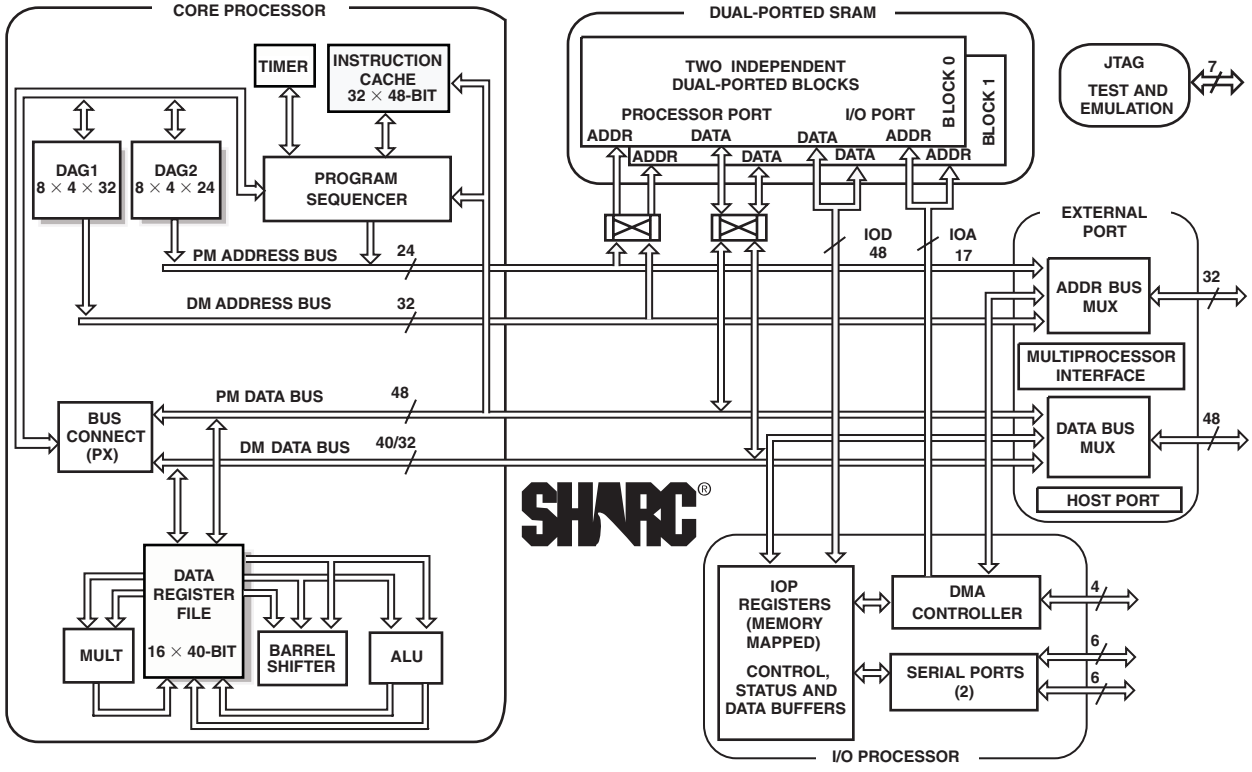

Figure 1. Functional Block Diagram

Rev. C

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Parallel Computations

Single-cycle multiply and ALU operations in parallel with dual memory read/write and instruction fetch

Multiply with add and subtract for accelerated FFT butterfly computation

1M bit On-Chip SRAM

Dual-ported for independent access by core processor and DMA

Off-Chip Memory Interfacing

4 gigawords addressable

Programmable wait state generation, page-mode DRAM support

DMA Controller

6 DMA channels for transfers between ADSP-21061 internal memory and external memory, external peripherals, host processor, or serial ports

Background DMA transfers at up to 40 MHz, in parallel with full-speed processor execution

Host Processor Interface to 16- and 32-Bit Microprocessors

Host can directly read/write ADSP-21061 internal memory

Multiprocessing

Glueless connection for scalable DSP multiprocessing architecture

Distributed on-chip bus arbitration for parallel bus connect of up to six ADSP-21061s plus host

240 MBps transfer rate over parallel bus

Serial Ports

Two 40 Mbps synchronous serial ports with companding hardware

Independent transmit and receive functions

CONTENTS

REVISION HISTORY

7/07—Rev B to Rev C

Added
Porting Code From the ADSP-21060 or ADSP-21062 8

Added several new lead (Pb) free models. See
Ordering Guide 53

GENERAL NOTE

This data sheet represents production released specifications for the ADSP-21061 (5 V) and ADSP-21061L (3.3 V) processors for 33 MHz, 40 MHz, 44 MHz, and 50 MHz speed grades. The product name“ADSP-21061” is used throughout this data sheet to represent all devices, except where expressly noted.

GENERAL DESCRIPTION

The ADSP-21061 SHARC—Super Harvard Architecture Computer—is a signal processing microcomputer that offers new capabilities and levels of performance. The ADSP-21061 SHARC is a 32-bit processor optimized for high performance DSP applications. The ADSP-21061 builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-21061 has a 20 ns instruction cycle time and operates at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table 1 shows performance benchmarks for the ADSP-21061/ADSP-21061L.

The ADSP-21061 SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including 1M bit SRAM memory, a host processor interface, a DMA controller, serial ports, and parallel bus connectivity for glueless DSP multiprocessing.

Table 1. Benchmarks (at 50 MHz)

Benchmark Algorithm	Speed	Cycles
1024 Point Complex FFT (Radix 4, with reversal)	.37 ms	18,221
FIR Filter (per tap)	20 ns	1
IIR Filter (per biquad)	80 ns	4
Divide (y/x)	120 ns	6
Inverse Square Root	180 ns	9
DMA Transfer Rate	300M Bps	

The ADSP-21061 continues SHARC's industry-leading standards of integration for DSPs, combining a high performance 32-bit DSP core with integrated, on-chip system features.

The block diagram on Page 1, illustrates the following architectural features:

- Computation units (ALU, multiplier, and shifter) with a shared data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting four 32-bit data transfers between memory and the core at every core processor cycle
- Interval timer
- On-chip SRAM
- External port for interfacing to off-chip memory and peripherals
- Host port and multiprocessor interface
- DMA controller
- Serial ports
- JTAG test access port

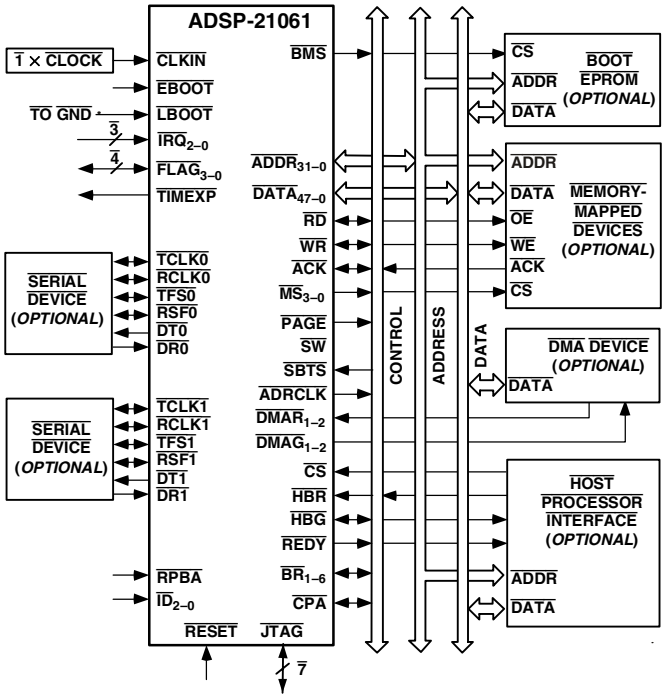

Figure 2. ADSP-21061/ADSP-21061L System Sample Configuration

SHARC FAMILY CORE ARCHITECTURE

The ADSP-21061 includes the following architectural features of the ADSP-21000 family core. The ADSP-21061 processors are code- and function-compatible with the ADSP-21020, ADSP-21060, and ADSP-21062 SHARC processors.

Independent, Parallel Computation Units

The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended-precision 40-bit floating-point, and 32-bit fixed-point data formats.

Data Register File

A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.

Single-Cycle Fetch of Instruction and Two Operands

The ADSP-21061 features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (Figure 1 on Page 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.

Instruction Cache

The ADSP-21061 includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

Data Address Generators with Hardware Circular Buffers

The ADSP-21061's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs of the ADSP-21061 contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance and simplifying implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21061 can conditionally execute a multiply, an add, a subtract, and a branch, all in a single instruction.

MEMORY AND I/O INTERFACE FEATURES

The ADSP-21061 processors add the following architectural features to the SHARC family core.

Dual-Ported On-Chip Memory

The ADSP-21061 contains one megabit of on-chip SRAM, organized as two blocks of 0.5M bits each. Each bank has eight 16-bit columns with 4k 16-bit words per column. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle (see Figure 4 for the ADSP-21061 memory map).

On the ADSP-21061, the memory can be configured as a maximum of 32k words of 32-bit data, 64k words for 16-bit data, 16k words of 48-bit instructions (and 40-bit data) or combinations of different word sizes up to 1 megabit. All the memory can be accessed as 16-bit, 32-bit, or 48-bit.

A 16-bit floating-point storage format is supported, which effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-21061's external port.

Off-Chip Memory and Peripherals Interface

The ADSP-21061's external port provides the processor's interface to off-chip memory and peripherals. The 4-gigaword off-chip address space is included in the ADSP-21061's unified address space. The separate on-chip buses—for program memory, data memory, and I/O—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus. The on-chip Super Harvard Architecture provides three-bus performance, while the off-chip unified address space gives flexibility to the designer.

Addressing of external memory devices is facilitated by on-chip decoding of high order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-21061 provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

Host Processor Interface

The ADSP-21061's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-21061's external port and is memory-mapped into the unified address space. Two channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

The host processor requests the ADSP-21061's external bus with the host bus request ($\overline{\text{HBR}}$), host bus grant ($\overline{\text{HBG}}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-21061, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

DMA Controller

The ADSP-21061's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

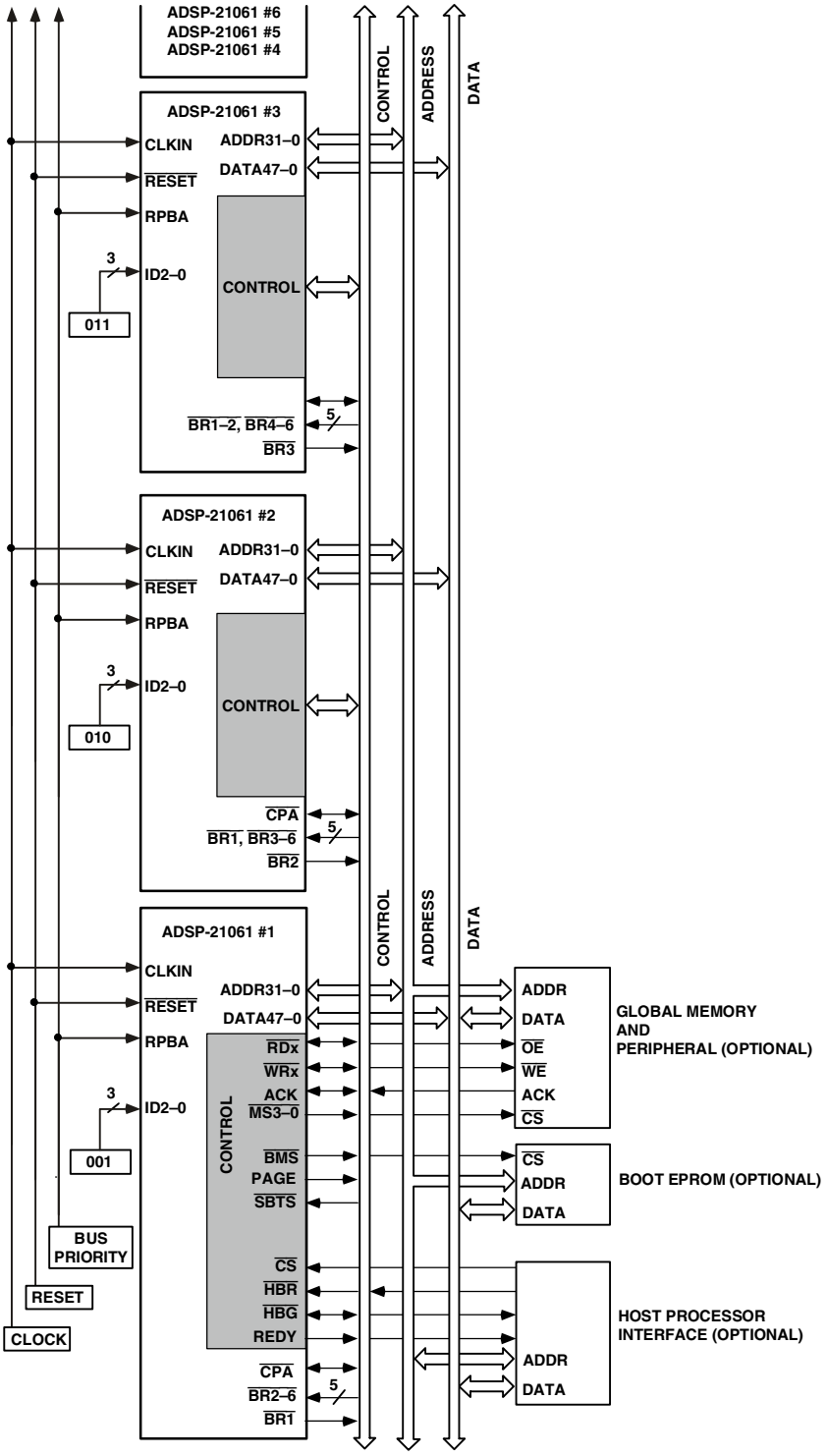

Figure 3. Shared Memory Multiprocessing System

DMA transfers can occur between the ADSP-21061's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-21061's internal memory and its serial ports.

DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

Six channels of DMA are available on the ADSP-21061—four via the serial ports, and two via the processor's external port (for either host processor, other ADSP-21061s, memory or I/O transfers). Programs can be downloaded to the ADSP-21061 using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA request/grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

Serial Ports

The ADSP-21061 features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of 40 Mbps. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers TDM multichannel mode.

The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 bits to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated. The serial ports also include keyword and key mask features to enhance interprocessor communication.

Multiprocessing

The ADSP-21061 offers powerful features tailored to multiprocessor DSP systems. The unified address space (see Figure 4) allows direct interprocessor accesses of each ADSP-21061's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-21061s and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible read-modify-write sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 500 Mbps over the external port. Broadcast writes allow simultaneous transmission of data to all ADSP-21061s and can be used to implement reflective semaphores.

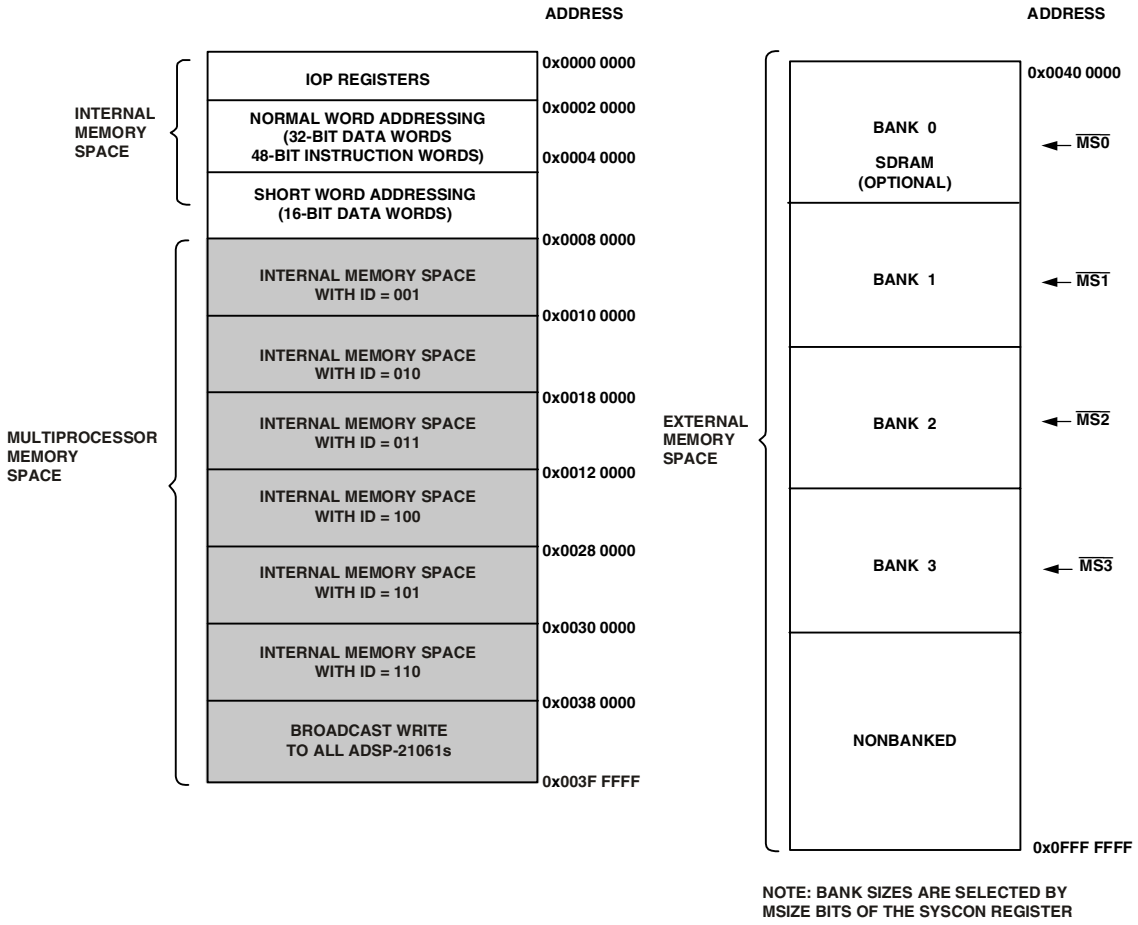

Figure 4. Memory Map

Program Booting

The internal memory of the ADSP-21061 can be booted at system power-up from either an 8-bit EPROM, or a host processor. Selection of the boot source is controlled by the $\overline{\text{BMS}}$ (boot memory select), EBOOT (EPROM boot), and LBOOT (host boot) pins. 32-bit and 16-bit host processors can be used for booting.

PORTING CODE FROM THE ADSP-21060 OR ADSP-21062

The ADSP-21061 is pin compatible with the ADSP-21060/ADSP-21061/ADSP-21062 processors. The ADSP-21061 pins that correspond to the link port pins of the ADSP-21060/ADSP-21062 are no-connects.

The ADSP-21061 is object code compatible with the ADSP-21060/ADSP-21062 processors except for the folowing functional elements:

- The ADSP-21061 memory is organized into two blocks with eight columns that are 4k deep per block. The ADSP-21060/ADSP-21062 memory has 16 columns per block.
- Link port functions are not available.
- Handshake external port DMA pins DMAR2 and DMAG2 are assigned to external port DMA Channel 6 instead of Channel 8.
- 2-D DMA capability of the SPORT is not available.
- The modify registers in SPORT DMA are not programmable.

On the ADSP-21061, Block 0 starts at the beginning of internal memory, normal word address 0x0002 0000. Block 1 starts at the end of Block 0, with contiguous addresses. The remaining addresses in internal memory are divided into blocks that alias into Block 1. This allows any code or data stored in Block 1 on the ADSP-21062 to retain the same addresses on the ADSP- 21061—these addresses will alias into the actual Block 1 of each processor.

If you develop your application using the ADSP-21062, but will migrate to the ADSP-21061, use only the first eight columns of each memory bank. Limit your application to 8k of instructions or up to 16k of data in each bank of the ADSP-21062, or any combination of instructions or data that does not exceed the memory bank.

DEVELOPMENT TOOLS

The ADSP-21061 is supported by a complete set of CROSSCORE®† software development tools, including Analog Devices emulators and VisualDSP++®‡ development environment. The same emulator hardware that supports other SHARC processors also fully emulates the ADSP-21061.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ runtime library that includes DSP and mathematical functions. A key point for these tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The ADSP-21061 SHARC DSP has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the ADSP-21061 development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tools' command line switches

The VisualDSP++ kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively,

† CROSSCORE is a registered trademark of Analog Devices, Inc.
‡ VisualDSP++ is a registered trademark of Analog Devices, Inc.

eliminating the need to start from the very beginning when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

Use the expert linker to visually manipulate the placement of code and data on the embedded system. View memory utilization in a color-coded graphical form, easily move code and data to different areas of the DSP or external memory with a drag of the mouse, and examine run-time stack and heap usage. The expert linker is fully compatible with existing linker definition file (LDF), allowing the developer to move between the graphical and textual environments.

In addition to the software development tools available from Analog Devices, third parties provide a wide range of tools supporting the SHARC processor family. Third-party software tools include DSP libraries, real-time operating systems, and block diagram design tools.

EVALUATION KIT

Analog Devices offers a range of EZ-KIT Lite®† evaluation platforms to use as a cost-effective method to learn more about developing or prototyping applications with Analog Devices processors, platforms, and software tools. Each EZ-KIT Lite includes an evaluation board along with an evaluation suite of the VisualDSP++ development and debugging environment with the C/C++ compiler, assembler, and linker. Also included are sample application programs, power supply, and a USB cable. All evaluation versions of the software tools are limited for use only with the EZ-KIT Lite product.

The USB controller on the EZ-KIT Lite board connects the board to the USB port of the user's PC, enabling the VisualDSP++ evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also allows in-circuit programming of the on-board flash device to store user-specific boot code, enabling the board to run as a standalone unit, without being connected to the PC.

With a full version of VisualDSP++ installed (sold separately), engineers can develop software for the EZ-KIT Lite or any custom-defined system. Connecting an Analog Devices JTAG emulator to the EZ-KIT Lite board enables high speed, nonintrusive emulation.

DESIGNING AN EMULATOR-COMPATIBLE DSP BOARD (TARGET)

The Analog Devices family of emulators are tools that every DSP developer needs to test and debug hardware and software systems. Analog Devices has supplied an IEEE 1149.1 JTAG test access port (TAP) on each JTAG DSP. Nonintrusive in-circuit emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing. The emulator uses the TAP to access the internal features of the DSP, allowing the developer to load code, set breakpoints, observe variables, observe memory, and examine registers. The DSP must be halted to send data and commands, but once an operation has been completed by the emulator, the DSP system is set running at full speed with no impact on system timing.

To use these emulators, the target board must include a header that connects the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, multiprocessor scan chains, signal buffering, signal termination, and emulator pod logic, see the *EE-68: Analog Devices JTAG Emulation Technical Reference* on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21061 architecture and functionality. For detailed information on the ADSP-21000 Family core architecture and instruction set, refer to the *ADSP-21061 SHARC User's Manual*, Revision 2.1.

† EZ-KIT Lite is a registered trademark of Analog Devices, Inc.

PIN FUNCTION DESCRIPTIONS

ADSP-21061 pin definitions are listed below. All pins are identical on the ADSP-21061 and ADSP-21061L. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for ADDR31-0, DATA47-0, FLAG3-0, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTx, DRx, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

Table 2. Pin Descriptions

Pin	Type	Function
$ADDR_{31-0}$	I/O/T	**External Bus Address.** The ADSP-21061 outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/write of the internal memory or IOP registers of other ADSP-21061s. The ADSP-21061 inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	**External Bus Data.** The ADSP-21061 inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over Bits 47 to 16 of the bus. 40-bit extended-precision floating-point data is transferred over Bits 47 to 8 of the bus. 16-bit short word data is transferred over Bits 31 to 16 of the bus. In PROM boot mode, 8-bit data is transferred over Bits 23 to 16. Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS}_{3-0}$	O/T	**Memory Select Lines.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-21061's system control register (SYSCON). The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS}_0$ can be used with the PAGE signal to implement a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{MS}_{3-0}$ lines are output by the bus master.
$\overline{RD}$	I/O/T	**Memory Read Strobe.** This pin is asserted (low) when the ADSP-21061 reads from external memory devices or from the internal memory of other ADSP-21061s. External devices (including other ADSP-21061s) must assert $\overline{RD}$ to read from the ADSP-21061's internal memory. In a multiprocessing system $\overline{RD}$ is output by the bus master and is input by all other ADSP-21061s.
$\overline{WR}$	I/O/T	**Memory Write Strobe.** This pin is asserted (low) when the ADSP-21061 writes to external memory devices or to the internal memory of other ADSP-21061s. External devices must assert $\overline{WR}$ to write to the ADSP-21061's internal memory. In a multiprocessing system $\overline{WR}$ is output by the bus master and is input by all other ADSP-21061s.
PAGE	O/T	**DRAM Page Boundary.** The ADSP-21061 asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-21061's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system PAGE is output by the bus master.
ADRCLK	O/T	**Clock Output Reference.** In a multiprocessing system ADRCLK is output by the bus master.
$\overline{SW}$	I/O/T	**Synchronous Write Select.** This signal is used to interface the ADSP-21061 to synchronous memory devices (including other ADSP-21061s). The ADSP-21061 asserts $\overline{SW}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{WR}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{SW}$ is output by the bus master and is input by all other ADSP-21061s to determine if the multiprocessor memory access is a read or write. $\overline{SW}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-21061(s).

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{SBTS}$ is asserted, or when the ADSP-21061 is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
ACK	I/O/S	**Memory Acknowledge.** External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21061 deasserts ACK as an output to add wait states to a synchronous access of its internal memory. In a multiprocessing system, a slave ADSP-21061 deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ (low) to place the external bus address, data, selects, and strobes in a high impedance state for the following cycle. If the ADSP-21061 attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor halts and the memory access is not complete until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21061 deadlock, or used with a DRAM controller.
$\overline{\text{IRQ}}_{2-0}$	I/A	**Interrupt Request Lines.** May be either edge-triggered or level-sensitive.
FLAG_{3-0}	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, they can be tested as a condition. As an output, they can be used to signal external peripherals.
TIMEXP	O	**Timer Expired.** Asserted for four cycles when the timer is enabled and TCOUNT decrements to zero.
$\overline{\text{HBR}}$	I/A	**Host Bus Request.** This pin must be asserted by a host processor to request control of the ADSP-21061's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-21061 that is bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-21061 places the address, data, select, and strobe lines in a high impedance state. $\overline{\text{HBR}}$ has priority over all ADSP-21061 bus requests $\overline{\text{BR}}_{6-1}$ in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant.** Acknowledges a bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted (held low) by the ADSP-21061 until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-21061 bus master and is monitored by all others.
$\overline{\text{CS}}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21061.
REDY	O (O/D)	**Host Bus Acknowledge.** The ADSP-21061 deasserts REDY (low) to add wait states to an asynchronous access of its internal memory or IOP registers by a host. This pin is an open-drain output (O/D) by default; it can be programmed in the ADREDY bit of the SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR}}_{2-1}$	I/A	**DMA Request 1** (DMA Channel 7) and **DMA Request 2** (DMA Channel 6).
$\overline{\text{DMAG}}_{2-1}$	O/T	**DMA Grant 1** (DMA Channel 7) and **DMA Grant 2** (DMA Channel 6).
$\overline{\text{BR}}_{6-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21061 processors to arbitrate for bus mastership. An ADSP-21061 only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID2-0 inputs) and monitors all others. In a multiprocessor system with less than six ADSP-21061s, the unused $\overline{\text{BR}}$x pins should be pulled high; the processor's own $\overline{\text{BR}}$x line must not be pulled high or low because it is an output.
$\overline{\text{ID2–0}}$	O (O/D)	**Multiprocessing ID.** Determines which multiprocessing bus request ($\overline{\text{BR1}}$– $\overline{\text{BR6}}$) is used by ADSP-21061. ID = 001 corresponds to $\overline{\text{BR1}}$, ID = 010 corresponds to $\overline{\text{BR2}}$, etc., ID = 000 in single-processor systems. These lines are a system configuration selection which should be hardwired or changed at reset only.
RPBA	I/S	**Rotating Priority Bus Arbitration Select.** When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-21061. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-21061.
$\overline{\text{CPA}}$	I/O (O/D)	**Core Priority Access.** Asserting its $\overline{\text{CPA}}$ pin allows the core processor of an ADSP-21061 bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open-drain output that is connected to all ADSP-21061s in the system. The $\overline{\text{CPA}}$ pin has an internal 5 kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{\text{CPA}}$ pin should be left unconnected.
DTx	O	**Data Transmit (Serial Ports 0, 1).** Each DT pin has a 50 kΩ internal pull-up resistor.
DRx	I	**Data Receive (Serial Ports 0, 1).** Each DR pin has a 50 kΩ internal pull-up resistor.
TCLKx	I/O	**Transmit Clock (Serial Ports 0, 1).** Each TCLK pin has a 50 kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock (Serial Ports 0, 1).** Each RCLK pin has a 50 kΩ internal pull-up resistor.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

Table 2. Pin Descriptions (Continued)

Pin	Type	Function
TFSx	I/O	**Transmit Frame Sync (Serial Ports 0, 1).**
RFSx	I/O	**Receive Frame Sync (Serial Ports 0, 1).**
EBOOT	I	**EPROM Boot Select.** When EBOOT is high, the ADSP-21061 is configured for booting from an 8-bit EPROM. When EBOOT is low, the LBOOT and $\overline{\text{BMS}}$ inputs determine booting mode. See the table in the $\overline{\text{BMS}}$ pin description below. This signal is a system configuration selection that should be hardwired.
LBOOT	I	**Link Boot.** Must be tied to GND.
$\overline{\text{BMS}}$	I/O/T*	**Boot Memory Select.** *Output*: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). In a multiprocessor system, $\overline{\text{BMS}}$ is output by the bus master. *Input:* When low, indicates that no booting will occur and that ADSP-21061 will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). *EBOOT* *LBOOT* *$\overline{\text{BMS}}$* *Booting Mode* 1 0 Output EPROM (Connect $\overline{\text{BMS}}$ to EPROM chip select.) 0 0 1(Input) Host Processor. 0 0 0 (Input) No Booting. Processor executes from external memory.
CLKIN	I	**Clock In.** External clock input to the ADSP-21061. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the minimum specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21061 to a known state and begins program execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20 kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21061. $\overline{\text{TRST}}$ has a 20 kΩ internal pull-up resistor.
$\overline{\text{EMU}}$	O	**Emulation Status.** Must be connected to the ADSP-21061 EZ-ICE target board connector only. $\overline{\text{EMU}}$ has a 50 kΩ internal pull-up resistor.
ICSA	O	**Reserved.** Leave unconnected.
VDD	P	**Power Supply.** Nominally 5.0 V dc for 5 V devices or 3.3 V dc for 3.3 V devices. (30 pins)
GND	G	**Power Supply Return.** (30 pins)
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected.

A = Asynchronous, G = Ground, I = Input, O = Output, P = Power Supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open-Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-21061 is a bus slave)

TARGET BOARD CONNECTOR FOR EZ-ICE PROBE

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, TDI, TDO, and GND signals be made accessible on the target system via a 14-pin connector (a 2-row, 7-pin strip header) such as that shown in Figure 5. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. The total trace length between the EZ-ICE connector and the farthest device sharing the EZ-ICE JTAG pin should be limited to 15 inches maximum for guaranteed operation. This length restriction must include EZ-ICE JTAG signals that are routed to one or more ADSP-2106x devices, or a combination of ADSP-2106x devices and other JTAG devices on the chain.

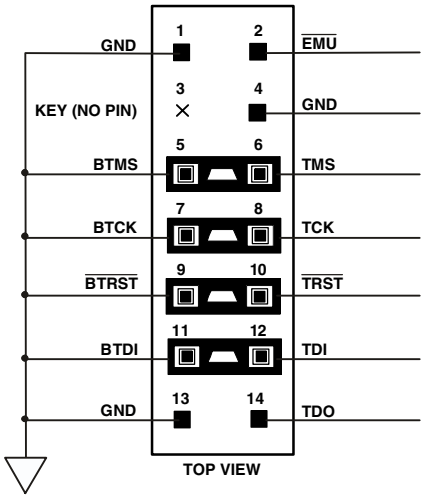

Figure 5. Target Board Connector For ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—Pin 3 must be removed from the header. The pins must be 0.025 inch square and at least 0.20 inches in length. Pin spacing should be 0.1 × 0.1 inches. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec. The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing.

When the connector is not being used for emulation, place jumpers between the Bxxx pins and the xxx pins as shown in Figure 5. If you are not going to use the test access port for board testing, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power-up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x. None of the Bxxx pins (Pins 5, 7, 9, and 11) are connected on the EZ-ICE probe.

The JTAG signals are terminated on the EZ-ICE probe as shown in Table 3.

Table 3. Core Instruction Rate/CLKIN Ratio Selection

Signal	Termination
TMS	Driven Through 22 Ω Resistor (16 mA Driver)
TCK	Driven at 10 MHz Through 22 Ω Resistor (16 mA Driver)
$\overline{\text{TRST}}$[1]	Active Low Driven Through 22 Ω Resistor (16 mA Driver) (Pulled Up by On-Chip 20 kΩ Resistor)
TDI	Driven by 22 Ω Resistor (16 mA Driver)
TDO	One TTL Load, Split Termination (160/220)
CLKIN	One TTL Load, Split Termination (160/220)
$\overline{\text{EMU}}$	Active Low, 4.7 kΩ Pull-Up Resistor, One TTL Load (Open-Drain Output from the DSP)

[1] $\overline{\text{TRST}}$ is driven low until the EZ-ICE probe is turned on by the emulator at software startup. After software startup, is driven high.

Figure 6 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

Connecting CLKIN to Pin 4 of the EZ-ICE header is optional. The emulator only uses CLKIN when directed to perform operations such as starting, stopping, and single-stepping multiple ADSP-2106xs in a synchronous manner. If you do not need these operations to occur synchronously on the multiple processors, simply tie Pin 4 of the EZ-ICE header to ground.

If synchronous multiprocessor operations are needed and CLKIN is connected, clock skew between the multiple ADSP-21061 processors and the CLKIN pin on the EZ-ICE header must be minimal. If the skew is too large, synchronous operations may be off by one or more cycles between processors. For synchronous multiprocessor operation TCK, TMS, CLKIN, and $\overline{\text{EMU}}$ should be treated as critical signals in terms of skew, and should be laid out as short as possible on your board. If TCK, TMS, and CLKIN are driving a large number of ADSP-21061s (more than eight) in your system, then treat them as a "clock tree" using multiple drivers to minimize skew. (See Figure 7 below and "JTAG Clock Tree" and "Clock Distribution" in the "High Frequency Design Considerations" section of the *ADSP-21061 SHARC User's Manual*, Revision 2.1.)

If synchronous multiprocessor operations are not needed (i.e., CLKIN is not connected), just use appropriate parallel termination on TCK and TMS. TDI, TDO, $\overline{\text{EMU}}$, and $\overline{\text{TRST}}$ are not critical signals in terms of skew.

For complete information on the SHARC EZ-ICE, see the *ADSP-21000 Family JTAG EZ-ICE User's Guide and Reference*.

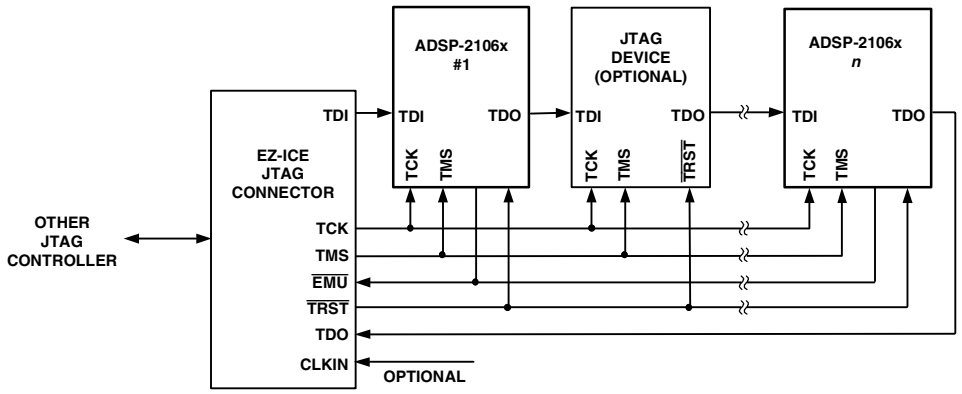

Figure 6. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

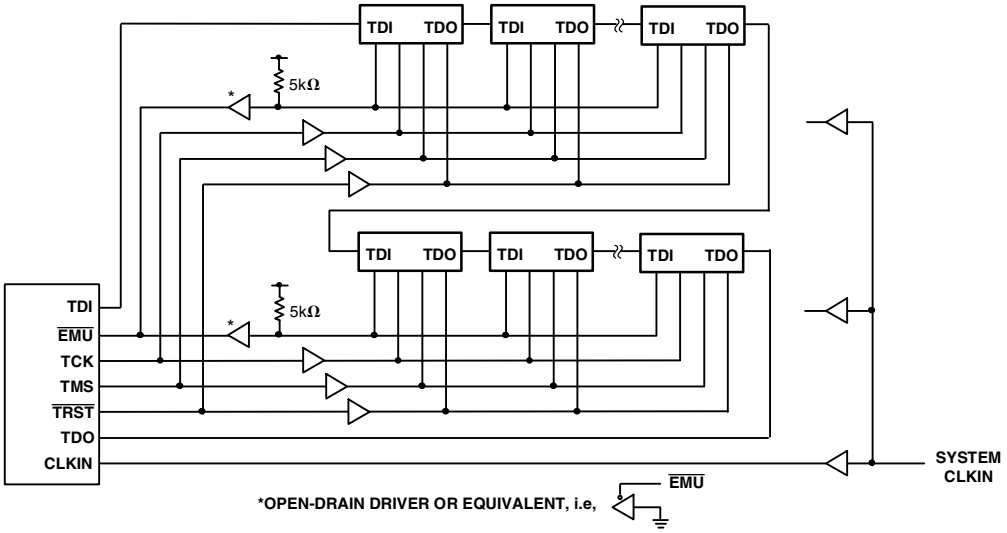

Figure 7. JTAG Clocktree for Multiple ADSP-2106x Systems

ADSP-21061 SPECIFICATIONS

OPERATING CONDITIONS (5 V)

Parameter	Description	K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	V
T_{CASE}	Case Operating Temperature	0	85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1.

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$.

ELECTRICAL CHARACTERISTICS (5 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1, 2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	4.1		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups:DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (5 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios:

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:
%PEAK $I_{DDINPEAK}$ + %HIGH $I_{DDINHIGH}$ + %LOW $I_{DDINLOW}$ + %IDLE I_{DDIDLE} = power consumption

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 30 ns, V_{DD} = Max	595	mA
	t_{CK} = 25 ns, V_{DD} = Max	680	mA
	t_{CK} = 20 ns, V_{DD} = Max	850	
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 30 ns, V_{DD} = Max	460	mA
	t_{CK} = 25 ns, V_{DD} = Max	540	mA
	t_{CK} = 20 ns, V_{DD} = Max	670	
$I_{DDINLOW}$ Supply Current (Internal)[3]	t_{CK} = 30 ns, V_{DD} = Max	270	mA
	t_{CK} = 25 ns, V_{DD} = Max	320	mA
	t_{CK} = 20 ns, V_{DD} = Max	390	
I_{DDIDLE} Supply Current (Idle)[4]	V_{DD} = Max	200	mA
I_{DDIDLE} Supply Current (Idle16)[5]	V_{DD} = Max	55	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.
[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.
[3] $I_{DDINLOW}$ is a composite average based on a range of low activity code.
[4] Idle denotes ADSP-21061L state during execution of IDLE instruction.
[5] Idle16 denotes ADSP-2106x state during execution of IDLE16 instruction.

EXTERNAL POWER DISSIPATION (5 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:
$P_{INT} = I_{DDIN} \times V_{DD}$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

—the number of output pins that switch during each cycle (O)

—the maximum frequency at which they can switch (f)

—their load capacitance (C)

—their voltage swing (V_{DD})

and is calculated by:

$$PEXT = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128k × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table 4. External Power Calculations

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 25 V	= 0.084 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 25 V	= 0.000 W
$\overline{WR}$	1	—	× 44.7 pF	× 20 MHz	× 25 V	= 0.022 W
Data	32	50	× 14.7 pF	× 10 MHz	× 25 V	= 0.059 W
ADDRCLK	1	—	× 4.7 pF	× 20 MHz	× 25 V	= 0.002 W

P_{EXT} = 0.167 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:
$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ADSP-21061L SPECIFICATIONS

OPERATING CONDITIONS (3.3 V)

Parameter	Description	A Grade		K Grade		Unit
		Min	Max	Min	Max	
V_{DD}	Supply Voltage	3.15	3.45	3.15	3.45	V
T_{CASE}	Case Operating Temperature	–40	+85	0	+85	°C
$V_{IH}1$[1]	High Level Input Voltage @ V_{DD} = Max	2.0	V_{DD} + 0.5	2.0	V_{DD} + 0.5	V
$V_{IH}2$[2]	High Level Input Voltage @ V_{DD} = Max	2.2	V_{DD} + 0.5	2.2	V_{DD} + 0.5	V
V_{IL}[1, 2]	Low Level Input Voltage @ V_{DD} = Min	–0.5	+0.8	–0.5	+0.8	V

[1] Applies to input and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}2–0$, FLAG3–0, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6–1}$, $ID_{2–0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, EBOOT, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1

[2] Applies to input pins: CLKIN, $\overline{RESET}$, $\overline{TRST}$

ELECTRICAL CHARACTERISTICS (3.3 V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{OH}[1,2]	High Level Output Voltage	@ V_{DD} = Min, I_{OH} = –2.0 mA	2.4		V
V_{OL}[1, 2]	Low Level Output Voltage	@ V_{DD} = Min, I_{OL} = 4.0 mA		0.4	V
I_{IH}[3, 4]	High Level Input Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{IL}[3]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{ILP}[4]	Low Level Input Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
I_{OZH}[5, 6, 7, 8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		10	µA
I_{OZL}[5]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		10	µA
I_{OZHP}	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = V_{DD} Max		350	µA
I_{OZLC}[7]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		1.5	mA
I_{OZLA}[9]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 1.5 V		350	µA
I_{OZLAR}[8]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		4.2	mA
I_{OZLS}[6]	Three-State Leakage Current	@ V_{DD} = Max, V_{IN} = 0 V		150	µA
C_{IN}[10, 11]	Input Capacitance	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		4.7	pF

[1] Applies to output and bidirectional pins: $DATA_{47–0}$, $ADDR_{31–0}$, 3-0, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, FLAG3-0, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6–1}$, CPA, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA.

[2] See "Output Drive Currents" for typical drive current capabilities.

[3] Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2–0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $ID_{2–0}$, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK.

[4] Applies to input pins with internal pull-ups: DR0, DR1, $\overline{TRST}$, TMS, TDI, $\overline{EMU}$.

[5] Applies to three-statable pins: $DATA_{47–0}$, $ADDR_{31–0}$, $\overline{MS}_{3–0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3–0}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, $\overline{BR}_{6–1}$, TFSx, RFSx, TDO, $\overline{EMU}$. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061 is not requesting bus mastership.)

[6] Applies to three-statable pins with internal pull-ups: DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[7] Applies to $\overline{CPA}$ pin.

[8] Applies to ACK pin when pulled up. (Note that ACK is pulled up internally with 2 kΩ during reset in a multiprocessor system, when $ID_{2–0}$ = 001 and another ADSP-21061L is not requesting bus mastership).

[9] Applies to ACK pin when keeper latch enabled.

[10] Applies to all signal pins.

[11] Guaranteed but not tested.

INTERNAL POWER DISSIPATION (3.3 V)

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note "SHARC Power Dissipation Measurements."

Specifications are based on the operating scenarios:

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK\ I_{DDINPEAK} + \%HIGH\ I_{DDINHIGH} + \%LOW\ I_{DDINLOW} + \%IDLE\ I_{DDIDLE} = power\ consumption$$

Parameter	Test Conditions	Max	Unit
$I_{DDINPEAK}$ Supply Current (Internal)[1]	t_{CK} = 25 ns, V_{DD} = Max	480	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	535	mA
$I_{DDINHIGH}$ Supply Current (Internal)[2]	t_{CK} = 25 ns, V_{DD} = Max	380	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	425	mA
$I_{DDINLOW}$ Supply Current (Internal)[3]	t_{CK} = 25 ns, V_{DD} = Max	220	mA
	t_{CK} = 22.5 ns, V_{DD} = Max	245	mA
I_{DDIDLE} Supply Current (Idle)[4]	V_{DD} = Max	180	mA
I_{DDIDLE} Supply Current (Idle)[5]	V_{DD} = Max	50	mA

[1] The test program used to measure $I_{DDINPEAK}$ represents worst-case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.
[2] $I_{DDINHIGH}$ is a composite average based on a range of high activity code. $I_{DDINLOW}$ is a composite average based on a range of low activity code.
[3] $I_{DDINLOW}$ is a composite average based on a range of low activity code.
[4] Idle denotes ADSP-21061L state during execution of IDLE instruction.
[5] Idle16 denotes ADSP-21061L state during execution of IDLE16 instruction.

EXTERNAL POWER DISSIPATION (3.3 V)

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:
$P_{INT} = I_{DDIN} \times V_{DD}$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- —the number of output pins that switch during each cycle (O)
- —the maximum frequency at which they can switch (f)
- —their load capacitance (C)
- —their voltage swing (V_{DD})

and is calculated by:

$$PEXT = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (CIN). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example: Estimate P_{EXT} with the following assumptions:

- A system with one bank of external data memory RAM (32-bit)
- Four 128k × 8 RAM chips are used, each with a load of 10 pF
- External data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching
- The instruction cycle rate is 40 MHz (t_{CK} = 25 ns)

The P_{EXT} equation is calculated for each class of pins that can drive:

Table 5. External Power Calculations

Pin Type	No. of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.037 W
$\overline{MS0}$	1	0	× 44.7 pF	× 10 MHz	× 10.9 V	= 0.000 W
$\overline{WR}$	1	—	× 44.7 pF	× 20 MHz	× 10.9 V	= 0.010 W
Data	32	50	× 14.7 pF	× 10 MHz	× 10.9 V	= 0.026 W
ADDRCLK	1	—	× 4.7 pF	× 20 MHz	× 10.9 V	= 0.001 W

P_{EXT} = 0.074 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:
$P_{TOTAL} = P_{EXT} + (I_{DDIN2} \times 5.0\ V)$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Note also that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed below may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	5 V	3.3 V
Supply Voltage (V_{DD})	–0.3 V to +7.0 V	–0.3 V to +4.6 V
Input Voltage	–0.5 V to V_{DD} +0.5 V	–0.5 V to V_{DD} +0.5 V
Output Voltage Swing	–0.5 V to V_{DD} +0.5 V	–0.5 V to V_{DD} +0.5 V
Load Capacitance	200 pF	200 pF
Storage Temperature Range	–65°C to +150°C	–65°C to +150°C
Lead Temperature (5 seconds)	280°C	280°C
Junction Temperature Under Bias	130°C	130°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE MARKING INFORMATION

The information presented in Figure 8 provides details about the package branding for the ADSP-21061 processor. For a complete listing of product availability, see Ordering Guide on Page 53.

Figure 8. Typical Package Marking (Actual Marking Format May Vary)

Table 6. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option
ccc	See Ordering Guide
vvvvvv.x	Assembly Lot Code
n.n	Silicon Revision
yyww	Date Code

TIMING SPECIFICATIONS

The timing specifications shown are based on a CLKIN frequency of 40 MHz (t_{CK} = 25 ns). The DT derating enables the calculation of timing specifications within the min to max range of the t_{CK} specification (see Table 7). DT is the difference between the derated CLKIN period (t_{CK}) and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25\ ns$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

For voltage reference levels, see Figure 29 under Test Conditions.

Timing Requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices. (O/D) = Open Drain, (A/D) = Active Drive.

Switching Characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Clock Input

Table 7. Clock Input

Parameter		ADSP-21061 50 MHz, 5 V Min	ADSP-21061 50 MHz, 5 V Max	ADSP-21061L 44 MHz, 3.3 V Min	ADSP-21061L 44 MHz, 3.3 V Max	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Min	ADSP-21061/ ADSP-21061L 40 MHz, 5 V and 3.3 V Max	ADSP-21061 33 MHz, 5 V Min	ADSP-21061 33 MHz, 5 V Max	Unit
Timing Requirements										
t_{CK}	CLKIN Period	20	100	22.5	100	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	7		7		7		7		ns
t_{CKH}	CLKIN Width High	5		5		5		5		ns
t_{CKRF}	CLKIN Rise/Fall (0.4 V to 2.0 V)		3		3		3		3	ns

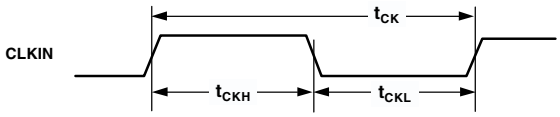

Figure 9. Clock Input

Reset

Table 8. Reset

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup Before CLKIN High[2]	14 + DT/2	t_{CK}	ns

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 µs while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including startup time of external clock oscillator).

[2] Only required if multiple ADSP-21061s must come out of reset synchronous to CLKIN with program counters (PC) equal. Not required for multiple ADSP-21061s communicating over the shared bus (through the external port), because the bus arbitration logic automatically synchronizes itself after reset.

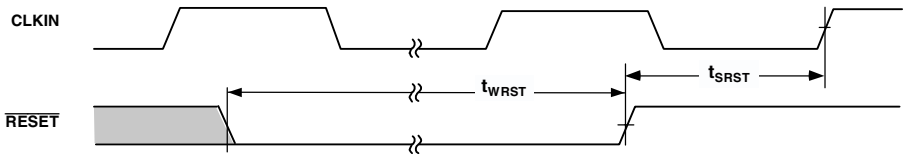

Figure 10. Reset

Interrupts

Table 9. Interrupts

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SIR}	$\overline{IRQ2–0}$ Setup Before CLKIN High[1]	18 + 3DT/4		ns
t_{HIR}	$\overline{IRQ2–0}$ Hold Before CLKIN High[1]		12 + 3DT/4	ns
t_{IPW}	$\overline{IRQ2–0}$ Pulsewidth[2]	$2+t_{CK}$		ns

[1] Only required for $\overline{IRQx}$ recognition in the following cycle.
[2] Applies only if t_{SIR} and t_{HIR} requirements are not met.

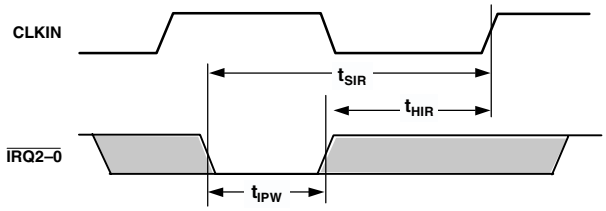

Figure 11. Interrupts

Timer

Table 10. Timer

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristic				
t_{DTEX}	CLKIN High to TIMEXP		15	ns

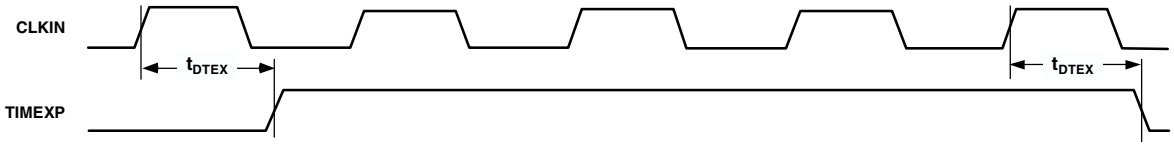

Figure 12. Timer

Flags

Table 11. Flags

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SFI}	FLAG3–0 IN Setup Before CLKIN High[1]	8 + 5DT/16		ns
t_{HFI}	FLAG3–0 IN Hold After CLKIN High[1]	0 – 5DT/16		ns
t_{DWRFI}	FLAG3–0 IN Delay After $\overline{RD}$/$\overline{WR}$ Low[1]		5 + 7DT/16	ns
t_{HFIWR}	FLAG3–0 IN Hold After $\overline{RD}$/$\overline{WR}$ Deasserted[1]	0		ns
Switching Characteristics				
t_{DFO}	FLAG3–0 OUT Delay After CLKIN High		16	ns
t_{HFO}	FLAG3–0 OUT Hold After CLKIN High	4		ns
t_{DFOE}	CLKIN High to FLAG3–0 OUT Enable	3		ns
t_{DFOD}	CLKIN High to FLAG3–0 OUT Disable		14	ns

[1] Flag inputs meeting these setup and hold times for Instruction Cycle N will affect conditional instructions in Instruction Cycle N+2.

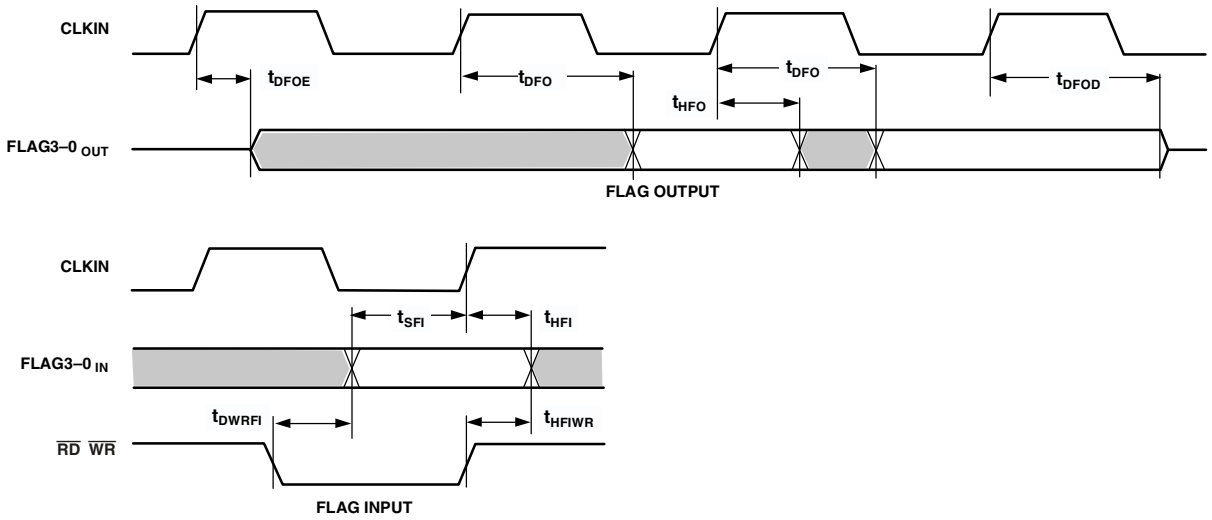

Figure 13. Flags

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 12. Memory Read—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		18 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		12 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address, Selects[3]	0.5		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	2.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 4]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[4]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DRHA}	Address, Selects Hold After $\overline{RD}$ High	0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	2 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	12.5 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 3DT/8 + HI		ns
t_{SADADC}	Address, Selects Setup Before ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

[1] Data delay/setup: user must meet t_{DAD} or t_{DRLD} or synchronous spec t_{SSDATI}.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] Data hold: user must meet t_{HDA} or t_{HDRH} or synchronous spec t_{HSDATI}. See Example System Hold Time Calculation on Page 44 for the calculation of hold times given capacitive and dc loads.
[4] ACK delay/setup: user must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} (Table 13 on Page 26) for deassertion of ACK (Low), all three specifications must be met for assertion of ACK (High).

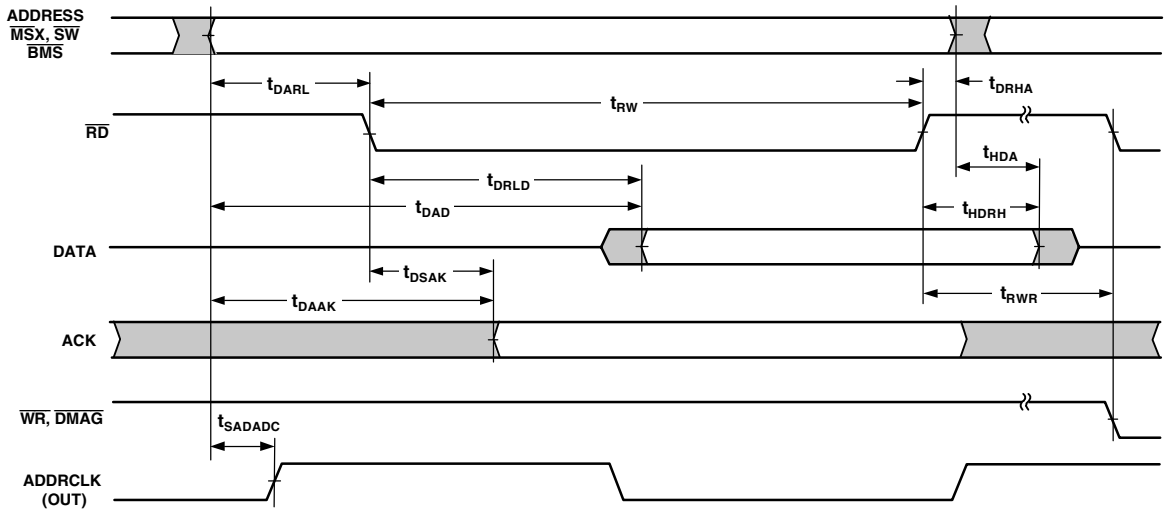

Figure 14. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21061 is the bus master accessing external memory space in asynchronous access mode. Note that timing for ACK, DATA, $\overline{RD}$, $\overline{WR}$, and $\overline{DMAGx}$ strobe timing parameters only applies to asynchronous access mode.

Table 13. Memory Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{DAAK}	ACK Delay from Address, Selects[1, 2]		15 + 7DT/8 + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		8 + DT/2 + W	ns
Switching Characteristics				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	17 + 15DT/16 + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	13 + 9DT/16 + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	7 + DT/2 + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	1 + DT/16 + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1 + DT/16 + H	6 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAGx}$ Low	8 + 7DT/16 + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	5 + 3DT/8 + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	–1 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High[2]	0 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

[1] ACK delay/setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] For more information, see Example System Hold Time Calculation on Page 44 for calculation of hold times given capacitive and dc loads.

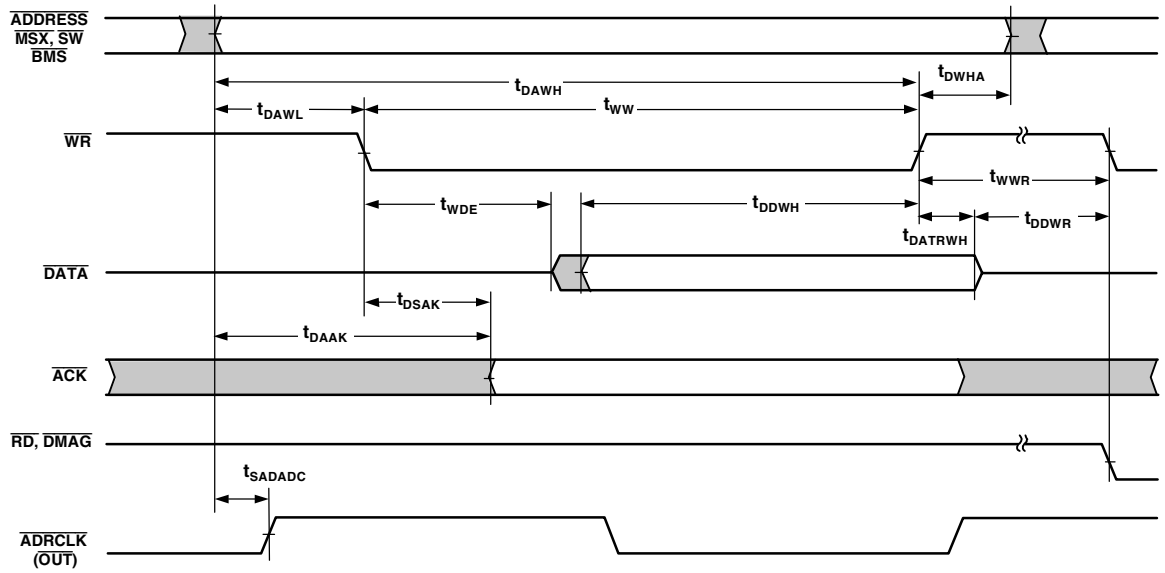

Figure 15. Memory Write—Bus Master

Synchronous Read/Write—Bus Master

Use these specifications for interfacing to external memory systems that require CLKIN—relative timing or for accessing a slave ADSP-21061 (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes except where noted (see Memory Read—Bus Master on Page 25 and Memory Write—Bus Master on Page 26). When accessing a slave ADSP-21061, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see Synchronous Read/Write—Bus Slave on Page 29). The slave ADSP-21061 must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Table 14. Synchronous Read/Write—Bus Master

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SSDATI}	Data Setup Before CLKIN (50 MHz, t_{CK} = 20 ns)[1]	2 + DT/8 1.5 + DT/8		ns
t_{HSDATI}	Data Hold After CLKIN	3.5 – DT/8		ns
t_{DAAK}	ACK Delay After Address, Selects[2, 3]		15 + 7DT/8 + W	ns
t_{SACKC}	ACK Setup Before CLKIN[3]	6.5 + DT/4		ns
t_{HACK}	ACK Hold After CLKIN	–1 – DT/4		ns
Switching Characteristics				
t_{DADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Delay After CLKIN[2]		6.5 – DT/8	ns
t_{HADRO}	Address, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$ Hold After CLKIN	–1 – DT/8		ns
t_{DPGC}	PAGE Delay After CLKIN	9 + DT/8	16 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay After CLKIN	–1.5 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay After CLKIN (50 MHz, t_{CK} = 20 ns)	–2.5 – 3DT/16 –1.5 – 3DT/16	4 – 3DT/16 4 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay After CLKIN	8 + DT/4	12 + DT/4	ns
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[4]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay After CLKIN	4 + DT/8	10 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 2)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 2)		ns

[1] This specification applies to the ADSP-21061KS-200 (5 V, 50 MHz) operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.
[2] The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$ is referenced.
[3] ACK delay/setup: User must meet t_{DAAK} or t_{DSAK} or synchronous specification t_{SAKC} for deassertion of ACK (low), all three specifications must be met for assertion of ACK (high).
[4] See Example System Hold Time Calculation on Page 44 for calculation of hold times given capacitive and dc loads.

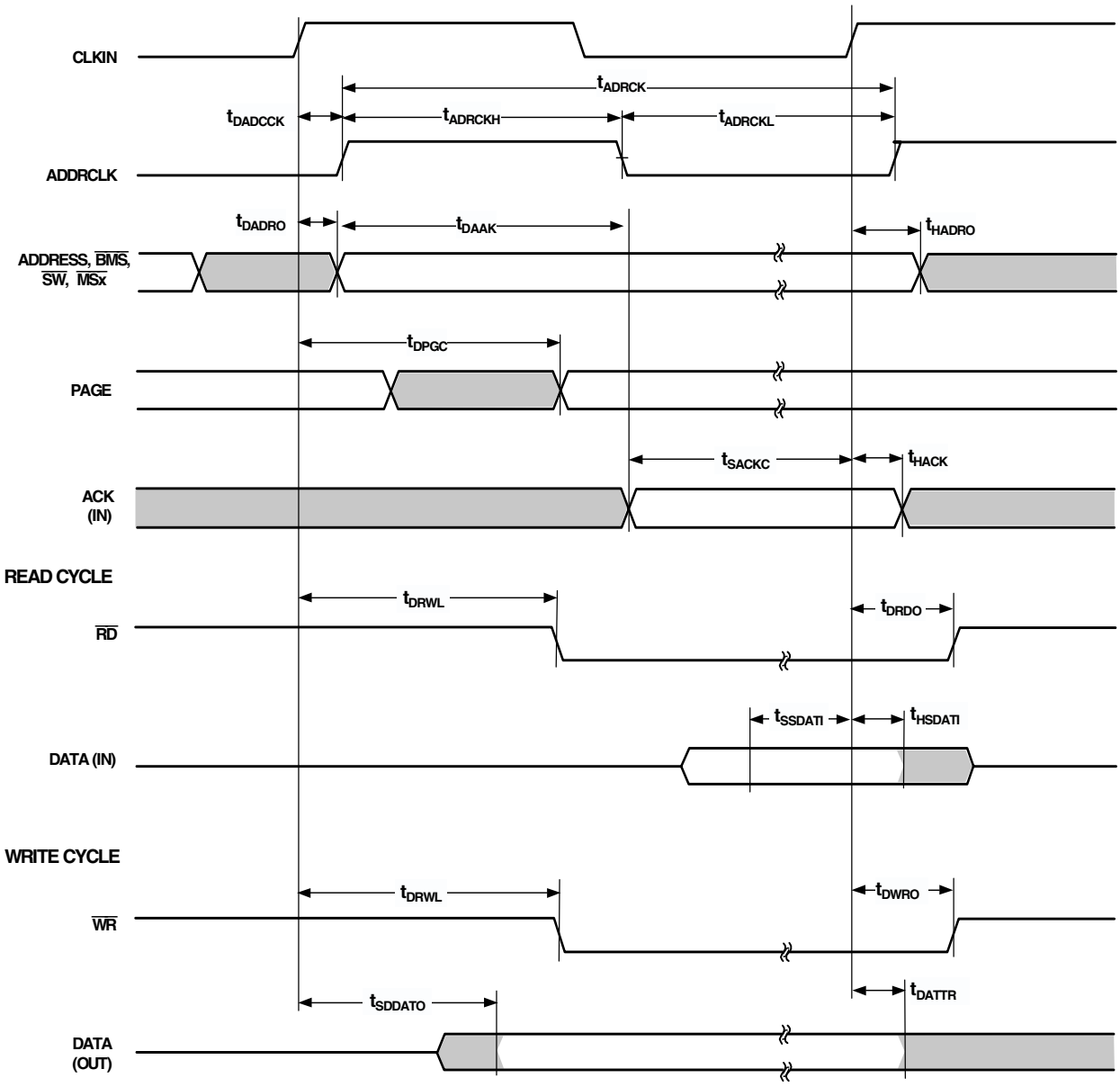

Figure 16. Synchronous Read/Write—Bus Master

Synchronous Read/Write—Bus Slave

Use these specifications for ADSP-21061 bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Table 15. Synchronous Read/Write—Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SADRI}	Address, $\overline{SW}$ Setup Before CLKIN	14 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold After CLKIN		5 + DT/2	ns
t_{SRWLI}	$\overline{RD}$/$\overline{WR}$ Low Setup Before CLKIN[1]	8.5 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}$/$\overline{WR}$ Low Hold After CLKIN	–4 – 5DT/16	8 + 7DT/16	ns
	44 MHz/50 MHz[2]	–3.5 – 5DT/16	8 + 7DT/16	
t_{RWHPI}	$\overline{RD}$/$\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	3		ns
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
t_{SDDATO}	Data Delay After CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable After CLKIN[3]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay After Address, $\overline{SW}$[4]		8	ns
t_{ACKTR}	ACK Disable After CLKIN[2]	–1 – DT/8	6 – DT/8	ns

[1] t_{SRWLI} (min) = 9.5 + 5DT/16 when multiprocessor memory space wait state (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min)= 4 + DT/8.

[2] This specification applies to the ADSP-21061LKS-176 (3.3 V, 44 MHz) and the ADSP-21061KS-200 (5 V, 50 MHz), operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.

[3] See Example System Hold Time Calculation on Page 44 for calculation of hold times given capacitive and dc loads.

[4] t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. If the address and inputs have setup times greater than 19 + 3DT/4, then ACK is valid 14 + DT/4 (max) after CLKIN. A slave that sees an address with an M field match will respond with ACK regardless of the state of MMSWS or strobes. A slave will three-state ACK every cycle with t_{ACKTR}.

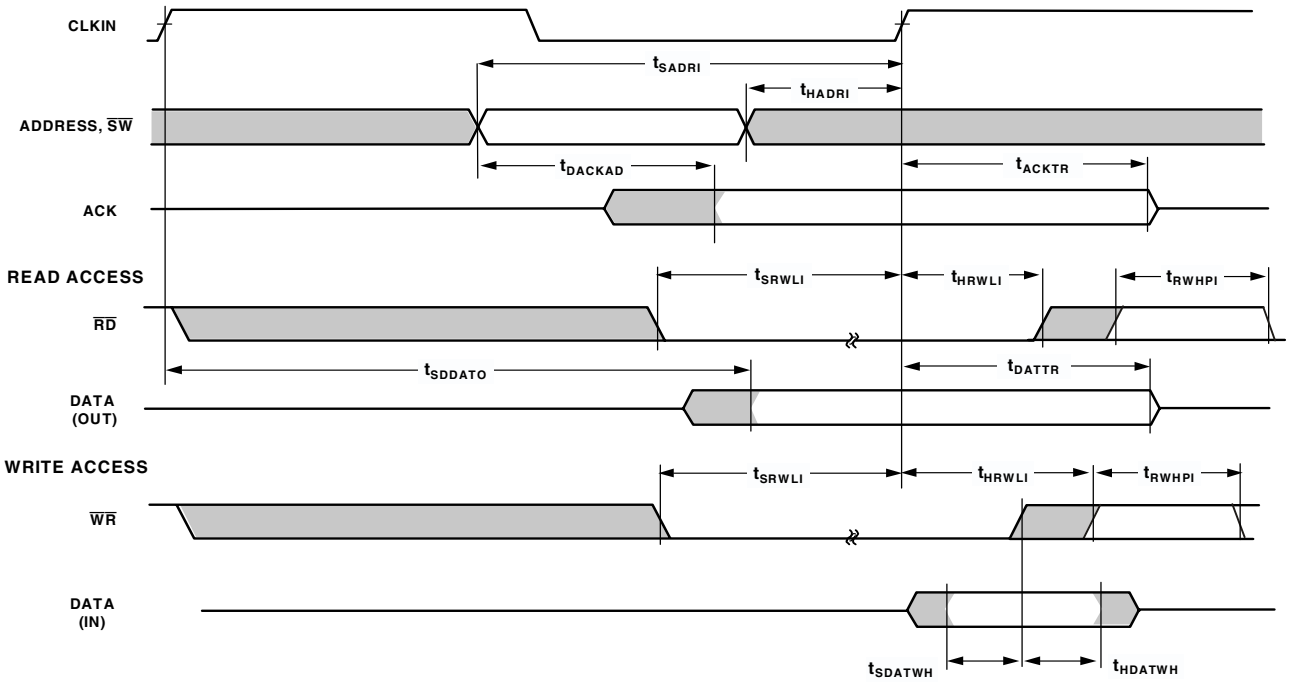

Figure 17. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request and Host Bus Request

Use these specifications for passing of bus mastership between multiprocessing ADSP-21061s ($\overline{BRx}$) or a host processor, both synchronous and asynchronous ($\overline{HBR}$, $\overline{HBG}$).

Table 16. Multiprocessor Bus Request and Host Bus Request

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid[1]		20 + 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup Before CLKIN[2]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold After CLKIN[2]		14 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup Before CLKIN	13 + DT/2		ns
t_{HHBGI}	$\overline{HBG}$ Hold After CLKIN High		6 + DT/2	ns
t_{SBRI}	$\overline{BRx}$, $\overline{CPA}$ Setup Before CLKIN[3]	13 + DT/2		ns
t_{HBRI}	$\overline{BRx}$, $\overline{CPA}$ Hold After CLKIN High		6 + DT/2	ns
t_{SRPBAI}	RPBA Setup Before CLKIN	20 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold After CLKIN		12 + 3DT/4	ns
Switching Characteristics				
t_{DHBGO}	$\overline{HBG}$ Delay After CLKIN		7 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold After CLKIN	–2 – DT/8		ns
t_{DBRO}	$\overline{BRx}$ Delay After CLKIN		5.5 – DT/8	ns
t_{HBRO}	$\overline{BRx}$ Hold After CLKIN	–2 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay After CLKIN[4]		6.5 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable After CLKIN	–2 – DT/8	4.5 – DT/8	ns
t_{DRDYCS}	REDY (O/D) or (A/D) Low from $\overline{CS}$ and $\overline{HBR}$ Low[5, 6]		8	ns
t_{TRDYHG}	REDY (O/D) Disable or REDY (A/D) High from $\overline{HBG}$[5, 7]	44 + 27DT/16		ns
t_{ARDYTR}	REDY (A/D) Disable from $\overline{CS}$ or $\overline{HBR}$ High[5]		10	ns

[1] For first asynchronous access after $\overline{HBR}$ and $\overline{CS}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-21061" section in the *ADSP-21061 SHARC User's Manual*, Revision 2.1.

[2] Only required for recognition in the current cycle.

[3] $\overline{CPA}$ assertion must meet the setup to CLKIN; deassertion does not need to meet the setup to CLKIN.

[4] For the ADSP-21061L (3.3 V), this specification is 8.5 – DT/8 ns max.

[5] (O/D) = open drain, (A/D) = active drive.

[6] For the ADSP-21061L (3.3 V), this specification is 12 ns max.

[7] For the ADSP-21061L (3.3 V), this specification is 40 + 23DT/16 ns min.

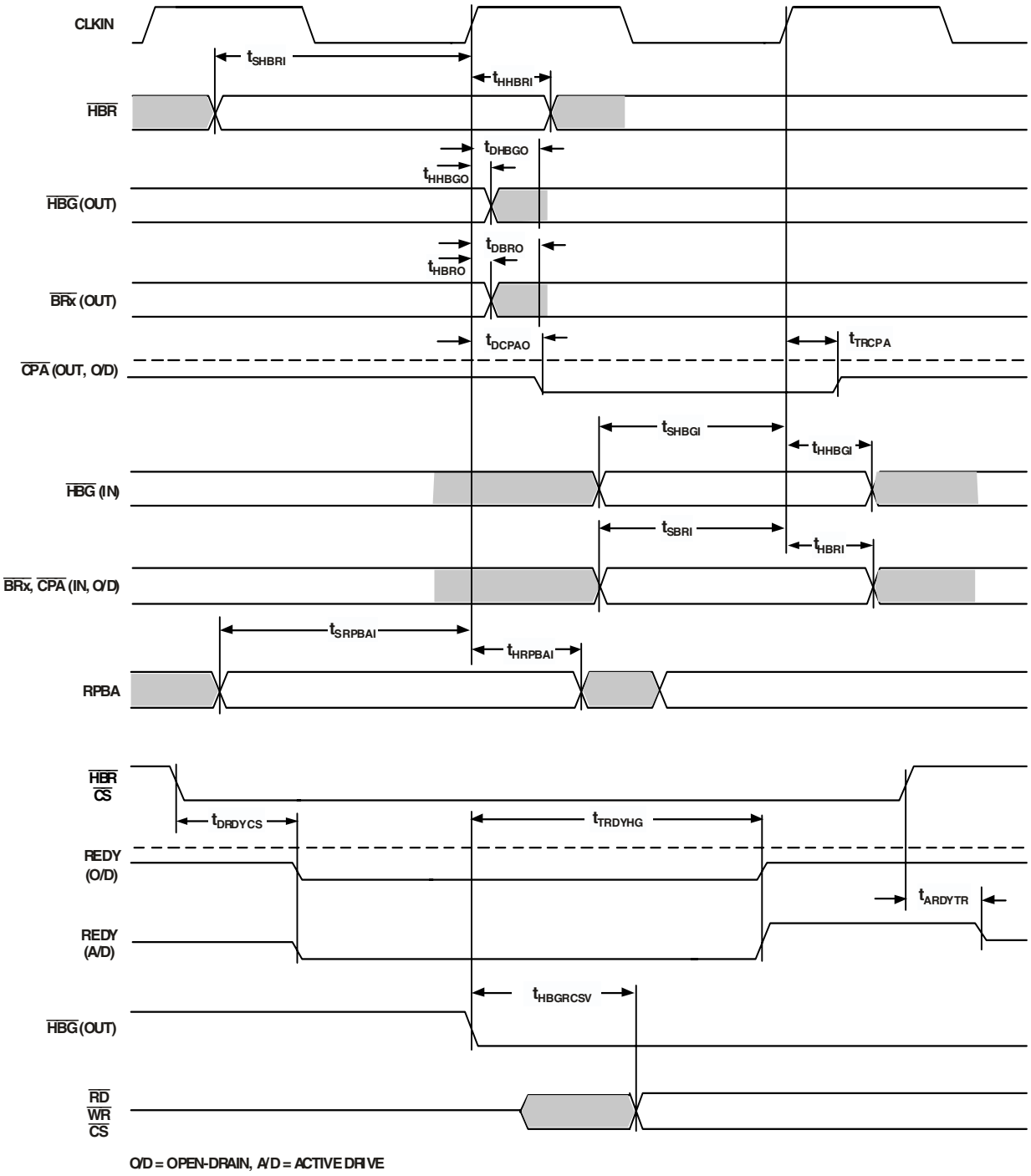

Figure 18. Multiprocessor Bus Request and Host Bus Request

Asynchronous Read/Write—Host to ADSP-21061

Use these specifications for asynchronous host processor accesses of an ADSP-21061, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-21061, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-21061's internal memory or IOP registers. $\overline{HBR}$ and $\overline{HBG}$ are assumed low for this timing.

Table 17. Read Cycle

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SADRDL}	Address Setup/$\overline{CS}$ Low Before $\overline{RD}$ Low[1]	0		ns
t_{HADRDH}	Address Hold/$\overline{CS}$ Hold Low After $\overline{RD}$	0		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (O/D) Disable	0		ns
$t_{DRDHRDY}$	$\overline{RD}$ High Delay After REDY (A/D) Disable	0		ns
Switching Characteristics				
$t_{SDATRDY}$	Data Valid Before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY (O/D) or (A/D) Low Delay After $\overline{RD}$ Low[2]		10	ns
t_{RDYPRD}	REDY (O/D) or (A/D) Low Pulsewidth for Read	45 + DT		ns
t_{HDARWH}	Data Disable After $\overline{RD}$ High	2	8	ns

[1] Not required if $\overline{RD}$ and address are valid $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. For first access after $\overline{HBR}$ asserted, ADDR31-0 must be a non-MMS value 1/2 t_{CLK} before $\overline{RD}$ or $\overline{WR}$ goes low or by $t_{HBGRCSV}$ after $\overline{HBG}$ goes low. This is easily accomplished by driving an upper address signal high when $\overline{HBG}$ is asserted. See the "Host Processor Control of the ADSP-21061" section in the ADSP-21061 *SHARC User's Manual*, Revision 2.1.
[2] For the ADSP-21061L (3.3 V), this specification is 13.5 ns max.

Table 18. Write Cycle

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SCSWRL}	$\overline{CS}$ Low Setup Before $\overline{WR}$ Low	0		ns
t_{HCSWRH}	$\overline{CS}$ Low Hold After $\overline{WR}$ High	0		ns
t_{SADWRH}	Address Setup Before $\overline{WR}$ High	5		ns
t_{HADWRH}	Address Hold After $\overline{WR}$ High	2		ns
t_{WWRL}	$\overline{WR}$ Low Width	8		ns
t_{WRWH}	$\overline{RD}$/$\overline{WR}$ High Width	6		ns
$t_{DWRHRDY}$	$\overline{WR}$ High Delay After REDY (O/D) or (A/D) Disable	0		ns
t_{SDATWH}	Data Setup Before $\overline{WR}$ High	3		ns
	50 MHz, T_{CK} = 20 ns[1]	2.5		
t_{HDATWH}	Data Hold After $\overline{WR}$ High	1		ns
Switching Characteristics				
$t_{DRDYWRL}$	REDY (O/D) or (A/D) Low Delay After $\overline{WR}$/$\overline{CS}$ Low[2]		11	ns
t_{RDYPWR}	REDY (O/D) or (A/D) Low Pulsewidth for Write	15		ns
t_{SRDYCK}	REDY (O/D) or (A/D) Disable to CLKIN	1 + 7DT/16	8 + 7DT/16	ns

[1] This specification applies to the ADSP-21061KS-200 (5 V, 50 MHz) operating at t_{CK} < 25 ns. For all other devices, use the preceding timing specification of the same name.
[2] For the ADSP-21061L (3.3 V), this specification is 13.5 ns max.

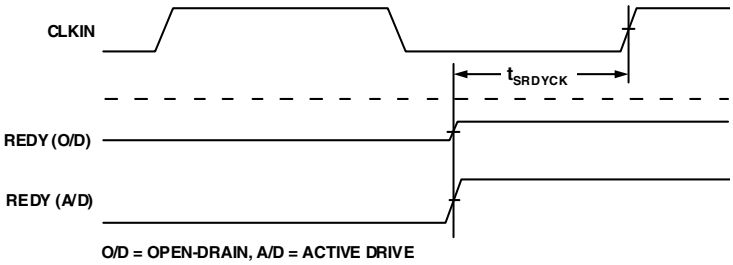

Figure 19. Synchronous REDY Timing

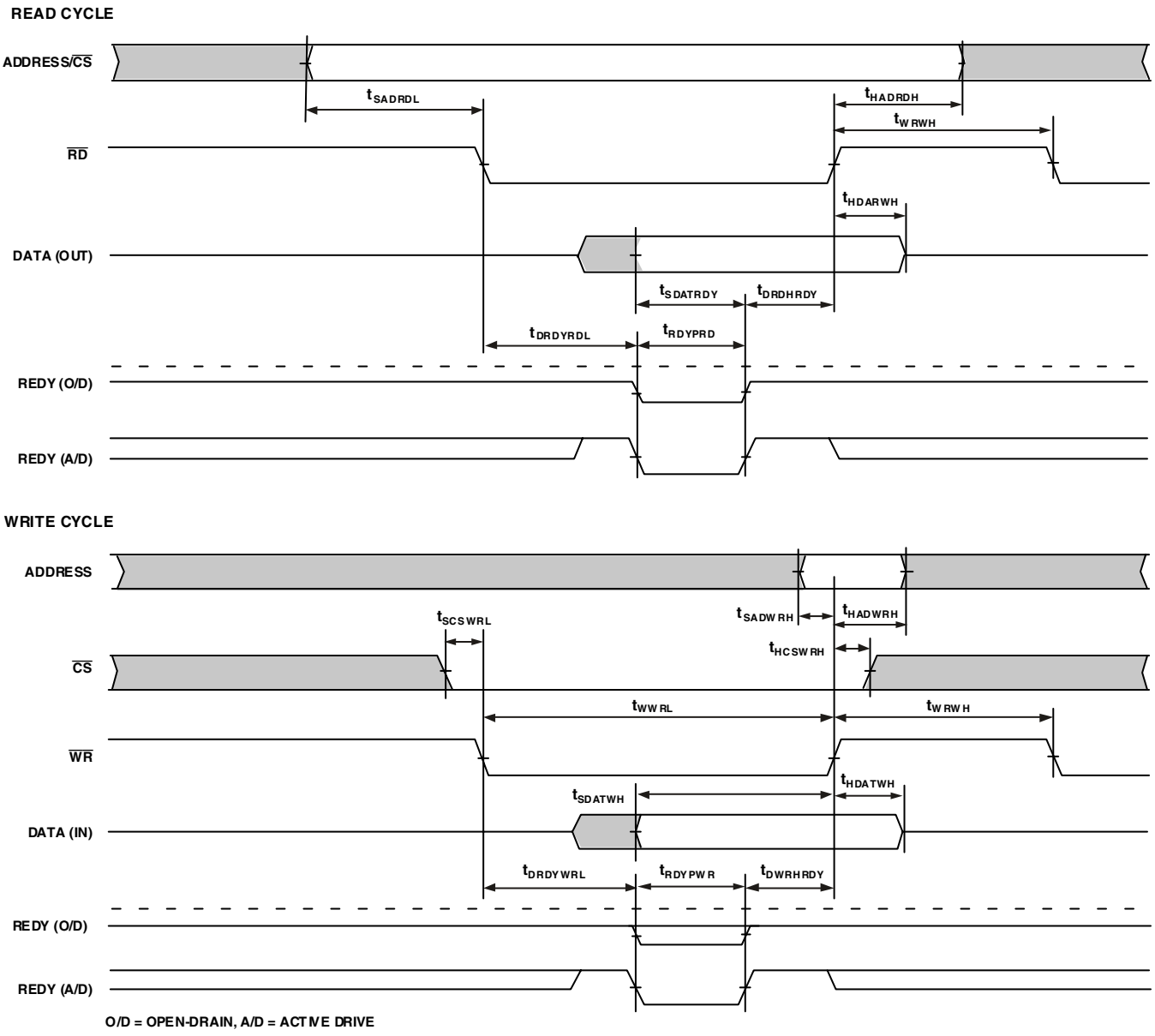

Figure 20. Asynchronous Read/Write—Host to ADSP-21061

Three-State Timing—Bus Master, Bus Slave, $\overline{HBR}$, $\overline{SBTS}$

These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{SBTS}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{SBTS}$ pin.

Table 19. Three-State Timing—Bus Master, Bus Slave

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{STSCK}	$\overline{SBTS}$ Setup Before CLKIN	12 + DT/2		ns
t_{HTSCK}	$\overline{SBTS}$ Hold Before CLKIN		6 + DT/2	ns
Switching Characteristics				
t_{MIENA}	Address/Select Enable After CLKIN	–1 – DT/8		ns
t_{MIENS}	Strobes Enable After CLKIN[1]	–1.5 – DT/8		ns
t_{MIENHG}	$\overline{HBG}$ Enable After CLKIN	–1.5 – DT/8		ns
t_{MITRA}	Address/Select Disable After CLKIN		0 – DT/4	ns
t_{MITRS}	Strobes Disable After CLKIN[1]		1.5 – DT/4	ns
t_{MITRHG}	$\overline{HBG}$ Disable After CLKIN		2.0 – DT/4	ns
t_{DATEN}	Data Enable After CLKIN[2]	9 + 5DT/16		ns
t_{DATTR}	Data Disable After CLKIN[2]	0 – DT/8	7 – DT/8	ns
t_{ACKEN}	ACK Enable After CLKIN[2]	7.5 + DT/4		ns
t_{ACKTR}	ACK Disable After CLKIN[2]	–1 – DT/8	6 – DT/8	ns
t_{ADCEN}	ADRCLK Enable After CLKIN	–2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable After CLKIN		8 – DT/4	ns
t_{MTRHBG}	Memory Interface Disable Before $\overline{HBG}$ Low[3]	0 + DT/8		ns
t_{MENHBG}	Memory Interface Enable After $\overline{HBG}$ High[3]	19 + DT		ns

[1] Strobes = $\overline{RD}$, $\overline{WR}$, PAGE, $\overline{DMAGx}$, $\overline{MSx}$, $\overline{BMS}$, $\overline{SW}$.
[2] In addition to bus master transition cycles, these specs also apply to bus master and bus slave synchronous read/write.
[3] Memory Interface = Address, $\overline{RD}$, $\overline{WR}$, $\overline{MSx}$, $\overline{SW}$, PAGE, $\overline{DMAGx}$, and $\overline{BMS}$ (in EPROM boot mode).

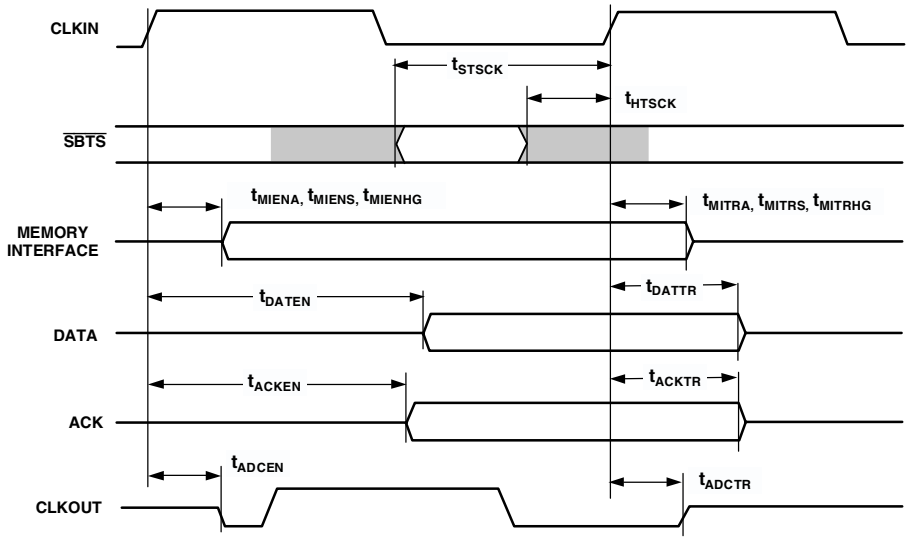

Figure 21. Three-State Timing (Bus Transition Cycle, $\overline{SBTS}$ Assertion)

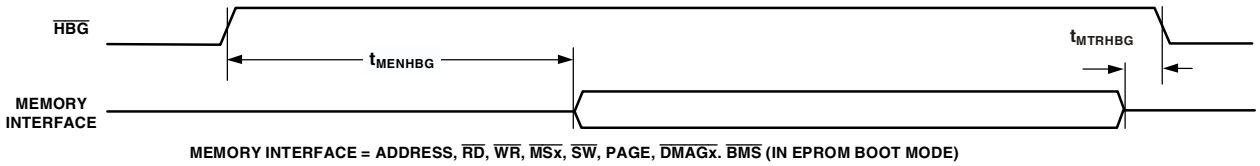

Figure 22. Three-State Timing (Bus Transition Cycle, $\overline{SBTS}$ Assertion)

DMA Handshake

These specifications describe the three DMA handshake modes. In all three modes, $\overline{\text{DMARx}}$ is used to initiate transfers. For Handshake mode, $\overline{\text{DMAGx}}$ controls the latching or enabling of data externally. For External Handshake mode, the data transfer is controlled by the ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{SW}}$, PAGE, $\overline{\text{MS3–0}}$, ACK, and $\overline{\text{DMAG}}$x signals. For Paced Master mode, the data transfer is controlled by ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, and ACK (not $\overline{\text{DMAG}}$). For Paced Master mode, the Memory Read-Bus Master, Memory Write-Bus Master, and Synchronous Read/Write-Bus Master timing specifications for ADDR31–0, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS3–0}}$, $\overline{\text{SW}}$, PAGE, DATA47–0, and ACK also apply.

Table 20. DMA Handshake

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{SDRLC}	$\overline{\text{DMARx}}$ Low Setup Before CLKIN[1]	5		ns
t_{SDRHC}	$\overline{\text{DMARx}}$ High Setup Before CLKIN[1]	5		ns
t_{WDR}	$\overline{\text{DMARx}}$ Width Low (Nonsynchronous)	6		ns
$t_{SDATDGL}$	Data Setup After $\overline{\text{DMAGx}}$ Low[2]		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold After $\overline{\text{DMAGx}}$ High	2		ns
t_{DATDRH}	Data Valid After $\overline{\text{DMARx}}$ High[2]		16 + 7DT/8	ns
t_{DMARLL}	$\overline{\text{DMARx}}$ Low Edge to Low Edge[3]	23 + 7DT/8		ns
t_{DMARH}	$\overline{\text{DMARx}}$ Width High	6		ns
Switching Characteristics				
t_{DDGL}	$\overline{\text{DMAGx}}$ Low Delay After CLKIN	9 + DT/4	15 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAGx}}$ High Width	6 + 3DT/8		ns
t_{WDGL}	$\overline{\text{DMAGx}}$ Low Width	12 + 5DT/8		ns
t_{HDGC}	$\overline{\text{DMAGx}}$ High Delay After CLKIN	–2 – DT/8	6 – DT/8	ns
$t_{VDATDGH}$	Data Valid Before $\overline{\text{DMAGx}}$ High[4]	8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable After $\overline{\text{DMAGx}}$ High[5]	0	7	ns
t_{DGWRL}	$\overline{\text{WR}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DGWRH}	$\overline{\text{DMAGx}}$ Low Before $\overline{\text{WR}}$ High	10 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High Before $\overline{\text{DMAGx}}$ High	1 + DT/16	3 + DT/16	ns
t_{DGRDL}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ Low	0	2	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low Before $\overline{\text{DMAGx}}$ High	11 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High Before $\overline{\text{DMAGx}}$ High	0	3	ns
t_{DGWR}	$\overline{\text{DMAGx}}$ High to $\overline{\text{WR}}$, $\overline{\text{RD}}$, $\overline{\text{DMAGx}}$ Low	5 + 3DT/8 + HI		ns
t_{DADGH}	Address/Select Valid to $\overline{\text{DMAGx}}$ High	17 + DT		ns
t_{DDGHA}	Address/Select Hold after $\overline{\text{DMAGx}}$ High[6]	–0.5		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if data bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

[1] Only required for recognition in the current cycle.
[2] $t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMARx}}$ is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMARx}}$ low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMARx}}$ is brought high.
[3] For the ADSP-21061L (3.3 V), this specification is 23.5 + 7DT/8 ns min.
[4] $t_{VDATDGH}$ is valid if $\overline{\text{DMARx}}$ is not being used to hold off completion of a read. If $\overline{\text{DMARx}}$ is used to prolong the read, then $t_{VDATDGH} = t_{CK} - .25t_{CCLK} - 8 + (n \times t_{CK})$ where n equals the number of extra cycles that the access is prolonged.
[5] See Example System Hold Time Calculation on Page 44 for calculation of hold times given capacitive and dc loads.
[6] For the ADSP-21061L (3.3 V), this specification is –1.0 ns min.

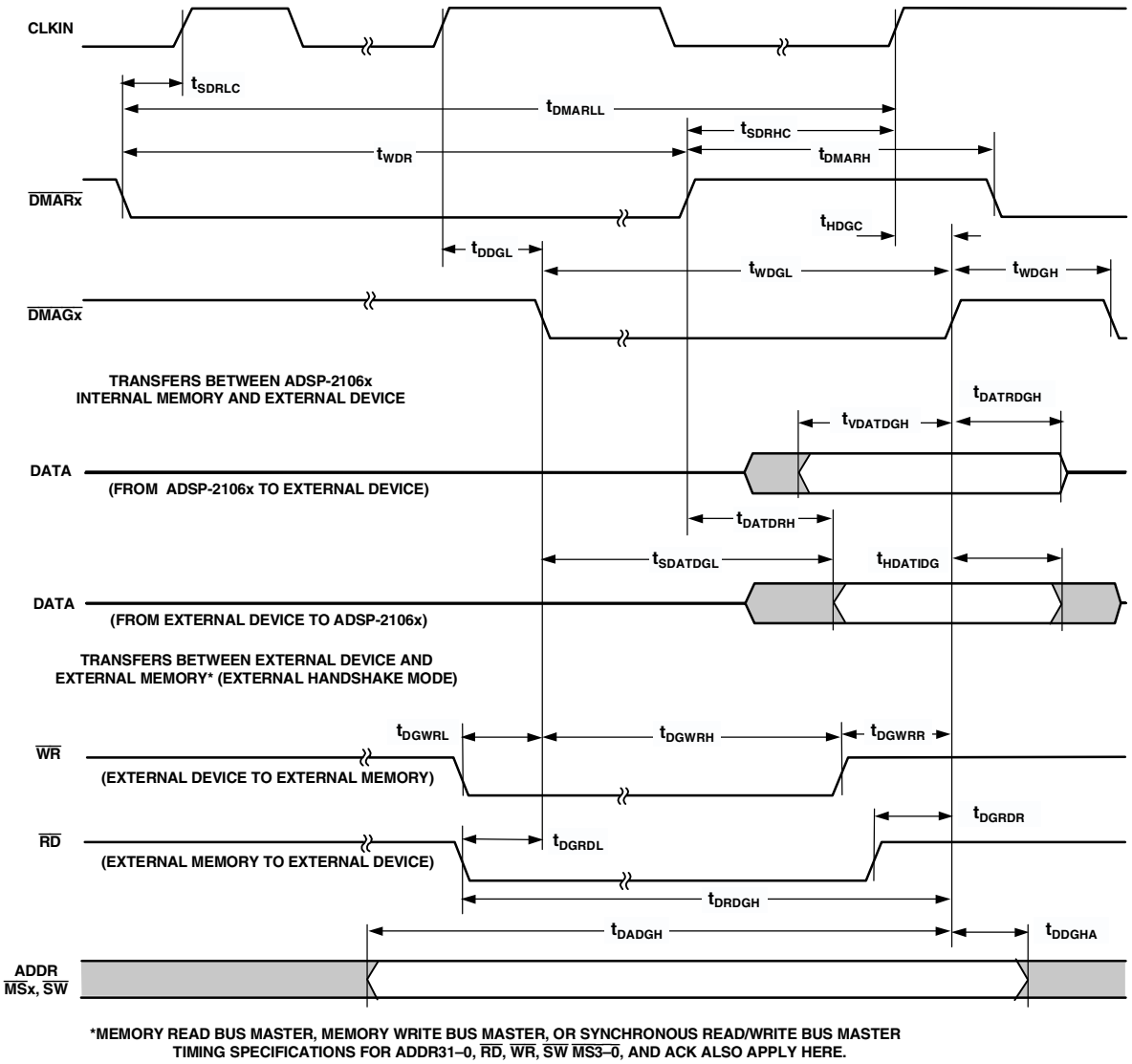

Figure 23. DMA Handshake

Serial Ports

To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold, 2) data delay and data setup and hold, and 3) SCLK width.

Table 21. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSE}	TFS/RFS Setup Before TCLK/RCLK[1]	3.5		ns
t_{HFSE}	TFS/RFS Hold After TCLK/RCLK[1, 2]	4		ns
t_{SDRE}	Receive Data Setup Before RCLK[1]	1.5		ns
t_{HDRE}	Receive Data Hold After RCLK[1]	4		ns
t_{SCLKW}	TCLK/RCLK Width	9		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 22. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Timing Requirements				
t_{SFSI}	TFS Setup Before TCLK[1]; RFS Setup Before RCLK[1]	8		ns
t_{HFSI}	TFS/RFS Hold After TCLK/RCLK[1, 2]	1		ns
t_{SDRI}	Receive Data Setup Before RCLK[1]	3		ns
t_{HDRI}	Receive Data Hold After RCLK[1]	3		ns

[1] Referenced to sample edge.
[2] RFS hold after RCK when MCE = 1, MFD = 0 is 0 ns minimum from drive edge. TFS hold after TCK for late external TFS is 0 ns minimum from drive edge.

Table 23. Serial Ports—External or Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	RFS Delay After RCLK (Internally Generated RFS)[1]		13	ns
t_{HOFSE}	RFS Hold After RCLK (Internally Generated RFS)[1]	3		ns

[1] Referenced to drive edge.

Table 24. Serial Ports—External Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSE}	TFS Delay After TCLK (Internally Generated TFS)[1]		13	ns
t_{HOFSE}	TFS Hold After TCLK (Internally Generated TFS)[1]	3		ns
t_{DDTE}	Transmit Data Delay After TCLK[1]		16	ns
t_{HODTE}	Transmit Data Hold After TCLK[1]	5		ns

[1] Referenced to drive edge.

Table 25. Serial Ports—Internal Clock

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DFSI}	TFS Delay After TCLK (Internally Generated TFS)[1]		4.5	ns
t_{HOFSI}	TFS Hold After TCLK (Internally Generated TFS)[1]	–1.5		ns
t_{DDTI}	Transmit Data Delay After TCLK[1]		7.5	ns
t_{HDTI}	Transmit Data Hold After TCLK[1]	0		ns
t_{SCLKIW}	TCLK/RCLK Width	$t_{SCLK}/2 - 1.5$	$t_{SCLK}/2 + 1.5$	ns

[1] Referenced to drive edge.

Table 26. Serial Ports—Enable and Three-State

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
t_{DDTEN}	Data Enable from External TCLK[1, 2]	4.5		ns
t_{DDTTE}	Data Disable from External TCLK[1]		10.5	ns
t_{DDTIN}	Data Enable from Internal TCLK[1]	0		ns
t_{DDTTI}	Data Disable from Internal TCLK[1]		3	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		22 + 3DT/8	ns
t_{DPTR}	SPORT Disable After CLKIN		17	ns

[1] Referenced to drive edge.
[2] For the ADSP-21061L (3.3 V), this specification is 3.5 ns min.

Table 27. Serial Ports—External Late Frame Sync

Parameter		5 V and 3.3 V Min	Max	Unit
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay from Late External TFS or External RFS with MCE = 1, MFD = 0[1]		12	ns
$t_{DDTENFS}$	Data Enable from Late FS or MCE = 1, MFD = 0[1]	3.5		ns

[1] MCE = 1, TFS enable and TFS valid follow $t_{DDTLFSE}$ and $t_{DDTENFS}$.

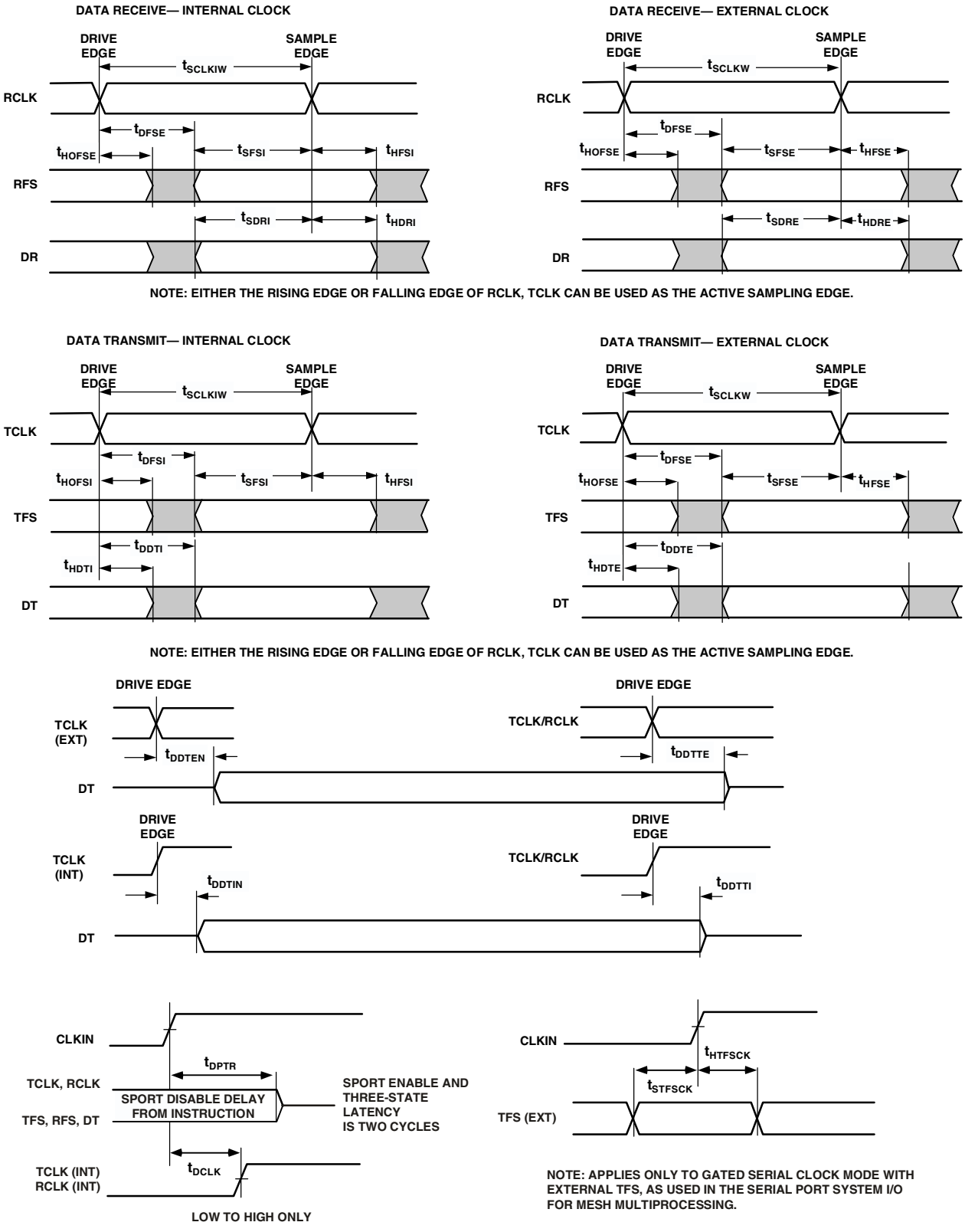

Figure 24. Serial Ports

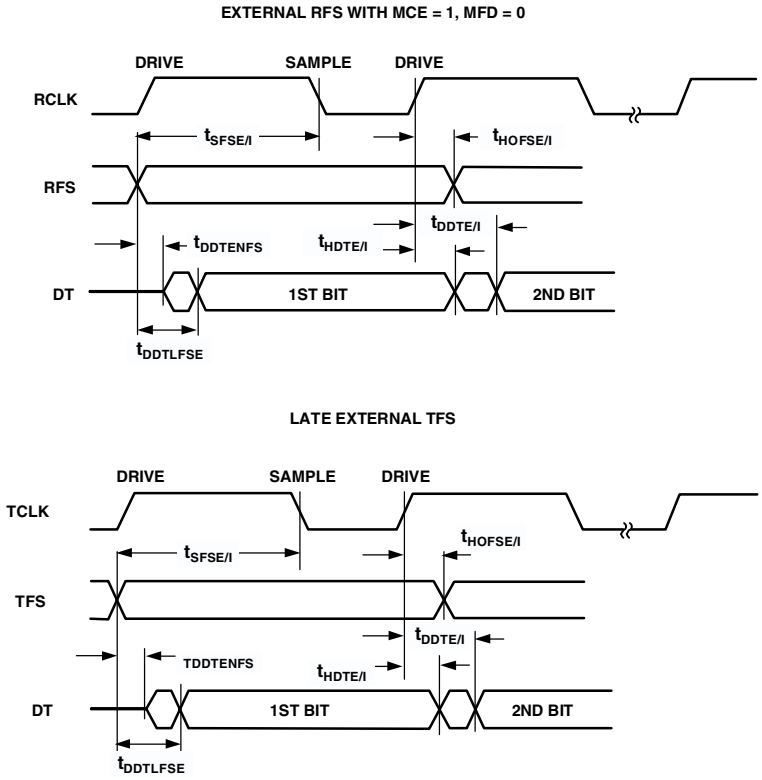

Figure 25. Serial Ports—External Late Frame Sync

JTAG Test Access Port and Emulation

For JTAG Test Access Port and Emulation, see Table 28 and Figure 26.

Table 28. JTAG Test Access Port and Emulation

Parameter		5 V and 3.3 V Min	5 V and 3.3 V Max	Unit
Timing Requirements				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup Before TCK High	t_{CK}		ns
t_{HTAP}	TDI, TMS Hold After TCK High	6		ns
t_{SSYS}	System Inputs Setup Before TCK Low[1]	7		ns
t_{HSYS}	System Inputs Hold After TCK Low[1]	18		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		13	ns
t_{DSYS}	System Outputs Delay After TCK Low[2]		18.5	ns

[1] System Inputs = DATA47–0, ADDR31–0, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR6–1}$, ID2–0, RPBA, $\overline{IRQ2–0}$, FLAG3–0, $\overline{CPA}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

[2] System Outputs = DATA47–0, ADDR31–0, $\overline{MS3–0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, ADRCLK, CLKOUT, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR6–1}$, $\overline{CPA}$, FLAG3–0, TIMEXP, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$.

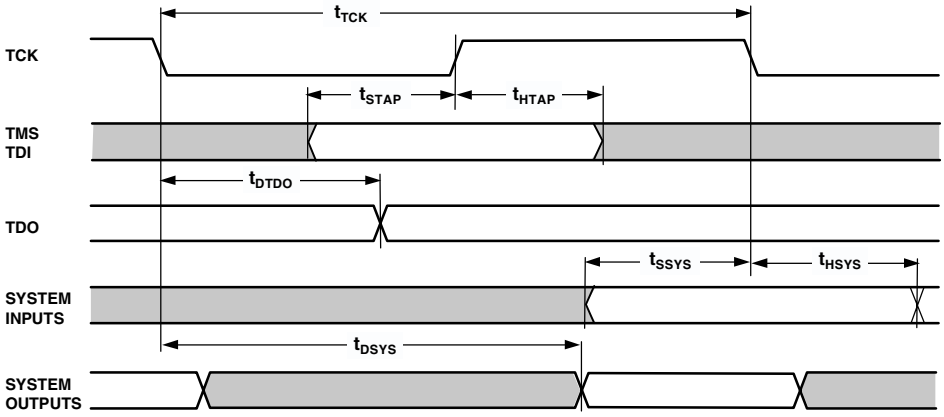

Figure 26. JTAG Test Access Port and Emulation

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$P_{EXT} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 27. The time $t_{MEASURED}$is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 27). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-21061's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{DATRWH} for the write cycle).

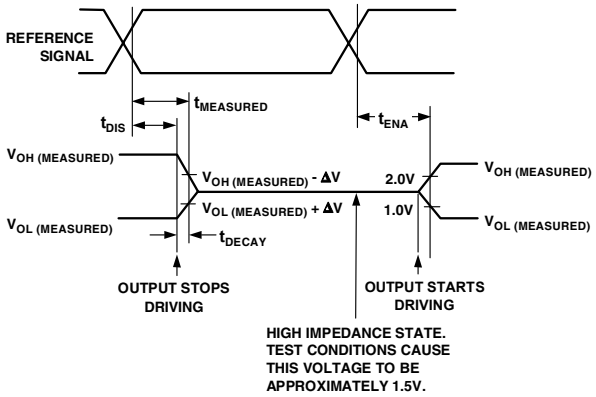

Figure 27. Output Enable/Disable

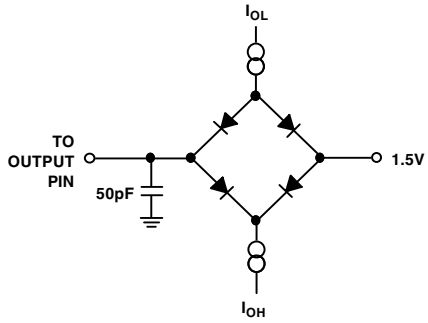

Figure 28. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

Figure 29. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Drive Characteristics

Figure 30 through Figure 37 show typical characteristics for the output drivers of the ADSP-21061 (5 V) and ADSP-21061L (3 V). The curves represent the current drive capability and switching behavior of the output drivers as a function of resistive and capacitive loading.

Capacitive Loading

Output delays and holds are based on standard capacitive loads: 50 pF on all pins (see Figure 28). The delay and hold specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 31, Figure 32, Figure 35, and Figure 36 show how output rise time varies with capacitance. Figure 33 and Figure 37 show graphically how output delays and holds vary with load capacitance. (Note that this graph or derating does not apply to output disable delays; see the previous section Output Disable Time under Test Conditions.) The graphs of Figure 31, Figure 32, Figure 35, and Figure 36 may not be linear outside the ranges shown.

Output Characteristics (5 V)

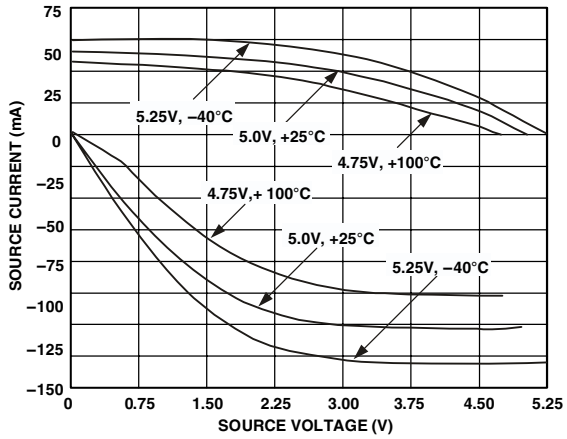

Figure 30. Typical Output Drive Currents (V_{DD} = 5 V)

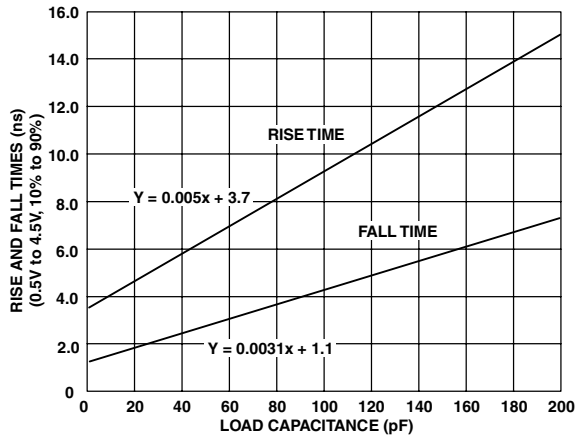

Figure 31. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 5 V)

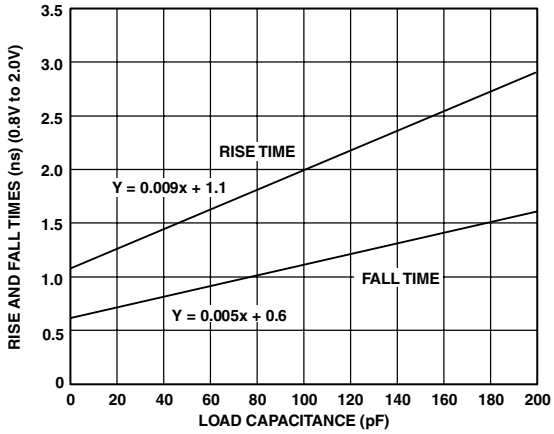

Figure 32. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 5 V)

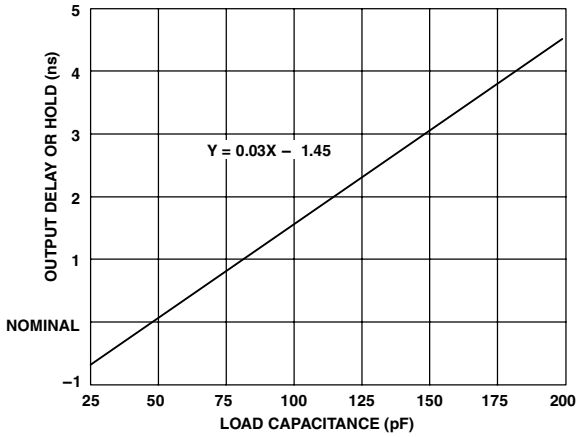

Figure 33. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 5 V)

Input/Output Characteristics (3.3 V)

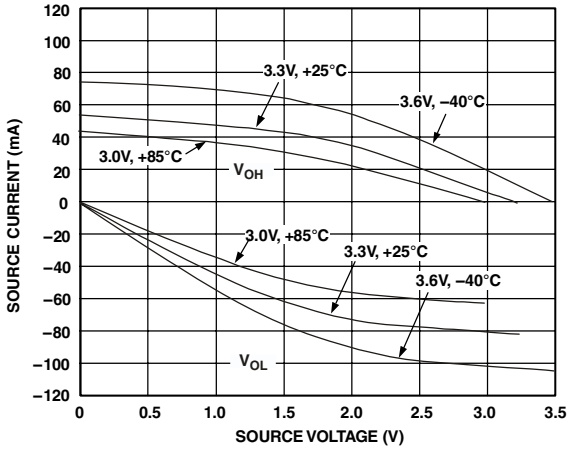

Figure 34. Typical Drive Currents (V_{DD} = 3.3 V)

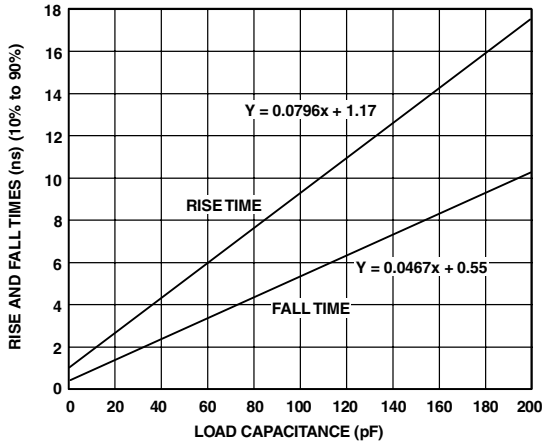

Figure 35. Typical Output Rise Time (10% to 90% V_{DD}) vs. Load Capacitance (V_{DD} = 3.3 V)

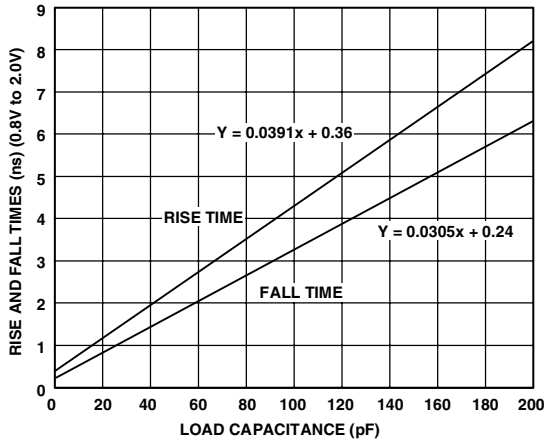

Figure 36. Typical Output Rise Time (0.8 V to 2.0 V) vs. Load Capacitance (V_{DD} = 3.3 V)

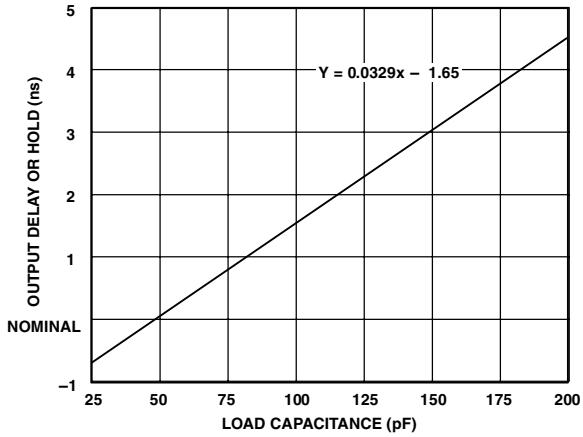

Figure 37. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature) (V_{DD} = 3.3 V)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-21061 is available in 240-lead thermally enhanced MQFP package. The top surface of the thermally enhanced MQFP contains a metal slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the metal slug is internally connected to GND through the device substrate.

The ADSP-21061L is available in 240-lead MQFP and 225-ball plastic BGA packages.

All packages are specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} is not exceeded, a heatsink and/or an airflow source may be used. A heat sink should be attached with a thermal adhesive.

$T_{CASE} = T_{AMB} + (PD\ \theta CA)$

T_{CASE} = Case temperature (measured on top surface of package)
PD =Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under Power Dissipation).

θ_{CA} =Value from tables below.

Table 29. ADSP-21061 (5 V Thermally Enhanced ED/MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	10	°C/W
	Airflow = 100	9	
	Airflow = 200	8	
	Airflow = 400	7	
	Airflow = 600	6	

Table 30. ADSP-21061L (3.3 V MQFP Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.6	°C/W
	Airflow = 100	17.6	
	Airflow = 200	15.6	
	Airflow = 400	13.9	
	Airflow = 600	12.2	

Table 31. ADSP-21061L (3.3 V PBGA Package)

Parameter	Condition (Linear Ft./Min.)	Typical	Unit
θ_{CA}	Airflow = 0	19.0	°C/W
	Airflow = 200	13.6	
	Airflow = 400	11.2	

225-BALL PBGA PIN CONFIGURATIONS

Table 32. ADSP-21061L 225-Lead Metric PBGA (B-225-2) Pin Assignments

Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number
$\overline{BMS}$	A01	ADDR25	D01	ADDR14	G01	ADDR6	K01	$\overline{EMU}$	N01
ADDR30	A02	ADDR26	D02	ADDR15	G02	ADDR5	K02	TDO	N02
$\overline{DMAR2}$	A03	$\overline{MS2}$	D03	ADDR16	G03	ADDR3	K03	$\overline{IRQ0}$	N03
DT1	A04	ADDR29	D04	ADDR19	G04	ADDR0	K04	$\overline{IRQ1}$	N04
RCLK1	A05	$\overline{DMAR1}$	D05	GND	G05	ICSA	K05	ID2	N05
TCLK0	A06	TFS1	D06	V_{DD}	G06	GND	K06	NC	N06
RCLK0	A07	$\overline{CPA}$	D07	V_{DD}	G07	V_{DD}	K07	NC	N07
ADRCLK	A08	$\overline{HBG}$	D08	V_{DD}	G08	V_{DD}	K08	NC	N08
$\overline{CS}$	A09	$\overline{DMAG2}$	D09	V_{DD}	G09	V_{DD}	K09	NC	N09
CLKIN	A10	$\overline{BR5}$	D10	V_{DD}	G10	GND	K10	NC	N10
PAGE	A11	$\overline{BR1}$	D11	GND	G11	GND	K11	NC	N11
$\overline{BR3}$	A12	DATA40	D12	DATA22	G12	DATA8	K12	NC	N12
DATA47	A13	DATA37	D13	DATA25	G13	DATA11	K13	NC	N13
DATA44	A14	DATA35	D14	DATA24	G14	DATA13	K14	DATA1	N14
DATA42	A15	DATA34	D15	DATA23	G15	DATA14	K15	DATA3	N15
$\overline{MS0}$	B01	ADDR21	E01	ADDR12	H01	ADDR2	L01	$\overline{TRST}$	P01
$\overline{SW}$	B02	ADDR22	E02	ADDR11	H02	ADDR1	L02	TMS	P02
ADDR31	B03	ADDR24	E03	ADDR13	H03	FLAG0	L03	EBOOT	P03
$\overline{HBR}$	B04	ADDR27	E04	ADDR10	H04	FLAG3	L04	ID0	P04
DR1	B05	GND	E05	GND	H05	RPBA	L05	NC	P05
DT0	B06	GND	E06	V_{DD}	H06	GND	L06	NC	P06
DR0	B07	GND	E07	V_{DD}	H07	GND	L07	NC	P07
REDY	B08	GND	E08	V_{DD}	H08	GND	L08	NC	P08
$\overline{RD}$	B09	GND	E09	V_{DD}	H09	GND	L09	NC	P09
ACK	B10	GND	E10	V_{DD}	H10	GND	L10	NC	P10
$\overline{BR6}$	B11	NC	E11	GND	H11	NC	L11	NC	P11
$\overline{BR2}$	B12	DATA33	E12	DATA18	H12	DATA4	L12	NC	P12
DATA45	B13	DATA30	E13	DATA19	H13	DATA7	L13	NC	P13
DATA43	B14	DATA32	E14	DATA21	H14	DATA9	L14	NC	P14
DATA39	B15	DATA31	E15	DATA20	H15	DATA10	L15	DATA0	P15
$\overline{MS3}$	C01	ADDR17	F01	ADDR9	J01	FLAG1	M01	TCK	R01
$\overline{MS1}$	C02	ADDR18	F02	ADDR8	J02	FLAG2	M02	$\overline{IRQ2}$	R02
ADDR28	C03	ADDR20	F03	ADDR7	J03	TIMEXP	M03	$\overline{RESET}$	R03
$\overline{SBTS}$	C04	ADDR23	F04	ADDR4	J04	TDI	M04	ID1	R04
TCLK1	C05	GND	F05	GND	J05	LBOOT (GND)	M05	NC	R05
RFS1	C06	GND	F06	V_{DD}	J06	NC	M06	NC	R06
TFS0	C07	V_{DD}	F07	V_{DD}	J07	NC	M07	NC	R07
RFS0	C08	V_{DD}	F08	V_{DD}	J08	NC	M08	NC	R08
$\overline{WR}$	C09	V_{DD}	F09	V_{DD}	J09	NC	M09	NC	R09
$\overline{DMAG1}$	C10	GND	F10	V_{DD}	J10	NC	M10	NC	R10
$\overline{BR4}$	C11	GND	F11	GND	J11	NC	M11	NC	R11
DATA46	C12	DATA29	F12	DATA12	J12	NC	M12	NC	R12

Table 32. ADSP-21061L 225-Lead Metric PBGA (B-225-2) Pin Assignments (Continued)

Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number	Pin Name	PBGA Pin Number
DATA41	C13	DATA26	F13	DATA15	J13	DATA2	M13	NC	R13
DATA38	C14	DATA28	F14	DATA16	J14	DATA5	M14	NC	R14
DATA36	C15	DATA27	F15	DATA17	J15	DATA6	M15	NC	R15

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
DATA42	DATA44	DATA47	BR3	PAGE	CLKIN	CS	ADRCLK	RCLK0	TCLK0	RCLK1	DT1	DMAR2	ADDR30	BMS	A
DATA39	DATA43	DATA45	BR2	BR6	ACK	RD	REDY	DR0	DT0	DR1	HBR	ADDR31	SW	MS0	B
DATA36	DATA38	DATA41	DATA46	BR4	DMAG1	WR	RFS0	TFS0	RFS1	TCLK1	SBTS	ADDR28	MS1	MS3	C
DATA34	DATA35	DATA37	DATA40	BR1	BR5	DMAG2	HBG	CPA	TFS1	DMAR1	ADDR29	MS2	ADDR26	ADDR25	D
DATA31	DATA32	DATA30	DATA33	NC	GND	GND	GND	GND	GND	GND	ADDR27	ADDR24	ADDR22	ADDR21	E
DATA27	DATA28	DATA26	DATA29	GND	GND	VDD	VDD	VDD	GND	GND	ADDR23	ADDR20	ADDR18	ADDR17	F
DATA23	DATA24	DATA25	DATA22	GND	VDD	VDD	VDD	VDD	VDD	GND	ADDR19	ADDR16	ADDR15	ADDR14	G
DATA20	DATA21	DATA19	DATA18	GND	VDD	VDD	VDD	VDD	VDD	GND	ADDR10	ADDR13	ADDR11	ADDR12	H
DATA17	DATA16	DATA15	DATA12	GND	VDD	VDD	VDD	VDD	VDD	GND	ADDR4	ADDR7	ADDR8	ADDR9	J
DATA14	DATA13	DATA11	DATA8	GND	GND	VDD	VDD	VDD	GND	ICSA	ADDR0	ADDR3	ADDR5	ADDR6	K
DATA10	DATA9	DATA7	DATA4	NC	GND	GND	GND	GND	GND	RPBA	FLAG3	FLAG0	ADDR1	ADDR2	L
DATA6	DATA5	DATA2	NC	NC	NC	NC	NC	NC	NC	LBOOT (GND)	TDI	TIMEXP	FLAG2	FLAG1	M
DATA3	DATA1	NC	NC	NC	NC	NC	NC	NC	NC	ID2	IRQ1	IRQ0	TDO	EMU	N
DATA0	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	ID0	EBOOT	TMS	TRST	P
NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	ID1	RESET	IRQ2	TCK	R

NC = NO CONNECT

Figure 38. BGA Pin Assignments (Top View, Summary)

240-LEAD MQFP PIN CONFIGURATIONS

Table 33. ADSP-21061 MQFP/ED (SP-240); ADSP-21061L MQFP (S-240) Pin Assignments

Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
TDI	1	ADDR20	41	TCLK0	81	DATA41	121	DATA14	161	NC	201
$\overline{TRST}$	2	ADDR21	42	TFS0	82	DATA40	122	DATA13	162	NC	202
V_{DD}	3	$\overline{GND}$	43	DR0	83	DATA39	123	DATA12	163	NC	203
TDO	4	ADDR22	44	RCLK0	84	V_{DD}	124	GND	164	NC	204
TIMEXP	5	ADDR23	45	RFS0	85	DATA38	125	DATA11	165	V_{DD}	205
$\overline{EMU}$	6	ADDR24	46	V_{DD}	86	DATA37	126	DATA10	166	NC	206
ICSA	7	V_{DD}	47	V_{DD}	87	DATA36	127	DATA9	167	NC	207
FLAG3	8	GND	48	GND	88	GND	128	V_{DD}	168	NC	208
FLAG2	9	V_{DD}	49	ADRCLK	89	NC	129	DATA8	169	NC	209
FLAG1	10	ADDR25	50	REDY	90	DATA35	130	DATA7	170	NC	210
FLAG0	11	ADDR26	51	$\overline{HBG}$	91	DATA34	131	DATA6	171	NC	211
GND	12	ADDR27	52	$\overline{CS}$	92	DATA33	132	GND	172	GND	212
ADDR0	13	GND	53	$\overline{RD}$	93	V_{DD}	133	DATA5	173	NC	213
ADDR1	14	$\overline{MS3}$	54	$\overline{WR}$	94	V_{DD}	134	DATA4	174	NC	214
V_{DD}	15	$\overline{MS2}$	55	GND	95	GND	135	DATA3	175	NC	215
ADDR2	16	$\overline{MS1}$	56	V_{DD}	96	DATA32	136	V_{DD}	176	NC	216
ADDR3	17	$\overline{MS0}$	57	GND	97	DATA31	137	DATA2	177	NC	217
ADDR4	18	$\overline{SW}$	58	CLKIN	98	DATA30	138	DATA1	178	NC	218
GND	19	$\overline{BMS}$	59	ACK	99	GND	139	DATA0	179	V_{DD}	219
ADDR5	20	ADDR28	60	$\overline{DMAG2}$	100	DATA29	140	GND	180	GND	220
ADDR6	21	GND	61	$\overline{DMAG1}$	101	DATA28	141	GND	181	V_{DD}	221
ADDR7	22	V_{DD}	62	PAGE	102	DATA27	142	NC	182	NC	222
V_{DD}	23	V_{DD}	63	V_{DD}	103	V_{DD}	143	NC	183	NC	223
ADDR8	24	ADDR29	64	$\overline{BR6}$	104	V_{DD}	144	NC	184	NC	224
ADDR9	25	ADDR30	65	$\overline{BR5}$	105	DATA26	145	NC	185	NC	225
ADDR10	26	ADDR31	66	$\overline{BR4}$	106	DATA25	146	NC	186	NC	226
GND	27	GND	67	$\overline{BR3}$	107	DATA24	147	NC	187	NC	227
ADDR11	28	$\overline{SBTS}$	68	$\overline{BR2}$	108	GND	148	V_{DD}	188	GND	228
ADDR12	29	$\overline{DMAR2}$	69	$\overline{BR1}$	109	DATA23	149	NC	189	ID2	229
ADDR13	30	$\overline{DMAR1}$	70	GND	110	DATA22	150	NC	190	ID1	230
V_{DD}	31	$\overline{HBR}$	71	V_{DD}	111	DATA21	151	NC	191	ID0	231
ADDR14	32	DT1	72	GND	112	V_{DD}	152	NC	192	LBOOT (GND)	232
ADDR15	33	TCLK1	73	DATA47	113	DATA20	153	NC	193	RPBA	233
GND	34	TFS1	74	DATA46	114	DATA19	154	NC	194	$\overline{RESET}$	234
ADDR16	35	DR1	75	DATA45	115	DATA18	155	GND	195	EBOOT	235
ADDR17	36	RCLK1	76	V_{DD}	116	GND	156	GND	196	$\overline{IRQ2}$	236
ADDR18	37	RFS1	77	DATA44	117	DATA17	157	V_{DD}	197	$\overline{IRQ1}$	237
V_{DD}	38	GND	78	DATA43	118	DATA16	158	NC	198	$\overline{IRQ0}$	238
V_{DD}	39	$\overline{CPA}$	79	DATA42	119	DATA15	159	NC	199	TCK	239
ADDR19	40	DT0	80	GND	120	V_{DD}	160	NC	200	TMS	240

OUTLINE DIMENSIONS

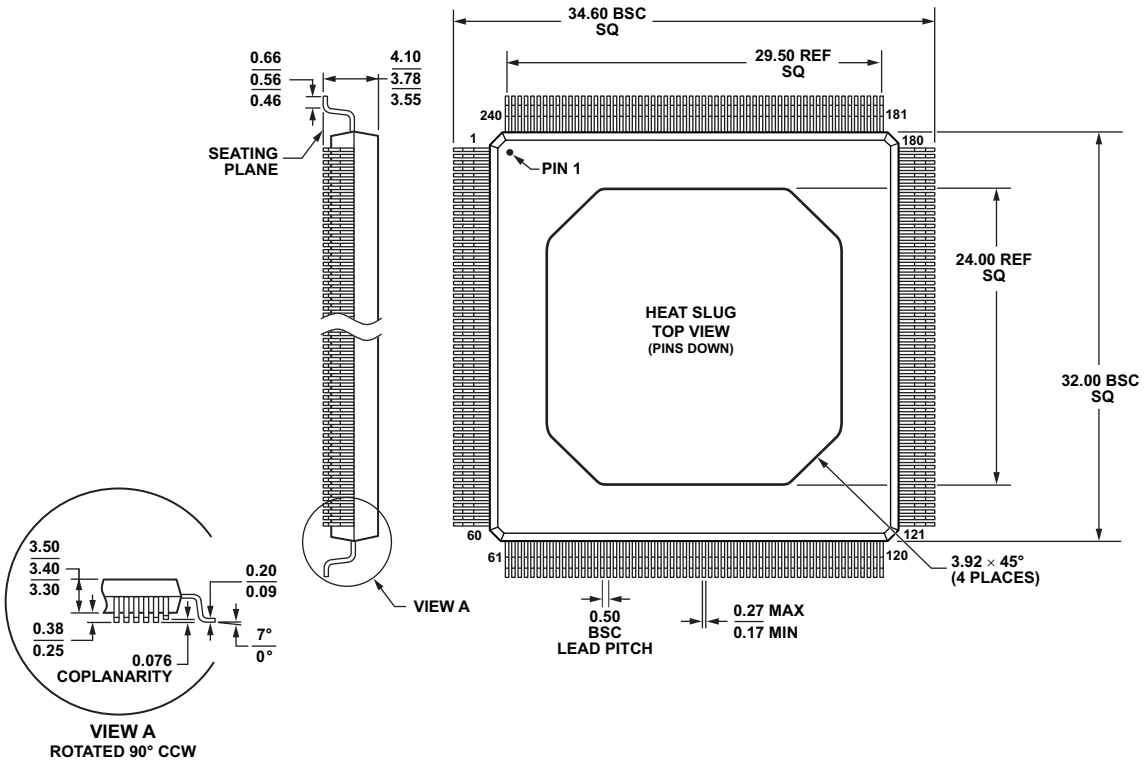

Figure 39. 240-Lead Metric Quad Flat Package, Thermally Enhanced [MQFP/ED] (SP-240-2)

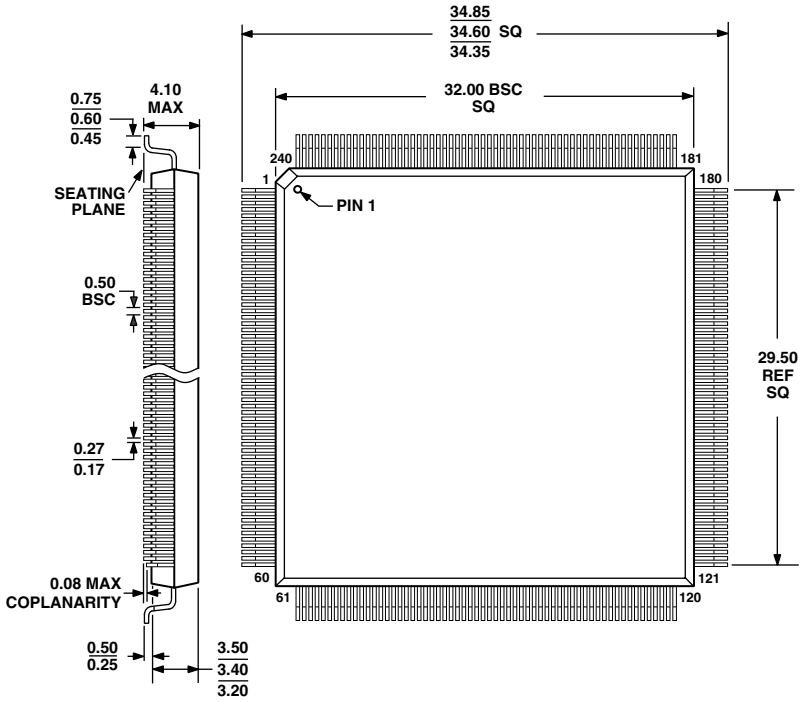

Figure 40. 240-Lead Metric Quad Flat Package, [MQFP] (S-240)

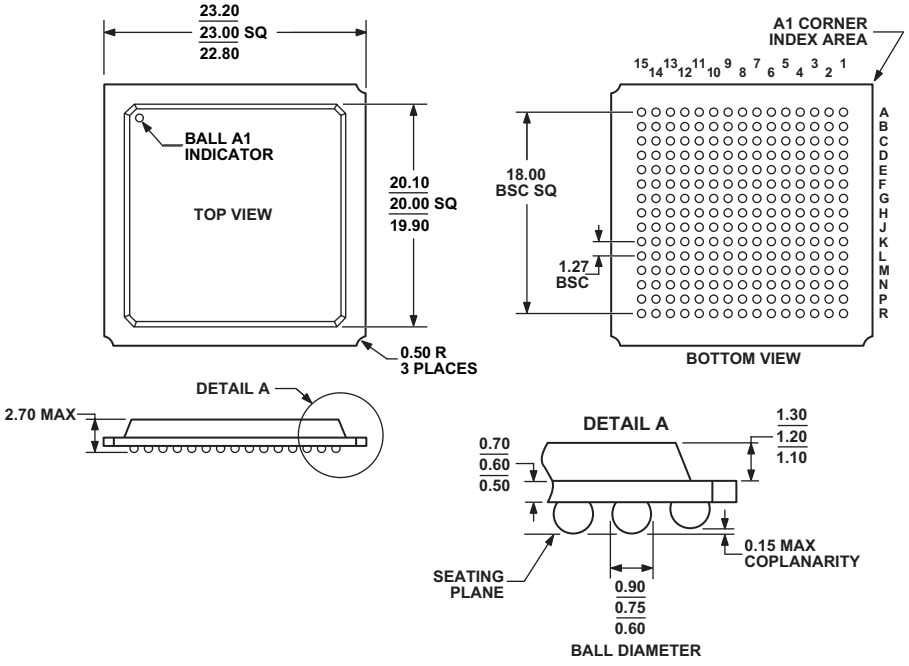

Figure 41. 225-Ball Plastic Ball Grid Array [PBGA] (B-225-2)

SURFACE-MOUNT DESIGN

Table 34 is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard.*

Table 34. BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
225-Ball Grid Array (PBGA)	Solder Mask Defined	0.63 mm diameter	0.73 mm diameter

ORDERING GUIDE

Model	Temperature Range	Instruction Rate	On-Chip SRAM	Operating Voltage	Package Description	Package Option
ADSP-21061KS-133	0°C to 85°C	33 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-133[1]	0°C to 85°C	33 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KS-160	0°C to 85°C	40 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-160[1]	0°C to 85°C	40 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KS-200	0°C to 85°C	50 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061KSZ-200[1]	0°C to 85°C	50 MHz	1M Bit	5 V	240-Lead MQFP_ED	SP-240-2
ADSP-21061LKB-160	0°C to 85°C	40 MHz	1M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21061LKBZ-160[1]	0°C to 85°C	40 MHz	1M Bit	3.3 V	225-Ball PBGA	B-225-2
ADSP-21061LKS-160	0°C to 85°C	40 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LKSZ-160[1]	0°C to 85°C	40 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LAS-176	–40°C to +85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LASZ-176[1]	–40°C to +85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LKS-176	0°C to 85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240
ADSP-21061LKSZ-176[1]	0°C to 85°C	44 MHz	1M Bit	3.3 V	240-Lead MQFP	S-240

[1] Z = RoHS Compliant Part.