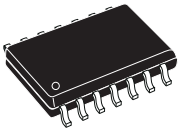
TDA7535

Delta/sigma cascade 20 bit stereo DAC

Features

- 20-bit resolution single ended output
- Analog reconstruction third order Chebyshev filter
- I^2S input data format
- On chip PLL
- System clock: 64 Fs
- 2 output channels
- 0.9 V_{RMS} single ended output dynamic
- 3.3 V power supply
- Reset
- Sampling rate 36 kHz to 48 kHz



SO14

The TDA7535 is available in SO14 package. The total power consumption is less than 75 mW.

TDA7535 is suitable for a wide variety of applications where high performance are required. Its low cost and single 3.3 V power supply make it ideal for several applications, such as CD players, MPEG audio, MIDI applications, CD-ROM drives, CD-Interactive, digital radio applications and so on. An evaluation board is available to perform measurement and to make listening tests.

Description

The TDA7535 is a stereo, digital-to-analog converter designed for audio application, including digital interpolation filter, a third order multi-bit Delta-Sigma DAC, a third order Chebyshev's reconstruction filter and a differential to single ended output converter. This device is fabricated in highly advanced CMOS, where high speed precision analog circuits are combined with high density logic circuits. The TDA7535, according to standard audio converters, can accept any I^2S data format.

Table 1. Device summary

Order code	Package	Packing
TDA7535	SO14	Tube
TDA7535013TR	SO14	Tape and reel

Contents

1 Block diagram and pin description

Figure 1. Block diagram

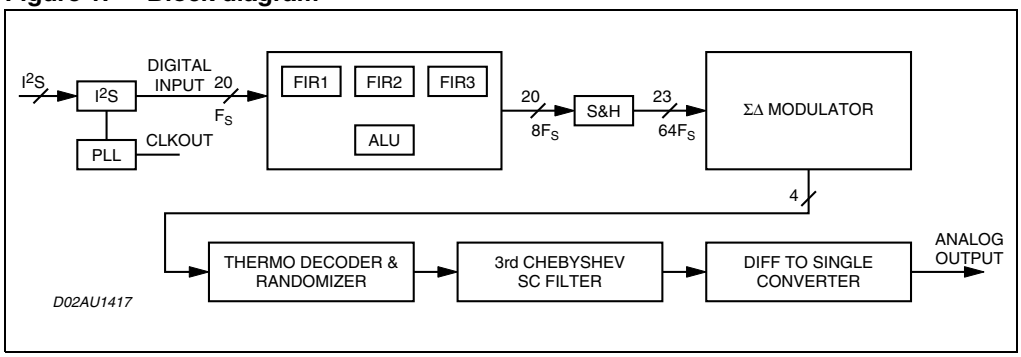


Figure 2. Pin connection (top view)

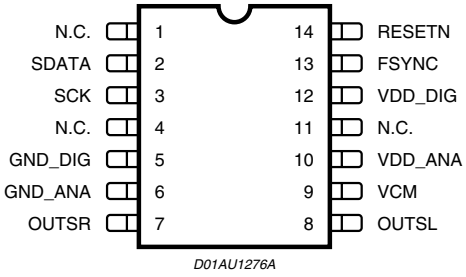


Table 2. Pin function

Pin #	Pin name	Input/output power	Description
1	N.C.	-	-
2	SDATA	I	I2S digital data input
3	SCK	I	I2S clock input
4	N.C.	-	-
5	GND_DIG	P	Digital ground
6	GND_ANA	P	Analog ground
7	OUTSR	O	Right channel single ended output
8	OUTSL	O	Left channel single ended output
9	VCM	P	Reference 1.65 V externally filtered
10	VDD_ANA	P	Analog 3.3 V supply
11	N.C.	-	-
12	VDD_DIG	P	Digital 3.3 V-supply
13	FSYNC	I	I2S Left-right channel selector
14	RESETN	I	Reset (active low)

2 Electrical specification

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DD} V_{CC}	Power supplies	Digital Analog	-0.5 to +4.6 -0.5 to +4.6	V V
V_{aio}	Analog input and output voltage		-0.5 to (V_{CC}+0.5)	V
V_{dio}	Digital input and output voltage		-0.5 to (V_{DD}+0.5)	V
V_{di5}	Digital input voltage (5 V tolerant)		-0.5 to 6.5	V
T_j	Operating junction temperature range		-40 to 125	°C
T_{stg}	Storage temperature		-55 to 150	°C

Warning: Operation at or beyond these limit may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient (1)	85	°C/W

1. In still air.

2.3 Recommended DC operating conditions

Table 5. Recommended DC operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	3.3 V digital power supply voltage		3.15	3.3	3.45	V
V_{CC}	3.3 V analog power supply voltage		3.15	3.3	3.45	V

2.4 Power consumption

Table 6. Power consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{dd}	Total maximum current	Power supply @ 3.3 V and T_j = 125 °C		21.5	25	mA

2.5 General interface electrical characteristics

Table 7. General interface electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{il}	Low level input current without pull-up device	V_i = 0 V(1)			1	µA
I_{ih}	High level input current without pull-up device	$V_i = V_{dd}$ (1)			1	µA
$I_{latchup}$	I/O latch-up current	V < 0 V, V > V_{dd}	200			mA
V_{esd}	Electrostatic protection	Leakage, 1 µA(2)	2000			V

1. The leakage currents are generally very small, <1nA. The value given here, 1mA, is the maximum that can occur after an Electrostatic Stress on the pin.
2. Human body model.

2.6 Low voltage CMOS interface DC electrical characteristics

Table 8. Low voltage CMOS interface DC electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{il}	Low Level Input Voltage				$0.2*V_{dd}$	V
V_{ih}	High Level Input Voltage		$0.8*V_{dd}$			V
V_{hyst}	Schmitt trigger hysteresis		0.8			V

2.7 DAC electrical characteristics

Table 9. DAC electrical characteristics

V_{dd} = 3.3 V; T_{amb} = 25 °C; Input signal frequency = sinus wave generated by audio precision Sys.2; Input signal amplitude (see notes); Noise integration bandwidth = 20 Hz to 22 kHz (A- weighted)

Parameter	Test condition	Min.	Typ.	Max.	Unit
Noise + distortion (1)	@0 dB @-6 dBb @-40 dB @-60 dB		89 94 96 96		dB dB dB dB
Total harmonic distortion	see note (2)	70(3)	94		dB
Dynamic range	see note (4)	84(5)	96		dB
Crosstalk	see note (6)		-95		dB
Full scale output voltage	V_{dd} = 3.15 to 3.45 V Full scale input	0.8	0.9	1.0	Vrms
Input sampling rate		36		48	kHz
Passband ripple			0.12		dB
Stopband	@ 3dB @ 90dB 44.1kHz sampling rate	21.53		24.80	kHz
Interchannel gain mismatch			0.05	0.1	dB

1. It is the ratio between the maximum input signal and the integration of the in-band noise after deducing the power of signal fundamental. It depends on the input signal amplitude. In this case 0dB means full scale digital, 1 kHz frequency used.
2. It is the ratio of the rms value of the signal fundamental component at 0 dB (full scale digital) to the rms value of all of the harmonic components in the band.
3. By correlation to beuch results. ATE limits are 60 dB.
4. Measured using the SNR at -60dB input signal, with 60dB added to compensate for small input signal.
5. By correlation to beuch results. ATE limits are 80 dB.
6. Left channel on with 0dB/1kHz input signal, Right channel on with DC input signal.

3 I²S interface

Figure 3. I²S interface diagram

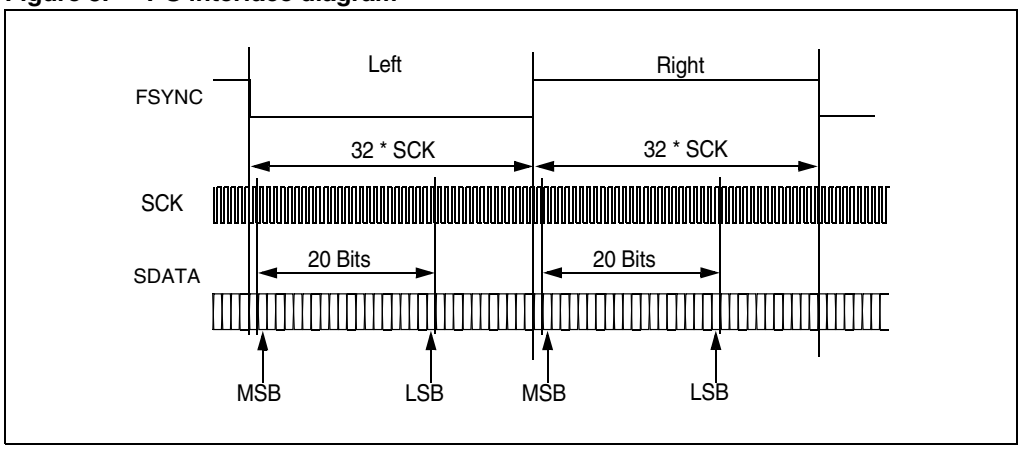


Figure 4. I²S timings

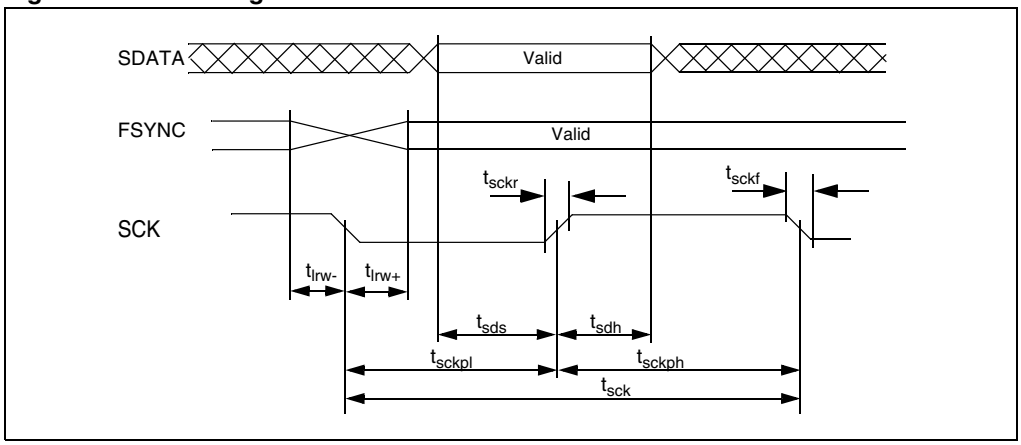


Table 10. Timing characteristics

Timing	Description	Min.	Max.	Unit
t_{sck}	Clock cycle(1)	1/(64*Fs) - 150ps$_{RMS}$	1/(64*Fs) + 150ps$_{RMS}$	ns
t_{sckpl}	SCK phase low	0.5*t_{sck} - 1%	0.5*t_{sck} +1%	ns
t_{sckph}	SCK phase high	0.5*t_{sck} - 1%	0.5*t_{sck} +1%	ns
t_{lrw-}	FSYNC switching time window before SCK falling edge(2)	0	0.125*t_{sck}-10	ns
t_{lrw+}	FSYNC switching time window after SCK falling edge(2))	0	0.125*t_{sck}-10	ns
t_{sds}	SDATA setup time	60		ns
t_{sdh}	SDATA hold time	30		ns

Table 10. Timing characteristics (continued)

Timing	Description	Min.	Max.	Unit
t_{sckr}	SCK rise time		22	ns
t_{sckf}	SCK fall time		20	ns

1. SCK clock defines the Fs, being the Sample Rate. This input clock needs a jitter below ~212ps$_{RMS}$.
2. FSYNC switches inside the time window as specified w.r.t. to falling edge of SCK.

Figure 5. Power up and reset sequence

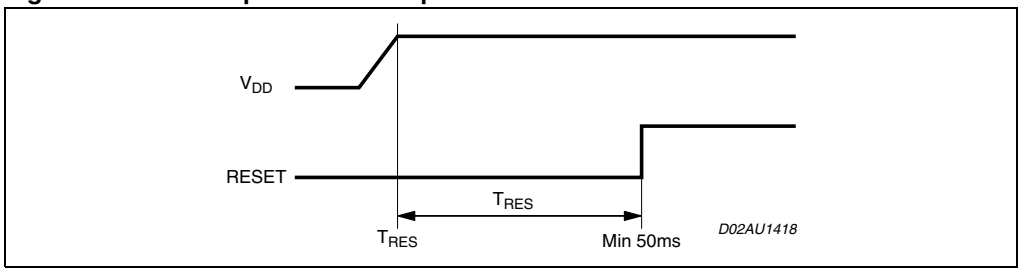
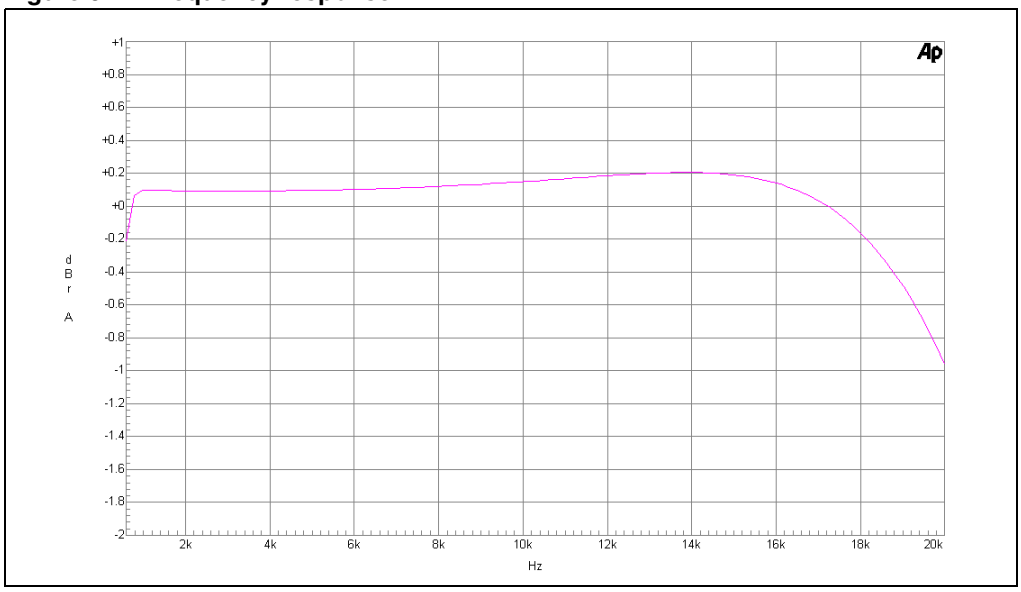
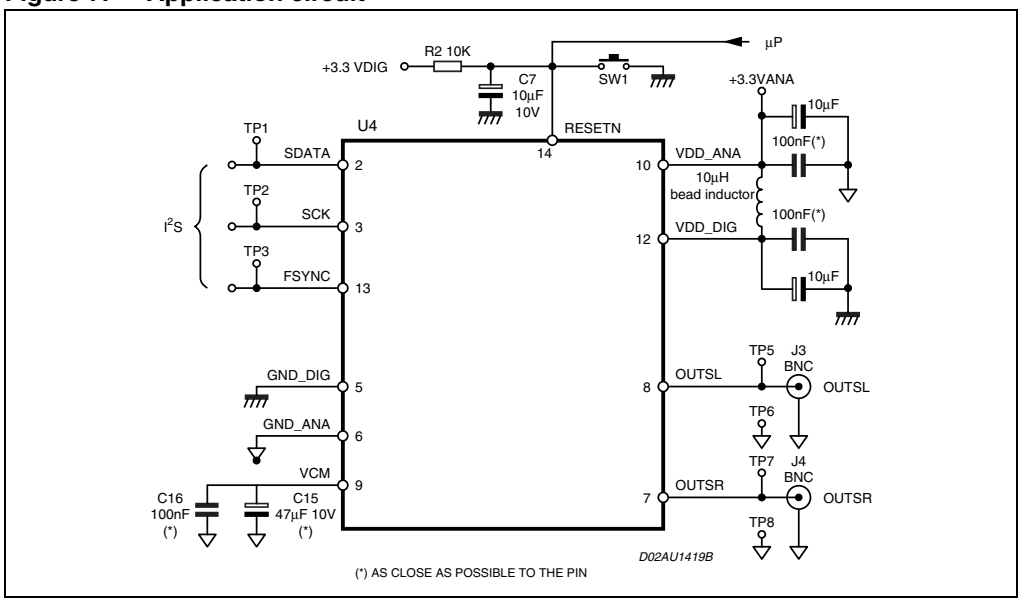


Figure 6. Frequency response



4 Application circuit

Figure 7. Application circuit



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

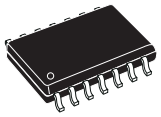
ECOPACK® is an ST trademark.

Figure 8. SO14 mechanical data and package dimensions

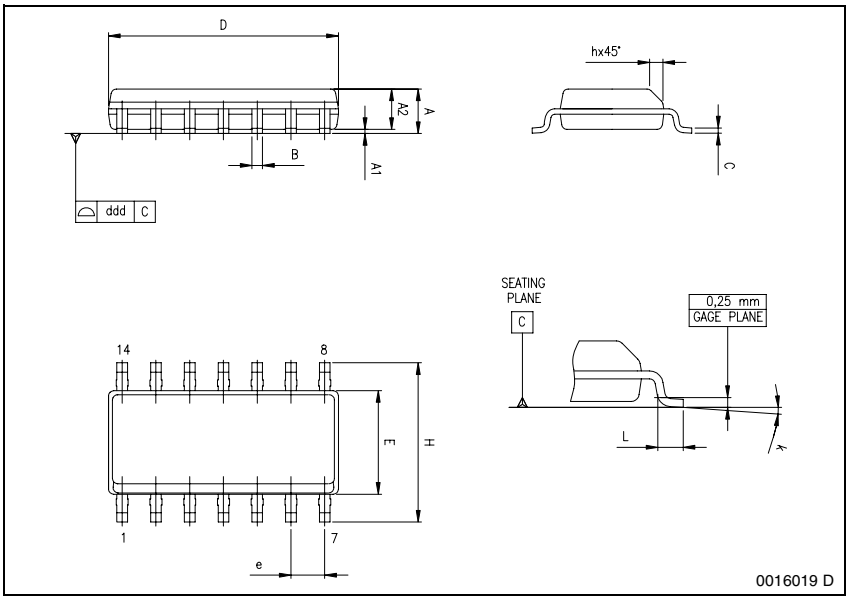
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.30	0.004		0.012
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D (1)	8.55		8.75	0.337		0.344
E	3.80		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.20	0.228		0.244
h	0.25		0.50	0.01		0.02
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO14



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
13-Dec- 2003	5	Initial release.
21-Dec- 2005	6	Update electrical characteristics. Add revision history table.
03-Feb-2006	7	Updated max. value of t_{sckr} and $t_{sck}t$ parameter on page 5/9.
06-Feb-2009	8	Document reformatted. Updated *Section 5: Package information on page 10*.

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