

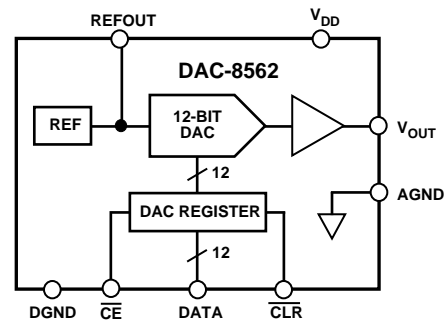
FEATURES

Complete 12-Bit DAC
No External Components
Single +5 Volt Operation
1 mV/Bit with 4.095 V Full Scale
True Voltage Output, ± 5 mA Drive
Very Low Power –3 mW

APPLICATIONS

Digitally Controlled Calibration
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The DAC8562 is a complete, parallel input, 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DAC, is a rail-to-rail amplifier, latch and reference. The reference (REFOUT) is trimmed to 2.5 volts, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The DAC8562 is coded straight binary. The op amp output swings from 0 to +4.095 volts for a one millivolt per bit resolution, and is capable of driving ± 5 mA. Built using low temperature-coefficient silicon-chrome thin-film resistors, excellent linearity error over temperature has been achieved as shown below in the linearity error versus digital input code plot.

Digital interface is parallel and high speed to interface to the fastest processors without wait states. The interface is very simple requiring only a single CE signal. An asynchronous CLR input sets the output to zero scale.

The DAC8562 is available in two different 20-pin packages, plastic DIP and SOL-20. Each part is fully specified for operation over -40°C to $+85^{\circ}\text{C}$, and the full $+5\text{ V} \pm 5\%$ power supply range.

For MIL-STD-883 applications, contact your local ADI sales office for the DAC8562/883 data sheet which specifies operation over the -55°C to $+125^{\circ}\text{C}$ temperature range.

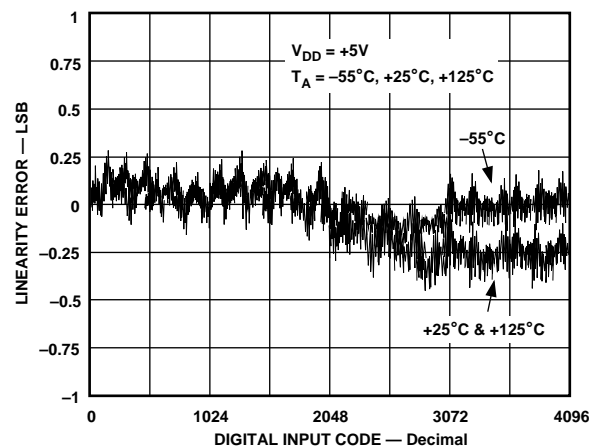


Figure 1. Linearity Error vs. Digital Input Code Plot

REV. A

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
 Tel: 617/329-4700 Fax: 617/326-8703

DAC8562—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ $V_{DD} = +5.0 \pm 5\%$, $R_S = \text{No Load}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 2	12			Bits
Relative Accuracy	INL	E Grade	−1/2	±1/4	+1/2	LSB
		F Grade	−1	±3/4	+1	LSB
Differential Nonlinearity	DNL	No Missing Codes	−1	±3/4	+1	LSB
Zero-Scale Error	V _{ZSE}	Data = 000 _H		+1/2	+3	LSB
Full-Scale Voltage	V _{FS}	Data - FFF _H ³				
		E Grade	4.087	4.095	4.103	V
		F Grade	4.079	4.095	4.111	V
Full-Scale Tempco	TCV _{FS}	Notes 3, 4		±16		ppm/°C
ANALOG OUTPUT						
Output Current	I _{OUT}	Data = 800 _H	±5	±7		mA
Load Regulation at Half Scale	LD _{REG}	R _L = 402 Ω to ∞, Data = 800 _H		1	3	LSB
Capacitive Load	C _L	No Oscillation ⁴		500		pF
REFERENCE OUTPUT						
Output Voltage	V _{REF}	Note 5	2.484	2.500	2.516	V
Output Source Current	I _{REF}		5	7		mA
Line Rejection	LN _{REJ}	I _{REF} = 0 to 5 mA			0.08	%/V
Load Regulation	LD _{REG}				0.1	%/mA
LOGIC INPUTS						
Logic Input Low Voltage	V _{IL}	Note 4	2.4		0.8	V
Logic Input High Voltage	V _{IH}					V
Input Leakage Current	I _{IL}				10	μA
Input Capacitance	C _{IL}				10	pF
INTERFACE TIMING SPECIFICATIONS ^{1, 4}						
Chip Enable Pulse Width	t _{CEW}		30			ns
Data Setup	t _{DS}		30			ns
Data Hold	t _{DH}		10			ns
Clear Pulse Width	t _{CLR_W}		20			ns
AC CHARACTERISTICS ⁴						
Voltage Output Settling Time ⁶	t _S	To ±1 LSB of Final Value		16		μs
Digital Feedthrough				35		nV sec
SUPPLY CHARACTERISTICS						
Positive Supply Current	I _{DD}	V _{IH} = 2.4 V, V _{IL} = 0.8 V		3	6	mA
		V _{IL} = 0 V, V _{DD} = +5 V		0.6	1	mA
Power Dissipation	P _{DISS}	V _{IH} = 2.4 V, V _{IL} = 0.8 V		15	30	mW
		V _{IL} = 0 V, V _{DD} = +5V		3	5	mW
Power Supply Sensitivity	PSS	ΔV _{DD} = ±5%		0.002	0.004	%/%

NOTES

¹All input control signals are specified with $t_r = t_f = 5 \text{ ns}$ (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

²1 LSB = 1 mV for 0 to +4.095 V output range.

³Includes internal voltage reference error.

⁴These parameters are guaranteed by design and not subject to production testing.

⁵Very little sink current is available at the REFOUT pin. Use external buffer if setting up a virtual ground.

⁶The settling time specification does not apply for negative going transitions within the last 6 LSBs of ground. Some devices exhibit double the typical settling time in this 6 LSB region.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ $V_{DD} = +5.0\text{ V} \pm 5\%$, $R_L = \text{No Load}$, $T_A = +25^\circ\text{C}$, applies to part number DAC8562GBC only, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Relative Accuracy	INL	No Missing Codes Data = 000 _H Data = FFF _H	−1	±3/4	+1	LSB
Differential Nonlinearity	DNL		−1	±3/4	+ 1	LSB
Zero-Scale Error	V _{ZSE}		+1/2	+3	LSB	
Full-Scale Voltage	V _{FS}		4.085	4.095	4.105	V
Reference Output Voltage	V _{REF}		2.490	2.500	2.510	V
LOGIC INPUTS						
Logic Input Low Voltage	V _{IL}		2.4		0.8	V
Logic Input High Voltage	V _{IH}				V	
Input Leakage Current	I _{IL}				10	μA
SUPPLY CHARACTERISTICS						
Positive Supply Current	I _{DD}	V _{IH} = 2.4 V, V _{IL} = 0.8 V		3	6	mA
		V _{IL} = 0 V, V _{DD} = +5 V		0.6	1	mA
Power Dissipation	P _{DISS}	V _{IH} = 2.4 V, V _{IL} = 0.8 V		15	30	mW
		V _{IL} = 0 V, V _{DD} = +5 V		3	5	mW
Power Supply Sensitivity	PSS	ΔV _{DD} = ±5%		0.002	0.004	%/%

NOTE

¹Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND and AGND	-0.3 V, +10 V
Logic Inputs to DGND	-0.3 V, $V_{DD} + 0.3\text{ V}$
V_{OUT} to AGND	-0.3 V, $V_{DD} + 0.3\text{ V}$
V_{REFOUT} to AGND	-0.3 V, $V_{DD} + 0.3\text{ V}$
AGND to DGND	-0.3 V, V_{DD}
I_{OUT} Short Circuit to GND	50 mA
Package Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}		
20-Pin Plastic DIP Package (P)	74°C/W
20-Lead SOIC Package (S)	89°C/W
Maximum Junction Temperature ($T_J \text{ max}$)	150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

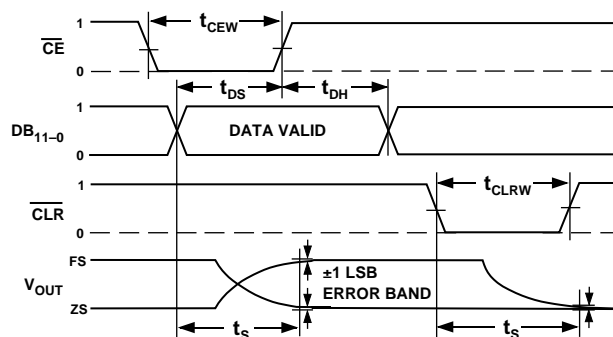


Figure 2. Timing Diagram

Table I. Control Logic Truth Table

\overline{CE}	\overline{CLR}	DAC Register Function
H	H	Latched
L	H	Transparent
$\uparrow +$	H	Latched with New Data
X	L	Loaded with All Zeros
H	$\uparrow +$	Latched All Zeros

$\uparrow +$ Positive Logic Transition; X Don't Care.

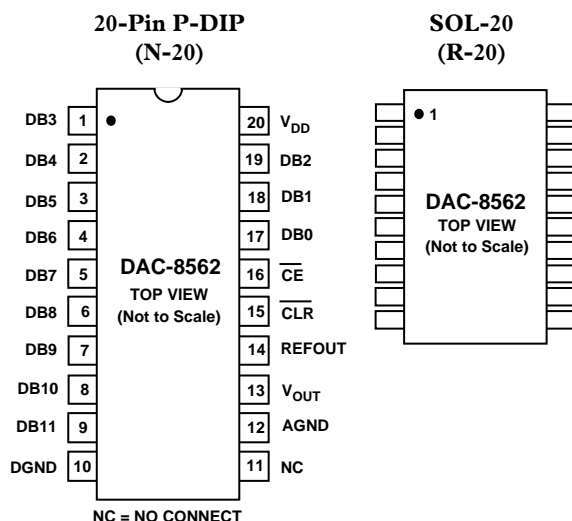
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



DAC8562

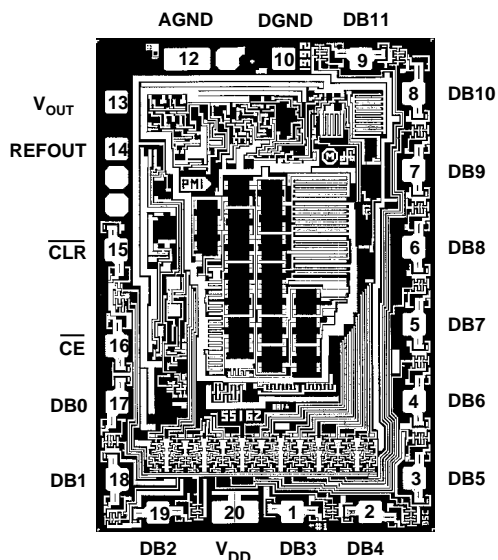
PIN CONFIGURATIONS



ORDERING GUIDE

Model	INL (LSB)	Temperature Range	Package Option
DAC8562EP	±1/2	−40°C to +85°C	N-20
DAC8562FP	±1	−40°C to +85°C	N-20
DAC8562FS	±1	−40°C to +85°C	R-20
DAC8562GBC	±1	+25°C	Dice

DICE CHARACTERISTICS



SUBSTRATE IS COMMON WITH V_{DD} .
TRANSISTOR COUNT: 524
DIE SIZE: 0.70 X 0.105 INCH; 7350 SQ MILS

Table II. Nominal Output Voltage vs. Input Code

Binary	Hex	Decimal	Output (V)
0000 0000 0000	000	0	0.000 Zero Scale
0000 0000 0001	001	1	0.001
0000 0000 0010	002	2	0.002
0000 0000 1111	00F	15	0.015
0000 0001 0000	010	16	0.016
0000 1111 1111	0FF	255	0.255
0001 0000 0000	100	256	0.256
0001 1111 1111	1FF	511	0.511
0010 0000 0000	200	512	0.512
0011 1111 1111	3FF	1023	1.023
0100 0000 0000	400	1024	1.024
0111 1111 1111	7FF	2047	2.047
1000 0000 0000	800	2048	2.048 Half Scale
1100 0000 0000	C00	3072	3.072
1111 1111 1111	FFF	4095	4.095 Full Scale

PIN DESCRIPTIONS

Pin	Name	Description
20	V _{DD}	Positive supply. Nominal value +5 volts, $\pm 5\%$.
1-9 17-19	DB0-DB11	Twelve Binary Data Bit inputs. DB11 is the MSB and DB0 is the LSB.
16	$\overline{\text{CE}}$	Chip Enable. Active low input.
15	$\overline{\text{CLR}}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale.
8	DGND	Digital ground for input logic.
12	AGND	Analog Ground. Ground reference for the internal bandgap reference voltage, the DAC, and the output buffer.
13	V _{OUT}	Voltage output from the DAC. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.
14	REFOUT	Nominal 2.5 V reference output voltage. This node must be buffered if required to drive external loads.
11	NC	No Connection. Leave pin floating.

OPERATION

The DAC8562 is a complete ready to use 12-bit digital-to-analog converter. Only one +5 V power supply is necessary for operation. It contains a voltage-switched, 12-bit, laser-trimmed digital-to-analog converter, a curvature-corrected bandgap reference, a rail-to-rail output op amp, and a DAC register. The parallel data interface consists of 12 data bits, DB0–DB11, and a active low CE strobe. In addition, an asynchronous CLR pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output (not available to the user) is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 ($= 4.095 \text{ V}/2.5 \text{ V}$) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

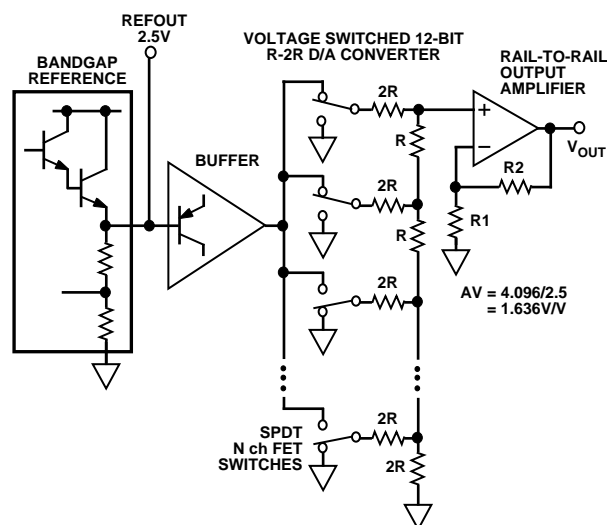


Figure 3. Equivalent DAC8562 Schematic of Analog Portion

The op amp has a 16 μs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the Typical Performances section of this data sheet.

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull down FETs that will pull an output load directly to GND. The output sourcing

current is provided by a P channel pull-up device that can supply GND terminated loads, especially important at the -5% supply tolerance value of 4.75 volts.

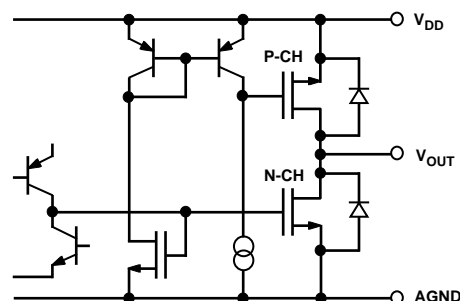


Figure 4. Equivalent Analog Output Circuit

Figures 5 and 6 in the typical performance characteristics section provide information on output swing performance near ground and full scale as a function of load. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the REFOUT pin. Since REFOUT is not intended to drive external loads, it must be buffered—refer to the applications section for more information. The equivalent emitter follower output circuit of the REFOUT pin is shown in Figure 3.

Bypassing the REFOUT pin is not required for proper operation. Figure 7 shows broadband noise performance.

POWER SUPPLY

The very low power consumption of the DAC8562 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, good analog accuracy is achieved.

For power-consumption sensitive applications it is important to note that the internal power consumption of the DAC8562 is strongly dependent on the actual logic-input voltage-levels present on the DB0–DB11, CE and CLR pins. Since these inputs are standard CMOS logic structures, they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total DAC8562 supply current as a function of the actual value of input logic voltage. Consequently for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A $V_{INL} = 0 \text{ V}$ on the DB0–DB11 pins provides the lowest standby dissipation of 600 μA with a +5 V power supply.

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As with any analog system, it is recommended that the DAC8562 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifier used in the DAC8562 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the DAC8562 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 11, provides information for operation below $V_{DD} = +4.75$ V.

TIMING AND CONTROL

The DAC8562 has a 12-bit DAC register that simplifies interface to a 12-bit (or wider) data bus. The latch is controlled by the Chip Enable (\overline{CE}) input. If the application does not involve a data bus, wiring \overline{CE} low allows direct operation of the DAC.

The data latch is level triggered and acquires data from the data bus during the time period when \overline{CE} is low. When \overline{CE} goes high, the data is latched into the register and held until \overline{CE} returns low. The minimum time required for the data to be present on the bus before \overline{CE} returns high is called the data setup time (t_{DS}) as seen in Figure 2. The data hold time (t_{DH}) is the amount of time that the data has to remain on the bus after \overline{CE} goes high. The high speed timing offered by the DAC8562 provides for direct interface with no wait states in all but the fastest microprocessors.

Typical Performance Characteristics

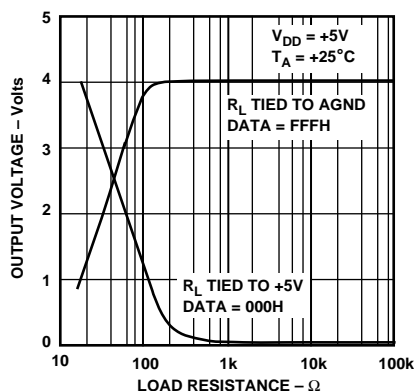


Figure 5. Output Swing vs. Load

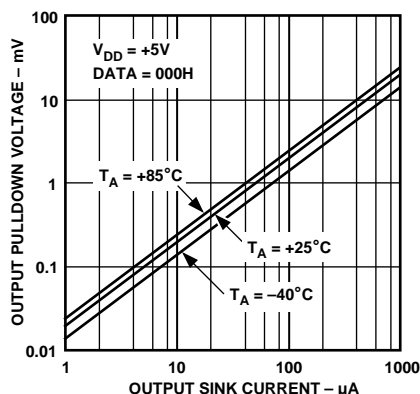


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

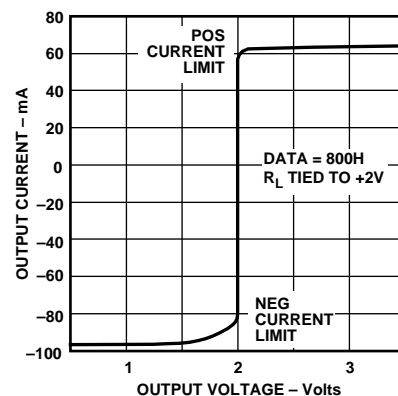


Figure 7. I_{OUT} vs. V_{OUT}

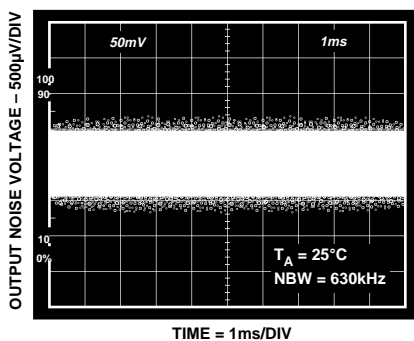


Figure 8. Broadband Noise

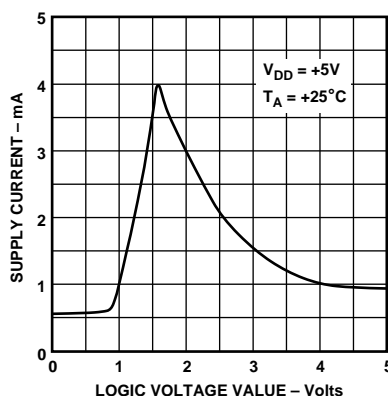


Figure 9. Supply Current vs. Logic Input Voltage

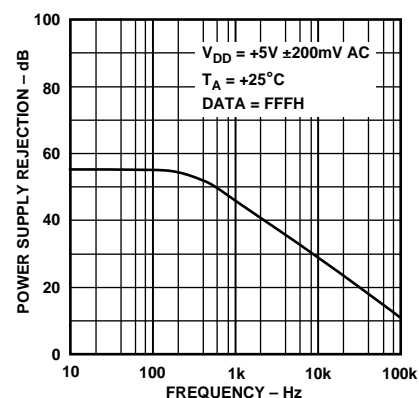


Figure 10. Power Supply Rejection vs. Frequency

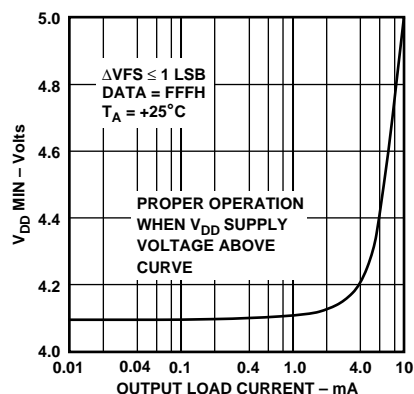


Figure 11. Minimum Supply Voltage vs. Load

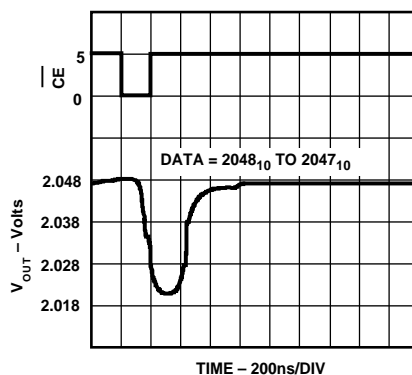


Figure 12. Midscale Transition Performance

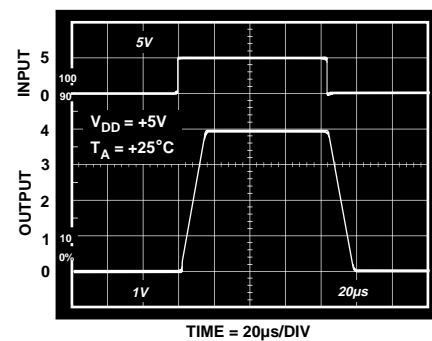


Figure 13. Large Signal Settling Time

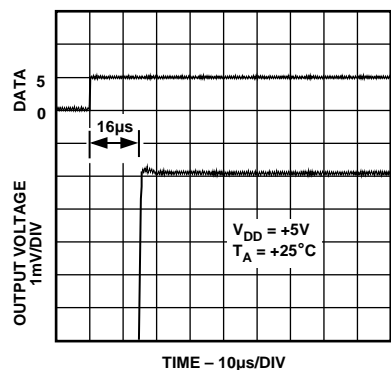


Figure 14. Output Voltage Rise Time Detail

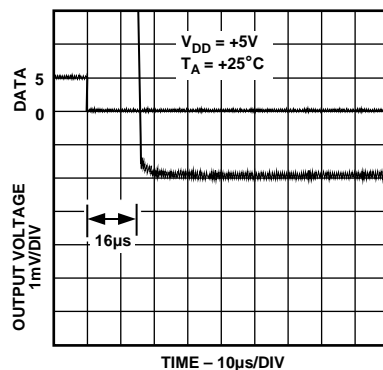


Figure 15. Output Voltage Fall Time Detail

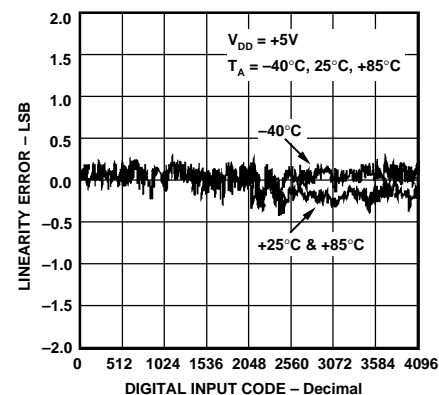


Figure 16. Linearity Error vs. Digital Code

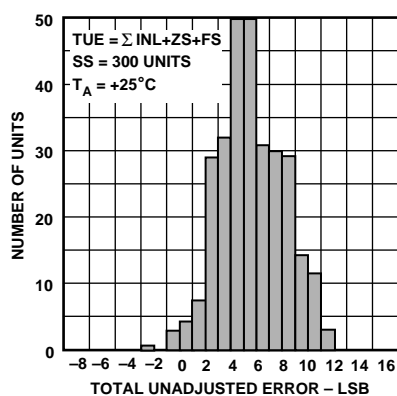


Figure 17. Total Unadjusted Error Histogram

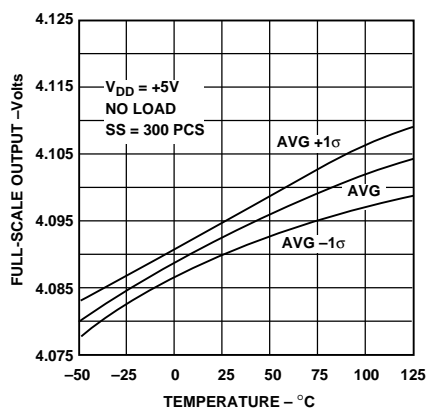


Figure 18. Full-Scale Voltage vs. Temperature

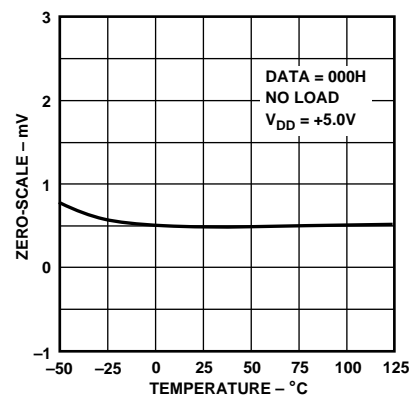


Figure 19. Zero-Scale Voltage vs. Temperature

DAC8562–Typical Performance Characteristics

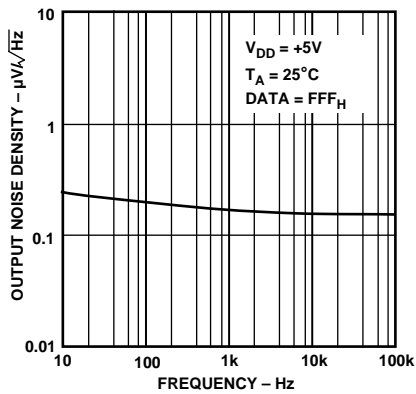


Figure 20. Output Voltage Noise Density vs. Frequency

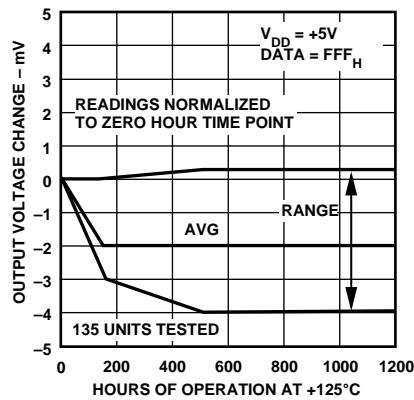


Figure 21. Long-Term Drift Accelerated by Burn-In

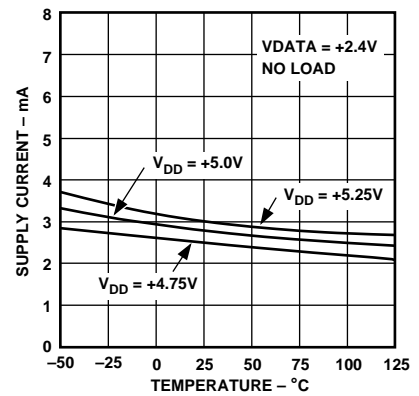


Figure 22. Supply Current vs. Temperature

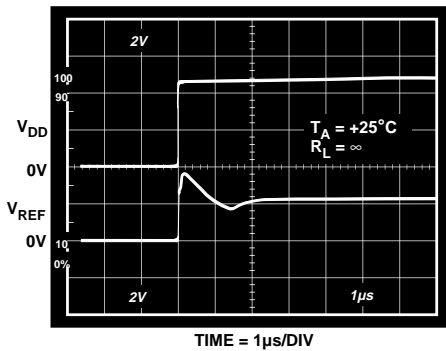


Figure 23. Reference Startup vs. Time

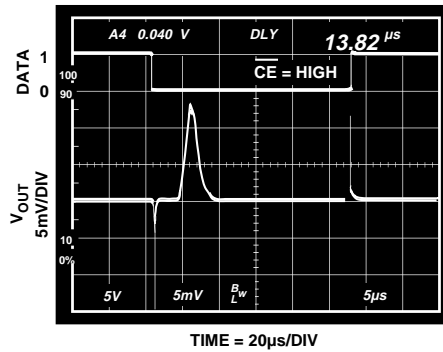


Figure 24. Digital Feedthrough vs. Time

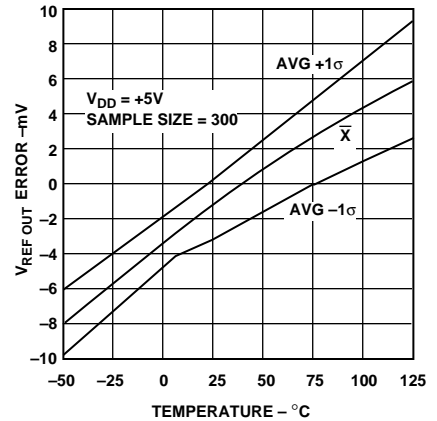


Figure 25. Reference Error vs. Temperature

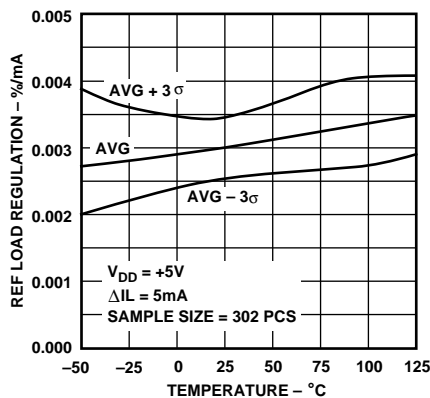


Figure 26. Reference Load Regulation vs. Temperature

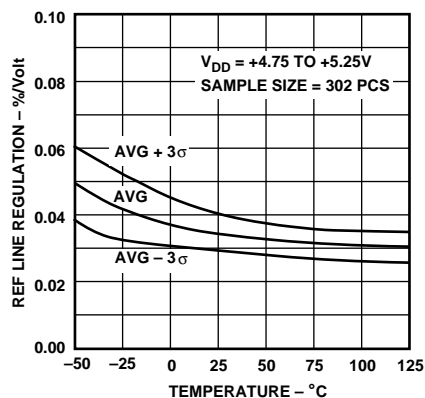


Figure 27. Reference Line Regulation vs. Temperature

DAC8562

Unipolar Output Operation

This is the basic mode of operation for the DAC8562. As shown in Figure 30, the DAC8562 has been designed to drive loads as low as 820 Ω in parallel with 500 pF. The code table for this operation is shown in Table III.

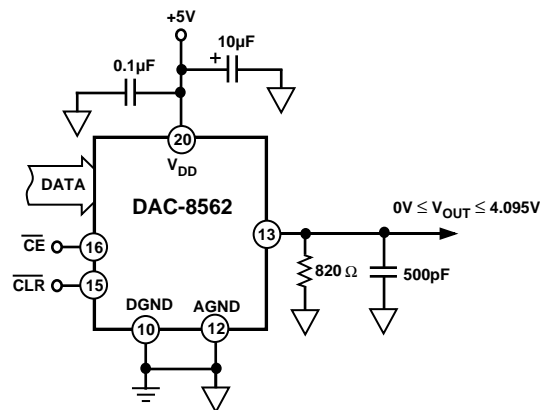


Figure 30. Unipolar Output Operation

Table III. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+4.095
801	2049	+2.049
800	2048	+2.048
7FF	2047	+2.047
000	0	0

Operating the DAC8562 on +12 V or +15 V Supplies Only
Although the DAC8562 has been specified to operate on a single, +5 V supply, a single +5 V supply may not be available in many applications. Since the DAC8562 consumes no more than 6 mA, maximum, then an integrated voltage reference, such as the REF02, can be used as the DAC8562 +5 V supply. The configuration of the circuit is shown in Figure 31. Notice that the reference's output voltage requires no trimming because of the REF02's excellent load regulation and tight initial output voltage tolerance. Although the maximum supply current of the DAC8562 is 6 mA, local bypassing of the REF02's output with at least 0.1 µF at the DAC's voltage supply pin is recommended to prevent the DAC's internal digital circuits from affecting the DAC's internal voltage reference.

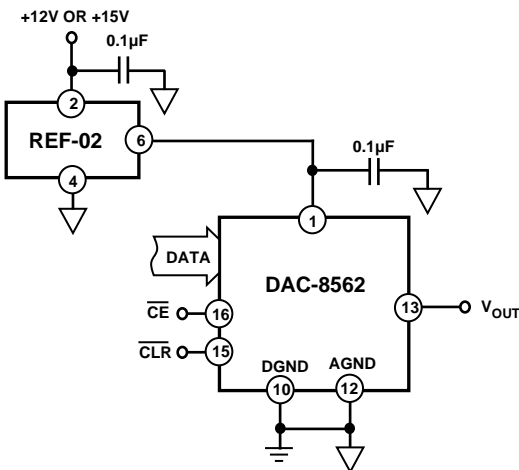


Figure 31. Operating the DAC8562 on +12 V or +15 V Supplies Using a REF02 Voltage Reference

Measuring Offset Error

One of the most commonly specified endpoint errors associated with real-world nonideal DACs is offset error.

In most DAC testing, the offset error is measured by applying the zero-scale code and measuring the output deviation from 0 volt. There are some DACs where offset errors may be present but not observable at the zero scale because of other circuit limitations (for example, zero coinciding with single supply ground). In these DACs, nonzero output at zero code cannot be read as the offset error. In the DAC8562, for example, the zero-scale error is specified to be +3 LSBs. Since zero scale coincides with zero volt, it is not possible to measure negative offset error.

By adding a pull-down resistor from the output of the DAC8562 to a negative supply as shown in Figure 32, offset errors can now be read at zero code. This configuration forces the output P-channel MOSFET to source current to the negative supply thereby allowing the designer to determine in which direction the offset error appears. The value of the resistor should be such that, at zero code, current through the resistor is 200 µA maximum.

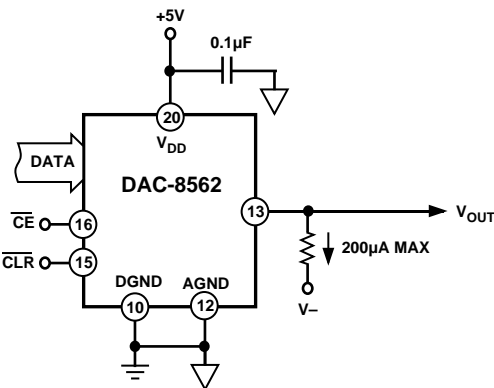


Figure 32. Measuring Zero-Scale or Offset Error

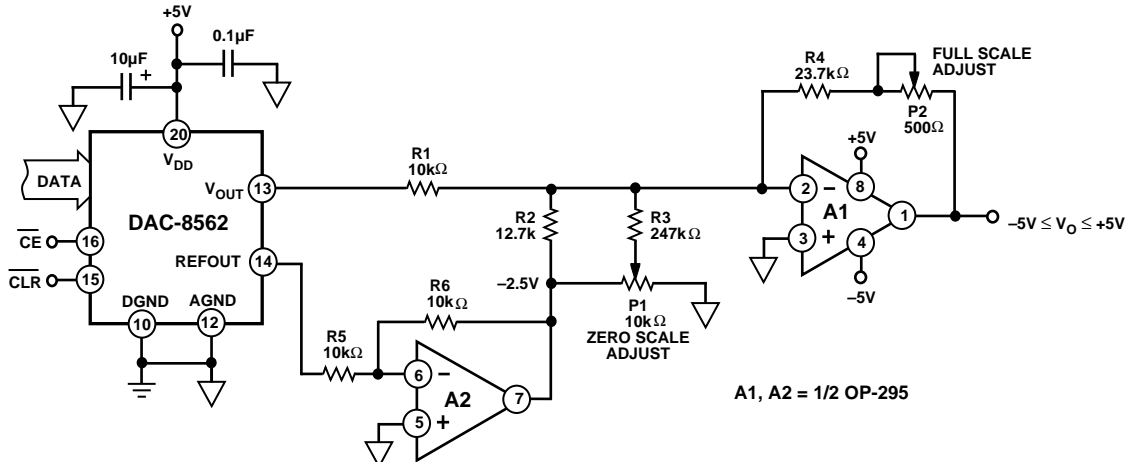


Figure 33. Bipolar Output Operation

Bipolar Output Operation

Although the DAC8562 has been designed for single supply operation, bipolar operation is achievable using the circuit illustrated in Figure 33. The circuit uses a single supply, rail-to-rail OP295 op amp and the DAC's internal +2.5 V reference to generate the -2.5 V reference required to level-shift the DAC output voltage. The circuit has been configured to provide an output voltage in the range $-5\text{ V} \leq V_{\text{OUT}} \leq +5\text{ V}$ and is coded in complementary offset binary. Although each DAC LSB corresponds to 1 mV, each output LSB has been scaled to 2.44 mV. Table IV provides the relationship between the digital codes and output voltage.

The transfer function of the circuit is given by:

$$V_O = -1\text{ mV} \times \text{Digital Code} \times \left(\frac{R_4}{R_1} \right) + 2.5 \times \left(\frac{R_4}{R_2} \right)$$

and, for the circuit values shown, becomes:

$$V_O = -2.44\text{ mV} \times \text{Digital Code} + 5\text{ V}$$

$$V_O = 1\text{ mV} \times \text{Digital Code} \times \left(\frac{R_4}{R_3 + R_4} \right) \times \left(1 + \frac{R_2}{R_1} \right)$$

$$- \text{REFOUT} \times \left(\frac{R_2}{R_1} \right)$$

For the $\pm 2.5\text{ V}$ output range and the circuit values shown in the table, the transfer equation becomes:

$$V_O = 1.22\text{ mV} \times \text{Digital Code} - 2.5\text{ V}$$

Similarly, for the $\pm 5\text{ V}$ output range, the transfer equation becomes:

$$V_O = 2.44\text{ mV} \times \text{Digital Code} - 5\text{ V}$$

Note that, for $\pm 5\text{ V}$ output voltage operation, R5 is required as a pull-down for REFOUT. Or, REFOUT can be buffered by an op amp configured as a follower that can source and sink current.

Table IV. Bipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	-4 9976
801	2049	-2.44E-3
800	2048	0
7FF	2047	+2.44E-3
000	0	+5

To maintain monotonicity and accuracy, R1, R2, R4, R5, and R6 should be selected to match within 0.01% and must all be of the same (preferably metal foil) type to assure temperature coefficient matching. Mismatching between R1 and R2 causes offset and gain errors while an R4 to R1 and R2 mismatch yields gain errors.

For applications that do not require high accuracy, the circuit illustrated in Figure 34 can also be used to generate a bipolar output voltage. In this circuit, only one op amp is used and no potentiometers are used for offset and gain trim. The output voltage is coded in offset binary and is given by:

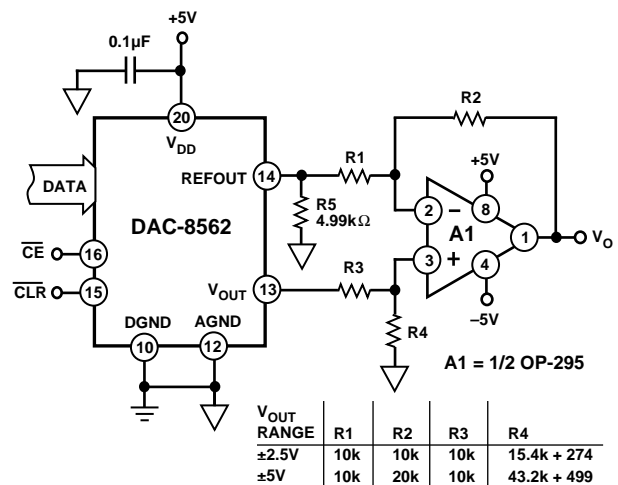


Figure 34. Bipolar Output Operation Without Trim Version 1

DAC8562

Alternatively, the output voltage can be coded in complementary offset binary using the circuit in Figure 35. This configuration eliminates the need for a pull-down resistor or an op amp for REFOUT. The transfer equation of the circuit is given by:

V_O = -1 mV × Digital Code × (R2 / R1) + REFOUT × (R4 / (R3 + R4)) × (1 + R2 / R1)

and, for the values shown, becomes:

V_O = -2.44 mV × Digital Code + 5 V

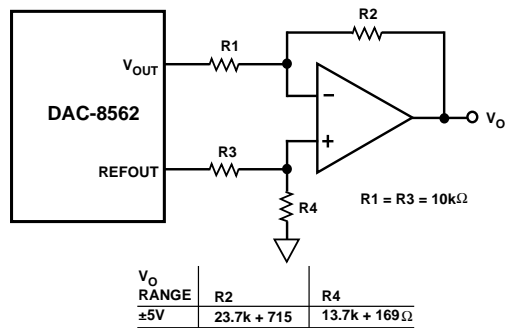


Figure 35 Bipolar Output Operation Without Trim Version 2

Generating a Negative Supply Voltage

Some applications may require bipolar output configuration, but only have a single power supply rail available. This is very common in data acquisition systems using microprocessor-based systems. In these systems, only +12 V, +15 V, and/or +5 V are available. Shown in Figure 36 is a method of generating a negative supply voltage using one CD4049, a CMOS hex inverter, operating on +12 V or +15 V. The circuit is essentially a charge pump where two of the six are used as an oscillator. For the values shown, the frequency of oscillation is approximately 3.5 kHz and is fairly insensitive to supply voltage because R1 > 2 × R2. The remaining four inverters are wired in parallel for higher output current. The square-wave output is level translated by C2 to a negative-going signal, rectified using a pair of 1N4001s, and then filtered by C3. With the values shown, the charge pump will provide an output voltage of -5 V for current loading in the range 0.5 mA ≤ I_OUT ≤ 10 mA with a +15 V supply and 0.5 mA ≤ I_OUT ≤ 7 mA with a +12 V supply.

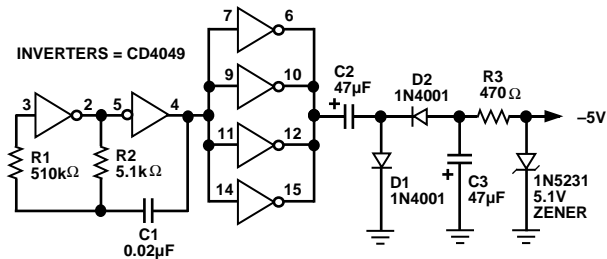


Figure 36. Generating a -5 V Supply When Only +12 V or +15 V Are Available

Audio Volume Control

The DAC8562 is well suited to control digitally the gain or attenuation of a voltage controlled amplifiers. In professional

audio mixing consoles, music synthesizers, and other audio processors, VCAs, such as the SSM2018, adjust audio channel gain and attenuation from front panel potentiometers. The VCA provides a clean gain transition control of the audio level when the slew rate of the analog input control voltage, V_C, is properly chosen. The circuit in Figure 37 illustrates a volume control application using the DAC8562 to control the attenuation of the SSM2018.

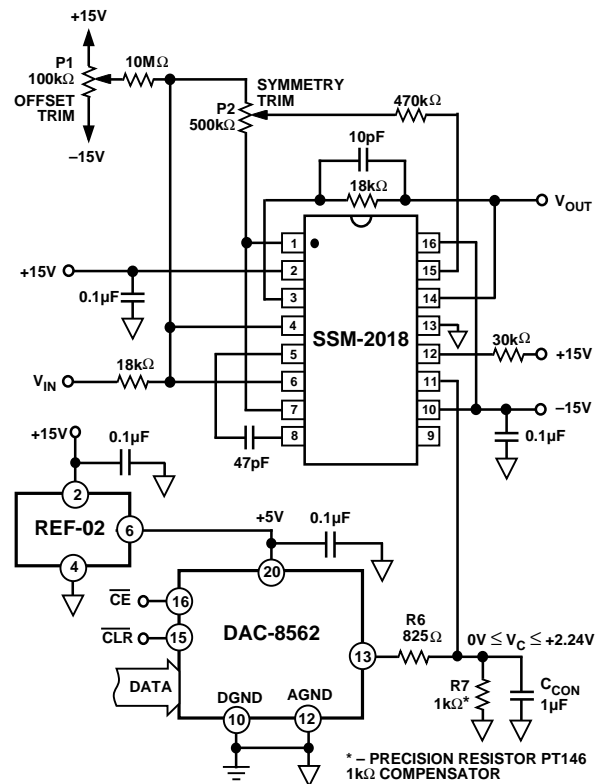


Figure 37. Audio Volume Control

Since the supply voltage available in these systems is typically ±15 V or ±18 V, a REF02 is used to supply the +5 V required to power the DAC. No trimming of the reference is required because of the reference's tight initial tolerance and low supply current consumption of the DAC8562. The SSM2018 is configured as a unity-gain buffer when its control voltage equals 0 volt. This corresponds to a 000_H code from the DAC8562. Since the SSM2018 exhibits a gain constant of -28 mV/dB (typical), the DAC's full-scale output voltage has to be scaled down by R6 and R7 to provide 80 dB of attenuation when the digital code equals FFF_H. Therefore, every DAC LSB corresponds to 0.02 dB of attenuation. Table V illustrates the attenuation versus digital code of the volume control circuit.

Table V. SSM2018 VCA Attenuation vs. DAC8562 Input Code

Hexadecimal Number in DAC Register	Control Voltage (V)	VCA Attenuation (dB)
000	0	0
400	+0.56	20
800	+1.12	40
C00	+1.68	60
FFF	+2.24	80

To compensate for the SSM2018's gain constant temperature coefficient of $-3300 \text{ ppm}/^\circ\text{C}$, a $1 \text{ k}\Omega$, temperature-sensitive resistor (R7) manufactured by the Precision Resistor Company with a temperature coefficient of $+3500 \text{ ppm}/^\circ\text{C}$ is used. A C_{CON} of $1 \mu\text{F}$ provides a control transition time of 1 ms which yields a click-free change in the audio channel attenuation. Symmetry and offset trimming details of the VCA can be found in the SSM2018 data sheet.

Information regarding the PT146 $1 \text{ k}\Omega$ "Compensator" can be obtained by contacting:

Precision Resistor Company, Incorporated
10601 75th Street North
Largo, FL 34647
(813) 541-5771

A High-Compliance, Digitally Controlled Precision Current Source

The circuit in Figure 38 shows the DAC8562 controlling a high-compliance, precision current source using an AMP05 instrumentation amplifier. The AMP05's reference pin becomes the input, and the "old" inputs now monitor the voltage across a precision current sense resistor, R_{CS} . Voltage gain is set to unity, so the transfer function is given by the following equation:

$$I_{\text{OUT}} = \frac{V_{\text{IN}}}{R_{\text{CS}}}$$

If R_{CS} equals 100Ω , the output current is limited to $+10 \text{ mA}$ with a 1 V input. Therefore, each DAC LSB corresponds to $2.4 \mu\text{A}$. If a bipolar output current is required, then the circuit in Figure 33 can be modified to drive the AMP05's reference pin with a $\pm 1 \text{ V}$ input signal.

Potentiometer P1 trims the output current to zero with the input at 0 V . Fine gain adjustment can be accomplished by adjusting R1 or R2.

A Digitally Programmable Window Detector

A digitally programmable, upper/lower limit detector using two DAC8562s is shown in Figure 39. The required upper and

lower limits for the test are loaded into each DAC individually by controlling HDAC/LDAC. If a signal at the test input is not within the programmed limits, the output will indicate a logic zero which will turn the red LED on.

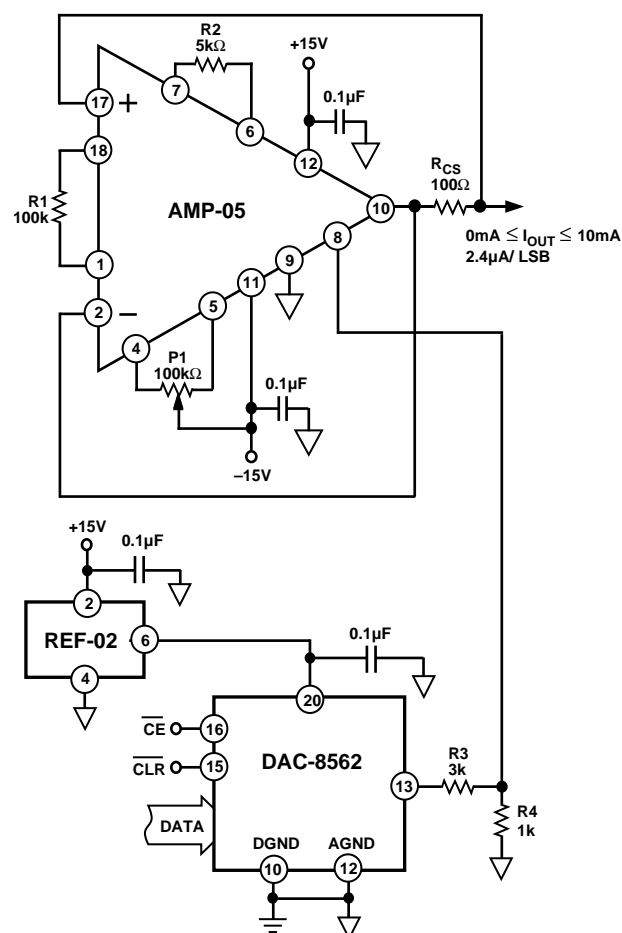


Figure 38. A High-Compliance, Digitally Controlled Precision Current Source

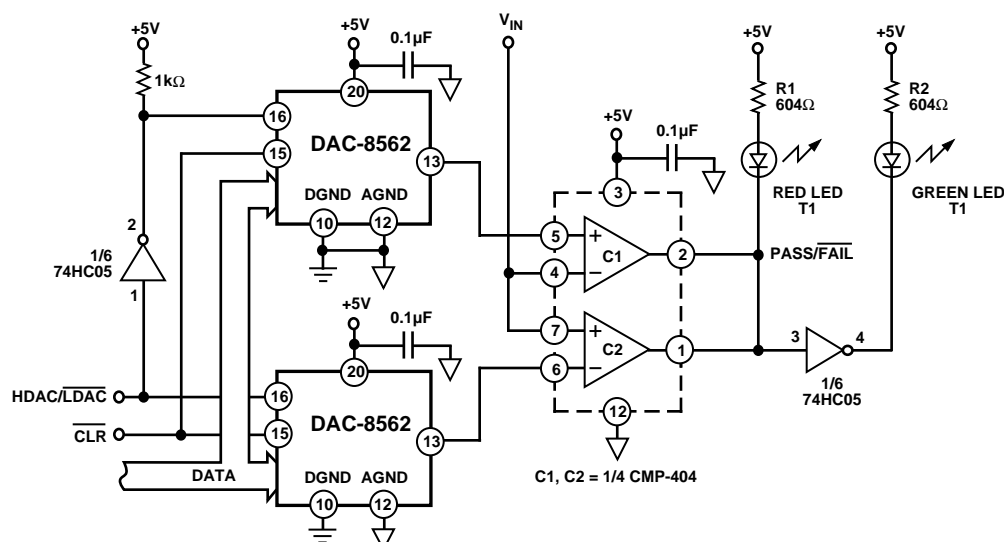


Figure 39. A Digitally Programmable Window Detector

DAC8562

Decoding Multiple DAC8562s

The \overline{CE} function of the DAC8562 can be used in applications to decode a number of DACs. In this application, all DACs receive the same input data; however, only one of the DACs' \overline{CE} input is asserted to transfer its parallel input register contents into the DAC. In this circuit, shown in Figure 40, the \overline{CE} timing is generated by a 74HC139 decoder and should follow the DAC8562's standard timing requirements. To prevent timing errors, the 74HC139 should not be activated by its \overline{ENABLE} input while the coded address inputs are changing. A simple timing circuit, R1 and C1, connected to the DACs' \overline{CLR} pins resets all DAC outputs to zero during power-up.

MICROPROCESSOR INTERFACING DAC-8562-MC68HC11 INTERFACE

The circuit illustrated in Figure 41 shows a parallel interface between the DAC8562 and a popular 8-bit microcontroller, the M68HC11, which is configured in a single-chip operating mode. The interface circuit consists of a pair of 74ACT11373 transparent latches and an inverter. The data is loaded into the latches in two 8-bit bytes; the first byte contains the four most significant bits, and the lower 8 bits are in the second byte. Data is taken from the microcontroller's port B output lines, and three interface control lines, \overline{CLR} , \overline{CE} , and MSB/LSB, are controlled by the M68HC11's PC2, PC1, and PC0 output lines, respectively. To transfer data into the DAC, PC0 is set, enabling U1's outputs. The first data byte is loaded into U1 where the four least significant bits of the byte are connected to MSB-DB8. PC0 is then cleared; this latches U1's inputs and enables U2's outputs. U2's outputs now become DB7-DB0. The DAC output is updated with the contents of U1 and U2.

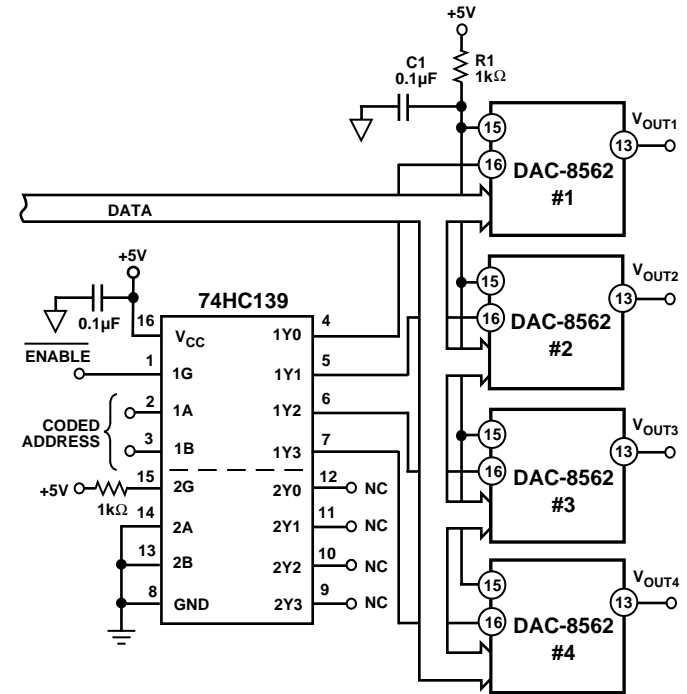


Figure 40. Decoding Multiple DAC8562s Using the \overline{CE} Pin

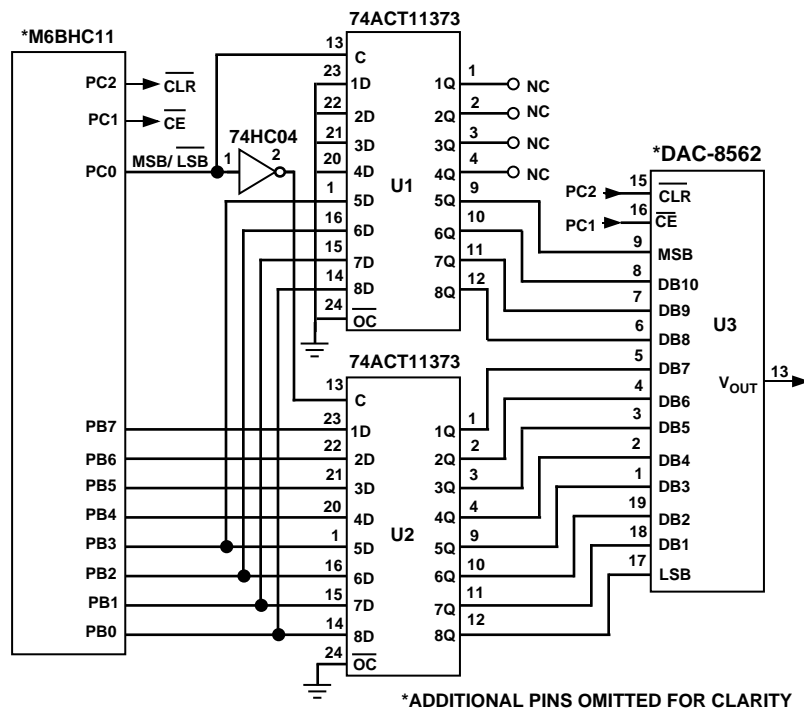


Figure 41. DAC8562 to MC68HC11 Interface

DAC8562 – M68HC11 Interface Program Source Code

```

*
* DAC8562 to M68HC11 Interface Assembly Program
* Adolfo A. Garcia
* September 14, 1992
*
* M68HC11 Register definitions
*
PORTB EQU $1004
PORTC EQU $1003      Port C control register
                        "0,0,0,0;CLR/,CE/,MSB-LSB/"
DDRC EQU $1007      Port C data direction
*
* RAM variables:
* MSBS are encoded from 0 (Hex) to F (Hex)
* LSBS are encoded from 00 (Hex) to F (Hex)
* DAC requires two 8-bit loads
*
MSBS EQU $00      Hi-byte: "0,0,0,0;MSB,DB10,DB9,DB8"
LSBS EQU $01      Lo-byte: "DB7,DB6,DB5,DB4;DB3,DB2,
                    DB1,DB0"
*
* Main Program
*
ORG $C000      Start of user's RAM in EVB
INIT LDS #$CFFF Top of C page RAM
*
* Initialize Port C Outputs
*
LDAA #$07      0,0,0,0;0,1,1,1
STAA DDRC      CLR/,CE/, and MSB-LSB/ are now enabled
                as outputs
LDAA #$06      0,0,0,0;0,1,1,0
* STAA PORTC    CLR/-Hi, CE/-Hi, MSB-LSB/-Lo
                Initialize Port C Outputs
*
* Call update subroutine
*
BSR UPDATE      Xfer 2 8-bit words to DAC8562
JMP $E000      Restart BUFFALO
*
* Subroutine UPDATE
*
UPDATE PSHX      Save registers X, Y, and A
PSHY
PSHA
*
* Enter contents of the Hi-byte input register
*
LDAA #$0A      0,0,0,0;1,0,1,0
STAA MSBS      MSBS are set to 0A (Hex)
*
* Enter Contents of Lo-byte input register
*
LDAA #$AA      1,0,1,0;1,0,1,0
STAA LSBS      LSBS are set to AA (Hex)
*
LDX #MSBS      Stack pointer at 1st byte to send via Port B
LDY #$1000     Stack pointer at on-chip registers
*
* Clear DAC output to zero
*
BCLR PORTC,Y $04 Assert CLR/
BSET PORTC,Y $04 De-assert CLR/
*
* Loading input buffer latches
*
TFRLP BSET PORTC,Y $01 Set hi-byte register load
LDAA 0,X      Get a byte to transfer via Port B
STAA PORTB    Write data to input register
INX          Increment counter to next byte for transfer
CPX #LSBS+1   Are we done yet ?
BEQ DUMP      If yes, update DAC output
BCLR PORTC,Y $01 Latch hi-byte register and set lo-byte register
                load
BRA TFRLP
*

```

DAC8562-M68HC11 Interface Program Source Code (Continued)

```

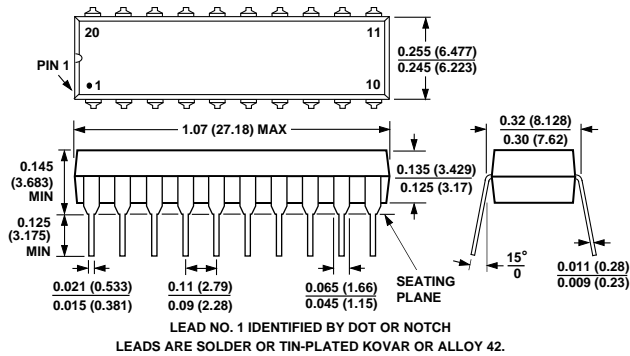
* Update DAC output with contents of input registers
*
DUMP BCLR PORTC,Y $02 Assert CE/
      BSET PORTC,Y $02 Latch DAC register
*
      PULA          When done, restore registers X, Y & A
      PULY
      PULX
      RTS          ** Return to Main Program **

```

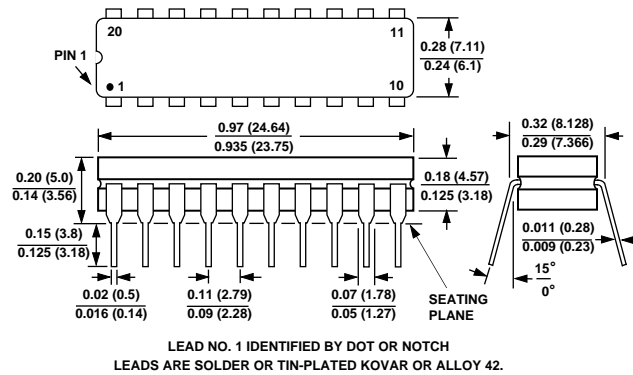

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Pin Plastic DIP (P-Suffix)



20-Pin Cerdip (R-Suffix)



20-Lead SOIC (S-Suffix)

