Micropower 8-Bit Current Output D/A Converter

FEATURES

- **Guaranteed Precision Full-Scale DAC Output Current at 25°C:**
  - LTC1329A-50 50μA ±1%
  - LTC1329-10 10μA ±3%
  - LTC1329-50 50μA ±3%
- Wide Output Voltage DC Compliance: –15V to 2.5V
- Wide Supply Range: 2.7V ≤ V_{CC} ≤ 6.5V
- Supply Current in Shutdown: 0.2μA
- Low Supply Current: 75μA for LTC1329-10, 95μA for LTC1329-50/LTC1329A-50
- Available in 8-Pin SO
- Triple Mode™ Interface Modes
  1. Standard 3-Wire Mode
  2. Pulse Mode 1-Wire Interface: Increment-Only
  3. Pulse Mode 2-Wire Interface: Increment/Decrement
- Can Read Back the 8-Bit DAC Value in 3-Wire Mode
- DAC Powers Up at Midrange
- **DAC Contents Are Retained in Shutdown**

APPLICATIONS

- LCD Contrast Control
- Backlight Brightness Control
- Battery Charger Current/Voltage Adjustment
- Power Supply Voltage Adjustment
- Trimmer Pot Elimination

DESCRIPTION

The LTC®1329-10/LTC1329-50/LTC1329A-50 are micropower 8-bit current output D/A converters (DACs) with an output range of 0μA to 10μA for the LTC1329-10 and 0μA to 50μA for the LTC1329-50/LTC1329A-50. The DAC current output can be biased from –15V to 2V or –15V to 2.5V in 3.3V and 5V systems, respectively. Supply current is only 95μA for the LTC1329-50/LTC1329A-50 and 75μA for LTC1329-10. A shutdown mode drops the supply current to 0.2μA.

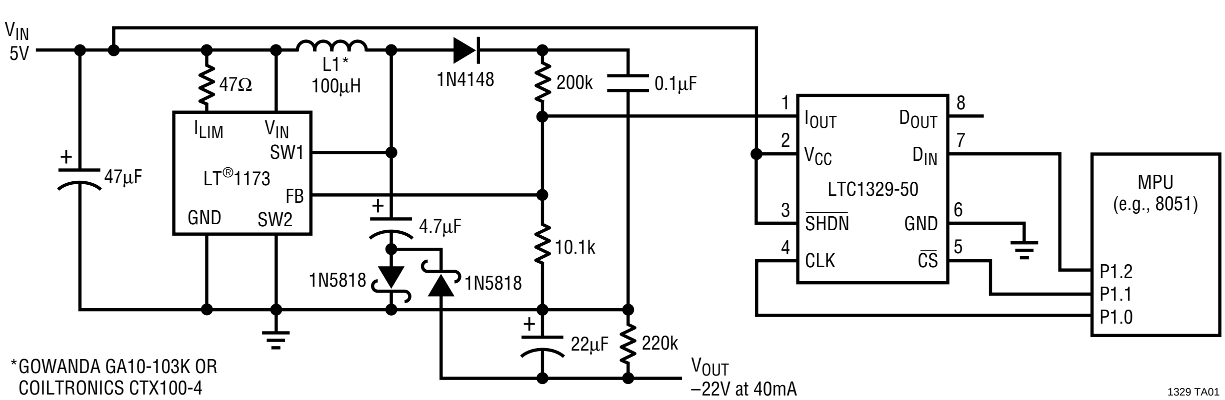
The LTC1329 can communicate with external circuitry by using one of three interface modes: standard 3-wire serial mode and two pulse modes. Upon power-up, the internal counter resets to 1000 0000B, the DAC output assumes midrange and the chip is configured in 3-wire or pulse mode depending on the signal level at $\overline{CS}$.

In 3-wire mode, the system MPU can serially transfer 8-bit data to and from the LTC1329. In pulse mode, the upper six bits of the DAC output can be programmed for increment-only (1-wire interface) or increment/decrement (2-wire interface) operation depending on the signal level at D_{IN}.

LTC1329 is available in 8-pin SO packages.

TYPICAL APPLICATION

Digitally Controlled LCD Bias Generator

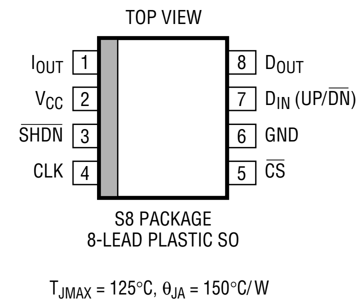


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage (All Inputs)............ −0.3V to (V_{CC} + 0.3V)
Output Voltage
  I_{OUT} .... −15V to (V_{CC} + 0.3V)
  D_{OUT} .... −0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration (All Outputs) .... Indefinite
Operating Temperature Range .... 0°C to 70°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec).................. 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1329CS8-10 LTC1329CS8-50 LTC1329ACS8-50
S8 PART MARKING
13291 1329A5 13295

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS **V_{CC} = 3.3V, T_A = 25°C, unless otherwise specified.**

SYMBOL	PARAMETER	CONDITIONS		LTC1329-10 MIN	TYP	MAX	LTC1329-50/LTC1329A-50 MIN	TYP	MAX	UNITS
V_{CC}			●	2.7		6.5	2.7		6.5	V
I_{CC}	Supply Current	$V_{\overline{SHDN}}$ = V_{DIN} = $V_{\overline{CS}}$ = V_{CC}, V_{CLK} = 0V, D_{OUT} = NC, I_{OUT} = NC	●		75	130		95	150	µA
		Shutdown	●		0.2	5		0.2	5	µA
	DAC Resolution				8			8		Bits
	DAC Full-Scale Current	Output Voltage at I_{OUT} = 0.45V, T_A = 25°C		9.7	10	10.3	48.5	50	51.5	µA
		(LTC1329-10, LTC1329-50)	●	9.5	10	10.5	47.5	50	52.5	µA
		Output Voltage at I_{OUT} = 0.45V, T_A = 25°C					49.5	50	50.5	µA
		(LTC1329A-50)	●				49.0	50	51.0	µA
	DAC Zero-Scale Current	Output Voltage at I_{OUT} = 0.45V	●			200			200	nA
	DAC Differential Nonlinearity	Monotonicity Guaranteed	●		±0.3	±0.9			±0.9	LSB
	Supply Voltage Rejection	V_{CC} = 3V to 5.5V, I_{OUT} = Full Scale, Output Voltage at I_{OUT} = 0.45V	●		±1	±2		±1	±2	LSB
		V_{CC} = 2.7V to 6.5V, Full Scale, Output Voltage at I_{OUT} = 0.45V	●		±2.5	±4		±2.5	±4	LSB
	Output Voltage Rejection	V_{CC} = 5V, I_{OUT} = Full Scale, Output Voltage at I_{OUT} = –15V to 0V	●		±0.25	±1			±0.25	LSB
		V_{CC} = 5V, I_{OUT} = Full Scale, Output Voltage at I_{OUT} = 0V to 2.5V	●			±1.5			±1.5	LSB
I_{IH}, I_{IL}	Logic Input Current	0V ≤ V_{IN} ≤ V_{CC}	●			±1			±1	µA
V_{IH}	High Level Input Voltage	V_{CC} = 5V	●	2.0			2.0			V
		V_{CC} = 3.3V	●	1.9			1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 5V	●			0.80			0.80	V
		V_{CC} = 3.3V	●			0.45			0.45	V
V_{OH}	High Level Output Voltage	V_{CC} = 5V, I_O = 400µA	●	2.4			2.4			V
		V_{CC} = 3.3V, I_O = 400µA	●	2.1			2.1			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5V, I_O = 2mA	●			0.4			0.4	V
		V_{CC} = 3.3V, I_O = 1mA	●			0.4			0.4	V
I_{OZ}	Three-State Output Leakage	$V_{\overline{CS}}$ = V_{CC}	●			±5			±5	µA

LINEAR TECHNOLOGY

RECOMMENDED OPERATING CONDITIONS V_{CC} = 3.3V, unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Serial Interface							
f_{CLK}	Clock Frequency		●			2	MHz
t_{CKS}	Setup Time, CLK↓ Before $\overline{CS}$↓		●	150			ns
$t_{\overline{CS}S}$	Setup Time, $\overline{CS}$↓ Before CLK↑		●	400			ns
t_{DV}	$\overline{CS}$↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{DS}	D_{IN} Setup Time Before CLK↑		●	150			ns
t_{DH}	D_{IN} Hold Time After CLK↑		●	150			ns
t_{DO}	CLK↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{CKHI}	CLK High Time		●	200			ns
t_{CKLO}	CLK Low Time		●	250			ns
$t_{\overline{CS}H}$	CLK↓ Before $\overline{CS}$↑		●	150			ns
t_{DZ}	$\overline{CS}$↑ to D_{OUT} in Hi-Z	See Test Circuits	●			400	ns
t_{CKH}	$\overline{CS}$↑ Before CLK↑		●			400	ns
$t_{\overline{CS}LO}$	$\overline{CS}$ Low Time	f_{CLK} = 2MHz (Note 4) V_{CLK} = 0V	● ●	4550 400			ns ns
$t_{\overline{CS}HI}$	$\overline{CS}$ High Time		●	400			ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

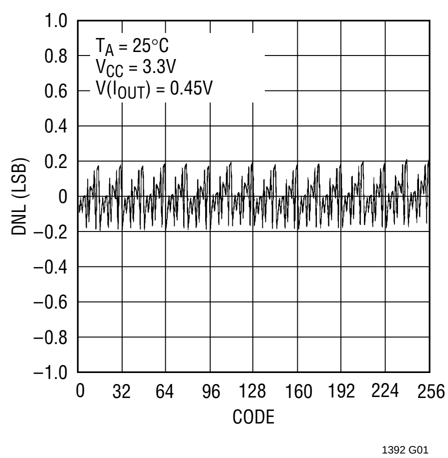
Note 2: Timing for all input signals is measured at 0.8V for a High-to-Low transition and at 2V for a Low-to-High transition.

Note 3: Timing specification are guaranteed but not tested.

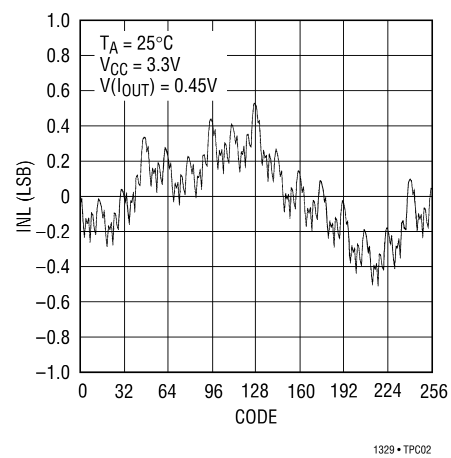
Note 4: This is the minimum time required for valid data transfer.

TYPICAL PERFORMANCE CHARACTERISTICS

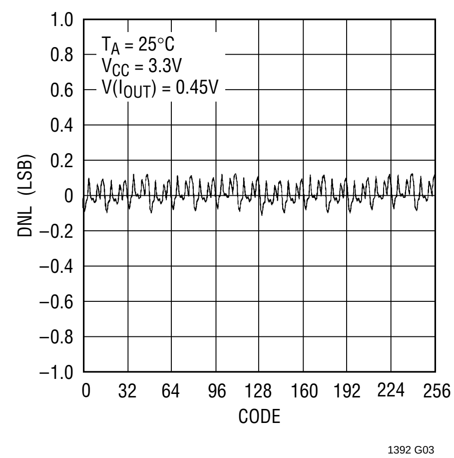
LTC1329-10 DNL vs Code



LTC1329-10 INL vs Code

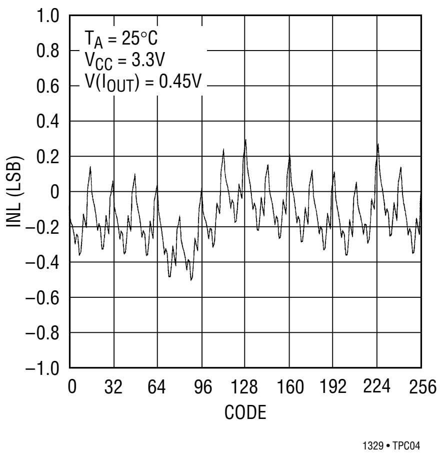


LTC1329-50 DNL vs Code

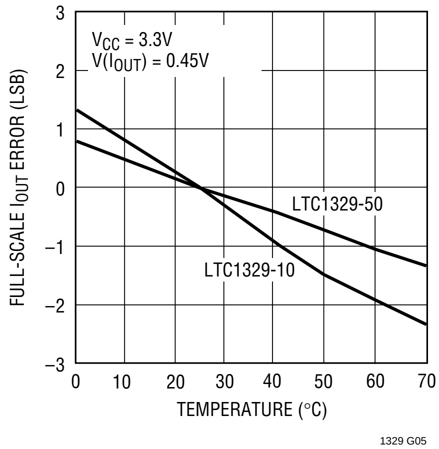


TYPICAL PERFORMANCE CHARACTERISTICS

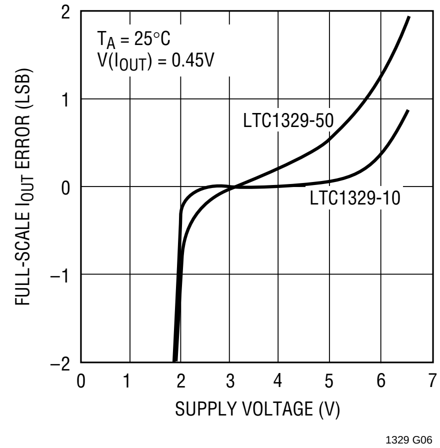
LTC1329-50 INL vs Code



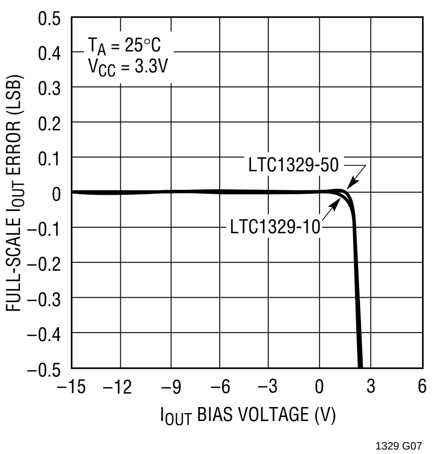
LTC1329-10/LTC1329-50 Full-Scale Current vs Temperature



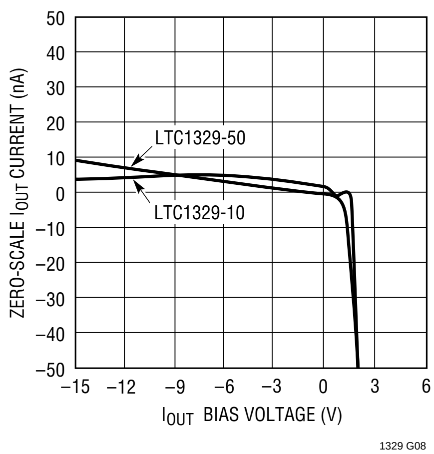
LTC1329-10/LTC1329-50 Supply Voltage Rejection



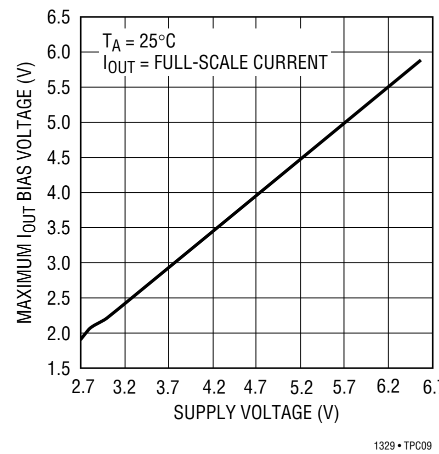
LTC1329-10/LTC1329-50 Bias Voltage Rejection (Full-Scale Current)



LTC1329-10/LTC1329-50 Bias Voltage Rejection (Zero-Scale Current)



Maximum I_{OUT} Bias Voltage vs Supply Voltage



PIN FUNCTIONS

I_{OUT} (Pin 1): DAC Current Output. In 3.3V or 5V systems, the DAC current output can be biased from –15V to 2V or –15V to 2.5V respectively.

V_{CC} (Pin 2): Voltage Supply (2.7V ≤ V_{CC} ≤ 6.5V). This supply must be kept free from noise and ripple by bypassing directly to the ground plane.

$\overline{\text{SHDN}}$ (Pin 3): Shutdown. A logic low puts the chip into Shutdown mode. The digital setting for the DAC is retained.

CLK (Pin 4): Shift Clock. This clock synchronizes the serial data in 3-wire mode. This pin has a Schmitt trigger input.

$\overline{\text{CS}}$ (Pin 5): Chip Select Input. In 3-wire mode, a logic low on this $\overline{\text{CS}}$ pin enables the LTC1329. Upon power-up, a logic high at $\overline{\text{CS}}$ puts the chip into pulse mode. If $\overline{\text{CS}}$ ever goes low, the chip is configured in 3-wire mode until the next power is cycled.

GND (Pin 6): Ground. Ground should be tied directly to a ground plane.

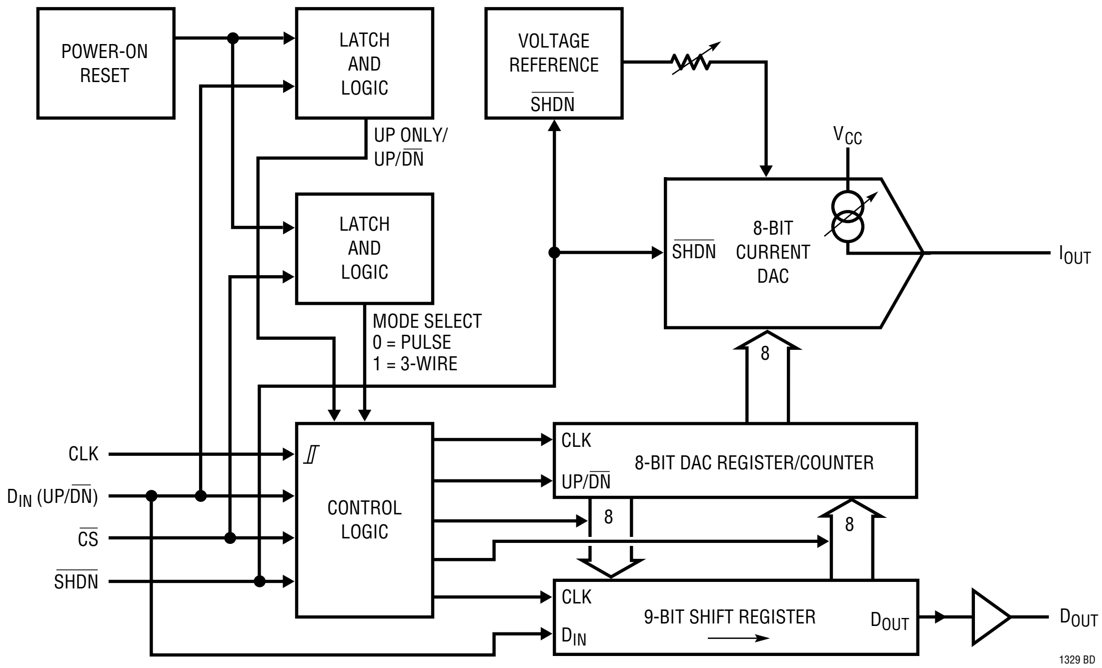
D_{IN} (UP/$\overline{\text{DN}}$)(Pin 7): Data Input. In 3-wire mode, the DAC data is shifted into D_{IN} on the rising edge of CLK. In pulse mode, upon power-up a logic high at D_{IN} puts the counter into increment-only mode. If D_{IN} ever goes low, the

PIN FUNCTIONS

counter is configured in increment/decrement mode until the power is cycled.

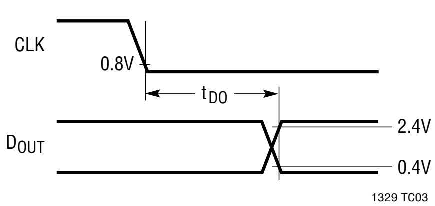
D_{OUT} (Pin 8): Data Output. In 3-wire mode, on every conversion D_{OUT} serially outputs the previous 8-bit DAC data. In pulse mode, D_{OUT} is three-stated.

BLOCK DIAGRAM

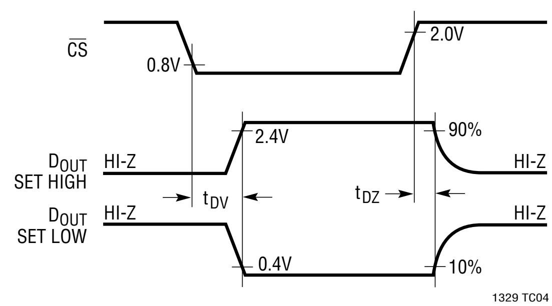


TEST CIRCUITS

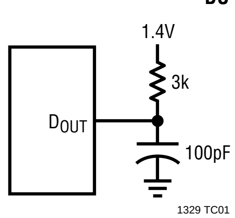
Voltage Waveforms for t_{DO}



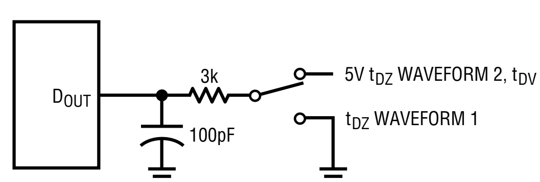
Voltage Waveforms for t_{DZ}, t_{DV}



Load Circuit for t_{DO}



Load Circuit for t_{DZ}, t_{DV}



SERIAL I/O OPERATING SEQUENCE

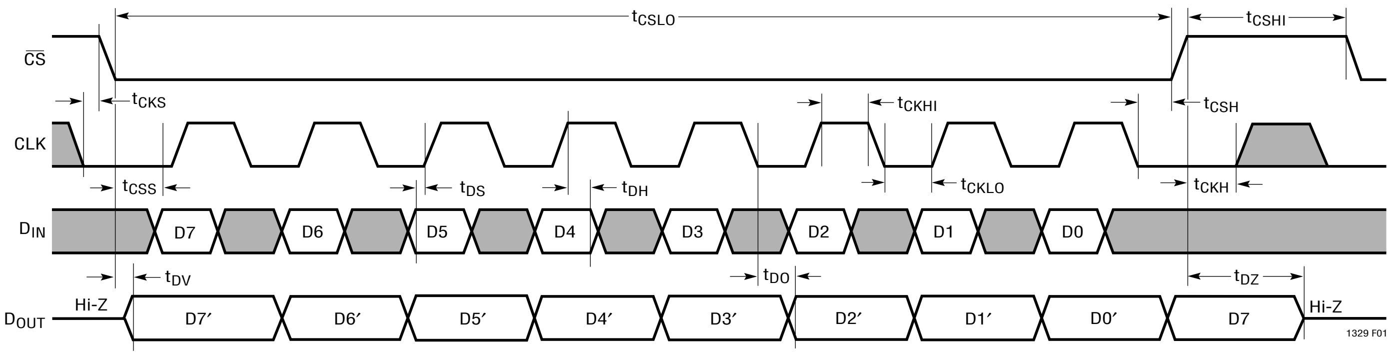


Figure 1. 3-Wire Interface Timing Specification

APPLICATIONS INFORMATION

8-BIT CURRENT OUTPUT DAC

The LTC1329-10/LTC1329-50/LTC1329A-50 are 8-bit, current output digital-to-analog (DAC) converters. For each part, the 8-bit DAC output is guaranteed monotonic and is digitally adjustable in 256 equal steps. Upon power up, the internal DAC register resets to 10000000B and the DAC output assumes midrange. The current output (I_{OUT}) can be biased from –15V to 2V or –15V to 2.5V in 3.3V and 5V systems, respectively. The LTC1329-10 features a full-scale output of 10µA trimmed to ±3% at room temperature (±5% over temperature), while the LTC1329-50 features a 50µA full scale and two accuracy grades; ±1% at room temperature (±2% over temperature) for the LTC1329A-50 and ±3% at room temperature (±5% over temperature) for the LTC1329-50. All versions include a flexible serial digital interface which allows easy interconnection to a variety of digital systems.

DIGITAL INTERFACE

Automatic Mode Selection

The LTC1329 family includes a serial interface capable of communicating with the host system using one of three protocols; standard 3-wire mode, a 2-wire up/down pulse mode and a 1-wire increment-only pulse mode. The LTC1329 family is designed to auto-configure itself depending on the way data is presented to it. A diagram illustrating this auto detection behavior is shown in Figure 2. At power-up, the interface is set to 1-wire pulse mode.

If the $\overline{CS}$ line ever goes low (as it will at the beginning of a valid 3-wire serial transfer) the chip immediately reconfigures itself into 3-wire mode and remains in this mode until the next time the power is cycled. If $\overline{CS}$ stays high, the LTC1329 family stays in pulse mode and watches the UP/$\overline{DN}$ pin to determine whether to switch to 2-wire mode. If UP/$\overline{DN}$ ever goes low (as it will the first time a "down" command is given) the chip switches into 2-wire pulse mode and remains in this mode until the next time the power is cycled. In a properly configured 1-wire system, $\overline{CS}$ and UP/$\overline{DN}$ will stay high continuously and the LTC1329-10/LTC1329-50/LTC1329A-50 will remain in 1-wire pulse mode. 2-wire pulse mode systems should give a single "down" pulse sometime before the first data pulses are sent to prevent the LTC1329 family from staying in 1-wire mode if the first several pulses happen to be "ups".

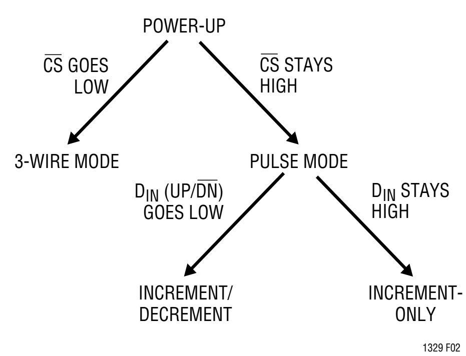


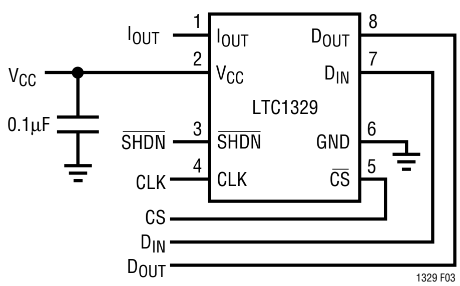
Figure 2. LTC1329 Operating Modes

APPLICATIONS INFORMATION

Standard 3-Wire Mode (Figure 3)

Refer to the Serial Interface Operating Sequence in Figure 1. When operating in 3-wire mode, the LTC1329-10/LTC1329-50/LTC1329A-50 will interface directly with most standard 3- or 4-wire serial interface systems. The clock (CLK) input synchronizes the data transfer with each input bit captured at the rising edge of CLK and each output data bit shifted out through D_{OUT} at the falling edge. A falling edge at $\overline{CS}$ initiates the data transfer and brings the D_{OUT} pin out of three-state. The serial 8-bit data representing the new DAC setting is shifted into the D_{IN} pin. Simultaneously, the previous DAC setting is shifted out of the D_{OUT} pin. After the new data is shifted in, a rising edge at $\overline{CS}$ transfers the data from the input shift register into the DAC register. The DAC output assumes the new value and the D_{OUT} pin returns to a high-impedance state.

$$I_{OUT} = (B7\ B6\ B5\ B4\ B3\ B2\ B1\ B0)I_{FULLSCALE}/255$$



D_{IN} AND D_{OUT} CAN BE TIED TOGETHER
FOR HALF DUPLEX DATA TRANSFER

Figure 3. 3-Wire Mode; Serial Interface (3-Wire Control by $\overline{CS}$, CLK and D_{IN})

1-Wire Interface (Pulse Mode, Figure 4)

In 1-wire pulse mode, each rising edge at CLK increments the upper six bits of the DAC register by one count. When incramented beyond 11111100B, the counter rolls over and sets the DAC to the minimum value (00000000B). In this way, a single pulse applied to CLK increases the DAC output by a single 4-LSB step and 63 pulses decrease the DAC output by one step. The last two LSBs are always zero in pulse mode.

$$I_{OUT} = (B7\ B6\ B5\ B4\ B3\ B2\ 0\ 0)I_{FULLSCALE}/255$$

To configure the LTC1329-10/LTC1329-50/LTC1329A-50 in 1-wire pulse mode, tie both the $\overline{CS}$ and D_{IN} pins to V_{CC}.

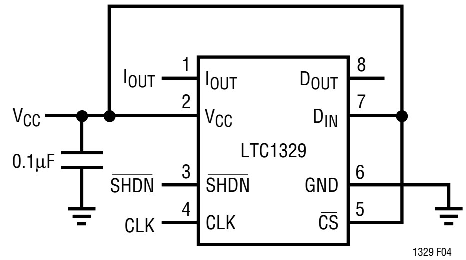


Figure 4. Pulse Mode: Increment Only (1-Wire Control by CLK)

2-Wire Interface (Pulse Mode, Figure 5)

In 2-wire pulse mode, a logic HIGH at UP/$\overline{DN}$ programs the DAC register to increment and each rising edge at CLK increments the upper six bits of the register by one count. Similarly, a logic LOW at UP/$\overline{DN}$ set the DAC register to decrement and a rising edge at CLK decrements the upper six bits of the register by one count. Each count in 2-wire mode changes the DAC output by a single four LSB step. The DAC register stops incramenting at 11111100B and stops decrementing at 00000000B and will not roll over in 2-wire pulse mode. The last two LSBs are always zero in pulse mode.

$$I_{OUT} = (B7\ B6\ B5\ B4\ B3\ B2\ 0\ 0)I_{FULLSCALE}/255$$

To configure the LTC1329-10/LTC1329-50/LTC1329A-50 in 2-wire pulse mode, tie $\overline{CS}$ to V_{CC} and bring the UP/$\overline{DN}$ pin low at least once during power-up.

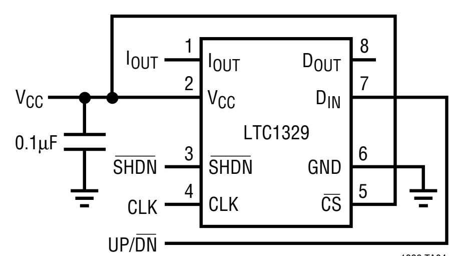
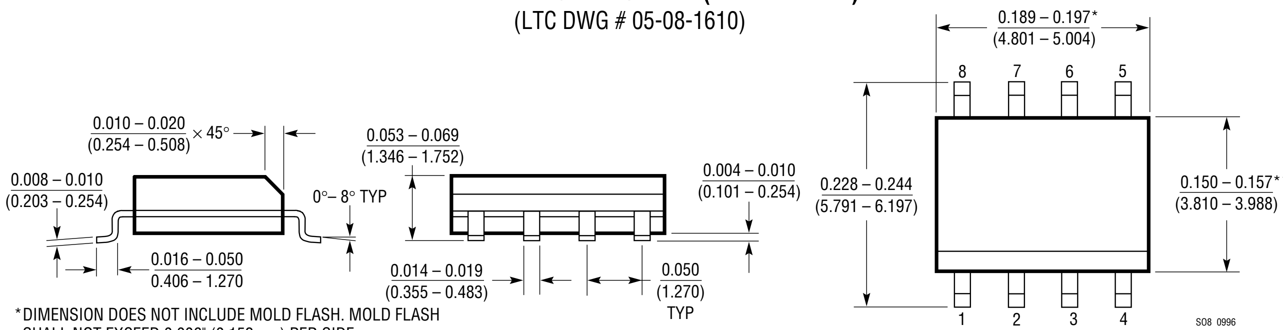


Figure 5. Pulse Mode; Increment/Decrement (2-Wire Control by CLK and UP/$\overline{DN}$)

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

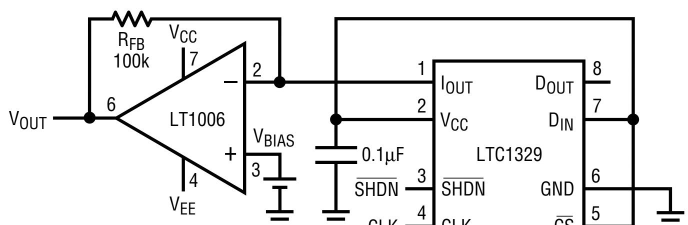
S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATIONS

Pulse Mode: Increment-Only
(1-Wire Control by CLK) with Voltage Output

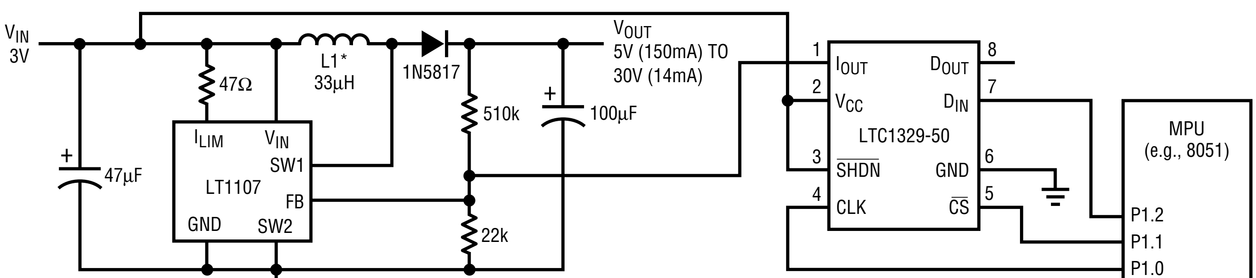


$V_{OUT} = (-I_{OUT})(R_{FB} + V_{BIAS})$
$V_{EE} < V_{BIAS} + V_{OUT}$

FOR V_{CC} = 3.3V, $-15V \le V_{BIAS} \le 2V$
FOR V_{CC} = 5V, $-15V \le V_{BIAS} \le 2.5V$

1329 TA02

Digitally Controlled Power Supply Adjustment



*COILTRONICS CTX33-4

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1451	12-Bit Micropower Serial Input V_{OUT} DAC	Higher Resolution, 8-Pin SO
LTC1452	12-Bit Multiplying Serial Input V_{OUT} DAC	Higher Resolution, 8-Pin SO
LTC8043	12-Bit Multiplying Serial Input I_{OUT} DAC	Higher Resolution, 8-Pin SO

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417 • (408) 432-1900
FAX: (408) 434-0507 • TELEX: 499-3977 • www.linear-tech.com

1329f LT/TP 0297 5K • PRINTED IN USA

LINEAR TECHNOLOGY