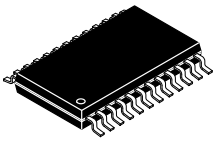
CAT5261

Dual Digitally Programmable Potentiometers (DPP™) with 256 Taps and SPI Interface

ON Semiconductor®

http://onsemi.com



TSSOP−24
Y SUFFIX
CASE 948AR

SOIC−24
W SUFFIX
CASE 751BK

Description

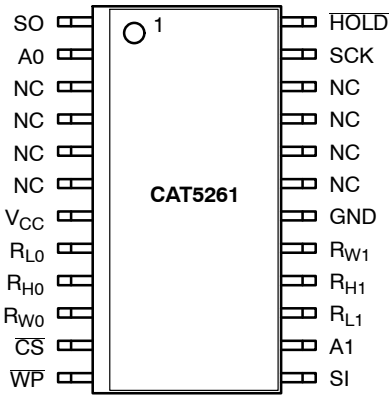
The CAT5261 is two Digitally Programmable Potentiometers (DPPs™) integrated with control logic and 8 bytes of NVRAM memory. Each DPP consists of a series of resistive elements connected between two externally accessible end points. The tap points between each resistive element are connected to the wiper outputs with CMOS switches. A separate 8−bit control register (WCR) independently controls the wiper tap switches for each DPP. Associated with each wiper control register are four 8−bit non−volatile memory data registers (DR) used for storing up to four wiper settings. Writing to the wiper control register or any of the non−volatile data registers is via a SPI serial bus. On power−up, the contents of the first data register (DR0) for each of the potentiometers is automatically loaded into its respective wiper control register.

The CAT5261 can be used as a potentiometer or as a two terminal, variable resistor. It is intended for circuit level or system level adjustments in a wide variety of applications. It is available in the −40°C to 85°C industrial operating temperature range and offered in a 24−lead SOIC and TSSOP package.

Features

- Two Linear−taper Digitally Programmable Potentiometers
- 256 Resistor Taps per Potentiometer
- End to End Resistance 50 kΩ or 100 kΩ
- Potentiometer Control and Memory Access via SPI Interface
- Low Wiper Resistance, Typically 100 Ω
- Nonvolatile Memory Storage for up to Four Wiper Settings for Each Potentiometer
- Automatic Recall of Saved Wiper Settings at Power Up
- 2.5 to 6.0 Volt Operation
- Standby Current less than 1 μA
- 1,000,000 Nonvolatile WRITE Cycles
- 100 Year Nonvolatile Memory Data Retention
- 24−lead SOIC and 24−lead TSSOP
- Industrial Temperature Range
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

PIN CONNECTIONS



SOIC−24 (W)
TSSOP−24 (Y)
(Top View)

ORDERING INFORMATION

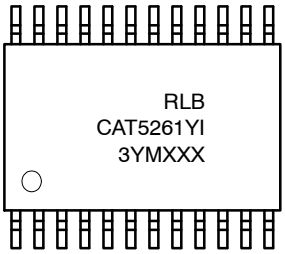
See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

MARKING DIAGRAMS

(SOIC−24)

L = Assembly Location
3 = Lead Finish − Matte−Tin
B = Product Revision (Fixed as “B”)
CAT = Fixed as “CAT”
5261W = Device Code
T = Temperature Range (I = Industrial)
− = Dash
RR = Resistance
  25 = 2.5 KΩ
  10 = 10 KΩ
  50 = 50 KΩ
  00 = 100 KΩ
Y = Production Year (Last Digit)
M = Production Month (1-9, O, N, D)
XXXX = Last Four Digits of Assembly Lot Number

(TSSOP−24)



R = Resistance
  1 = 2.5 KΩ
  2 = 10 KΩ
  4 = 50 KΩ
  5 = 100 KΩ
L = Assembly Location
B = Product Revision (Fixed as “B”)
CAT5261Y = Device Code
I = Temperature Range (I = Industrial)
3 = Lead Finish − Matte−Tin
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number

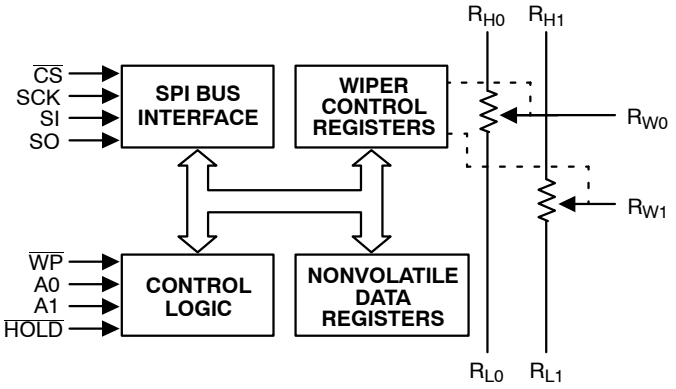


Figure 1. Functional Diagram

Table 1. PIN DESCRIPTIONS

Pin #	Name	Function
1	SO	Serial Data Output
2	A0	Device Address, LSB
3	NC	No Connect
4	NC	No Connect
5	NC	No Connect
6	NC	No Connect
7	V_{CC}	Supply Voltage
8	R_{L0}	Low Reference Terminal for Potentiometer 0
9	R_{H0}	High Reference Terminal for Potentiometer 0
10	R_{W0}	Wiper Terminal for Potentiometer 0
11	$\overline{CS}$	Chip Select
12	$\overline{WP}$	Write Protection
13	SI	Serial Input
14	A1	Device Address
15	R_{L1}	Low Reference Terminal for Potentiometer 1
16	R_{H1}	High Reference Terminal for Potentiometer 1
17	R_{W1}	Wiper Terminal for Potentiometer 1
18	GND	Ground
19	NC	No Connect
20	NC	No Connect
21	NC	No Connect
22	NC	No Connect
23	SCK	Bus Serial Clock
24	$\overline{HOLD}$	Hold

Pin Descriptions

SI: Serial Input

SI is the serial data input pin. This pin is used to input all opcodes, byte addresses and data to be written to the CAT5261. Input data is latched on the rising edge of the serial clock.

SO: Serial Output

SO is the serial data output pin. This pin is used to transfer data out of the CAT5261. During a read cycle, data is shifted out on the falling edge of the serial clock.

SCK: Serial Clock

SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the CAT5261. Opcodes, byte addresses or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK.

A0, A1: Device Address Inputs

These inputs set the device address when addressing multiple devices. A total of four devices can be addressed on a single bus. A match in the slave address must be made with the address input in order to initiate communication with the CAT5261.

R_H, R_L: Resistor End Points

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W: Wiper

The RW pins are equivalent to the wiper terminal of a mechanical potentiometer.

$\overline{CS}$: Chip Select

$\overline{CS}$ is the Chip select pin. $\overline{CS}$ low enables the CAT5261 and $\overline{CS}$ high disables the CAT5261. $\overline{CS}$ high takes the SO output pin to high impedance and forces the devices into a Standby mode (unless an internal write operation is underway). The CAT5261 draws ZERO current in the Standby mode. A high to low transition on $\overline{CS}$ is required prior to any sequence being initiated. A low to high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle.

$\overline{WP}$: Write Protect

$\overline{WP}$ is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When $\overline{WP}$ is tied low, all non−volatile write operations to the Data registers are inhibited (change of wiper control register is allowed). $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the registers. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation.

$\overline{HOLD}$: Hold

The $\overline{HOLD}$ pin is used to pause transmission to the CAT5261 while in the middle of a serial sequence without having to retransmit entire sequence at a later time. To pause, $\overline{HOLD}$ must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, $\overline{HOLD}$ is brought high, while SCK is low. ($\overline{HOLD}$ should be held high any time this function is not being used.) $\overline{HOLD}$ may be tied high directly to V_{CC} or tied to V_{CC} through a resistor.

$\overline{WP}$: Write Protect Input

The $\overline{WP}$ pin when tied low prevents non−volatile writes to the device (change of wiper control register is allowed) and when tied high or left floating normal read/write operations are allowed.

Serial Bus Protocol

The CAT5261 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the CAT5261 to interface directly with many of today's popular microcontrollers. The CAT5261 contains an 8−bit instruction register. The instruction set and the operation codes are detailed in the Instruction Set Table 13 on page 9.

Device Operation

The CAT5261 is two resistor arrays integrated with an SPI serial interface logic, two 8−bit wiper control registers and eight 8−bit, non−volatile memory data registers. Each resistor array contains 255 separate resistive elements connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L). R_H and R_L are symmetrical and may be interchanged. The tap positions between and at the ends of the series resistors are connected to the output wiper terminals (R_W) by a After the device is selected with $\overline{CS}$ going low the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op−codes that define the operation to be performed.

CMOS transistor switch. Only one tap point for each potentiometer is connected to its wiper terminal at a time and is determined by the value of the wiper control register. Data can be read or written to the wiper control registers or the non−volatile memory data registers via the SPI bus. Additional instructions allows data to be transferred between the wiper control registers and each respective potentiometer's non−volatile data registers. Also, the device can be instructed to operate in an "increment/decrement" mode.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	−55 to +125	°C
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−2.0 to +V_{CC} + 2.0	V
V_{CC} with Respect to Ground	−0.2 to +7.0	V
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Lead Soldering Temperature (10 s)	300	°C
Wiper Current	±6	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameters	Ratings	Units
V_{CC}	+2.5 to +6.0	V
Industrial Temperature	−40 to +85	°C

Table 4. POTENTIOMETER CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
R_{POT}	Potentiometer Resistance (−00)			100		kΩ
R_{POT}	Potentiometer Resistance (−50)			50		kΩ
	Potentiometer Resistance Tolerance				±20	%
	R_{POT} Matching				1	%
	Power Rating	25°C, each pot			50	mW
I_W	Wiper Current				±3	mA
R_W	Wiper Resistance	I_W = ±3 mA @ V_{CC} = 3 V		200	300	Ω
R_W	Wiper Resistance	I_W = ±3 mA @ V_{CC} = 5 V		100	150	Ω
V_{TERM}	Voltage on any R_H or R_L Pin		0		V_{CC}	V
VN	Noise	(Note 3)				nV√Hz
	Resolution			0.4		%
	Absolute Linearity (Note 4)	Rw(n)(actual)−R(n)(expected) (Note 7)			±1	LSB (Note 6)
	Relative Linearity (Note 5)	Rw(n+1)−[Rw(n)+LSB] (Note 7)			±0.2	LSB (Note 6)
TC_{RPOT}	Temperature Coefficient of R_{POT}	(Note 3)		±300		ppm/°C
TC_{RATIO}	Ratiometric Temp. Coefficient	(Note 3)			20	ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	(Note 3)		10/10/25		pF
fc	Frequency Response	R_{POT} = 50 kΩ (Note 3)		0.4		MHz

1. The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods of less than 20 ns.
2. Latch−up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} +1 V.
3. This parameter is tested initially and after a design or process change that affects the parameter.
4. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
5. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
6. LSB = R_{TOT} / 255 or (R_H − R_L) / 255, single pot
7. n = 0, 1, 2, ..., 255

Table 5. D.C. OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +6.0 V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current	f_{SCL} = 400 kHz, SDA = Open V_{CC} = 6 V, Inputs = GNDs		1	mA
I_{CC2}	Power Supply Current	f_{SCK} = 400 kHz, SDA Open		5	mA
	Non−volatile WRITE	V_{CC} = 6 V, Input = GND			
I_{SB}	Standby Current (V_{CC} = 5 V)	V_{IN} = GND or V_{CC}, SDA = Open		1	μA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		10	μA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	μA
V_{IL}	Input Low Voltage		−1	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 1.0	V
V_{OL1}	Output Low Voltage (V_{CC} = 3 V)	I_{OL} = 3 mA		0.4	V
V_{OH1}	Output High Voltage	I_{OH} = −1.6 mA	V_{CC} − 0.8		V

Table 6. PIN CAPACITANCE (Note 8) (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5 V, unless otherwise specified.)

Symbol	Test	Conditions	Max	Units
C_{OUT} (Note 8)	Output Capacitance (SO)	V_{OUT} = 0 V	8	pF
C_{IN} (Note 8)	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$, A0, A1)	V_{IN} = 0 V	6	pF

Table 7. A.C. CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{SU}	Data Setup Time	C_L = 50 pF	50		ns
t_H	Data Hold Time		50		ns
t_{WH}	SCK High Time		125		ns
t_{WL}	SCK Low Time		125		ns
f_{SCK}	Clock Frequency		DC	3	MHz
t_{LZ}	$\overline{HOLD}$ to Output Low Z			50	ns
t_{RI} (Note 8)	Input Rise Time			2	μs
t_{FI} (Note 8)	Input Fall Time			2	μs
t_{HD}	$\overline{HOLD}$ Setup Time		100		ns
t_{CD}	$\overline{HOLD}$ Hold Time		100		ns
t_V	Output Valid from Clock Low			200	ns
t_{HO}	Output Hold Time		0		ns
t_{DIS}	Output Disable Time			250	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			100	ns
t_{CS}	$\overline{CS}$ High Time		2		ns
t_{CSS}	$\overline{CS}$ Setup Time		250		ns
t_{CSH}	$\overline{CS}$ Hold Time		250		ns

8. This parameter is tested initially and after a design or process change that affects the parameter.

Table 8. POWER UP TIMING (Notes 9, 10)

Symbol	Parameter	Max	Units
t_{PUR}	Power−up to Read Operation	1	ms
t_{PUW}	Power−up to Write Operation	1	ms

Table 9. WIPER TIMING

Symbol	Parameter	Min	Max	Units
t_{WRPO}	Wiper Response Time After Power Supply Stable	5	10	μs
t_{WRL}	Wiper Response Time After Instruction Issued	5	10	μs

Table 10. WRITE CYCLE LIMITS

Symbol	Parameter	Max	Units
t_{WR}	Write Cycle Time	5	ms

Table 11. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END} (Note 11)	Endurance	MIL−STD−883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR} (Note 11)	Data Retention	MIL−STD−883, Test Method 1008	100		Years
V_{ZAP} (Note 11)	ESD Susceptibility	MIL−STD−883, Test Method 3015	2000		V
I_{LTH} (Note 11)	Latch−Up	JEDEC Standard 17	100		mA

9. This parameter is tested initially and after a design or process change that affects the parameter.
10. t_{PUR} and t_{PUW} are delays required from the time V_{CC} is stable until the specified operation can be initiated.
11. This parameter is tested initially and after a design or process change that affects the parameter.

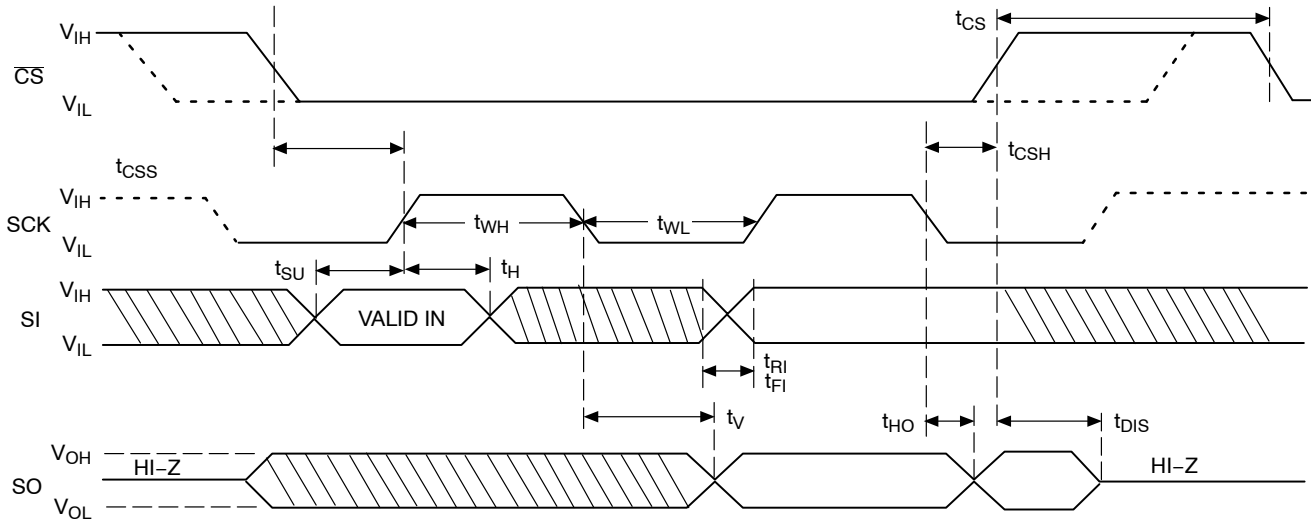


Figure 2. Synchronous Data Timing

NOTE: Dashed Line = mode (1, 1)

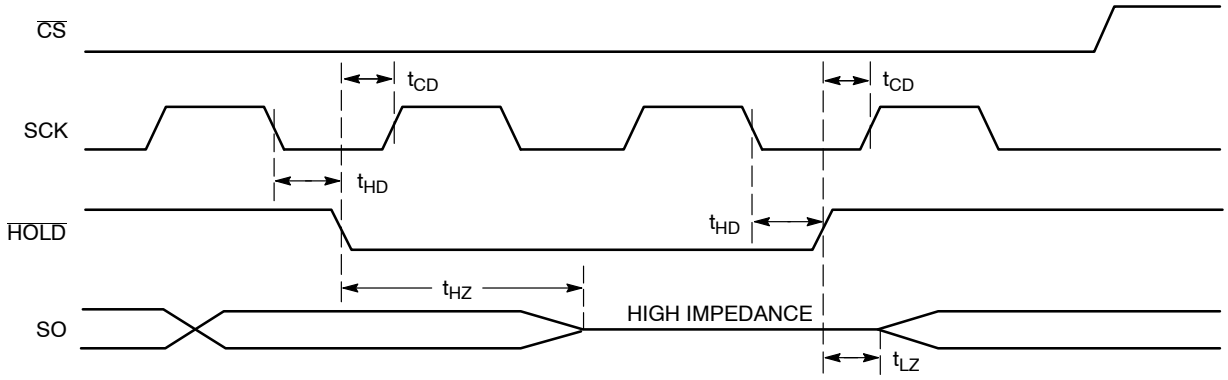


Figure 3. HOLD Timing

Instruction and Register Description

Device Type / Address Byte

The first byte sent to the CAT5261 from the master/ processor is called the Device Address Byte. The most significant four bits of the Device Type address are a device type identifier. These bits for the CAT5261 are fixed at 0101[B] (refer to Figure 4).

The two least significant bits in the slave address byte, A1 – A0, are the internal slave address and must match the physical device address which is defined by the state of the A1 – A0 input pins for the CAT5261 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A1 – A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}. The remaining two bits in the device address byte must be set to 0.

Instruction Byte

The next byte sent to the CAT5261 contains the instruction and register pointer information. The four most significant bits used provide the instruction opcode I3 – I0. The R1 and R0 bits point to one of the four data registers of each associated potentiometer. The least two significant bits point to one of two Wiper Control Registers. The format is shown in Figure 5.

Table 12. DATA REGISTER SELECTION

Data Register Selected	R1	R0
DR0	0	0
DR1	0	1

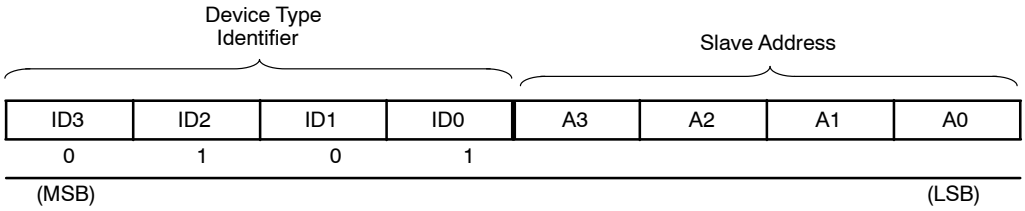


Figure 4. Identification Byte Format

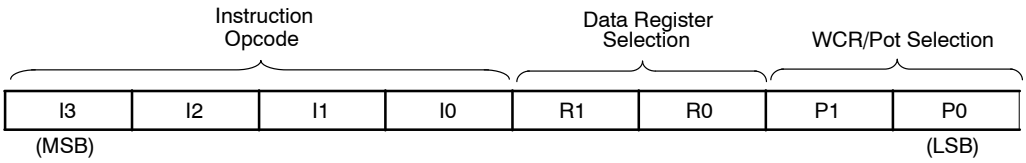


Figure 5. Instruction Byte Format

Wiper Control and Data Registers

Wiper Control Register (WCR)

The CAT5261 contains two 8−bit Wiper Control Registers, one for each potentiometer. The Wiper Control Register output is decoded to select one of 256 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written by the host via Write Wiper Control Register instruction; it may be written by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction; it can be modified one step at a time by the Increment/decrement instruction (see Instruction section for more details). Finally, it is loaded with the content of its data register zero (DR0) upon power−up.

The Wiper Control Register is a volatile register that loses its contents when the CAT5261 is powered−down. Although the register is automatically loaded with the value in DR0 upon power−up, this may be different from the value present at power−down.

Data Registers (DR)

Each potentiometer has four 8−bit non−volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Control Register. Any data changes in one of the Data Registers is a non−volatile operation and will take a maximum of 5 ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as standard memory locations for system parameters or user preference data.

Write in Process

The contents of the Data Registers are saved to nonvolatile memory when the $\overline{CS}$ input goes HIGH after a write sequence is received. The status of the internal write cycle can be monitored by issuing a Read Status command to read the Write in Process (WIP) bit.

Instructions

Five of the ten instructions are three bytes in length. These instructions are:

- **Read Wiper Control Register –** read the current wiper position of the selected potentiometer in the WCR
- **Write Wiper Control Register –** change current wiper position in the WCR of the selected potentiometer
- **Read Data Register –** read the contents of the selected Data Register
- **Write Data Register –** write a new value to the selected Data Register
- **Read Status –** Read the status of the WIP bit which when set to “1” signifies a write cycle is in progress.

Table 13. INSTRUCTION SET

Instruction	Instruction Set								Operation
	I3	I2	I1	I0	R1	R0	WCR1/ P1	WCR0/ P0	
Read Wiper Control Register	1	0	0	1	0	0	1/0	1/0	Read the contents of the Wiper Control Register pointed to by P1−P0
Write Wiper Control Register	1	0	1	0	0	0	1/0	1/0	Write new value to the Wiper Control Register pointed to by P1−P0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P1−P0 and R1−R0
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P1−P0 and R1−R0
XFR Data Register to Wiper Control Register	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Data Register pointed to by P1−P0 and R1−R0 to its associated Wiper Control Register
XFR Wiper Control Register to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the Wiper Control Register pointed to by P1−P0 to the Data Register pointed to by R1−R0
Global XFR Data Registers to Wiper Control Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by R1−R0 of all four pots to their respective Wiper Control Registers
Global XFR Wiper Control Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Control Registers to their respective data Registers pointed to by R1−R0 of all four pots
Increment/Decrement Wiper Control Register	0	0	1	0	0	0	1/0	1/0	Enable Increment/decrement of the Control Latch pointed to by P1−P0
Read Status (WIP bit)	0	1	0	1	0	0	0	1	Read WIP bit to check internal write cycle status

NOTE: 1/0 = data is one or zero

The basic sequence of the three byte instructions is illustrated in Figure 7. These three−byte instructions exchange data between the WCR and one of the Data Registers. The WCR controls the position of the wiper. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a Data Register is a write to non−volatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the potentiometers and one of its associated registers; or the transfer can occur between both potentiometers and one associated register.

Four instructions require a two−byte sequence to complete, as illustrated in Figure 6. These instructions transfer data between the host/processor and the CAT5261; either between the host and one of the data registers or directly between the host and the Wiper Control Register. These instructions are:

- **XFR Data Register to Wiper Control Register –** This transfers the contents of one specified Data Register to the associated Wiper Control Register.
- **XFR Wiper Control Register to Data Register –** This transfers the contents of the specified Wiper Control Register to the specified associated Data Register.
- **Global XFR Data Register to Wiper Control Register –** This transfers the contents of all specified Data Registers to the associated Wiper Control Registers.
- **Global XFR Wiper Counter Register to Data Register –** This transfers the contents of all Wiper Control Registers to the specified associated Data Registers.

Increment/Decrement Command

The final command is Increment/Decrement (Figures 8 and 9). The Increment/Decrement command is different from the other commands. Once the command is issued the master can clock the selected wiper up and/or down in one segment steps; thereby providing a fine tuning capability to the host. For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the R_L terminal.

See Instructions format for more detail.

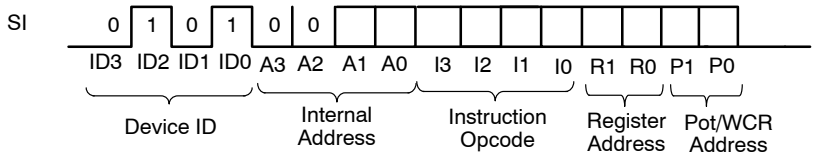


Figure 6. Two−Byte Instruction Sequence

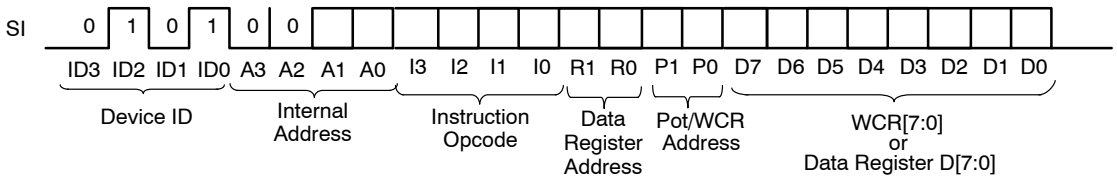


Figure 7. Three−Byte Instruction Sequence

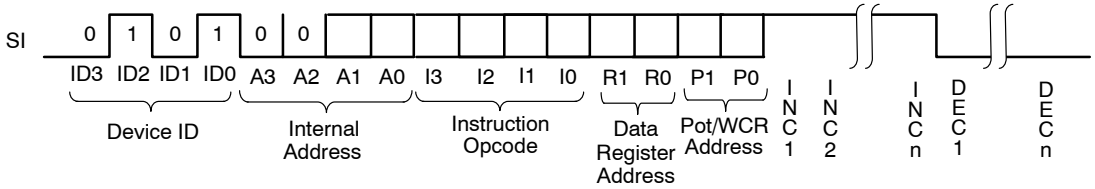


Figure 8. Increment/Decrement Instruction Sequence

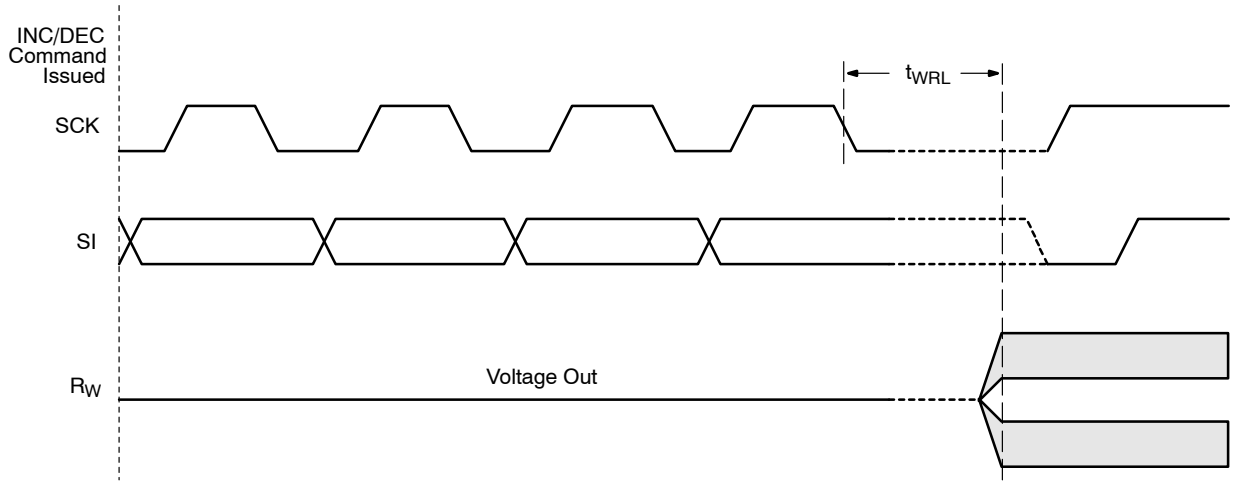


Figure 9. Increment/Decrement Timing Limits

Instruction Format

Table 14. READ WIPER CONTROL REGISTER (WCR)

	DEVICE ADDRESSES								INSTRUCTION								DATA								
$\overline{CS}$	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	P1	P0	7	6	5	4	3	2	1	0	$\overline{CS}$

Table 15. WRITE WIPER CONTROL REGISTER (WCR)

	DEVICE ADDRESSES								INSTRUCTION								DATA								
$\overline{CS}$	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	P1	P0	7	6	5	4	3	2	1	0	$\overline{CS}$

Table 16. READ DATA REGISTER (DR)

	DEVICE ADDRESSES								INSTRUCTION								DATA								
$\overline{CS}$	0	1	0	1	0	0	A1	A0	1	0	1	1	R1	R0	P1	P0	7	6	5	4	3	2	1	0	$\overline{CS}$

Table 17. WRITE DATA REGISTER (DR)

	DEVICE ADDRESSES								INSTRUCTION								DATA									
$\overline{CS}$	0	1	0	1	0	0	A1	A0	1	1	0	0	R1	R0	P1	P0	7	6	5	4	3	2	1	0	$\overline{CS}$	High Voltage Write Cycle

Table 18. READ STATUS (WIP)

	DEVICE ADDRESSES								INSTRUCTION								DATA								
$\overline{CS}$	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	70	60	50	40	30	20	10	WIP	$\overline{CS}$

Table 19. GLOBAL TRANSFER DATA REGISTER (DR) TO WIPER CONTROL REGISTER (WCR)

	DEVICE ADDRESSES								INSTRUCTION								
$\overline{CS}$	0	1	0	1	0	0	A 1	A 0	0	0	0	1	R 1	R 0	0	0	$\overline{CS}$

Table 20. GLOBAL TRANSFER WIPER CONTROL REGISTER (WCR) TO DATA REGISTER (DR)

	DEVICE ADDRESSES								INSTRUCTION									
$\overline{CS}$	0	1	0	1	0	0	A 1	A 0	1	0	0	0	R 1	R 0	0	0	$\overline{CS}$	High Voltage Write Cycle

Table 21. TRANSFER WIPER CONTROL REGISTER (WCR) TO DATA REGISTER (DR)

	DEVICE ADDRESSES								INSTRUCTION									
$\overline{CS}$	0	1	0	1	0	0	A 1	A 0	1	1	1	0	R 1	R 0	P 1	P 0	$\overline{CS}$	High Voltage Write Cycle

Table 22. TRANSFER DATA REGISTER (DR) TO WIPER CONTROL REGISTER (WCR)

	DEVICE ADDRESSES								INSTRUCTION								
$\overline{CS}$	0	1	0	1	0	0	A 1	A 0	1	1	0	1	R 1	R 0	P 1	P 0	$\overline{CS}$

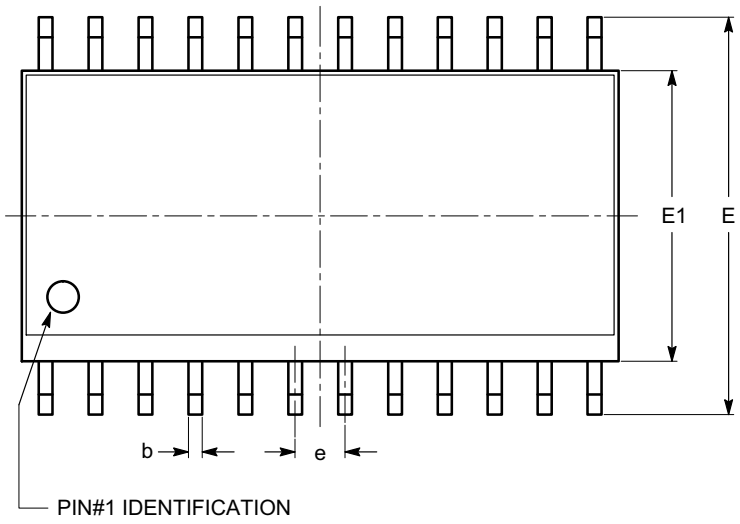
Table 23. INCREMENT (I)/DECREMENT (D) WIPER CONTROL REGISTER (WCR)

	DEVICE ADDRESSES								INSTRUCTION								DATA					
$\overline{CS}$	0	1	0	1	0	0	A 1	A 0	0	0	1	0	0	0	P 1	P 0	I/D	I/D	. . .	I/D	I/D	$\overline{CS}$

NOTE: Any write or transfer to the Non−volatile Data Registers is followed by a high voltage cycle after a STOP has been issued.

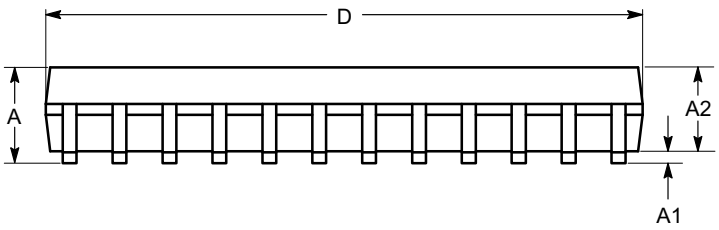
PACKAGE DIMENSIONS

SOIC−24, 300 mils
CASE 751BK−01
ISSUE O

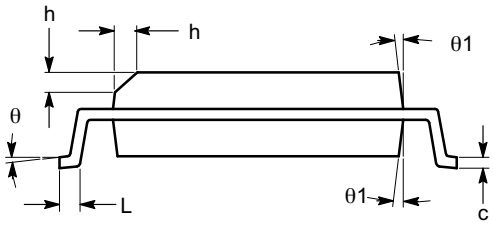


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	15.20		15.40
E	10.11		10.51
E1	7.34		7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40		1.27
θ	0º		8º
θ1	5º		15º



SIDE VIEW

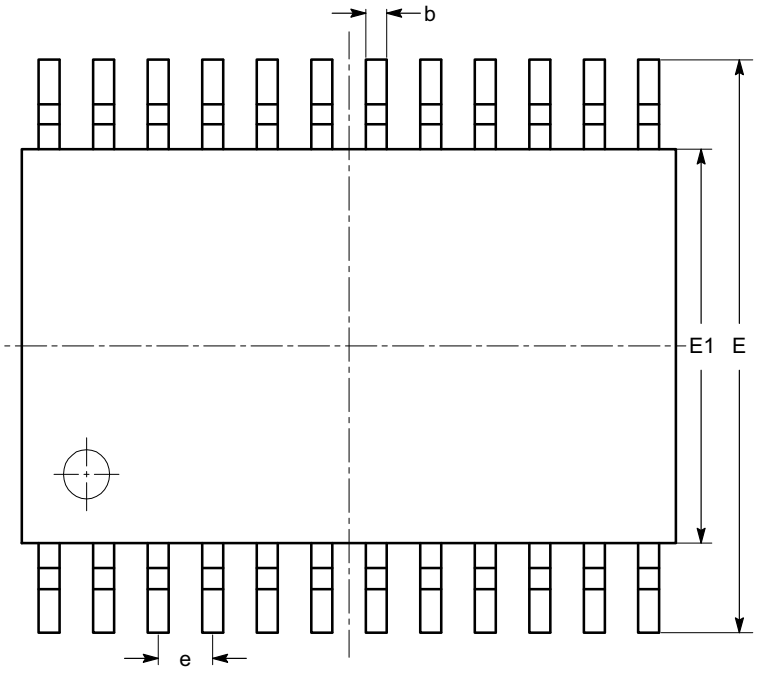


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

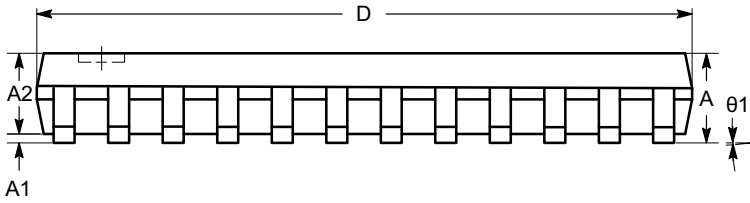
PACKAGE DIMENSIONS

TSSOP24, 4.4x7.8
CASE 948AR−01
ISSUE A

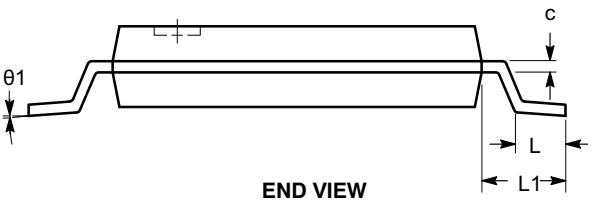


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.70
L1		1.00 REF	
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

Example of Ordering Information (Note 14)

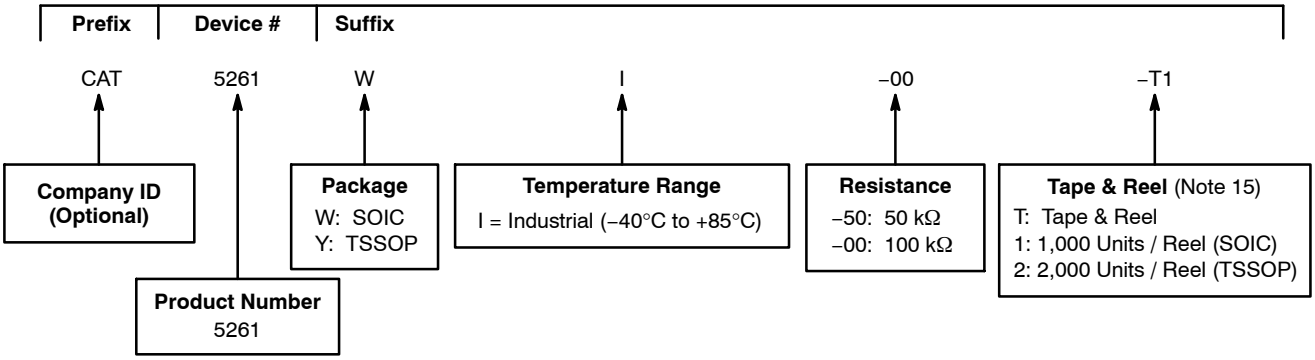


Table 24. ORDERING INFORMATION

Orderable Part Number	Resistance (kΩ)	Package	Lead Finish
CAT5261WI–50–T1	50	SOIC	Matte–Tin
CAT5261WI–00–T1	100		
CAT5261YI–50–T2	50	TSSOP	
CAT5261YI–00–T2	100		
CAT5261WI50	50	SOIC	
CAT5261WI00	100		
CAT5261YI50	50	TSSOP	
CAT5261YI00	100		

12. All packages are RoHS–compliant (Lead–free, Halogen–free).
13. The standard lead finish is Matte–Tin.
14. The device used in the above example is a CAT5261WI–00–T1 (SOIC, Industrial Temperature, 100 kΩ, Tape & Reel, 1,000/Reel).
15. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5773–3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

CAT5261/D