Single Digitally Controlled (XDCP™) Potentiometer

Description

The X9421 integrates a single digitally controlled potentiometer (XDCP) on a monolithic CMOS integrated circuit.

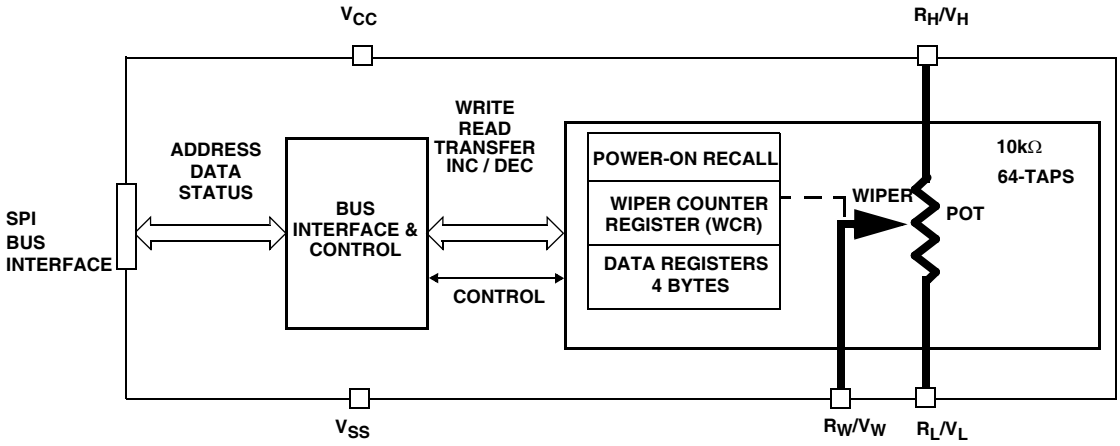
The digital controlled potentiometer is implemented using 63 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the SPI bus interface. The potentiometer has associated with it a volatile Wiper Counter Register (WCR) and a four non-volatile Data Registers that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array though the switches. Power-up recalls the contents of the default data register (DR0) to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Single Voltage Potentiometer
- 64 Resistor Taps
- SPI Serial Interface for Write, Read, and Transfer Operations of the Potentiometer
- Wiper Resistance, 150Ω Typical at 5V
- 4 Non-Volatile Data Registers
- Non-Volatile Storage of Multiple Wiper Positions
- Power-on Recall. Loads Saved Wiper Position on Power-up.
- Standby Current < 5µA Max
- V_{CC} : 2.7V to 5.5V Operation
- 2.5kΩ, 10kΩ End to End Resistance
- 100 yr. Data Retention
- Endurance: 100, 000 Data Changes per Bit per Register
- 14 Ld TSSOP, 16 Ld SOIC
- Low Power CMOS
- Pb-Free Available (RoHS Compliant)

Block Diagram



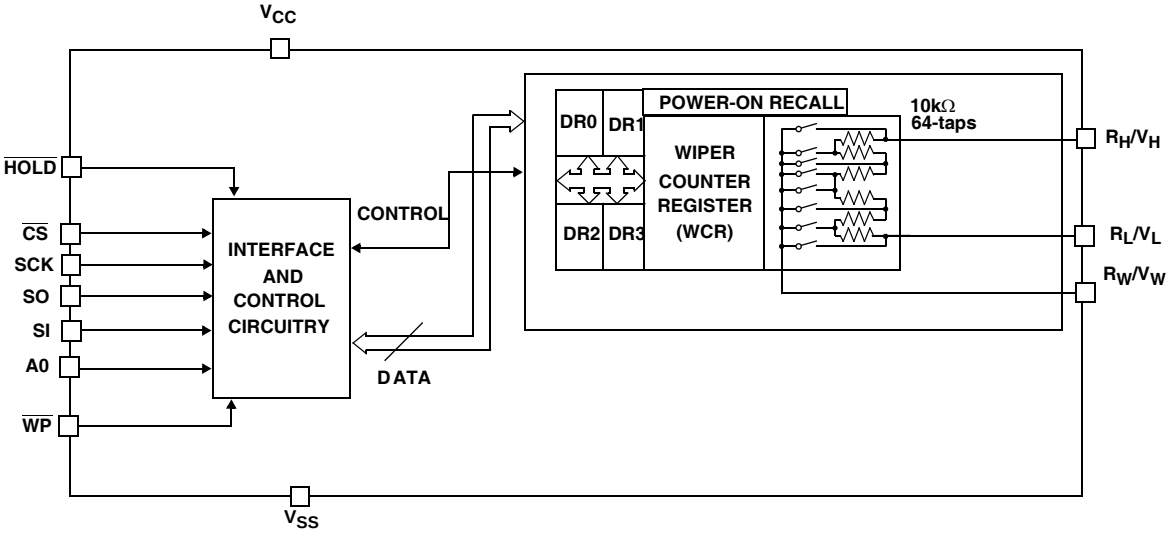
Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMETER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE
X9421YS16*	X9421YS	5 ±10%	2.5	0 to +70	16 Ld SOIC (300 mil)
X9421YS16Z* (Note)	X9421YS Z			0 to +70	16 Ld SOIC (300 mil) (Pb-Free)
X9421YS16I*	X9421YS I			-40 to +85	16 Ld SOIC (300 mil)
X9421YS16IZ* (Note)	X9421YS ZI			-40 to +85	16 Ld SOIC (300 mil) (Pb-Free)
X9421YV14*	X9421 YV			0 to +70	14 Ld TSSOP (4.4mm)
X9421YV14Z* (Note)	X9421 YVZ			0 to +70	14 Ld TSSOP (4.4mm) (Pb-Free)
X9421YV14I*	X9421 YV I			-40 to +85	14 Ld TSSOP (4.4mm)
X9421YV14IZ* (Note)	X9421 YVZI			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-Free)
X9421WS16*	X9421WS		10	0 to +70	16 Ld SOIC (300 mil)
X9421WS16Z* (Note)	X9421WS Z			0 to +70	16 Ld SOIC (300 mil) (Pb-Free)
X9421WS16I*	X9421WS I			-40 to +85	16 Ld SOIC (300 mil)
X9421WS16IZ* (Note)	X9421WS ZI			-40 to +85	16 Ld SOIC (300 mil) (Pb-Free)
X9421WV14*	X9421 WV			0 to +70	14 Ld TSSOP (4.4mm)
X9421WV14Z* (Note)	X9421 WV Z			0 to +70	14 Ld TSSOP (4.4mm) (Pb-Free)
X9421WV14I*	X9421 WV I			-40 to +85	14 Ld TSSOP (4.4mm)
X9421WV14IZ* (Note)	X9421 WVZI			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-Free)
X9421YS16-2.7*	X9421YS F	2.7 to 5.5	2.5	0 to +70	16 Ld SOIC (300 mil)
X9421YS16Z-2.7* (Note)	X9421YS ZF			0 to +70	16 Ld SOIC (300 mil) (Pb-Free)
X9421YS16I-2.7*	X9421 YS G			-40 to +85	16 Ld SOIC (300 mil)
X9421YS16IZ-2.7* (Note)	X9421 YS ZG			-40 to +85	16 Ld SOIC (300 mil) (Pb-Free)
X9421YV14-2.7*	X9421 YVF			0 to +70	14 Ld TSSOP (4.4mm)
X9421YV14Z-2.7* (Pb-free)	X9421 YVZF			0 to +70	14 Ld TSSOP (4.4mm) (Pb-Free)
X9421YV14I-2.7*	X9421 YVG			-40 to +85	14 Ld TSSOP (4.4mm)
X9421YV14IZ-2.7* (Pb-free)	X9421 YVZG			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-Free)
X9421WS16-2.7*	X9421WS F		10	0 to +70	16 Ld SOIC (300 mil)
X9421WS16Z-2.7* (Note)	X9421WS ZF			0 to +70	16 Ld SOIC (300 mil) (Pb-Free)
X9421WS16I-2.7*	X9421WS G			-40 to +85	16 Ld SOIC (300 mil)
X9421WS16IZ-2.7* (Note)	X9421WS ZG			-40 to +85	16 Ld SOIC (300 mil) (Pb-Free)
X9421WV14-2.7*	X9421 WVF			0 to +70	14 Ld TSSOP (4.4mm)
X9421WV14Z-2.7* (Pb-free)	X9421 WVZF			0 to +70	14 Ld TSSOP (4.4mm) (Pb-Free)
X9421WV14I-2.7*	X9421 WVG			-40 to +85	14 Ld TSSOP (4.4mm)
X9421WV14IZ-2.7* (Pb-free)	X9421 WVZG			-40 to +85	14 Ld TSSOP (4.4mm) (Pb-Free)

*Add "T1" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

Detailed Functional Diagrams



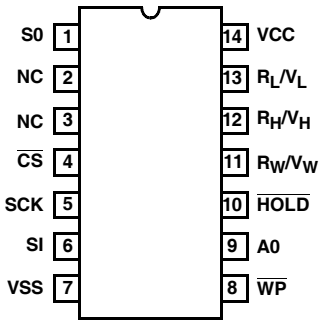
Circuit Level Applications

- Vary the Gain of a Voltage Amplifier
- Provide Programmable DC Reference Voltages for Comparators and Detectors
- Control the Volume in Audio Circuits
- Trim Out the Offset Voltage Error in a Voltage Amplifier Circuit
- Set the Output Voltage of a Voltage Regulator
- Trim the Resistance in Wheatstone Bridge Circuits
- Control the Gain, Characteristic Frequency and Q-factor in Filter Circuits
- Set the Scale Factor and Zero Point in Sensor Signal Conditioning Circuits
- Vary the Frequency and Duty Cycle of Timer ICs
- Vary the DC Biasing of a Pin Diode Attenuator in RF Circuits
- Provide a Control Variable (I, V, or R) in Feedback Circuits

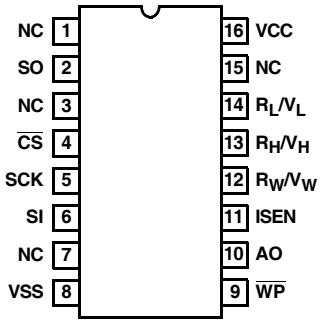
System Level Applications

- Adjust the contrast in LCD displays
- Control the Power Level of LED Transmitters in Communication Systems
- Set and Regulate the DC Biasing Point in an RF Power Amplifier in Wireless Systems
- Control the Gain in Audio and Home Entertainment Systems
- Provide the Variable DC Bias for Tuners in RF Wireless Systems
- Set the Operating Points in Temperature Control Systems
- Control the Operating Point for Sensors in Industrial Systems
- Trim Offset and Gain Errors in Artificial Intelligent Systems

X9421
(14 LD TSSOP)
TOP VIEW



X9421
(16 LD SOIC)
TOP VIEW



Pin Assignments

TSSOP PIN NO.	SOIC PIN NO.	SYMBOL	DESCRIPTION
1	2	SO	Serial Data Output
2, 3	3, 1, 7, 5	NC	No Connect
4	4	$\overline{CS}$	Chip Select
5	5	SCK	Serial Clock
6	6	SI	Serial Data Input
7	8	VSS	System Ground
8	9	$\overline{WP}$	Hardware Write Protect
9	10	A0	Device Address
10		$\overline{HOLD}$	Device select. Pause the serial bus.
11	12	R_W/V_W	Wiper Terminal of the Potentiometer.
12	13	R_H/V_H	High Terminal of the Potentiometer.
13	14	R_L/V_L	Low Terminal of the Potentiometer.
14	16	VCC	System Supply Voltage

Pin Descriptions

Host Interface Pins

SERIAL OUTPUT (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

SERIAL INPUT

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the potentiometer and pot register are input on this pin. Data is latched by the rising edge of the serial clock.

SERIAL CLOCK (SCK)

The SCK input is used to clock data into and out of the X9421.

CHIP SELECT ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9421 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device will be in the standby state. $\overline{CS}$ LOW enables the X9421, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

HOLD ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

DEVICE ADDRESS (A_0)

The address input is used to set the least significant bit of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9421. A maximum of two devices may occupy the SPI serial bus.

Potentiometer Pins

V_H/R_H, V_L/R_L

The V_H/R_H and V_L/R_L inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

V_W/R_W

The wiper output is equivalent to the wiper output of a mechanical potentiometer.

HARDWARE WRITE PROTECT INPUT ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents nonvolatile writes to the Data Registers. Writing to the Wiper Counter Register is not restricted.

SYSTEM/DIGITAL SUPPLY (V_{CC})

VCC is the supply voltage for the system/digital section. VSS is the system ground.

Principles of Operation

The X9421 is a highly integrated microcircuit incorporating a resistor array and associated registers and counter and the serial interface logic providing direct communication between the host and the XDCP potentiometer.

Serial Interface

The X9421 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

Array Description

The X9421 is comprised of one resistor array containing 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (V_H/R_H and V_L/R_L inputs).

At both ends of the array and between each resistor segment is a CMOS switch connected to the wiper (V_W/R_W) output. Within the individual array only one switch may be turned on at a time.

These switches are controlled by a Wiper Counter Register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches. The block diagram of the potentiometer is shown in Figure 1.

Wiper Counter Register (WCR)

The X9421 contains a Wiper Counter Register. The WCR can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction. Finally, it is loaded with the contents of its data register zero (DR0) upon power-up.

The Wiper Counter Register is a volatile register; that is, its contents are lost when the X9421 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down.

Data Registers

The potentiometer has four 6-bit nonvolatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the WCR. It should be noted all operations changing data in one of the Data Registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Register Descriptions

TABLE 1. DATA REGISTERS, (6-BIT), NONVOLATILE

0	**0**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
(MSB)							(LSB)

There are four 6-bit Data Registers associated with the potentiometer.

- {D5~D0}: These bits are for general purpose Nonvolatile data storage or for storage of up to four different wiper values.

TABLE 2. WIPER COUNTER REGISTER, (6-BIT), VOLATILE

0	**0**	**WP5**	**WP4**	**WP3**	**WP2**	**WP1**	**WP0**
(MSB)							(LSB)

- {WP5~WP0}: These bits specify the wiper position of the potentiometer.

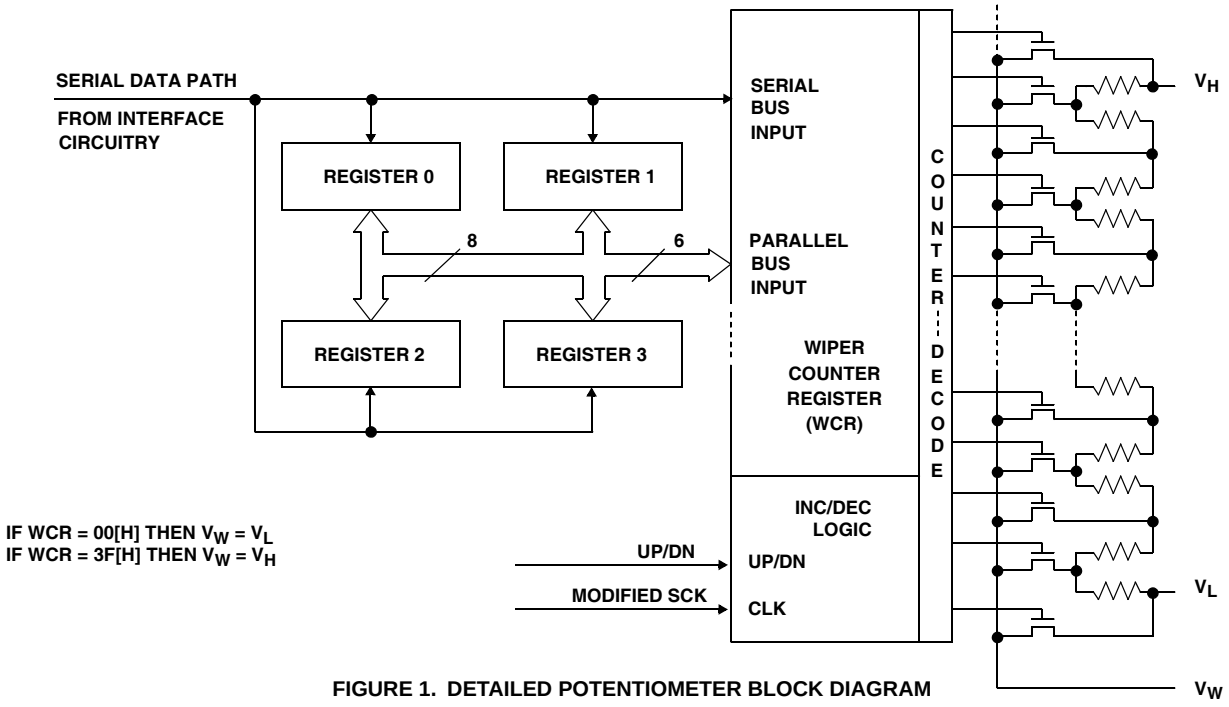


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

Write In Process

The contents of the Data Registers are saved to nonvolatile memory when the $\overline{CS}$ pin goes from LOW to HIGH after a complete write sequence is received by the device. The progress of this internal write operation can be monitored by a Write In Process bit (WIP). The WIP bit is read with a Read Status command.

Instructions

Address/Identification (ID) Byte

The first byte sent to the X9421 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Address or Identification byte. The most significant four bits of the slave address are a device type identifier, for the X9421 this is fixed as 0101[B] (refer to Figure 2).

The least significant bit in the ID byte selects one of two devices on the bus. The physical device address is defined by the state of the A_0 input pin. The X9421 compares the serial data stream with the address input state; a successful compare of the address bit is required for the X9421 to successfully continue the command sequence. The A_0 input can be actively driven by a CMOS input signal or tied to V_{CC} or V_{SS}.

The remaining three bits in the ID byte must be set to 110.

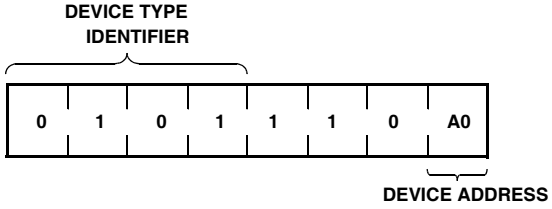


FIGURE 2. ADDRESS/IDENTIFICATION BYTE FORMAT

Instruction Byte

The next byte sent to the X9421 contains the instruction and register pointer information. The four most significant bits are the instruction. The next two bits point to one of four Data Registers. The format is shown below in Figure 3.

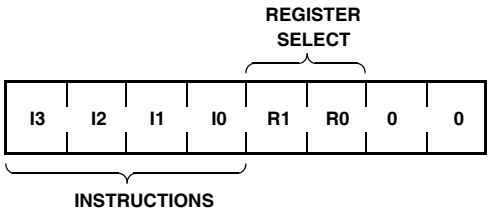


FIGURE 3. INSTRUCTION BYTE FORMAT

The four high order bits of the instruction byte specify the operation. The next two bits (R_1 and R_0) select one of the four registers that is to be acted upon when a register oriented instruction is issued. The last two bits are defined as 0.

Two of the eight instructions are two bytes in length and end with the transmission of the instruction byte. These instructions are:

- XFR Data Register to Wiper Counter Register —This instruction transfers the contents of one specified Data Register to the Wiper Counter Register.
- XFR Wiper Counter Register to Data Register—This instruction transfers the contents of the Wiper Counter Register to the specified associated Data Register.

The basic sequence of the two byte instructions is illustrated in Figure 4. These two-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action will be delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a Data Register is a write to nonvolatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between the potentiometer and one of its associated registers.

Five instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9421; either between the host and one of the Data Registers or directly between the host and the WCR. These instructions are:

- Read Wiper Counter Register—read the current wiper position of the pot,
- Write Wiper Counter Register—change current wiper position of the pot,
- Read Data Register—read the contents of the selected data register;
- Write Data Register—write a new value to the selected data register.
- Read Status—This command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The sequence of these operations is shown in Figure 5 and Figure 6.

The final command is Increment/Decrement. It is different from the other commands, because it's length is indeterminate. Once the command is issued, the master can clock the wiper up and/or down in one resistor segment step; thereby, providing a fine tuning capability to the host. For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper will move one resistor segment towards the V_H/R_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper will move one resistor segment towards the V_L/R_L terminal. A detailed illustration of the sequence and timing for this operation are shown in Figure 7 and 8.

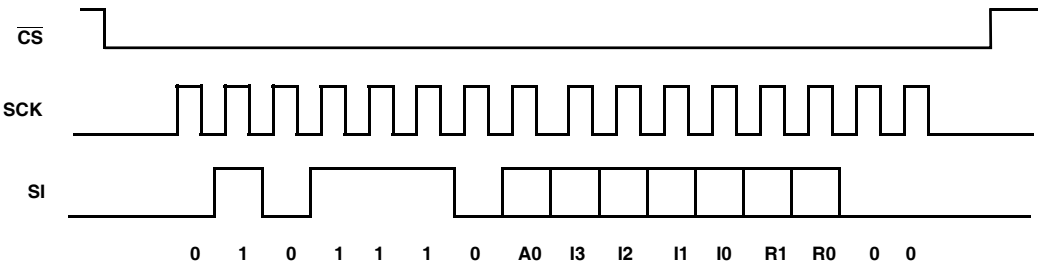


FIGURE 4. TWO-BYTE INSTRUCTION SEQUENCE

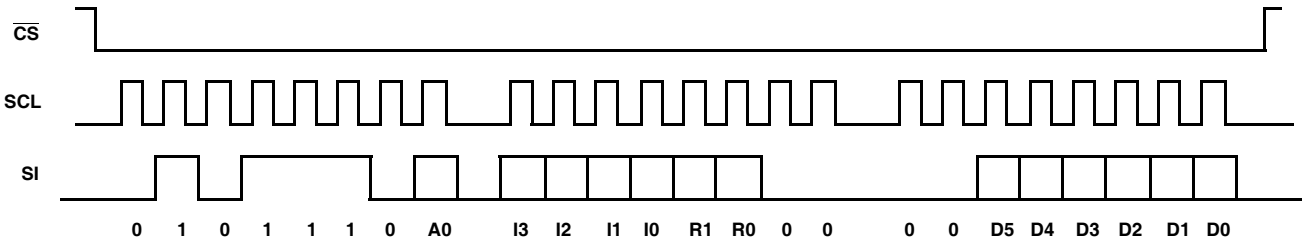


FIGURE 5. THREE-BYTE INSTRUCTION SEQUENCE (WRITE)

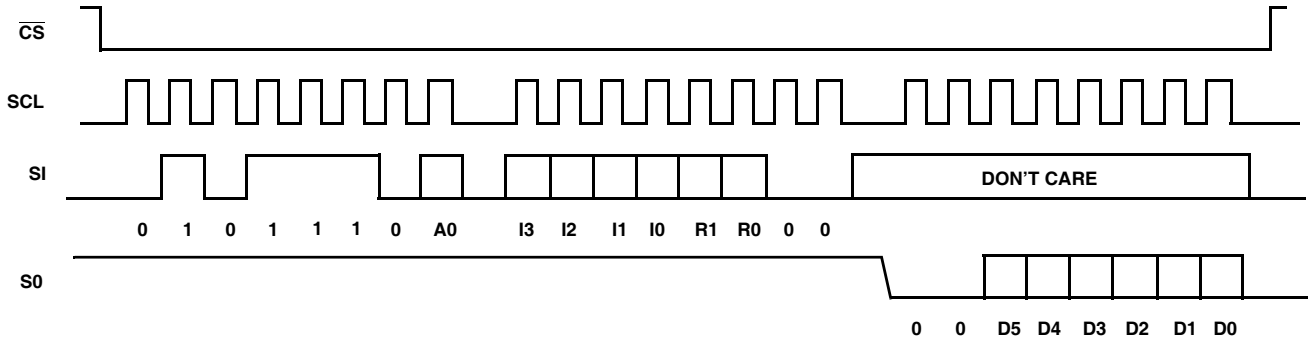


FIGURE 6. THREE-BYTE INSTRUCTION SEQUENCE (READ)

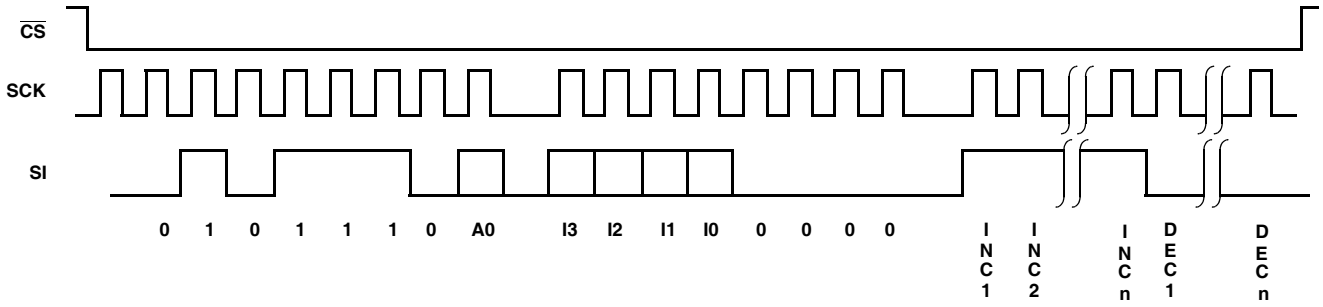


FIGURE 7. INCREMENT/DECREMENT INSTRUCTION SEQUENCE

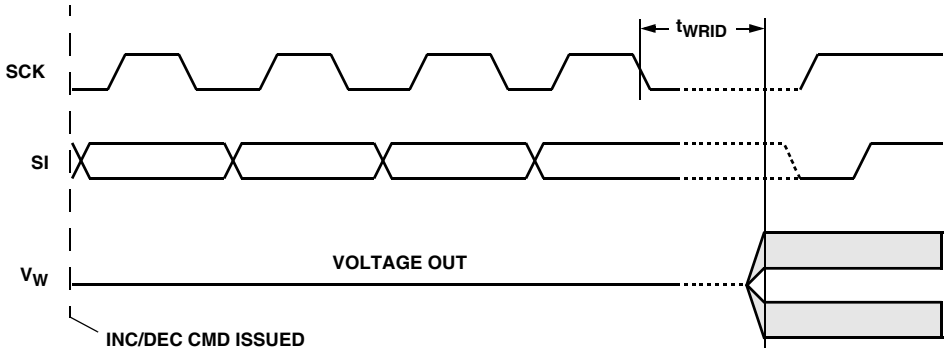


FIGURE 8. INCREMENT/DECREMENT TIMING LIMITS

TABLE 3. INSTRUCTION SET

INSTRUCTION	INSTRUCTION SET								OPERATION
	I_3	I_2	I_1	I_0	R_1	R_0			
Read Wiper Counter Register	1	0	0	1	0	0	0	0	Read the contents of the Wiper Counter Register
Write Wiper Counter Register	1	0	1	0	0	0	0	0	Write new value to the Wiper Counter Register
Read Data Register	1	0	1	1	1/0	1/0	0	0	Read the contents of the Data Register pointed to by R_1 - R_0
Write Data Register	1	1	0	0	1/0	1/0	0	0	Write new value to the Data Register pointed to by R_1 - R_0
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	0	0	Transfer the contents of the Data Register pointed to by R_1 - R_0 to the Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	0	0	Transfer the contents of the Wiper Counter Register to the Data Register pointed to by R_1 - R_0
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	0	0	Enable Increment/decrement of the Wiper Counter Register
Read Status (WIP bit)	0	1	0	1	0	0	0	1	Read the status of the internal write cycle, by checking the WIP bit.

Instruction Format

NOTES:

1. “A0”: stands for the device addresses sent by the master.
2. WPx refers to wiper position data in the Wiper Counter Register
   “I”: stands for the increment operation, SI held HIGH during active SCK phase (high).
3. “D”: stands for the decrement operation, SI held LOW during active SCK phase (high).

Read Wiper Counter Register (WCR)

$\overline{CS}$ FALLING EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE								WIPER POSITION (SENT BY X9421 ON SO)								$\overline{CS}$ RISING EDGE
	0	1	0	1	1	1	0	A0	1	0	0	1	0	0	0	0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Write Wiper Counter Register (WCR)

$\overline{CS}$ FALLING EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE								DATA BYTE (SENT BY HOST ON SI)								$\overline{CS}$ RISING EDGE
	0	1	0	1	1	1	0	A0	1	0	1	0	0	0	0	0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Read Data Register (DR)

Read the contents of the Register pointed to by R1 - R0.

$\overline{CS}$ FALLING EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE				REGISTER ADDRESSES				DATA BYTE (SENT BY X9421 ON SO)								$\overline{CS}$ RISING EDGE
	0	1	0	1	1	1	0	A0	1	0	1	1	R1	R0	0	0	0	0	WP5	WP4	WP3	WP2	WP1	WP0	

Write Data Register (DR)

Write a new value to the Register pointed to by R1 - R0.

$\overline{CS}$ FALLING EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE				REGISTER ADDRESSES				DATA BYTE (SENT BY HOST ON SI)								$\overline{CS}$ RISING EDGE	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	1	1	0	A0	1	1	0	0	R1	R0	0	0	0	0	WP5	WP4	WP3	WP2	WP1	WP0		

Transfer Data Register (DR) to Wiper Counter Register (WCR)

Transfer the contents of the Register pointed to by R1 - R0 to the WCR.

$\overline{CS}$ FALLING EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE				REGISTER ADDRESSES				$\overline{CS}$ RISING EDGE
	0	1	0	1	1	1	0	A0	1	1	0	1	R1	R0	0	0	

Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ FALLIN G EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE				REGISTER ADDRESSES				$\overline{CS}$ RISING EDGE	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	1	1	0	A0	1	1	1	0	R1	R0	0	0		

Increment/Decrement Wiper Counter Register (WCR)

$\overline{CS}$ FALLING EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE								INCREMENT/DECREMENT (SENT BY MASTER ON SDA)						$\overline{CS}$ RISING EDGE
	0	1	0	1	1	1	0	A0	0	0	1	0	0	0	0	0	I/D	I/D	.	.	.	I/D	I/D	

Read Status

$\overline{CS}$ FALLING EDGE	DEVICE TYPE IDENTIFIER				DEVICE ADDRESSES				INSTRUCTION OPCODE								DATA BYTE (SENT BY X9421 ON SO)								$\overline{CS}$ RISING EDGE
	0	1	0	1	1	1	0	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	WIP	

Absolute Maximum Ratings

Supply Voltage (V_{CC} Limits)
- X9421 . . . . . 5V ±10%
- X9421-2.7 . . . . . 2.7V to 5.5V

Voltage on SCK, SDA any address input with respect to V_{SS}: . . . . . -1V to +7V
$\Delta V = | (V_H - V_L) |$ 5V
I_W (10s) . . . . . ±6mA
Any VH/RH, VL/RL, VW/RW . . . . . VSS to VCC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
14 Lead TSSOP	92
16 Lead SOIC	82

Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range
- Commercial . . . . . 0°C to +70°C
- Industrial. . . . . .-40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details

Analog Specifications (Over recommended operating conditions unless otherwise stated.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			
			MIN. (Note 5)	TYP. (Note 6)	MAX. (Note 5)	UNITS
Rtotal	End to End Resistance Tolerance		-20		+20	%
	Power Rating	+25°C, each pot			50	mW
R_W	Wiper Resistance	Wiper Current Iw = $(V_H - V_L)/R_{TOTAL}$, V_{CC} = 5V		150	250	Ω
		Wiper Current Iw = $(V_H - V_L)/R_{TOTAL}$, V_{CC} = 3V		400	1000	Ω
V_{TERM}	Voltage on any V_H/R_H, V_L/R_L, V_W/R_W	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Noise	Ref: 1kHz		-120		dBV
	Resolution (Note 4)	(Note 5)		1.6		%
	Absolute Linearity (Note 1)	$V_{w(n)(actual)} - V_{w(n)(expected)}$	-1		+1	MI (Note 3)
	Relative Linearity (Note 2)	$V_{w(n+1)} - [V_{w(n)} + MI]$	-0.2		+0.2	MI (Note 3)
	Temperature Coefficient of R_{TOTAL}	(Note 5)		±300		ppm/°C
	Ratio metric Temperature Coefficient	(Note 5)		±20		ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	See “Circuit #3 SPICE Macro Model” on page 13		10/10/25		pF
I_{AL}	Rh, RI, Rw leakage current	VIN = VSS to VCC. Device is in stand-by mode.		0.1	10	µA

DC Electrical Specifications (Over the recommended operating conditions unless otherwise specified).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			
			MIN (Note 5)	TYP (Note 6)	MAX (Note 5)	UNITS
I_{CC1}	V_{CC} Supply Current (Active)	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}			400	µA
I_{CC2}	V_{CC} Supply Current (Nonvolatile Write)	f_{SCK} = 2MHz, SO = Open, Other Inputs = V_{SS}			3.5	mA
I_{SB}	V_{CC} Current (Standby)	SCK = SI = V_{SS}, Addr. = V_{SS}			3	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{SS} to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}			10	µA
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7		V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		-0.5		V_{CC} x 0.1	V
V_{OL}	Output LOW Voltage	I_{OL} = 3mA			0.4	V

ENDURANCE AND DATA RETENTION

PARAMETER	MIN	UNITS
Minimum Endurance	100,000	Data Changes per Bit per Register
Data Retention	100	Years

CAPACITANCE

SYMBOL	TEST	TYP	UNITS	TEST CONDITIONS
C_{OUT} (Note 5)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN} (Note 5)	Input Capacitance (A0, SI, and SCK)	6	pF	V_{IN} = 0V

POWER-UP TIMING

SYMBOL	PARAMETER	MIN	MAX	UNITS
$t_R V_{CC}$ (Note 5)	V_{CC} Power-up Ramp	0.2	50	V/msec

NOTES:

1. Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
2. Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
3. MI = RTOT/63 or (V_H - V_L)/63, single pot
4. Typical = Individual array resolution.
5. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
6. Limits should be considered typical and are not production tested.
7. This parameter is not production tested. Parameter established by characterization.

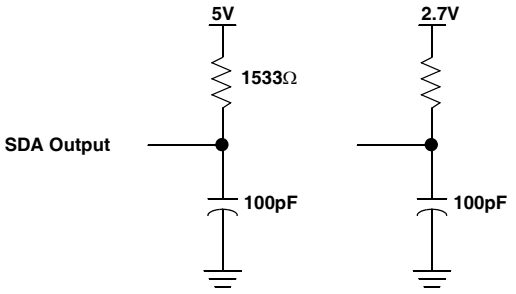
Power-up Requirements

(Power-up sequencing can affect correct recall of the wiper registers) The preferred power-on sequence is as follows: First V_{CC} and then the potentiometer pins, R_H, R_L, and R_W. Voltage should not be applied to the potentiometer pins before V_{CC} is applied. The V_{CC} ramp rate specification should be met, and any glitches or slope changes in the V_{CC} line should be held to <100mV if possible. Also, V_{CC} should not reverse polarity by more than 0.5V. Recall of wiper position will not be complete until V_{CC} reaches its final value.

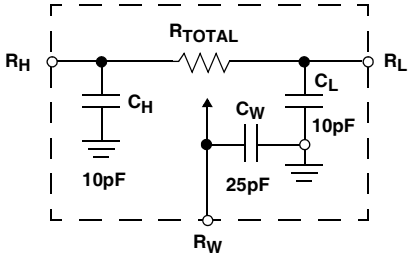
AC Test Conditions

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

Equivalent AC Load Circuit



Circuit #3 SPICE Macro Model



AC Timing

SYMBOL	PARAMETER	MIN (Note 5)	TYP (Note 6)	MAX (Note 5)	UNITS
f_{SCK}	SSI/SPI Clock Frequency			2.0	MHz
t_{CYC}	SSI/SPI Clock Cycle Time	500			ns
t_{WH}	SSI/SPI Clock High Time	200			ns
t_{WL}	SSI/SPI Clock Low Time	200			ns
t_{LEAD}	Lead Time	250			ns
t_{LAG}	Lag Time	250			ns
t_{SU}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Setup Time	50			ns
t_H	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Hold Time	50			ns
t_{RI}(7)	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Rise Time			2	µs
t_{FI}(7)	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ Input Fall Time			2	µs
t_{DIS}	SO Output Disable Time	0		500	ns
t_V	SO Output Valid Time			150	ns
t_{HO}	SO Output Hold Time	0			ns
t_{RO}	SO Output Rise Time		50		ns
t_{FO}	SO Output Fall Time		50		ns
t_{HOLD}	$\overline{HOLD}$ Time	400			ns
t_{HSU}	$\overline{HOLD}$ Setup Time	100			ns
t_{HH}	$\overline{HOLD}$ Hold Time	100			ns
t_{HZ}	$\overline{HOLD}$ Low to Output in High Z		100		ns
t_{LZ}	$\overline{HOLD}$ High to Output in Low Z		100		ns
T_I	Noise Suppression Time Constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs		20		ns
t_{CS}	$\overline{CS}$ Deselect Time	2			µs
t_{WPASU}	$\overline{WP}$, A0 and A1 Setup Time	0			ns
t_{WPAH}	$\overline{WP}$, A0 and A1 Hold Time	0			ns

High-Voltage Write Cycle Timing

SYMBOL	PARAMETER	TYP (NOTE 6)	MAX (NOTE 5)	UNITS
t_{WR}	High-voltage Write Cycle Time (Store Instructions)	5	10	ms

XDCP Timing

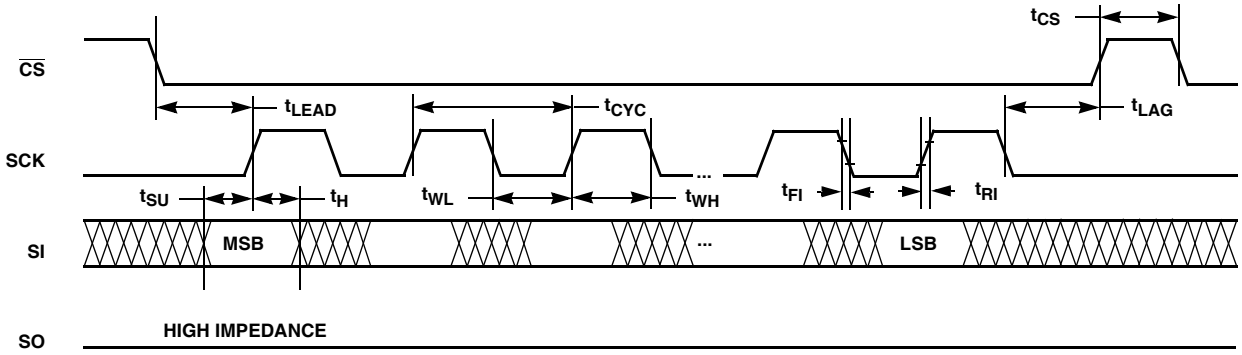
SYMBOL	PARAMETER	MIN (NOTE 5)	MAX (NOTE 5)	UNITS
t_{WRPO}	Wiper Response Time After The Power Supply Is Stable		10	µs
t_{WRL}	Wiper Response Time After Instruction Issued (All Load Instructions)		10	µs
t_{WRID}	Wiper Response Time From An Active SCL/SCK Edge (Increment/Decrement Instruction)		10	µs

Symbol Table

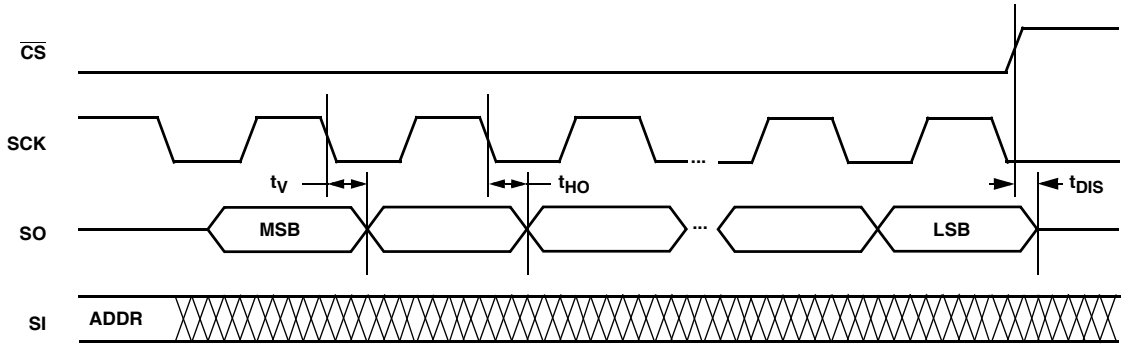
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM LOW TO HIGH	WILL CHANGE FROM LOW TO HIGH
	MAY CHANGE FROM HIGH TO LOW	WILL CHANGE FROM HIGH TO LOW
	DON'T CARE: CHANGES ALLOWED	CHANGING: STATE NOT KNOWN
	N/A	CENTER LINE IS HIGH IMPEDANCE

Timing Diagrams

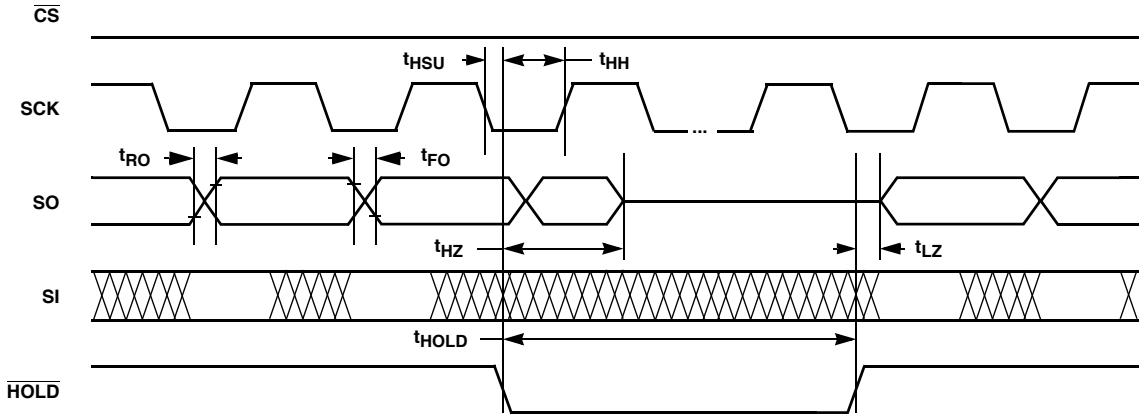
Input Timing



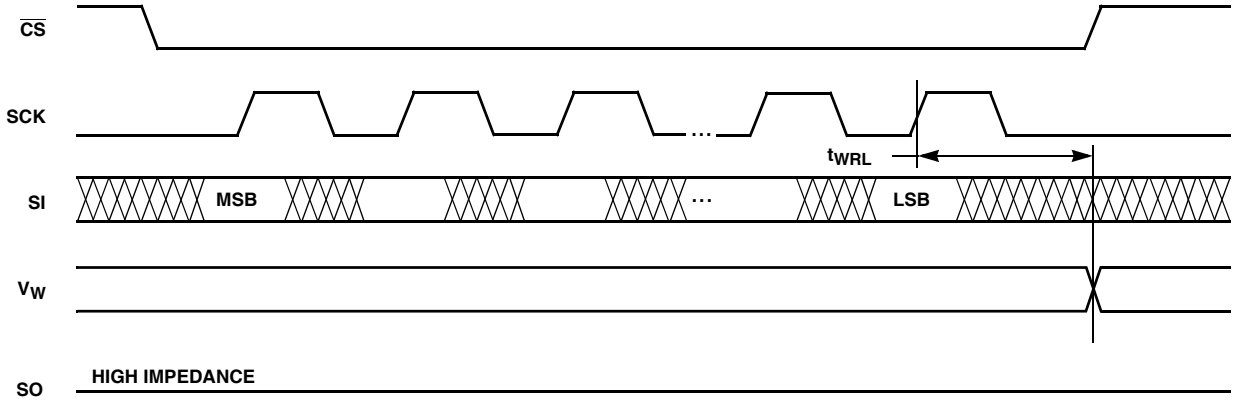
Output Timing



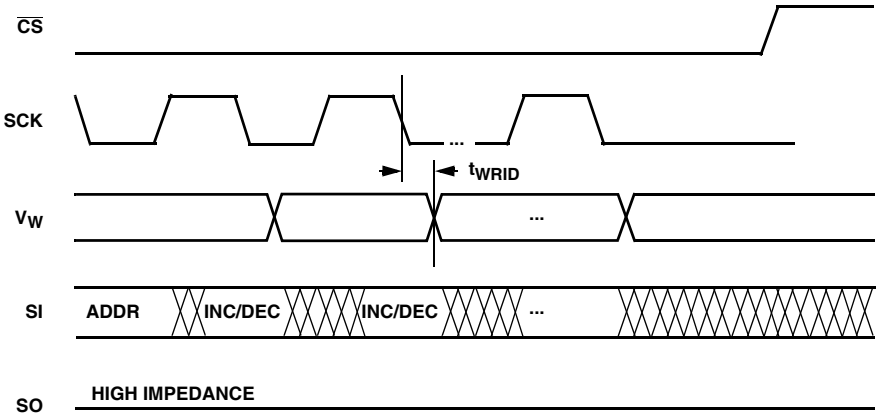
Hold Timing



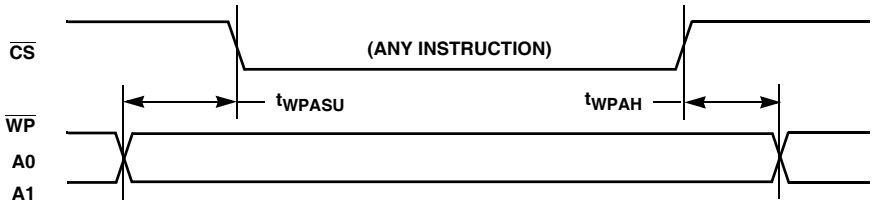
XDCP Timing (for All Load Instructions)



XDCP Timing (for Increment/Decrement Instruction)



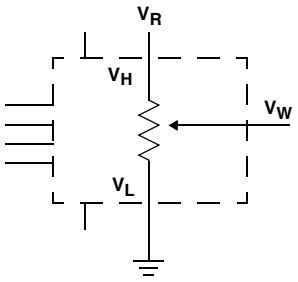
Write Protect and Device Address Pins Timing



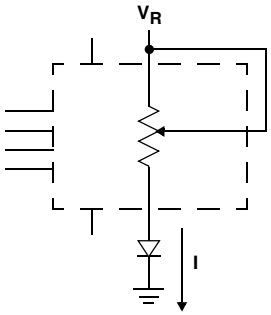
Applications information

1. Electronic potentiometers provide three powerful application advantages: The variability and reliability of a solid-state potentiometer,
2. The flexibility of computer-based digital controls)
3. the retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data.

Basic Configurations of Electronic Potentiometers



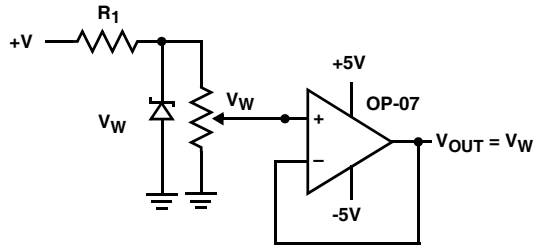
THREE TERMINAL POTENTIOMETER;
VARIABLE VOLTAGE DIVIDER



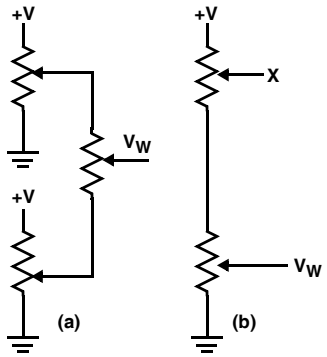
TWO TERMINAL VARIABLE RESISTOR;
VARIABLE CURRENT

Application Circuits

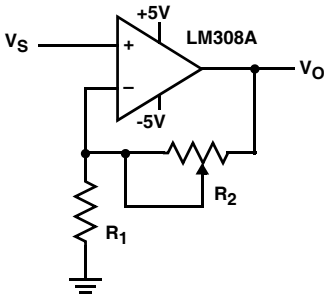
BUFFERED REFERENCE VOLTAGE



CASCADING TECHNIQUES

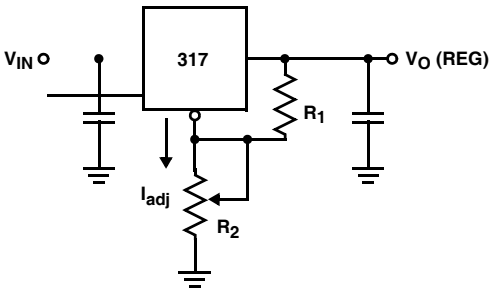


NONINVERTING AMPLIFIER



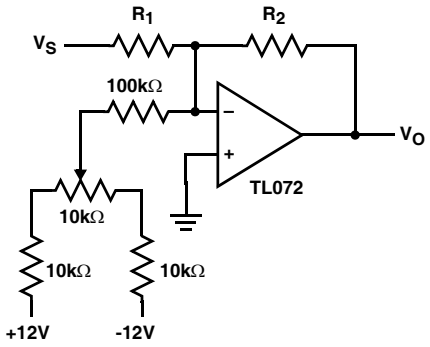
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR

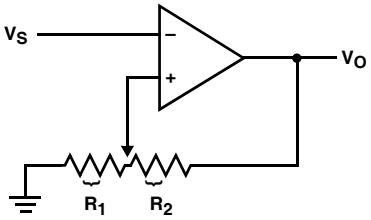


V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj}$ R_2

OFFSET VOLTAGE ADJUSTMENT

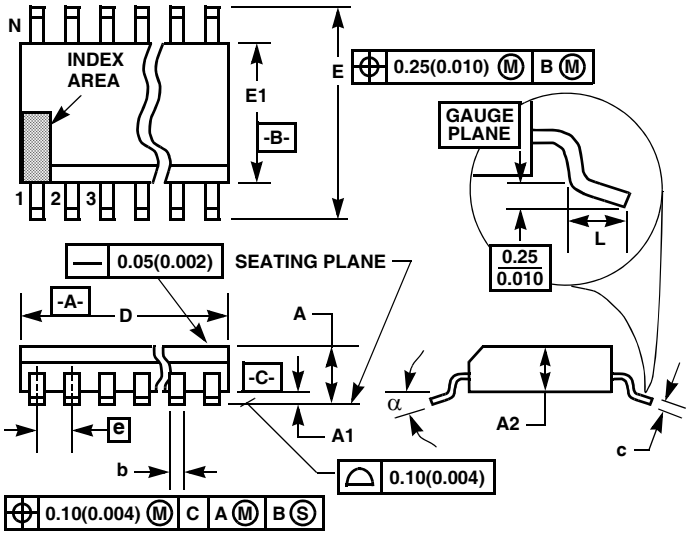


COMPARATOR WITH HYSTERITISIS



$V_{UL} = \{R_1/CR_1+R_2\}$ V_O(max)
$V_{LL} = \{R_1/CR_1+R_2\}$ V_O(min)

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

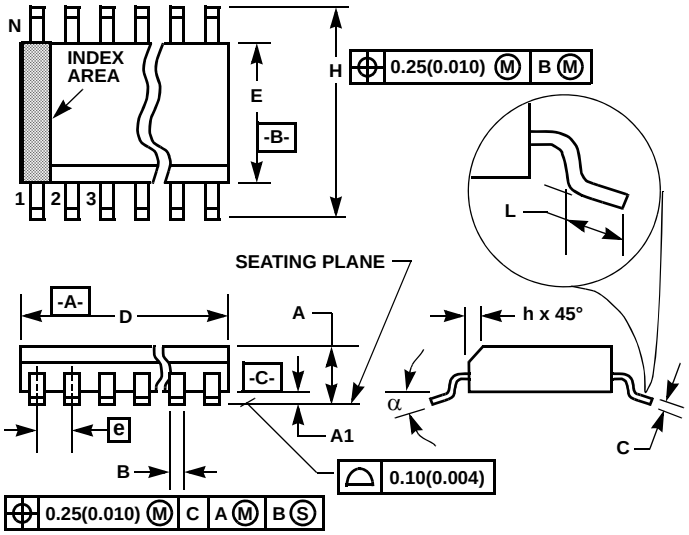
M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 2 4/06

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 6/05