Terminal Voltage ±3V or ±5V, 128 Taps I^2C Serial Interface

The Intersil ISL23711 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, and a control section. The wiper position is controlled by an I^2C interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. The wiper terminal can be connected to either end of the resistor array or at any one of the Tap Positions in between, providing 128 steps of resolution between R_L and R_H. The "position" of the wiper is determined by the value assigned to the volatile Wiper Register (WR). The WR can be directly written to and read from using standard I^2C interface protocol. The device is available in either a 10kΩ or 50kΩ version.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Industrial and Automotive Control
- Parameter and Bias Adjustments
- Amplifier Bias and Control

Ordering Information

PART NUMBER (BRAND)	RESISTANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL23711WIU10Z (AOE) (Notes 1, 2)	10K	-40 to +85	10 Ld MSOP (Pb-Free)	M10.118
ISL23711UIU10Z (AOD) (Notes 1, 2)	50K	-40 to +85	10 Ld MSOP (Pb-Free)	M10.118

NOTES:

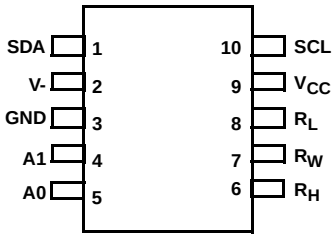
1. Add "-T" suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

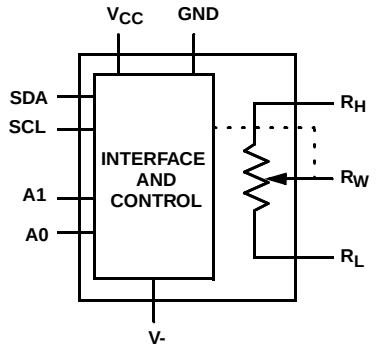
- I^2C Serial Interface with Hardwire Slave Address Allows up to Four Devices
- DCP Terminal Voltage, from V- to V_{CC}
- 127 Resistive Elements
  - Typical R_{TOTAL} tempco ±50ppm/°C
  - Typical ratiometric tempco ±4ppm/°C
  - End to end resistance range ±20%
  - Wiper resistance = 70Ω typ at V_{CC} = 3.3V
- Low Power CMOS
  - Standby current, 500nA max
  - Active current, 200μA max
  - V_{CC} = 2.7V to 5.5V
  - V- = -2.7V to -5.5V
- R_{TOTAL} Values = 10kΩ, 50kΩ
- Volatile Wiper Storage
- Package
  - 10 Ld MSOP
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

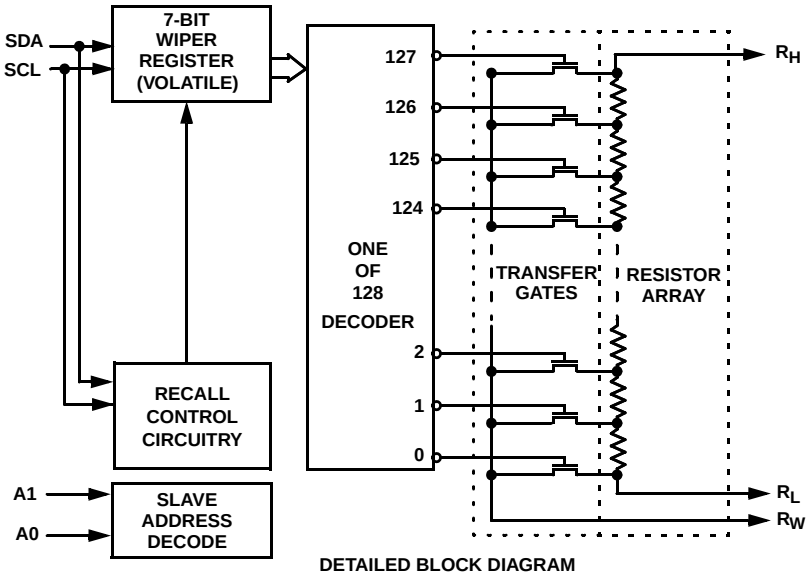
ISL23711
(10 LD MSOP)
TOP VIEW



Block Diagram



SIMPLE BLOCK DIAGRAM



DETAILED BLOCK DIAGRAM

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	SDA	Data I/O for I^2C serial interface. It has an open drain output and may be wire ORed with other open drain active low outputs.
2	V-	Negative supply voltage for the potentiometer wiper control.
3	GND	Ground. Should be connected to a digital ground
4	A1	A1 and A0 are address select pins used to set the slave address for the I^2C serial interface.
5	A0	A1 and A0 are address select pins used to set the slave address for the I^2C serial interface.
6	R_H	A fixed terminal for one end of the potentiometer resistor.
7	R_W	The wiper terminal which is equivalent to the movable terminal of a potentiometer.
8	R_L	A fixed terminal for one end of the potentiometer resistor.
9	V_{CC}	Positive logic supply voltage.
10	SCL	Clock input for the I^2C serial interface.

Absolute Maximum Ratings

Temperature under bias . . . . . -65°C to +135°C
Storage temperature . . . . . -65°C to +150°C
Voltage on SDA, SCL, A0, and A1
with Respect to GND . . . . . -0.3 to V_{CC}+0.3V
Voltage on V- (referenced to GND) . . . . . -6V
$\Delta V = |V_{(RH)}-V_{(RL)}|$ 12V
Lead Temperature (soldering 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA
V_{CC} . . . . . -0.3V to 6V
R_H, R_L, R_W . . . . . V- to V_{CC}
ESD Rating (MIL-STD-883, Method 3015.7 . . . . . >2kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
MSOP Package	170

Recommended Operating Conditions

Temperature Range (Industrial) . . . . . -40°C to +85°C
V_{CC} . . . . . 2.7V to 5.5V
V- . . . . . -2.7V to -5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE:

3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L Resistance	W option		10		kΩ
		U option		50		kΩ
	R_H to R_L Resistance Tolerance		-20		+20	%
V_{RH},V_{RL}	R_H, R_L Terminal Voltage		V-		V_{CC}	V
R_W	Wiper Resistance	V- = -5.5V; V_{CC} = +5.5V Wiper current = (V_{CC} - V-)/R_{TOTAL}		70	200	Ω
C_H/C_L/C_W	Potentiometer Capacitance (Note 13)			10/10/25		pF
I_{LkgDCP}	Leakage on R_H, R_L, R_W pins	Voltage at pins; V- to V_{CC}	-1	0.1	1	µA
VOLTAGE DIVIDER MODE (V- @ R_L; V_{CC} @ R_H; Voltage at R_W = V_{RW} unloaded)						
INL (Note 6)	Integral Non-linearity		-1		1	LSB (Note 2)
DNL (Note 5)	Differential Non-linearity	W, U options	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-scale Error	W option	0	1	4	LSB (Note 2)
		U option	0	0.5	2	
FSerror (Note 4)	Full-scale Error	W option	-4	-1	0	LSB (Note 2)
		U option	-2	-0.5	0	
TC_V (Notes 7, 13)	Ratiometric Temperature Coefficient	DCP register set from 16 to 120d, T = -40°C to +85°C		±4		ppm/°C
RESISTOR MODE (Measurements between R_W and R_L with R_H not connected, or between R_W and R_H with R_L not connected)						
RINL (Note 11)	Integral Non-linearity	DCP register set between 20 hex and 7F hex. Monotonic over all tap positions	-1		1	MI (Note 8)
RDNL (Note 10)	Differential Non-linearity		-0.5		0.5	MI (Note 8)
Roffset (Note 9)	Offset	DCP register set to 00 hex, W option	0	2	5	MI (Note 8)
		DCP register set to 00 hex, U option	0	0.5	2	MI (Note 8)
TC_R (Notes 12, 13)	Resistance Temperature Coefficient	DCP register set from 16 to 127d, T = -40°C to +85°C		±50		ppm/°C

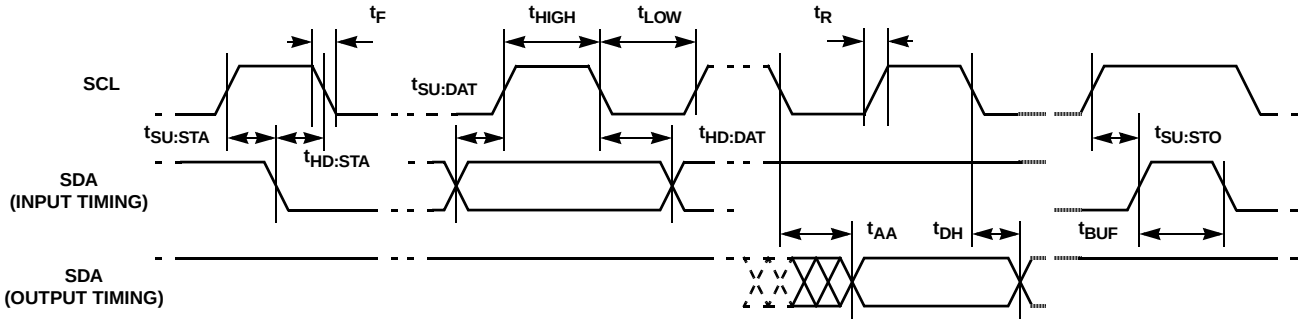
Operating Specifications Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
I_{CC1}	V_{CC} Supply Current, Volatile Write/Read	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Write states only)			200	µA
I_{V-}	V- Supply Current, Volatile Write/Read	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Write states only)	-100		-1	µA
I_{SB}	V_{CC} Current (Standby)	V_{CC} = +5.5V, I^2C Interface in Standby State			500	nA
		V_{CC} = +3.6V, I^2C Interface in Standby State			300	nA
I_{V-SB}	V- Current (Standby)	V- = -5.5V, I^2C Interface in Standby State	-500			nA
		V- = -2.7V, I^2C Interface in Standby State	-300		-1	nA
I_{LkgDig}	Leakage Current, at Pins SDA, SCL, A0, and A1	Voltage at pin from GND to V_{CC}	-10		10	µA
t_{DCP} (Note 13)	DCP Wiper Response Time	SCL falling edge of last bit of DCP Data Byte to wiper change		1		µs
Vpor	Power-on Recall for V_{CC}			2.5		V
SERIAL INTERFACE SPECS						
V_{IL}	A0, A1, SDA, and SCL Input Buffer LOW Voltage		-0.3		0.3*V_{CC}	V
V_{IH}	A0, A1, SDA, and SCL Input Buffer HIGH Voltage		0.7*V_{CC}		V_{CC}+ 0.3	V
Hysteresis	SDA and SCL Input Buffer Hysteresis		0.05* V_{CC}			V
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 4mA		0		0.4	V
Cpin (Note 14)	A0, A1, SDA, and SCL Pin Capacitance				10	pF
f_{SCL}	SCL Frequency				400	kHz
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed			50	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window			900	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition	1300			ns
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{CC} crossing	1300			ns
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{CC} crossing	600			ns
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}	600			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}	600			ns
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window	0			ns
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}	600			ns
$t_{HD:STO}$	STOP Condition Setup Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}	600			ns

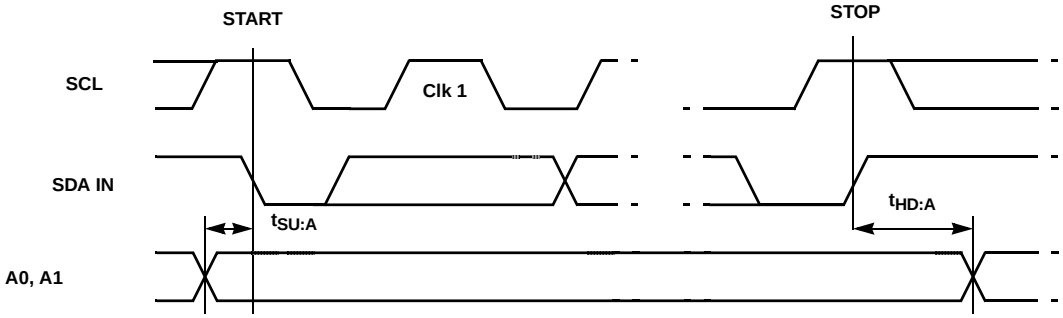
Operating Specifications Over the recommended operating conditions unless otherwise specified. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window	0			ns
t_R (Note 14)	SDA, SCL, A0, A1 Rise Time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns
t_F (Note 14)	SDA, SCL, A0, A1 Fall Time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 14)	Capacitive Loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 14)	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F For Cb = 400pF, max is about 2~2.5kΩ For Cb = 40pF, max is about 15~20kΩ	1			kΩ
$t_{SU:A}$	A0, A1 Setup Time	Before START condition	600			ns
$t_{HD:A}$	A0, A1 Hold Time	After STOP condition	600			ns

SDA vs SCL Timing



A0, A1 Pin Timing



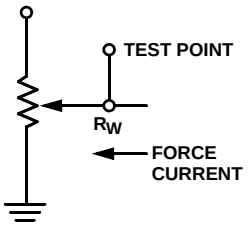
NOTES:

1. Typical values are for T_A = 25°C and ±5V supply voltage.
2. LSB: $[V(RW)_{127} – V(RW)_0] / 127$. $V(RW)_{127}$ and $V(RW)_0$ are V(RW) for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $(V(RW)_0 – V-) / LSB$.
4. FS error = $[V(RW)_{127} – V_{CC}] / LSB$.
5. DNL = $[V(RW)_i – V(RW)_{i-1}] / LSB-1$, for i = 1 to 127. i is the DCP register setting.
6. INL = $V(RW)_i – (i • LSB – V(RW)_0)$ for i = 1 to 127.
7. $TC_V = \frac{Max(V(RW)_i) – Min(V(RW)_i)}{[Max(V(RW)_i) + Min(V(RW)_i)]/2} \times \frac{10^6}{125°C}$

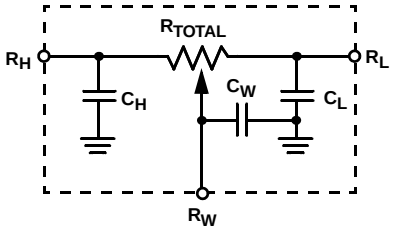
   for i = 16 to 120 decimal, Max( ) is the maximum value of the wiper voltage and Min ( ) is the minimum value of the wiper voltage over the temperature range.
8. MI = $|R_{127} – R_0| / 127$. R_{127} and R_0 are the measured resistances for the DCP register set to 7F hex and 00 hex respectively.
9. Roffset = R_0 / MI, when measuring between R_W and R_L.
   Roffset = R_{127} / MI, when measuring between R_W and R_H.
10. RDNL = $(R_i – R_{i-1}) / MI$, for i = 16 to 127.
11. RINL = $[R_i – (MI • i) – R_0] / MI$, for i = 16 to 127.
12. $TC_R = \frac{[Max(Ri) – Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$

    for i = 16 to 127, Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
13. This parameter is not 100% tested.
14. These are I^2C specific parameters and are not directly tested, however they are used during device testing to validate device specification.

Test Circuit



Equivalent Circuit



Pin Descriptions

Potentiometer Pins

R_H AND R_L

The high (R_H) and low (R_L) terminals of the ISL23711 are equivalent to the fixed terminals of a mechanical potentiometer. The terminology of R_L and R_H references the relative position of the terminal in relation to wiper movement direction selected by the I^2C serial input and not the voltage potential on the terminal.

R_W

R_W is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the control inputs.

BUS INTERFACE PINS

Serial Data Input/Output (SDA)

The SDA is a bidirectional serial data input/output pin for the I^2C interface. It receives device address, operation code, wiper register address and data from an I^2C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

SDA requires an external pull-up resistor, since it's an open drain output.

Serial Clock (SCL)

This input is the serial clock of the I^2C serial interface.

Device Address (A1-A0)

The Address inputs are used to set the least significant 2 bits of the 7-bit I^2C interface slave address. A match in the slave address serial data stream must be made with the Address input pins in order to initiate communication with the ISL23711. A maximum of 4 ISL23711 devices may occupy the I^2C serial bus.

Principles of Operation

The ISL23711 is an integrated circuit incorporating one DCP with It's associated register, and an I^2C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised

of 127 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The R_W pin is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal is controlled by a 7-bit volatile Wiper Register (WR). When the WR contains all zeroes (00h), the wiper terminal (R_W) is closest to its “Low” terminal (R_L). When the WR contains all ones (7Fh), the wiper terminal (R_W) is closest to its “High” terminal (R_H). As the value of the WR increases from all zeroes (0 decimal) to all ones (127 decimal), the wiper moves monotonically from the position closest to R_L to the position closest to R_H. At the same time, the resistance between R_W and R_L increases monotonically, while the resistance between R_H and R_W decreases monotonically.

While the ISL23711 is being powered up, the WR is reset to 20h (64 decimal), which locates the R_W at the center between R_L and R_H.

The WR can be read or written directly using the I^2C serial interface as described in the following sections.

Memory Description

- A read operation to address 0 outputs the value of the volatile WR.
- A write operation to address 0 only writes to the volatile WR.

I^2C Serial Interface

The ISL23711 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL23711 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 1). On power-up of the ISL23711 the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL23711 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 1).

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 1). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 2).

The ISL23711 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL23711 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1, and A0. The LSB is in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation. (See Table 1.)

TABLE 1. IDENTIFICATION BYTE FORMAT

Logic values at pins A1, and A0 respectively

0	1	0	1	0	A1	A0	R/$\overline{W}$
(MSB)							(LSB)

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL23711 responds with an ACK.

Read Operation

A Read operation is initiated by a master using the following sequence: a START, the Identification byte (slave address) with the R/$\overline{W}$ bit set to “1”. At the moment of the first acknowledge by the ISL23711 (slave device), the master-transmitter becomes a master receiver and receives the data byte from the slave-transmitter.The Master receives the data byte and issues a non-acknowledge (SDA is HIGH), then a STOP to terminate the read operation. Since the ISL 23711 has just one WR, it will transmit only one byte (see Figure 4).

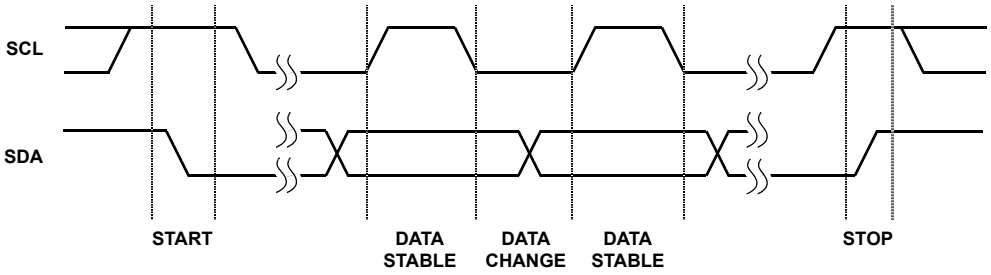


FIGURE 1. VALID DATA CHANGES, START, AND STOP CONDITIONS

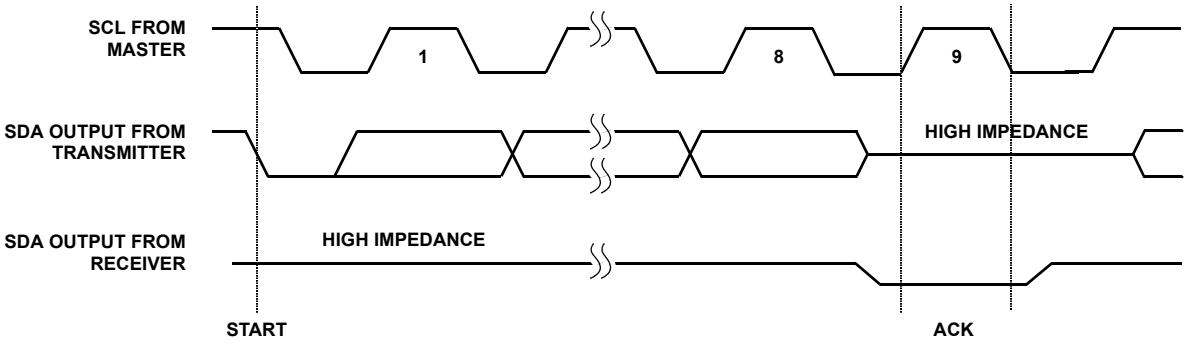


FIGURE 2. ACKNOWLEDGE RESPONSE FROM RECEIVER

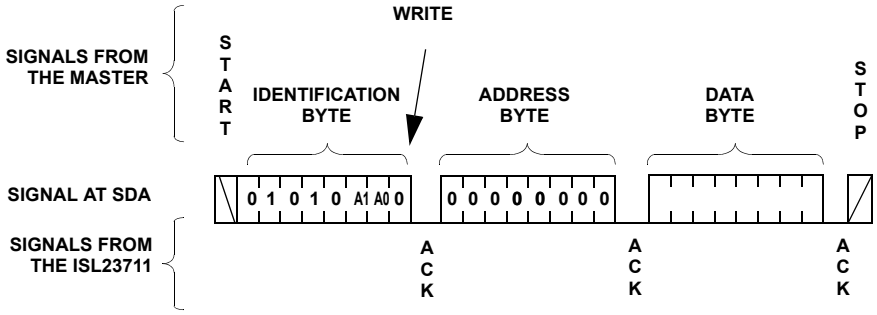


FIGURE 3. BYTE WRITE SEQUENCE

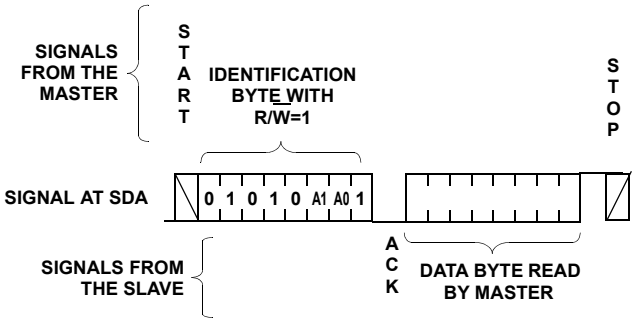
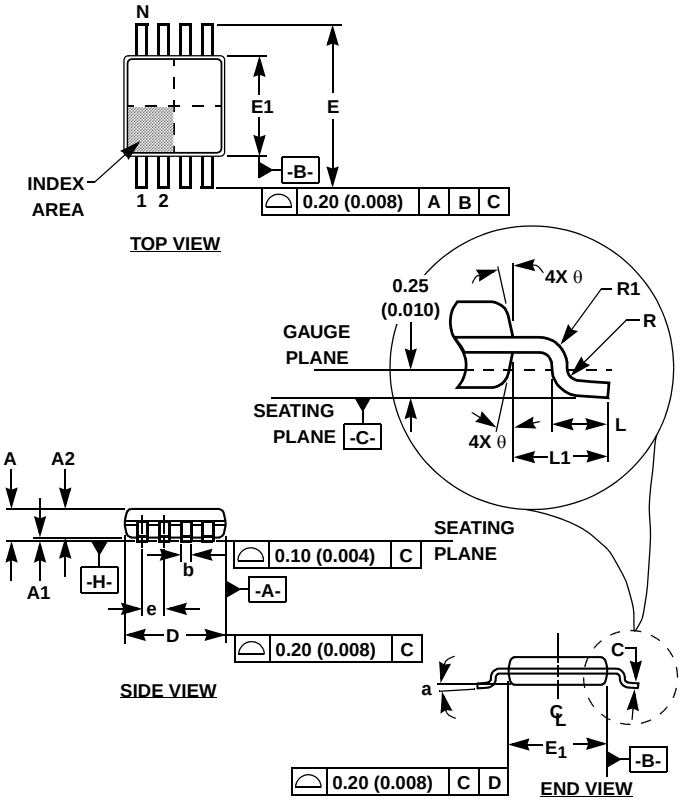


FIGURE 4. READ SEQUENCE

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)

10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5^o	15^o	5^o	15^o	-
α	0^o	6^o	0^o	6^o	-

Rev. 0 12/02

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension “D” does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions and are measured at Datum Plane. [- H -] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A -] and [- B -] to be determined at Datum plane [- H -].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only