

Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

General Description

The MAX5389 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10k Ω , 50k Ω , and 100k Ω . Operating from a single +2.6V to +5.5V power supply, the device provides a low 35ppm/ $^{\circ}$ C end-to-end temperature coefficient. The MAX5389 features an up/down interface.

The small package size, low supply operating voltage, low supply current, and automotive temperature range of the MAX5389 make the device uniquely suited for the portable consumer market, battery backup industrial applications, and the automotive market.

The MAX5389 is specified over the automotive -40 $^{\circ}$ C to +125 $^{\circ}$ C temperature range and is available in a 14-pin TSSOP package.

Applications

Audio Mixing
Mechanical Potentiometer Replacement
Low-Drift Programmable Filters and Amplifiers
Adjustable Voltage References/Linear Regulators
Programmable Delays and Time Constants
Automotive Electronics
Low-Voltage Battery Applications

Features

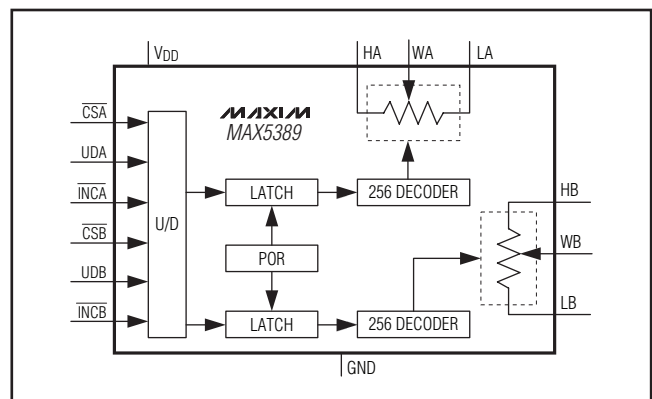
- ◆ Dual, 256-Tap Linear Taper Positions
- ◆ Single +2.6V to +5.5V Supply Operation
- ◆ Low (< 1 μ A) Quiescent Supply Current
- ◆ 10k Ω , 50k Ω , 100k Ω End-to-End Resistance Values
- ◆ Up/Down Interface
- ◆ Power-On Sets Wiper to Midscale
- ◆ -40 $^{\circ}$ C to +125 $^{\circ}$ C Operating Temperature Range

Ordering Information

PART	PIN-PACKAGE	END-TO-END RESISTANCE (k Ω)
MAX5389LAUD+	14 TSSOP	10
MAX5389MAUD+	14 TSSOP	50
MAX5389NAUD+	14 TSSOP	100

Note: All devices are specified over the -40 $^{\circ}$ C to +125 $^{\circ}$ C operating temperature range
+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V _{DD} to GND	-0.3V to +6V	Continuous Power Dissipation (T _A = +70°C)	
H ₋ , W ₋ , L ₋ to GND	-0.3V to the lower of (V _{DD} + 0.3V) and +6V	14-Pin TSSOP (derate 10mW/°C above +70°C)	796.8mW
All Other Pins to GND	-0.3V to +6V	Operating Temperature Range	-40°C to +125°C
Continuous Current into H ₋ , W ₋ , and L ₋		Junction Temperature	+150°C
MAX5389L	±5mA	Storage Temperature Range	-65°C to +150°C
MAX5389M	±2mA	Lead Temperature (soldering, 10s)	+300°C
MAX5389N	±1mA	Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.6V to +5.5V, V_{H-} = V_{DD}, V_{L-} = 0, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Resolution	N		256			Taps	
DC PERFORMANCE (Voltage-Divider Mode)							
Integral Nonlinearity	INL	(Note 2)	-0.5		+0.5	LSB	
Differential Nonlinearity	DNL	(Note 2)	-0.5		+0.5	LSB	
Dual Code Matching		Register A = register B	-0.5		+0.5	LSB	
Ratiometric Resistor Tempco		($\Delta V_W/V_W$)/ ΔT , no load		+5		LSB	
Full-Scale Error		Code = FFH	MAX5389L	-3	-2.5	LSB	
			MAX5389M	-1	-0.5		
			MAX5389N	-0.5	-0.25		
Zero-Scale Error		Code = 00H	MAX5389L		+2.5	LSB	
			MAX5389M		+0.5		
			MAX5389N		+0.25		
DC PERFORMANCE (Variable-Resistor Mode) (Note 3)							
Integral Nonlinearity	R-INL	V _{DD} > +2.6V	MAX5389L		±1.0	LSB	
			MAX5389M		±0.5		
			MAX5389N		±0.25		
		V _{DD} > +4.75V	MAX5389L		±0.4		LSB
			MAX5389M		±0.3		
			MAX5389N		±0.25		
Differential Nonlinearity	R-DNL	V _{DD} ≥ 2.6V	-0.5		+0.5	LSB	
DC PERFORMANCE (Resistor Characteristics)							
Wiper Resistance (Note 4)	R _{WL}	V _{DD} > 2.6V		250	600	Ω	
		V _{DD} > 4.75V		150	200		
Terminal Capacitance	C _{H-} , C _{L-}	Measured to GND		10		pF	
Wiper Capacitance	C _{W-}	Measured to GND		50		pF	
End-to-End Resistor Tempco	TCR	No load		35		ppm/°C	
End-to-End Resistor Tolerance	ΔR _{HL}	Wiper not connected	-25		+25	%	

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = +2.6V$ to $+5.5V$, $V_{H_} = V_{DD}$, $V_{L_} = 0$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DD} = +5V$, $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC PERFORMANCE						
Crosstalk		(Note 5)		-90		dB
-3dB Bandwidth	BW	Code = 80H, 10pF load, $V_{DD} = +2.6V$	MAX5389L	600		kHz
			MAX5389M	150		
			MAX5389N	75		
Total Harmonic Distortion Plus Noise	THD+N	Measured at W, $V_{H_} = 1V_{RMS}$ at 1kHz		0.015		%
Wiper Settling Time (Note 6)	t_s		MAX5389L	300		ns
			MAX5389M	1000		
			MAX5389N	2000		
POWER SUPPLIES						
Supply Voltage Range	V_{DD}		2.6		5.5	V
Standby Current		Digital inputs = V_{DD} or GND		1		μA
DIGITAL INPUTS						
Minimum Input High Voltage	V_{IH}		70			% x V_{DD}
Maximum Input Low Voltage	V_{IL}				30	% x V_{DD}
Input Leakage Current			-1		+1	μA
Input Capacitance				5		pF
TIMING CHARACTERISTICS (Note 7)						
Maximum $\overline{INC_}$ Frequency	f_{MAX}				10	MHz
\overline{CS} to $\overline{INC_}$ Setup Time	t_{CI}		25			ns
\overline{CS} to $\overline{INC_}$ Hold Time	t_{CH}		0			ns
$\overline{INC_}$ Low Period	t_{L}		25			ns
$\overline{INC_}$ High Period	t_{H}		25			ns
$UD_$ to $\overline{INC_}$ Setup Time	t_{DI}		50			ns
$UD_$ to $\overline{INC_}$ Hold Time	t_{DH}		0			ns

Note 1: All devices are 100% production tested at $T_A = +25^{\circ}C$. Specifications over temperature limits are guaranteed by design and characterization.

Note 2: DNL and INL are measured with the potentiometer configured as a voltage-divider (Figure 1) with $H_ = V_{DD}$ and $L_ = GND$. The wiper terminal is unloaded and measured with a high-input-impedance voltmeter.

Note 3: R-DNL and R-INL are measured with the potentiometer configured as a variable resistor (Figure 1). DNL and INL are measured with potentiometer configured as a variable resistor. $H_$ is unconnected and $L_ = GND$. For $V_{DD} = +5V$, the wiper terminal is driven with a source current of $400\mu A$ for the $10k\Omega$ configuration, $80\mu A$ for the $50k\Omega$ configuration, and $40\mu A$ for the $100k\Omega$ configuration. For $V_{DD} = +2.6V$, the wiper terminal is driven with a source current of $200\mu A$ for the $10k\Omega$ configuration, $40\mu A$ for the $50k\Omega$ configuration, and $20\mu A$ for the $100k\Omega$ configuration.

Note 4: The wiper resistance is the worst value measured by injecting the currents given in Note 3 into $W_$ with $L_ = GND$. $R_W = (V_W - V_H)/I_W$.

Note 5: Drive HA with a 1kHz, GND to V_{DD} amplitude, tone. LA = LB = GND. No load. WB is at midscale with a 10pF load. Measure WB.

Note 6: The wiper-settling time is the worst case 0 to 50% rise time, measured between tap 0 and tap 127. $H_ = V_{DD}$, $L_ = GND$, and the wiper terminal is loaded with 10pF capacitance to ground.

Note 7: Digital timing is guaranteed by design and characterization, not production tested.

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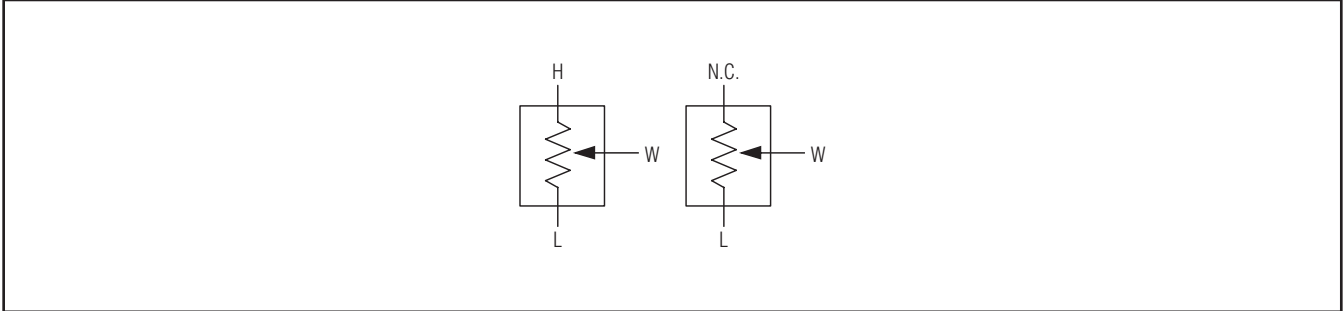
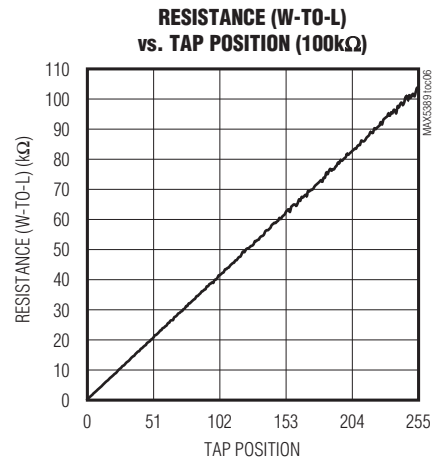
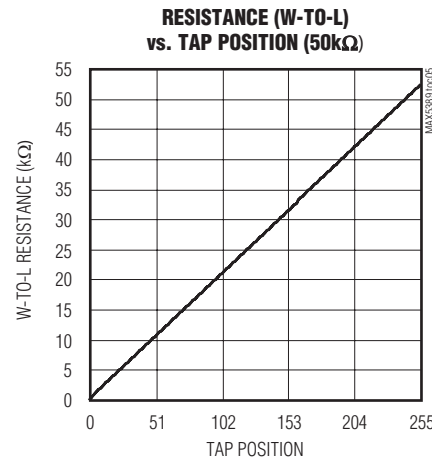
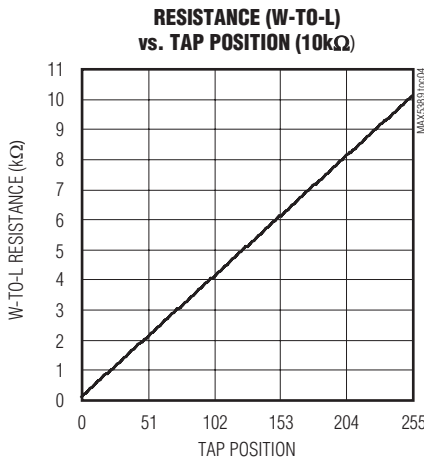
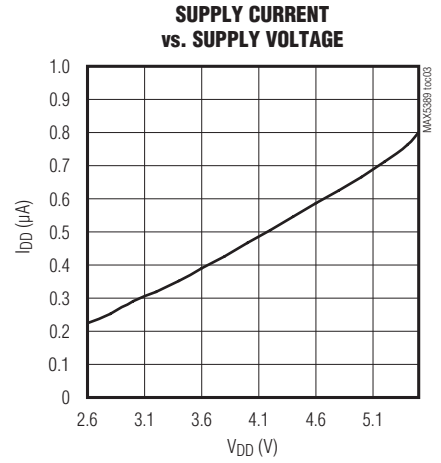
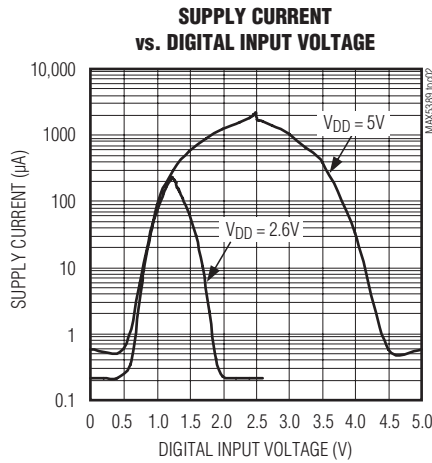
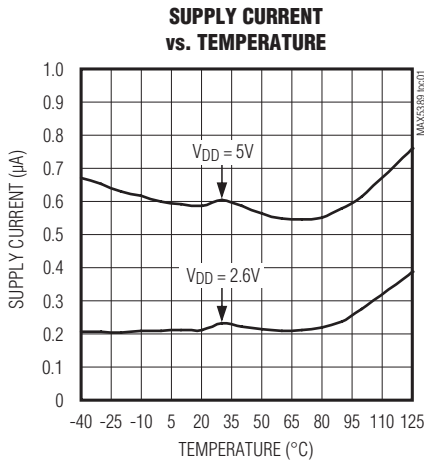


Figure 1. Voltage-Divider and Variable Resistor Configurations

Typical Operating Characteristics

($V_{DD} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

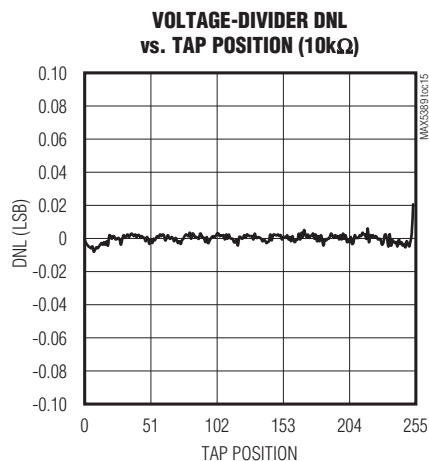
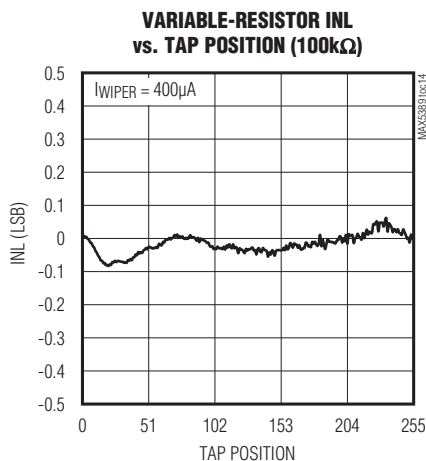
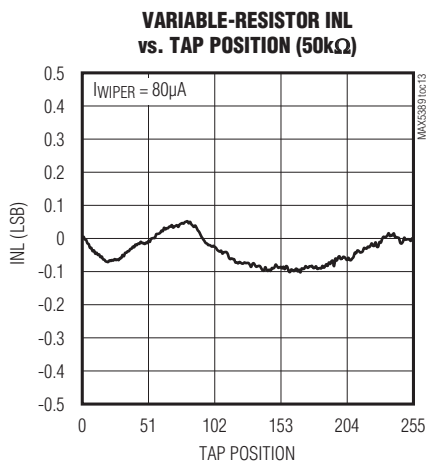
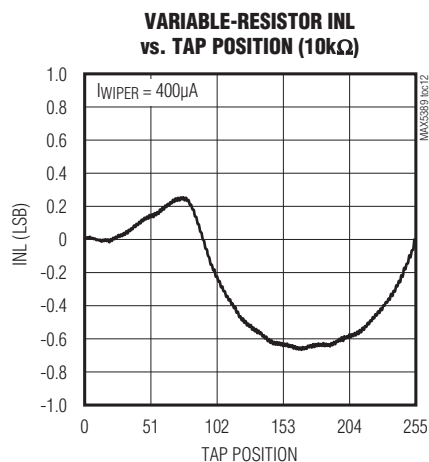
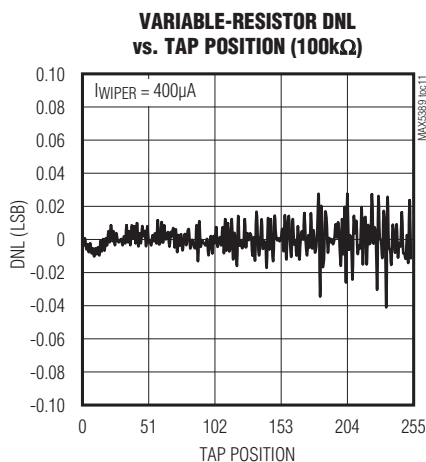
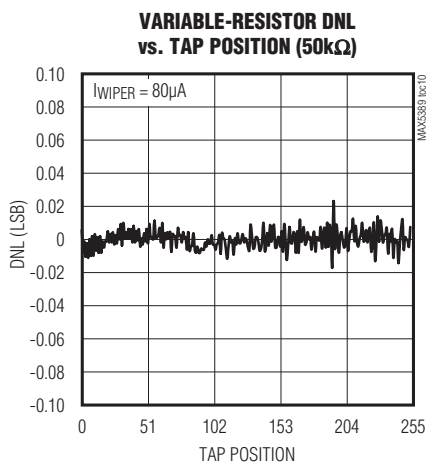
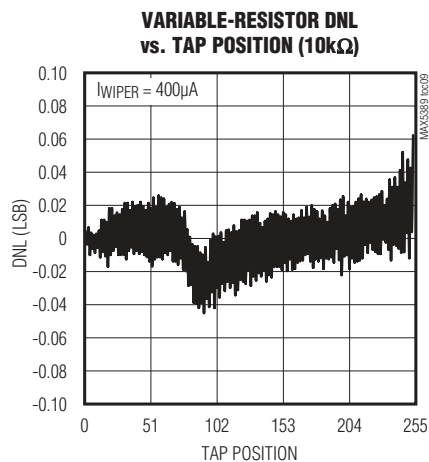
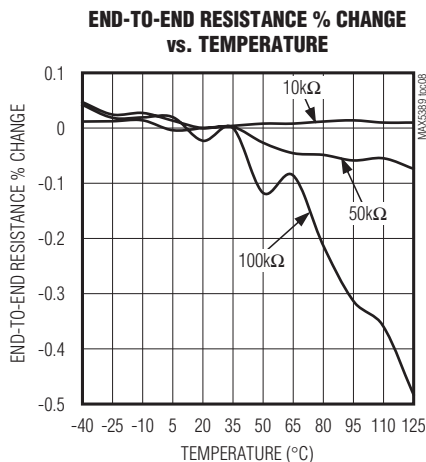
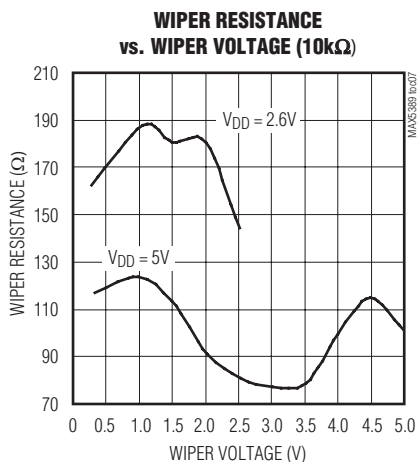


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Typical Operating Characteristics (continued)

($V_{DD} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

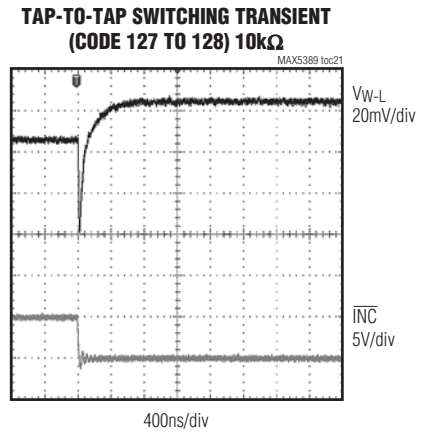
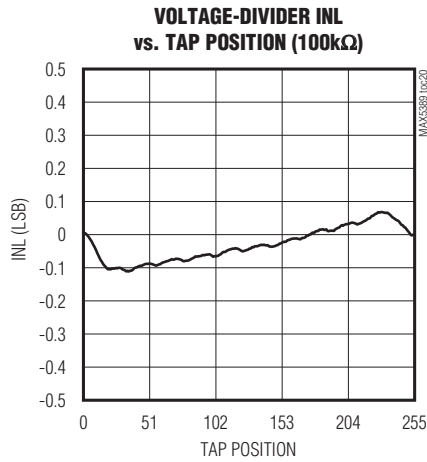
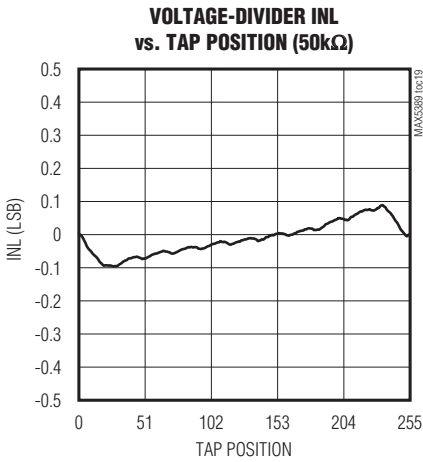
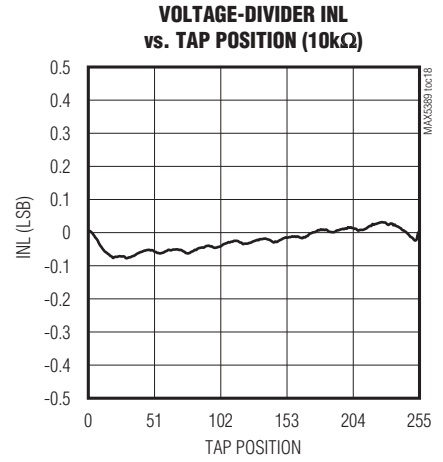
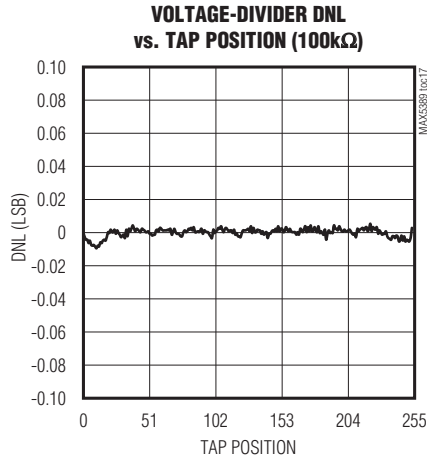
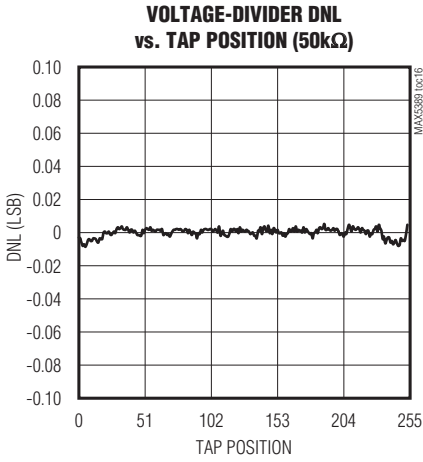
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Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)



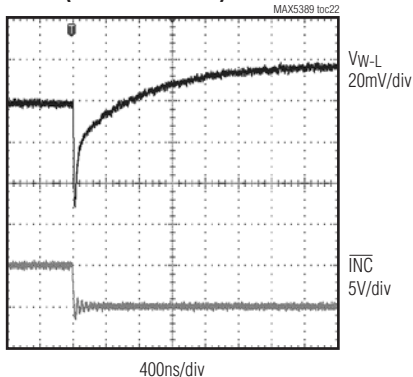
Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

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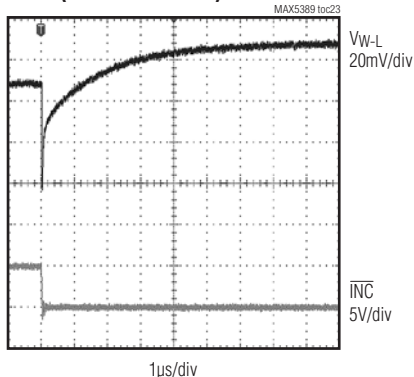
Typical Operating Characteristics (continued)

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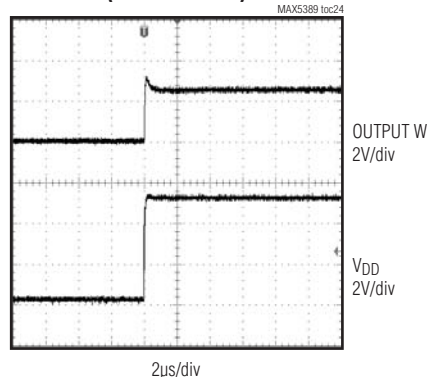
TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128) 50k Ω



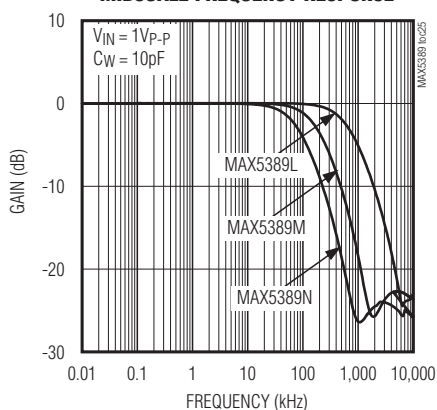
TAP-TO-TAP SWITCHING TRANSIENT (CODE 127 TO 128) 100k Ω



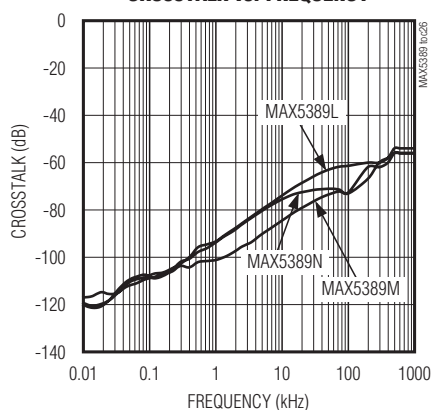
POWER-ON WIPER TRANSIENT (CODE 0 TO 128)



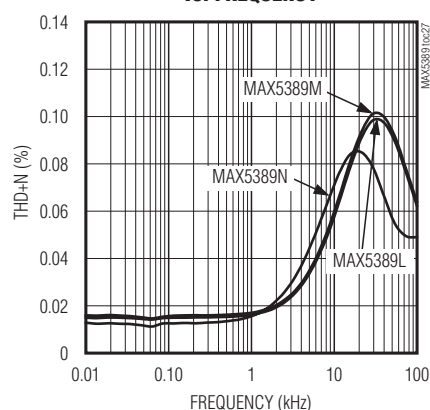
MIDSCALE FREQUENCY RESPONSE



CROSSTALK vs. FREQUENCY

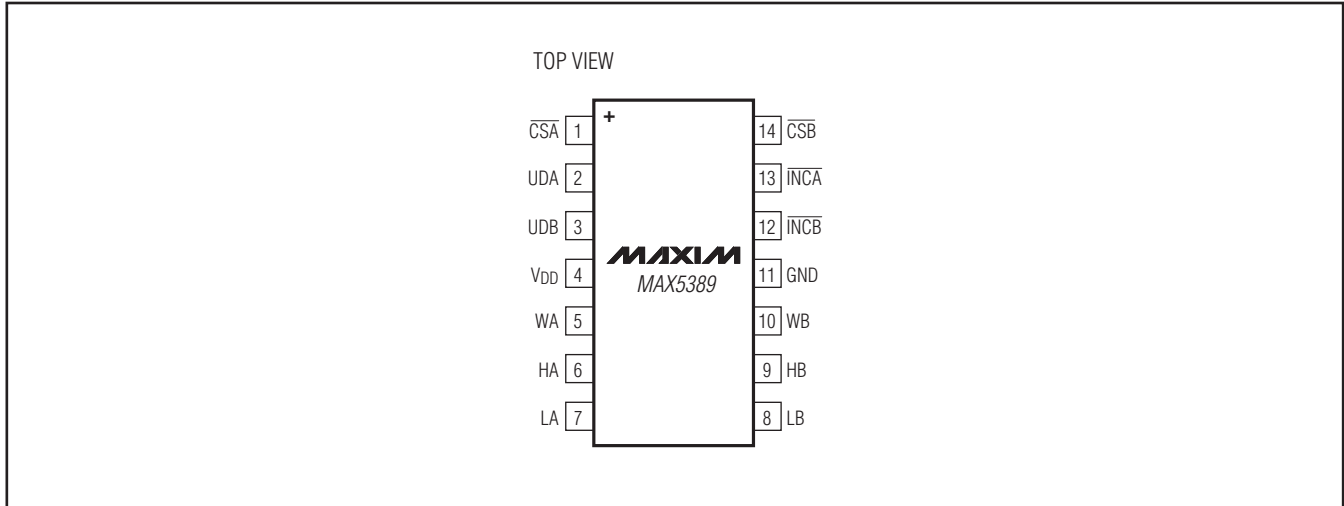


TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{CSA}}$	Active-Low Register A Chip-Select Input. Drive $\overline{\text{CSA}}$ low to change wiper position WA through $\overline{\text{INCA}}$ and UDA.
2	UDA	Register A Up/Down Control Input. With UDA low, a high-to-low transition at $\overline{\text{INCA}}$ decrements the WA position towards LA. With UDA high, a high-to-low transition at $\overline{\text{INCA}}$ increments WA position toward HA.
3	UDB	Register B Up/Down Control Input. With UDB low, a high-to-low transition at $\overline{\text{INCB}}$ decrements the WB position towards LB. With UDB high, a high-to-low transition at $\overline{\text{INCB}}$ increments WB position toward HB.
4	VDD	Power-Supply Input. Bypass VDD to GND with a 0.1 μ F capacitor close to the device.
5	WA	Resistor A Wiper Terminal
6	HA	Resistor A High Terminal. The voltage at HA can be higher or lower than the voltage at LA. Current can flow into or out of HA.
7	LA	Resistor A Low Terminal. The voltage at LA can be higher or lower than the voltage at HA. Current can flow into or out of LA.
8	LB	Resistor B Low Terminal. The voltage at LB can be higher or lower than the voltage at HB. Current can flow into or out of LB.
9	HB	Resistor B High Terminal. The voltage at HB can be higher or lower than the voltage at LB. Current can flow into or out of HB.
10	WB	Resistor B Wiper Terminal
11	GND	Ground
12	$\overline{\text{INCB}}$	Register B Wiper Increment Control Input. With UDB low, a high-to-low transition at $\overline{\text{INCB}}$ decrements the WB position towards LB. With UDB high, a high-to-low transition at $\overline{\text{INCB}}$ increments WB position toward HB.
13	$\overline{\text{INCA}}$	Register A Wiper Increment Control Input. With UDA low, a high-to-low transition at $\overline{\text{INCA}}$ decrements the WA position towards LA. With UDA high, a high-to-low transition at $\overline{\text{INCA}}$ increments WA position toward HA.
14	$\overline{\text{CSB}}$	Active-Low Register B Chip-Select Input. Drive $\overline{\text{CSB}}$ low to change wiper position WA through $\overline{\text{INCB}}$ and UDB.

Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

Detailed Description

The MAX5389 dual, 256-tap, volatile, low-voltage linear taper digital potentiometer offers three end-to-end resistance values of 10kΩ, 50kΩ, and 100kΩ. The potentiometer consists of 255 fixed resistors in series between terminals H₋ and L₋. The potentiometer wiper, W₋, is programmable to access any one of the 256 tap points on the resistor string. On power-up, the wiper position is set to midscale (tap 128).

The potentiometers are programmable independent of each other. The MAX5389 features an up/down interface.

Up/Down Interface

Logic inputs \overline{CS}_- , UD₋, and \overline{INC}_- determine the wiper position of the device (Table 1). With \overline{CS}_- low and UD₋ high, a high-to-low (falling edge) transition on \overline{INC}_- increments the internal counter which moves the wiper, W₋, closer to H₋. When both \overline{CS}_- and UD₋ are low, the falling edge of \overline{INC}_- decrements the internal counter

and moves the tap point, W₋ closer to L₋, (Figure 2). The wiper performs a make-before-break transition ensuring that W₋ is never disconnected from the resistor string during a transition from one tap point to another. When the wiper is at either end of the resistor array additional transitions in the direction of the end point do not change the counter value.

Table 1. Up/Down Control Table

\overline{CS}_-	UD ₋	\overline{INC}_-	W ₋
H	X	X	No change
L	L	↑	No change
L	H	↑	No change
L	L	↓	Decrement
L	H	↓	Increment

X = Don't care.
 ↑ = Low-to-high transition.
 ↓ = High-to-low transition.

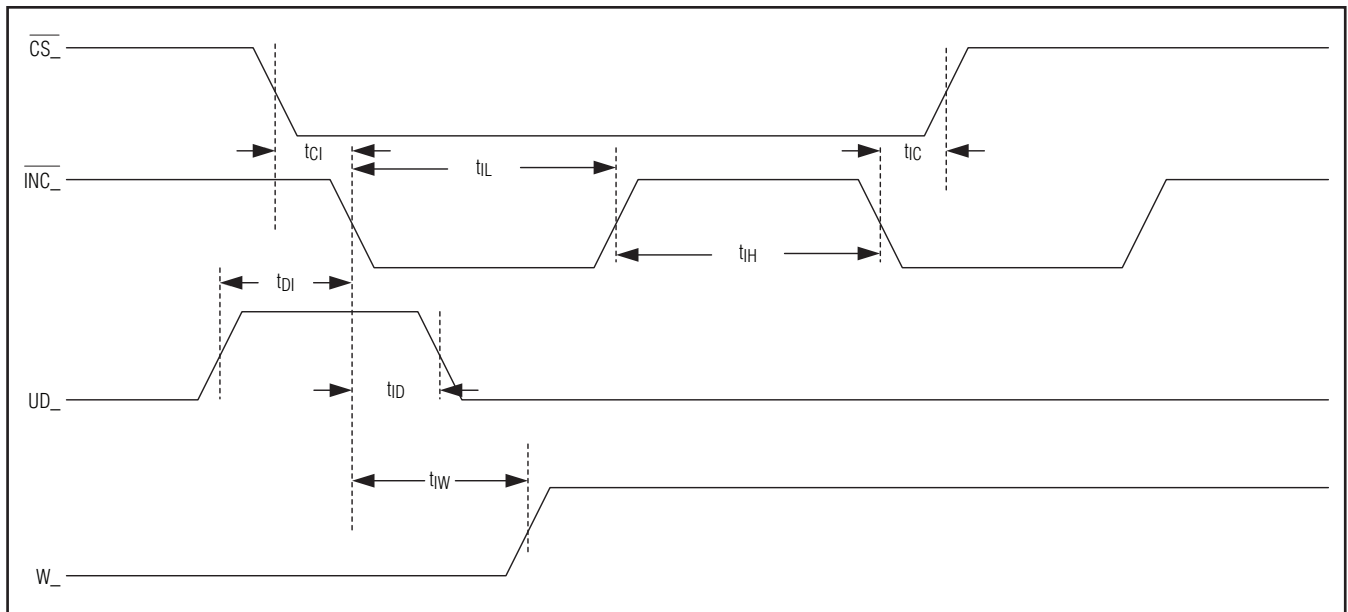


Figure 2. Up/Down Interface Timing Diagram

Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

Applications Information

Variable Gain Amplifier

Figure 3 shows a potentiometer adjusting the gain of a noninverting amplifier. Figure 4 shows a potentiometer adjusting the gain of an inverting amplifier.

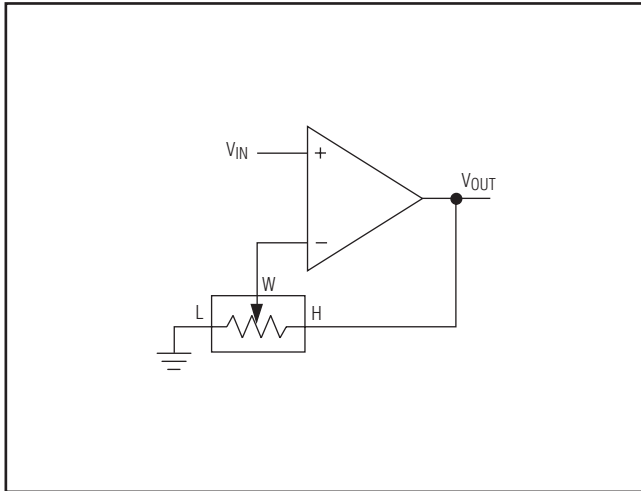


Figure 3. Variable Gain Noninverting Amplifier

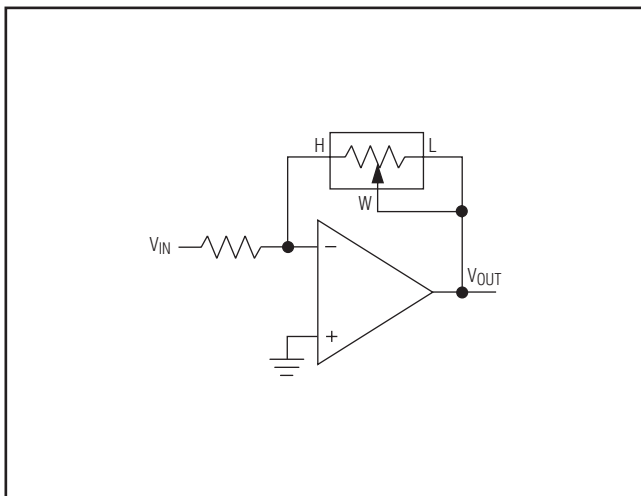


Figure 4. Variable Gain Inverting Amplifier

Adjustable Dual Linear Regulator

Figure 5 shows an adjustable dual linear regulator using a dual potentiometer as two variable resistors.

Adjustable Voltage Reference

Figure 6 shows an adjustable voltage reference circuit using a potentiometer as a voltage-divider.

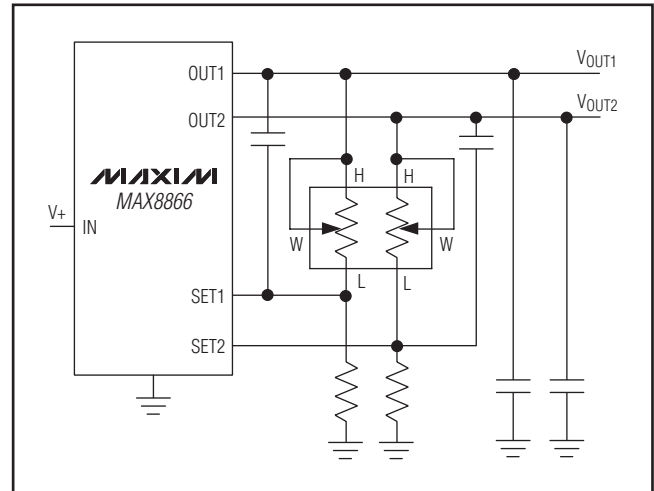


Figure 5. Adjustable Dual Linear Regulator

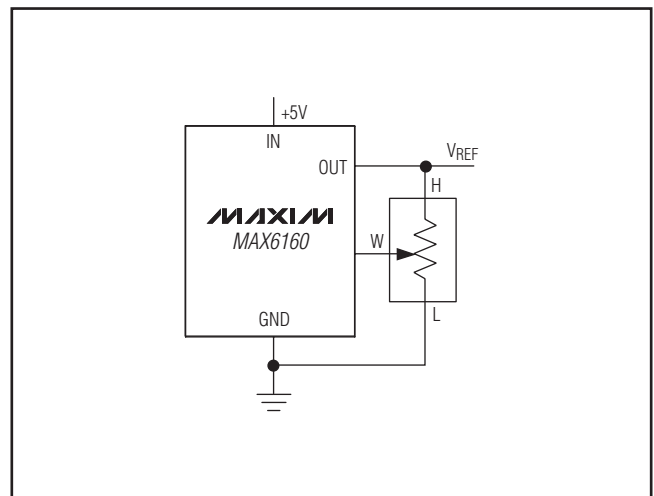


Figure 6. Adjustable Voltage Reference

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Variable Gain Current to Voltage Converter

Figure 7 shows a variable gain current to voltage converter using a potentiometer as a variable resistor.

LCD Bias Control

Figure 8 shows a positive LCD bias control circuit using a potentiometer as a voltage-divider.

Figure 9 shows a positive LCD bias control circuit using a potentiometer as a variable resistor.

Programmable Filter

Figure 10 shows a programmable filter using a dual potentiometer.

Offset Voltage Adjustment Circuit

Figure 11 shows an offset voltage adjustment circuit using a dual potentiometer.

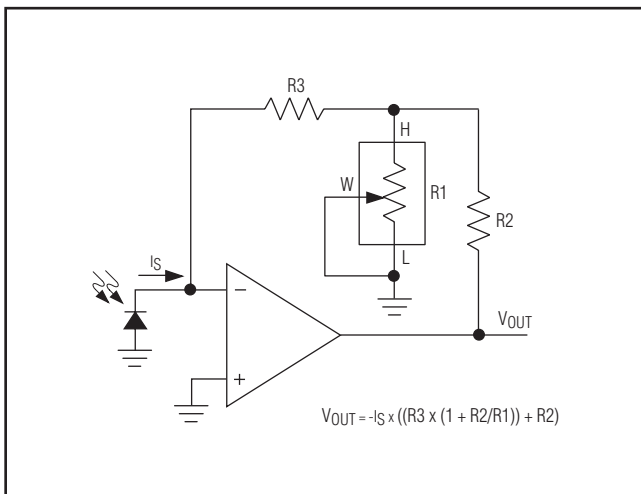


Figure 7. Variable Gain I-to-V Converter

$$V_{OUT} = -I_s \times ((R3 \times (1 + R2/R1)) + R2)$$

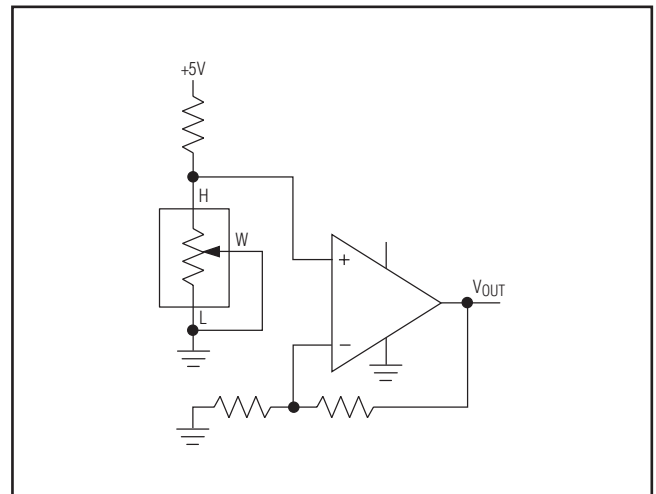


Figure 9. Positive LCD Bias Control Using a Variable Resistor

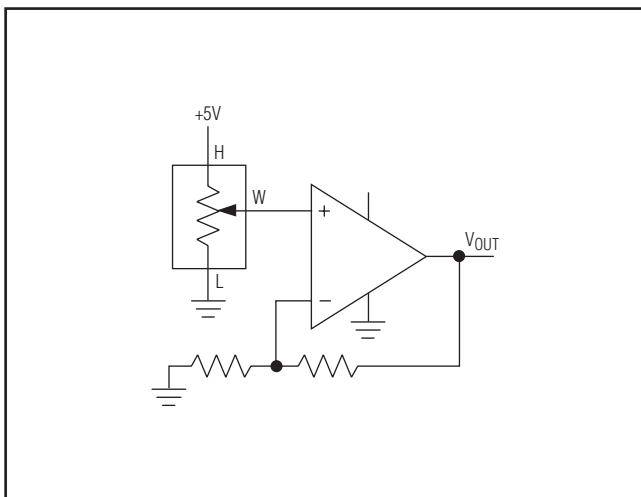


Figure 8. Positive LCD Bias Control Using a Voltage-Divide

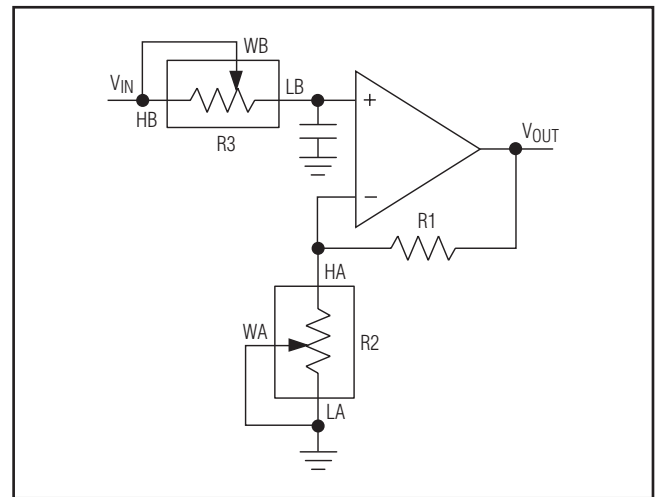


Figure 10. Programmable Filter

Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

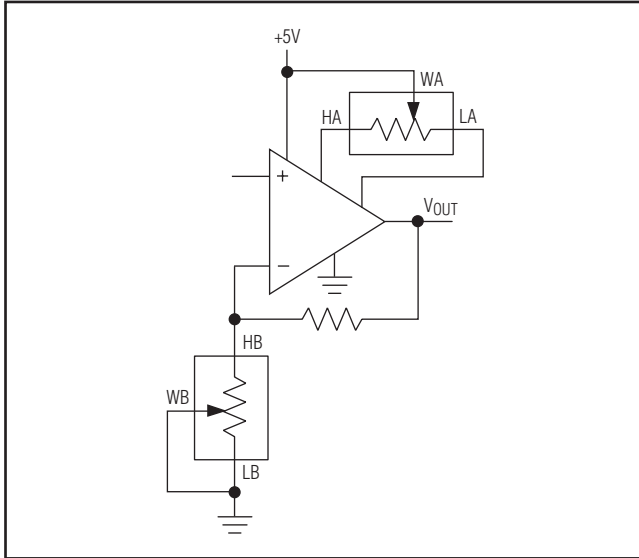


Figure 11. Offset Voltage Adjustment Circuit

Process Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	21-0066	90-0113

Dual, 256-Tap, Volatile, Low-Voltage Linear Taper Digital Potentiometer

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/10	Initial release	—
1	4/10	Added Soldering Temperature in <i>Absolute Maximum Ratings</i> ; corrected code in Conditions of -3dB Bandwidth specification in <i>Electrical Characteristics</i> ; corrected Table 1 and Figure 5	2, 3, 9, 10
2	11/10	Updated <i>Electrical Characteristics</i> table globals, updated drawings for optimal circuit operation	2, 3, 10, 11, 12

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