19-3511; Rev 3; 11/07

EVALUATION KIT AVAILABLE

32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

General Description

The MAX5432–MAX5435 nonvolatile, linear-taper, digital potentiometers perform the function of a mechanical potentiometer, but replace the mechanics with a simple 2-wire serial interface. Each device performs the same function as a discrete potentiometer or a variable resistor and has 32 tap points.

The MAX5432–MAX5435 feature an internal, nonvolatile, electrically erasable programmable read-only memory (EEPROM) that returns the wiper to its previously stored position at power-up. The fast-mode I²C-compatible serial interface allows communication at data rates up to 400kbps, minimizing board space and reducing interconnection complexity. Each device is available with multiple factory-preset I²C addresses (see the *Ordering Information/Selector Guide*).

Use the MAX5432–MAX5435 in applications requiring digitally controlled resistors. Two resistance values are available (50kΩ and 100kΩ) in a voltage-divider or variable resistor configuration. The nominal resistor temperature coefficient is 35ppm/°C end-to-end, and only 5ppm/°C ratiometric, making the devices ideal for applications requiring a low-temperature-coefficient variable resistor such as low-drift, programmable-gain amplifier circuit configurations.

The MAX5432/MAX5433 are available in a 3mm x 3mm 8-pin TDFN package and the MAX5434/MAX5435 are available in a 6-pin thin SOT23 package. The MAX5432–MAX5435 are specified over the extended (-40°C to +85°C) temperature range.

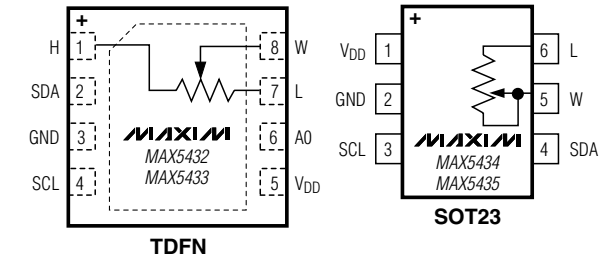
Applications

Mechanical Potentiometer Replacement
Low-Drift Programmable-Gain Amplifiers
Volume Control
Liquid-Crystal Display (LCD) Screen Adjustment

Features

- **Tiny 3mm x 3mm 8-Pin TDFN and 6-Pin Thin SOT23 Packages**
- **Power-On Recall of Wiper Position from Nonvolatile Memory**
- **35ppm/°C End-to-End Resistance Temperature Coefficient**
- **5ppm/°C Ratiometric Temperature Coefficient**
- **50kΩ/100kΩ Resistor Values**
- **Fast 400kbps I²C-Compatible Serial Interface**
- **500nA (typ) Static Supply Current**
- **+2.7V to +5.25V Single-Supply Operation**
- **32 Tap Positions**
- **±0.15 LSB INL (typ), ±0.15 LSB DNL (typ)**

Pin Configurations



Ordering Information/Selector Guide

PART	PIN-PACKAGE	TOP MARK	I²C ADDRESS	R (kΩ)	PKG CODE
MAX5432LETA+	8 TDFN-EP*	ANG	010100A_0**	50	T833-1
MAX5432META+	8 TDFN-EP*	ANI	010110A_0**	50	T833-1
MAX5433LETA+	8 TDFN-EP*	ANF	010100A_0**	100	T833-1
MAX5433META+	8 TDFN-EP*	ANH	010110A_0**	100	T833-1
MAX5434LEZT+T	6 Thin SOT23-6	AABX	0101000	50	Z6-1

*EP = Exposed pad.
**A_0 represents the logic state of input A0 of the device in the TDFN package.
+Denotes a lead-free package.
T = Tape and reel.
Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

Ordering Information/Selector Guide continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6.0V
SDA, SCL to GND.....-0.3V to +6.0V
A0, H, L, and W to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Continuous Current into H, L, and W
MAX5432/MAX5434.....±1.3mA
MAX5433/MAX5435.....±0.6mA
Input/Output Latchup Immunity.....±50mA

Continuous Power Dissipation (T_A = +70°C)
6-Pin Thin SOT23 (derate 9.1mW/°C above +70°C)....727mW
8-Pin TDFN (derate 18.2mW/°C above +70°C) 1454.5mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Resolution				32			Taps
End-to-End Resistance	R_{H-L}	MAX5432/MAX5434		37.5	50	62.5	kΩ
		MAX5433/MAX5435		75	100	125	
End-to-End Resistance Temperature Coefficient	TC_R				35		ppm/°C
Ratiometric Resistance Temperature Coefficient					5		ppm/°C
Integral Nonlinearity	INL	Variable resistor (Note 2)	V_{DD} = 5V		±0.15	±0.5	LSB
			V_{DD} = 3V		±0.15	±0.5	
		Voltage-divider, MAX5432/MAX5433 (Note 3)	V_{DD} = 5V		±0.15	±0.5	
			V_{DD} = 3V		±0.15	±0.5	
Differential Nonlinearity	DNL	Variable resistor (Note 2)	V_{DD} = 5V		±0.15	±0.5	LSB
			V_{DD} = 3V		±0.15	±0.5	
		Voltage-divider, MAX5432/MAX5433 (Note 3)	V_{DD} = 5V		±0.15	±0.5	
			V_{DD} = 3V		±0.15	±0.5	
Full-Scale Error (Note 4)		MAX5432, 50kΩ				-0.5	LSB
		MAX5433, 100kΩ				-0.5	
Zero-Scale Error (Note 5)		MAX5432, 50kΩ				+0.5	LSB
		MAX5433, 100kΩ				+0.5	
Wiper Resistance	R_W	MAX5432/MAX5433 (Note 6)			610	1200	Ω
DIGITAL INPUTS							
Input High Voltage	V_{IH}	(Note 7)		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}	(Note 7)				0.3 x V_{DD}	V
Input Leakage Current	I_{LEAK}					±1	µA
Input Capacitance					5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
-3dB Bandwidth (Note 8)		MAX5432/MAX5434		500		kHz
		MAX5433/MAX5435		250		
Wiper Settling Time (Note 9)		MAX5432/MAX5434		0.5		µs
		MAX5433/MAX5435		1.0		
NONVOLATILE MEMORY RELIABILITY						
Data Retention		T_A = +85°C		50		Years
Endurance		T_A = +25°C		200,000		Stores
		T_A = +85°C		50,000		
POWER SUPPLY						
Power-Supply Voltage	V_{DD}		2.70		5.25	V
Standby Current	I_{DD}	Digital inputs = V_{DD} or GND, T_A = +25°C		0.5	2	µA
Programming Current		During nonvolatile write; digital inputs = V_{DD} or GND (Note 10)		200	900	µA

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Figures 1 and 2) (Note 11)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}				400	kHz
Setup Time for START Condition	t_{SU-STA}		0.6			µs
Hold Time for START Condition	t_{HD-STA}		0.6			µs
CLK High Time	t_{HIGH}		0.6			µs
CLK Low Time	t_{LOW}		1.3			µs
Data Setup Time	t_{SU-DAT}		100			ns
Data Hold Time	t_{HD-DAT}		0		0.9	µs
SDA, SCL Rise Time	t_R				300	ns
SDA, SCL Fall Time	t_F				300	ns
Setup Time for STOP Condition	t_{SU-STO}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
Pulse Width of Spike Suppressed	t_{SP}			50		ns
Capacitive Load for Each Bus Line	C_B	(Note 12)		400		pF
Nonvolatile Store Time		Idle time required after a nonvolatile memory write (Note 13)			12	ms

Note 1: All devices are production tested at T_A = +25°C and are guaranteed by design and characterization for -40°C < T_A < +85°C.

32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

TIMING CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, V_H = V_{DD}, V_L = GND, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{DD} = +5V, T_A = +25°C.) (Figures 1 and 2) (Note 1)

Note 2: The DNL and INL are measured with the potentiometer configured as a variable resistor. For the 3-terminal potentiometers (MAX5432/MAX5433), H is unconnected and L = GND. At V_{DD} = 5V, W is driven with a source current of 80µA for the 50kΩ configuration, and 40µA for the 100kΩ configuration. At V_{DD} = 3V, W is driven with a source current of 40µA for the 50kΩ configuration, and 20µA for the 100kΩ configuration.

Note 3: The DNL and INL are measured with the potentiometer configured as a voltage-divider with H = V_{DD} and L = GND (MAX5432/MAX5433 only). The wiper terminal is unloaded and measured with an ideal voltmeter.

Note 4: Full-scale error is defined as $\frac{V_W - V_H}{\left(\frac{V_H}{31}\right)}$.

Note 5: Zero-scale error is defined as $\frac{V_W - V_L}{\left(\frac{V_H}{31}\right)}$.

Note 6: The wiper resistance is the worst value measured by injecting the currents given in Note 2 into W with L = GND. $R_W = (V_W - V_H) / I_W$.

Note 7: The device draws current in excess of the specified supply current when the digital inputs are driven with voltages between (V_{DD} - 0.5V) and (GND + 0.5V). See the Supply Current vs. Digital Input Voltage graph in the *Typical Operating Characteristics*.

Note 8: Wiper is at midscale with a 10pF capacitive load. Potentiometer set to midscale, L = GND, an AC source is applied to H, and the output is measured as 3dB lower than the DC W/H value in dB.

Note 9: This is measured from the STOP pulse to the time it takes the output to reach 50% of the output step size (divider mode). It is measured with a maximum external capacitive load of 10pF.

Note 10: The programming current exists only during NV writes (12ms typ).

Note 11: Digital timing is guaranteed by design and characterization, and is not production tested.

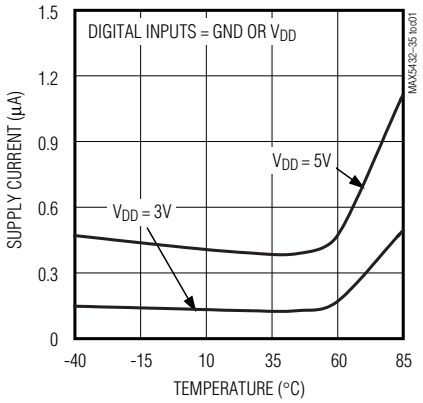
Note 12: An appropriate bus pullup resistance must be selected depending on board capacitance. Refer to the I²C-bus specification document linked to this web address: www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf

Note 13: The idle time begins from the initiation of the stop pulse.

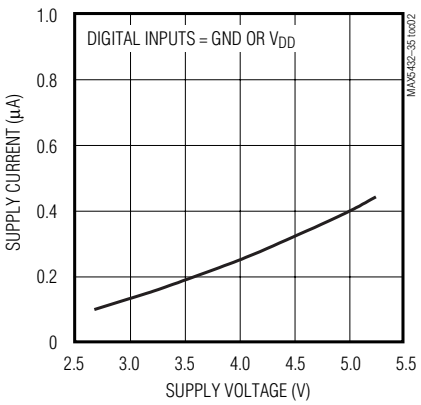
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

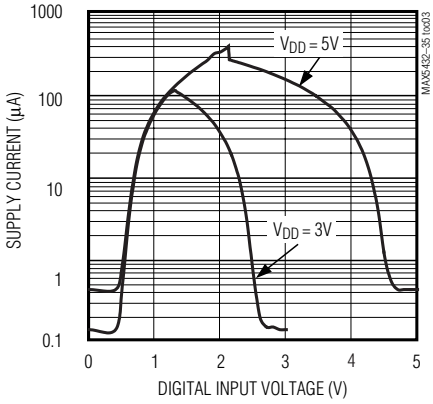
STANDBY SUPPLY CURRENT vs. TEMPERATURE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



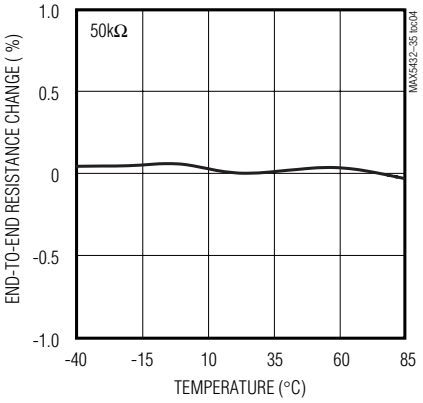
SUPPLY CURRENT vs. DIGITAL INPUT VOLTAGE



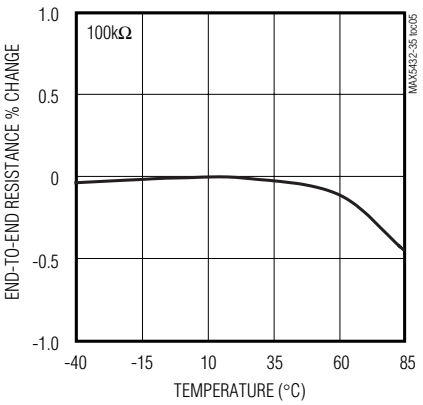
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

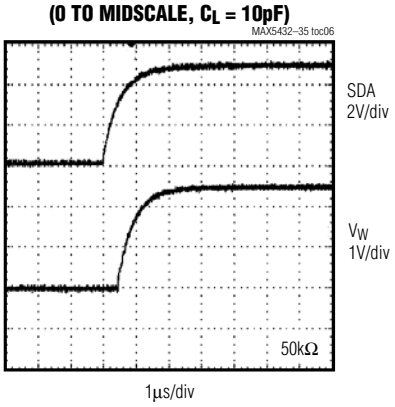
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



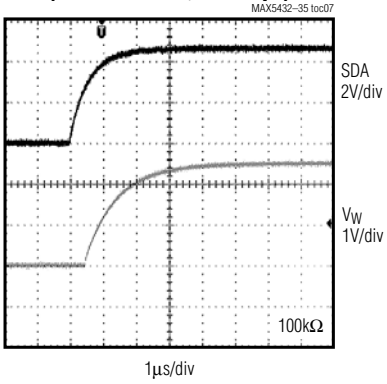
END-TO-END RESISTANCE % CHANGE vs. TEMPERATURE



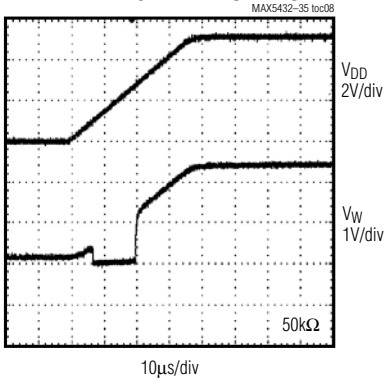
TAP-TO-TAP SWITCHING TRANSIENT (0 TO MIDSCALE, C_L = 10pF)



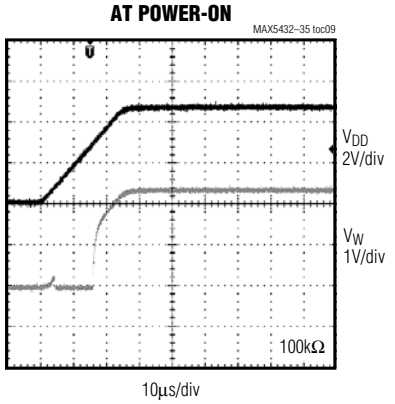
TAP-TO-TAP SWITCHING TRANSIENT (0 TO MIDSCALE, C_L = 10pF)



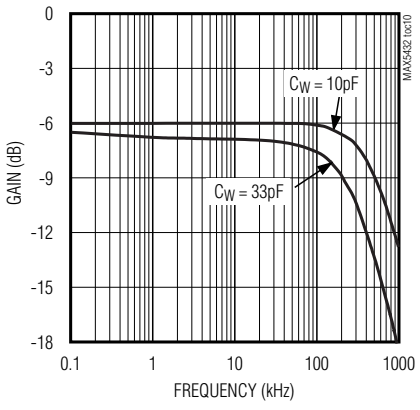
WIPER TRANSIENT AT POWER-ON



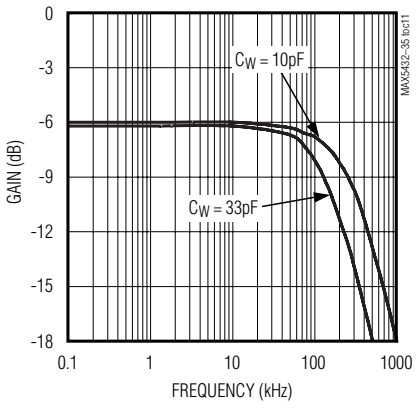
MIDSCALE WIPER TRANSIENT AT POWER-ON



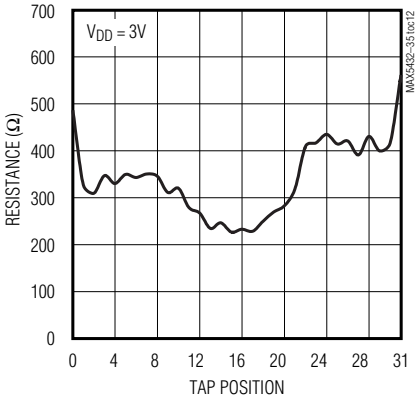
MIDSCALE WIPER RESPONSE vs. FREQUENCY (MAX5432)



MIDSCALE WIPER RESPONSE vs. FREQUENCY (MAX5433)



WIPER RESISTANCE vs. TAP POSITION (MAX5432)

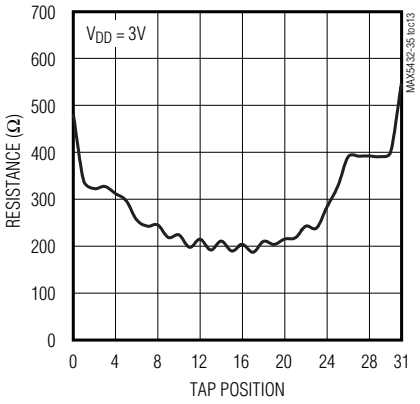


32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

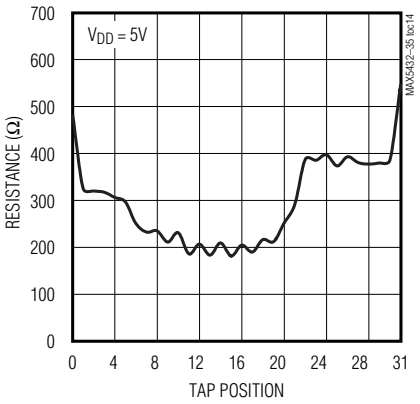
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

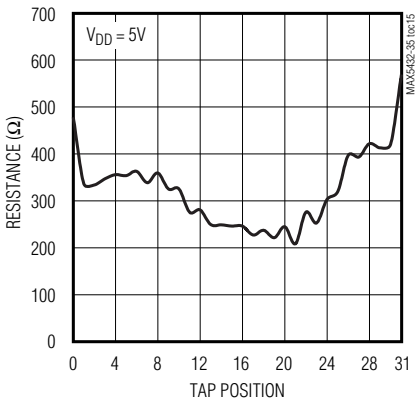
WIPER RESISTANCE vs. TAP POSITION (MAX5433)



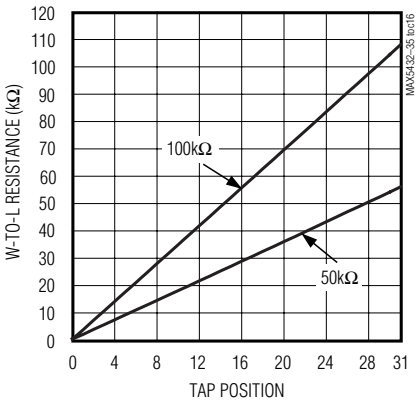
WIPER RESISTANCE vs. TAP POSITION (MAX5432)



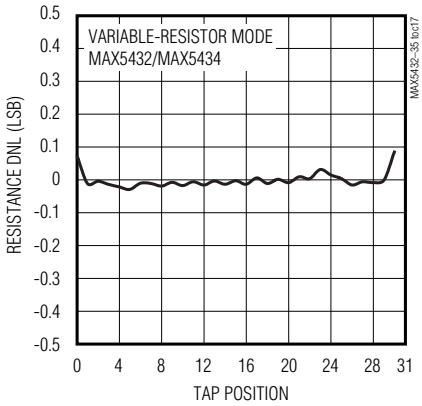
WIPER RESISTANCE vs. TAP POSITION (MAX5433)



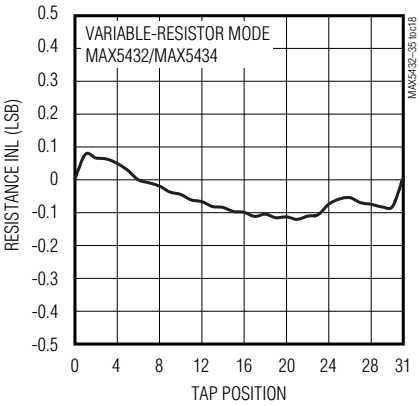
W-TO-L RESISTANCE vs. TAP POSITION



RESISTANCE DNL vs. TAP POSITION



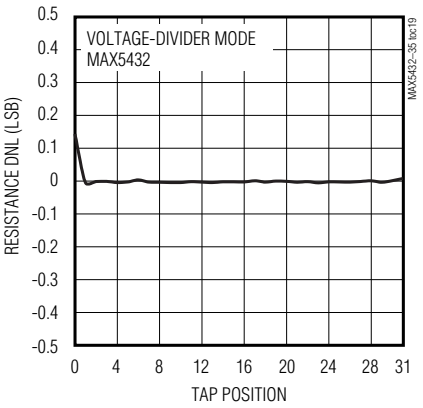
RESISTANCE INL vs. TAP POSITION



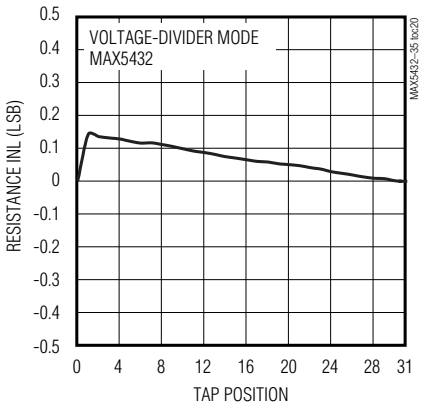
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

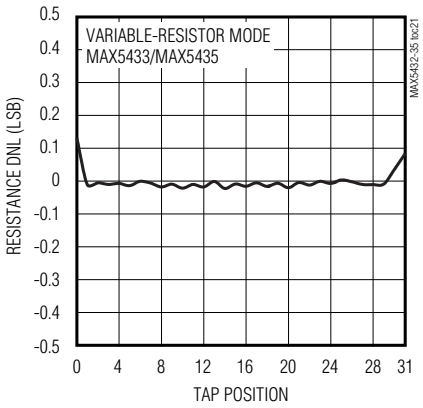
RESISTANCE DNL vs. TAP POSITION



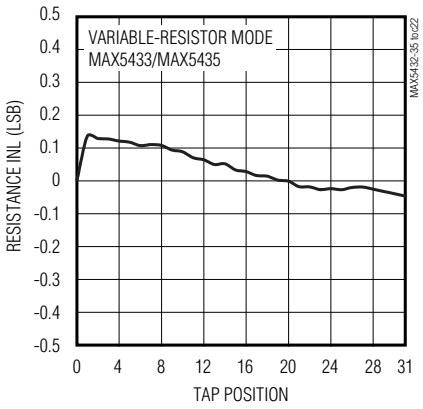
RESISTANCE INL vs. TAP POSITION



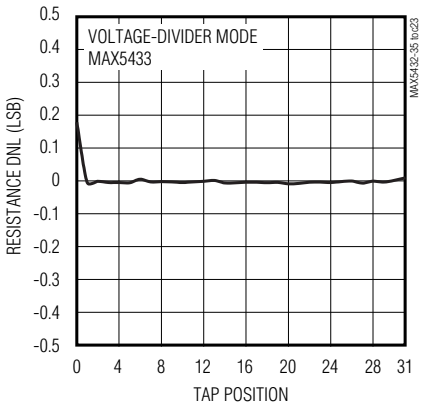
RESISTANCE DNL vs. TAP POSITION



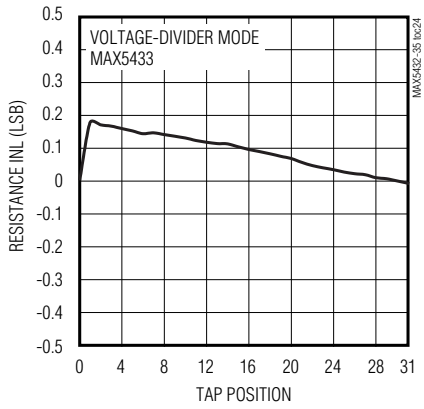
RESISTANCE INL vs. TAP POSITION



RESISTANCE DNL vs. TAP POSITION



RESISTANCE INL vs. TAP POSITION



32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

Pin Description

PIN		NAME	FUNCTION
TDFN	THIN SOT23		
1	—	H	High Terminal
2	4	SDA	I²C-Compatible Interface Data Input
3	2	GND	Ground
4	3	SCL	I²C-Compatible Interface Clock Input
5	1	V_{DD}	Power-Supply Input. Bypass with a 0.1µF capacitor from V_{DD} to GND.
6	—	A0	Address Input. Sets the I²C address. Connect to V_{DD} or GND. Do not leave A0 floating.
7	6	L	Low Terminal
8	5	W	Wiper Terminal
EP	—	EP	Exposed Pad. Internally connected to GND.

Detailed Description

The MAX5432–MAX5435 contain a resistor array with 31 resistive elements. The MAX5432/MAX5434 provide a total end-to-end resistance of 50kΩ, and the MAX5433/MAX5435 provide an end-to-end resistance of 100kΩ.

The MAX5432/MAX5433 allow access to the high, low, and wiper terminals for a standard voltage-divider configuration. Connect H, L, and W in any desired configuration as long as their voltages fall between GND and V_{DD}. The MAX5434/MAX5435 are variable resistors with H internally connected to the wiper.

A simple 2-wire I²C-compatible serial interface moves the wiper among the 32 tap points. Eight data bits, an address byte, and a control byte program the wiper position. A nonvolatile memory stores and recalls the wiper position in the nonvolatile memory upon power-up. The nonvolatile memory is guaranteed for 200,000 wiper store cycles and 50 years for wiper data retention.

Digital Interface

The MAX5432–MAX5435 feature an internal, nonvolatile EEPROM that returns the wiper to its previously stored position at power-up. The shift register decodes the control and address bits, routing the data to the proper memory registers. Write data to the volatile memory register to immediately update the wiper position, or write data to the nonvolatile register for storage. Writing to the nonvolatile register takes a minimum of 12ms.

The volatile register retains data as long as the device is enabled and powered. Removing power clears the volatile register. The nonvolatile register retains data even after power is removed. Upon power-up, the power-on reset circuitry and internal oscillator control the transfer of data from the nonvolatile register to the volatile register.

Serial Addressing

The MAX5432–MAX5435 operate as a slave that sends and receives data through an I²C- and SMBus™-compatible 2-wire interface. The interface uses a serial data access (SDA) line and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to and from the MAX5432–MAX5435, and generates the SCL clock that synchronizes the data transfer (Figure 1).

SDA operates as both an input and an open-drain output. SDA requires a pullup resistor, typically 4.7kΩ. SCL only operates as an input. SCL requires a pullup resistor (4.7kΩ typ) if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output.

Each transmission consists of a START (S) condition (Figure 3) sent by a master, followed by the MAX5432–MAX5435 7-bit slave address plus the 8th bit (Figure 4), 1 command byte (Figure 7) and 1 data byte, and finally a STOP (P) condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning the SDA from low to

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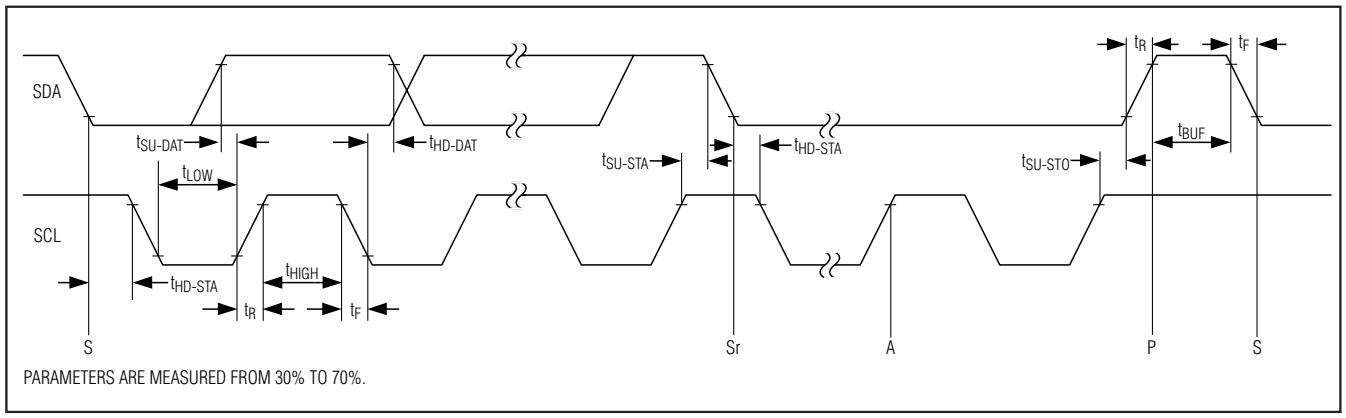


Figure 1. I²C Serial-Interface Timing Diagram

high while SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable while SCL is high (Figure 5).

Acknowledge

The acknowledge bit is a clocked 9th bit that the recipient uses to handshake receipt of each byte of data (Figure 6). Each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, so the SDA line is stable low during the high period of the clock pulse. When the master transmits to the MAX5432–MAX5435, the devices generate the acknowledge bit because the MAX5432–MAX5435 are the recipients.

Slave Address

The MAX5432–MAX5435 have a 7-bit-long slave address (Figure 4). The 8th bit following the 7-bit slave address is the NOP/$\overline{W}$ bit. Set the NOP/$\overline{W}$ bit low for a write command and high for a no-operation command.

Table 1a shows four possible slave addresses for the MAX5432/MAX5433 and Table 1b shows three possible slave addresses for the MAX5434/MAX5435. The first 4 bits (MSBs) of the slave addresses are always 0101. Bits A2 and A1 are factory programmed for the MAX5432/MAX5433 (Table 1a). Connect the A0 input (MAX5432/MAX5433 only) to either GND or V_{DD} to select one of two I²C device addresses. Each device must have a unique address to share the bus. A maximum of four MAX5432/MAX5433 devices can share the same bus. Bits A2, A1, and A0 are factory programmed for the MAX5434/MAX5435 (Table 1b).

Table 1a. Address Codes (MAX5432/MAX5433 Only)

PART SUFFIX	ADDRESS BYTE							
	A6	A5	A4	A3	A2	A1	A0	NOP/$\overline{W}$
L	0	1	0	1	0	0	0	NOP/$\overline{W}$
L	0	1	0	1	0	0	1	NOP/$\overline{W}$
M	0	1	0	1	1	0	0	NOP/$\overline{W}$
M	0	1	0	1	1	0	1	NOP/$\overline{W}$

Table 1b. Address Codes (MAX5434/MAX5435 Only)

PART SUFFIX	ADDRESS BYTE							
	A6	A5	A4	A3	A2	A1	A0	NOP/$\overline{W}$
L	0	1	0	1	0	0	0	NOP/$\overline{W}$
M	0	1	0	1	1	0	0	NOP/$\overline{W}$
N*	0	1	0	1	0	1	0	NOP/$\overline{W}$

**MAX5434 only.*

Message Format for Writing

A write to the MAX5432–MAX5435 consists of the transmission of the device's slave address with the 8th bit set to zero, followed by at least 1 byte of information. The 1st byte of information is the command byte. The bytes received after the command byte are the data bytes. The 1st data byte goes into the internal register of the MAX5432–MAX5435 as selected by the command byte (Figure 8).

32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

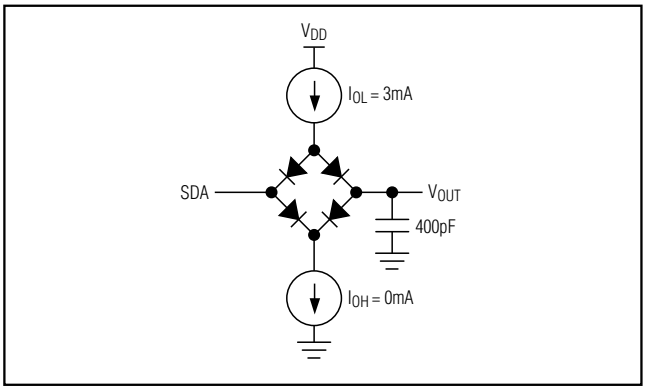


Figure 2. Load Circuit

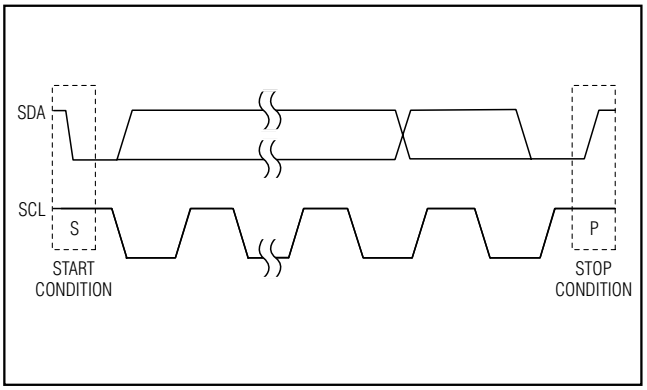


Figure 3. Start and Stop Conditions

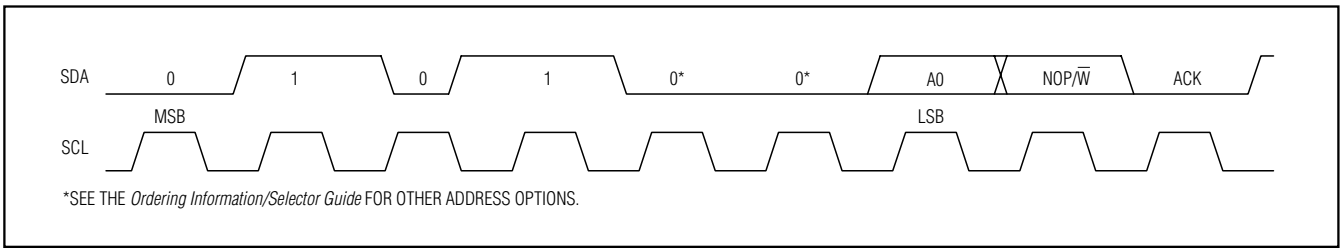


Figure 4. Slave Address

Command Byte

Use the command byte to select the destination of the wiper data (nonvolatile or volatile memory registers) and swap data between nonvolatile and volatile memory registers (see Table 2).

Data Byte

The MAX5432–MAX5435 use the first 5 bits (MSBs, D7–D3) of the data byte to set the position of the wiper. The last 3 bits (D2, D1, and D0) are don't care bits (see Table 2).

Command Descriptions

VREG: The data byte writes to the volatile memory register and the wiper position updates with the data in the volatile memory register.

NVREG: The data byte writes to the nonvolatile memory register. The wiper position is unchanged.

NVREGxVREG: Data transfers from the nonvolatile memory register to the volatile memory register (wiper position updates).

VREGxNVREG: Data transfers from the volatile memory register into the nonvolatile memory register.

Table 2. Command Byte Summary

REGISTER	ADDRESS BYTE									COMMAND BTYE									DATA BYTE									
SCL CYCLE NUMBER	START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	STOP
		A6	A5	A4	A3	A2	A1	A0	NOP/$\overline{W}$	ACK	C7	C6	C5	C4	C3	C2	C1	C0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	
VREG		0	1	0	1	A2	A1	A0	0		0	0	0	1	0	0	0	1		D7	D6	D5	D4	D3	X	X	X		
NVREG		0	1	0	1	A2	A1	A0	0		0	0	1	0	0	0	0	1		D7	D6	D5	D4	D3	X	X	X		
NVREGxVREG		0	1	0	1	A2	A1	A0	0		0	1	1	0	0	0	0	1		D7	D6	D5	D4	D3	X	X	X		
VREGxNVREG		0	1	0	1	A2	A1	A0	0		0	1	0	1	0	0	0	1		D7	D6	D5	D4	D3	X	X	X		

X = *Don't care.*

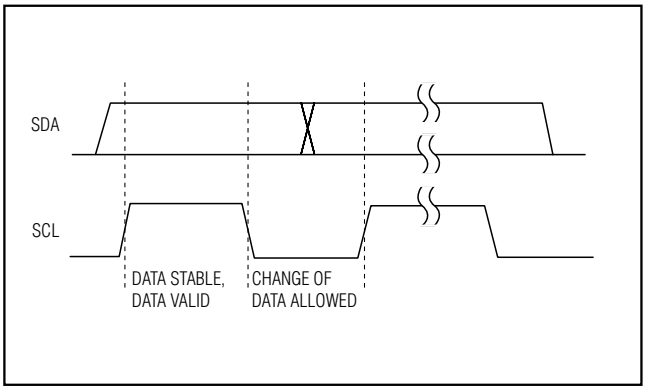


Figure 5. Bit Transfer

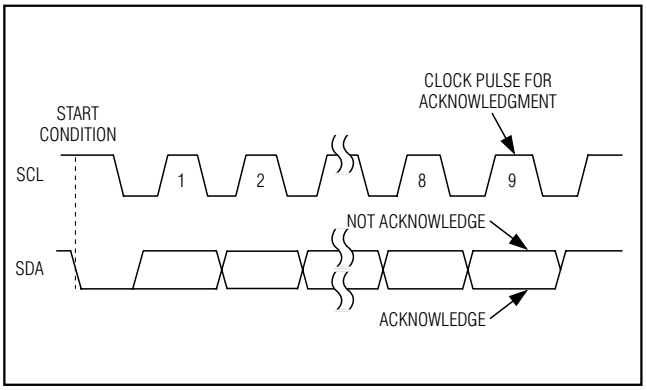


Figure 6. Acknowledge

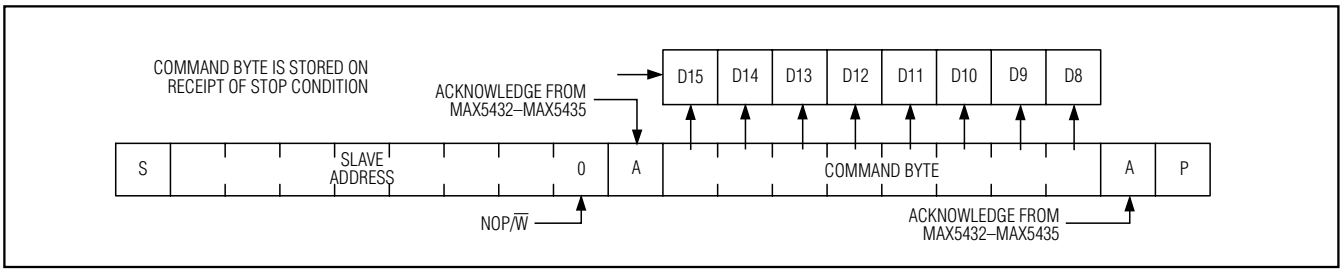


Figure 7. Command Byte Received

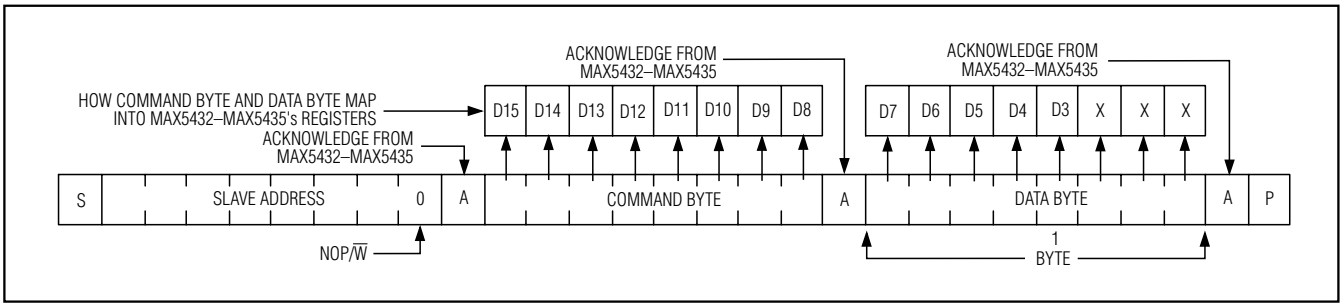


Figure 8. Command and Single Data Byte Received

Nonvolatile Memory

The internal EEPROM consists of a 5-bit nonvolatile register that retains the value written to it before the device is powered down. The nonvolatile register is programmed with the zeros at the factory. Wait a minimum of 12ms after writing to NVREG before sending another command.

Power-Up

Upon power-up, the MAX5432–MAX5435 load the data stored in the nonvolatile memory register into the volatile memory register, updating the wiper position with the data stored in the nonvolatile memory register. This initialization period takes 20µs.

Standby

The MAX5432–MAX5435 feature a low-power standby mode. When the device is not being programmed, it goes into standby mode and current consumption is typically 0.5µA.

32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

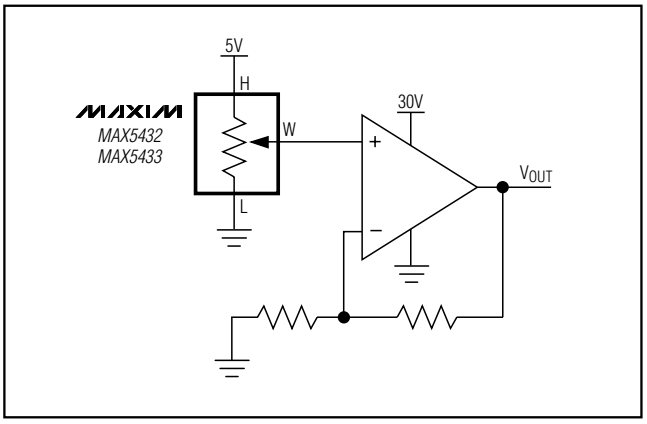


Figure 9. Positive LCD Bias Control Using a Voltage-Divider

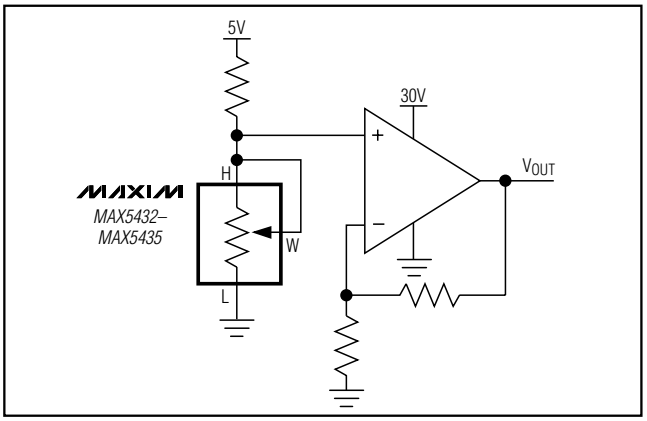


Figure 10. Positive LCD Bias Control Using a Variable Resistor

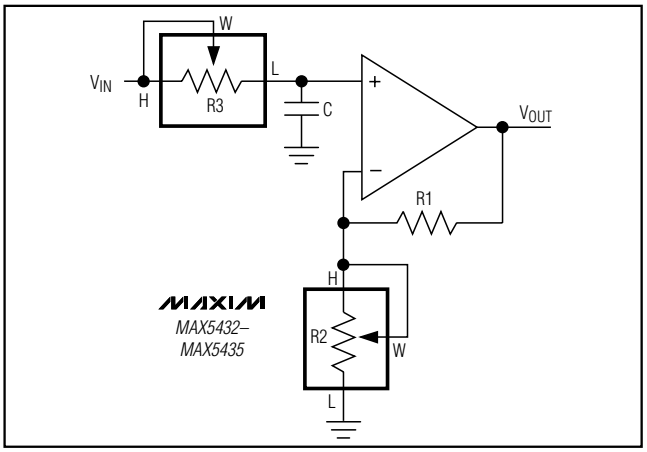


Figure 11. Programmable Filter

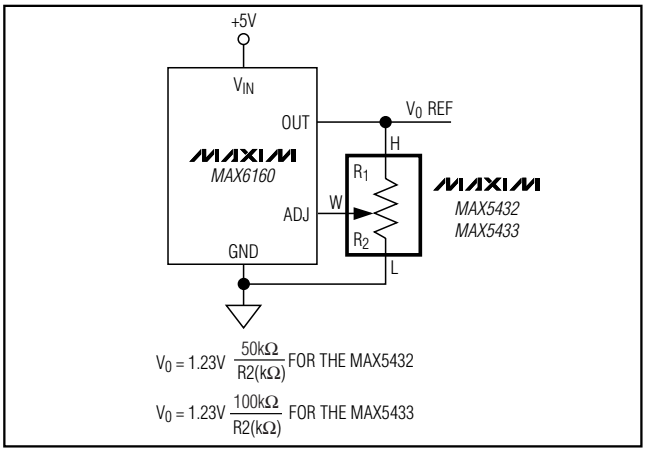


Figure 12. Adjustable Voltage Reference

Applications Information

Use the MAX5432–MAX5435 in applications requiring digitally controlled adjustable resistance, such as LCD contrast control (where voltage biasing adjusts the display contrast), or for programmable filters with adjustable gain and/or cutoff frequency.

Positive LCD Bias Control

Figures 9 and 10 show an application where the voltage-divider or variable resistor is used to make an adjustable, positive LCD bias voltage. The op-amp provides buffering and gain to the resistor-divider network made by the potentiometer (Figure 9) or to a fixed resistor and a variable resistor (Figure 10).

Programmable Filter

Figure 11 shows the configuration for a 1st-order programmable filter. The gain of the filter is adjusted by R2, and the cutoff frequency is adjusted by R3. Use the following equations to calculate the gain (G) and the 3dB cutoff frequency (f_C).

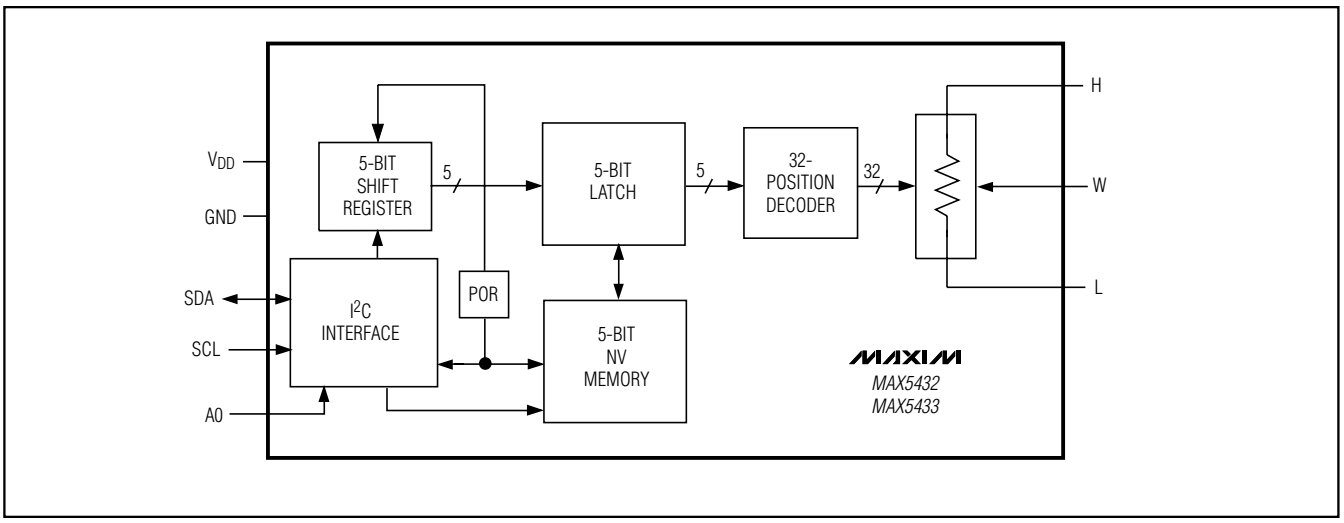
$$G = 1 + \frac{R1}{R2}$$

$$f_C = \frac{1}{2\pi \times R3 \times C}$$

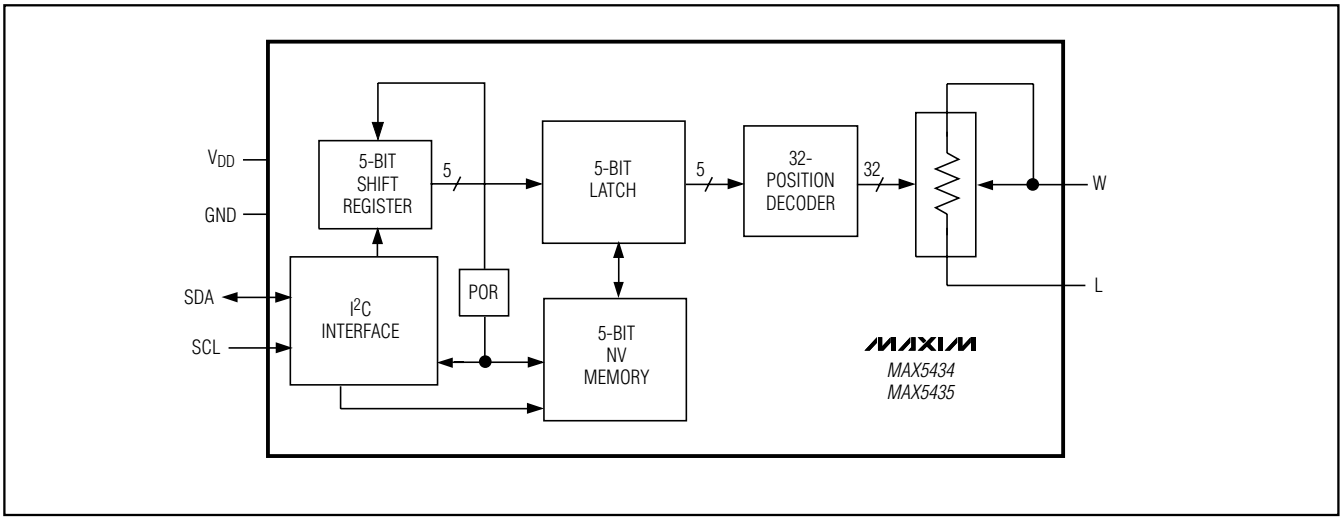
Adjustable Voltage Reference

Figure 12 shows the MAX5432/MAX5433 used as the feedback resistors in an adjustable voltage reference application. Independently adjust the output voltages of the MAX6160 from 1.23V to (V_{IN} - 0.2V) by changing the wiper position of the MAX5432/MAX5433.

MAX5432/MAX5433 Functional Diagram



MAX5434/MAX5435 Functional Diagram



32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

Ordering Information/Selector Guide (continued)

PART	PIN-PACKAGE	TOP MARK	I²C ADDRESS	R (kΩ)	PKG CODE
MAX5434MEZT+T	6 Thin SOT23-6	AABY	0101100	50	Z6-1
MAX5434NEZT+T	6 Thin SOT23-6	AABS	0101010	50	Z6-1
MAX5435LEZT+T	6 Thin SOT23-6	AABW	0101000	100	Z6-1
MAX5435MEZT+T	6 Thin SOT23-6	AABV	0101100	100	Z6-1

**EP = Exposed pad.*
***A_0 represents the logic state of input A0 of the device in the TDFN package.*
+Denotes a lead-free package.
T = Tape and reel.
Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

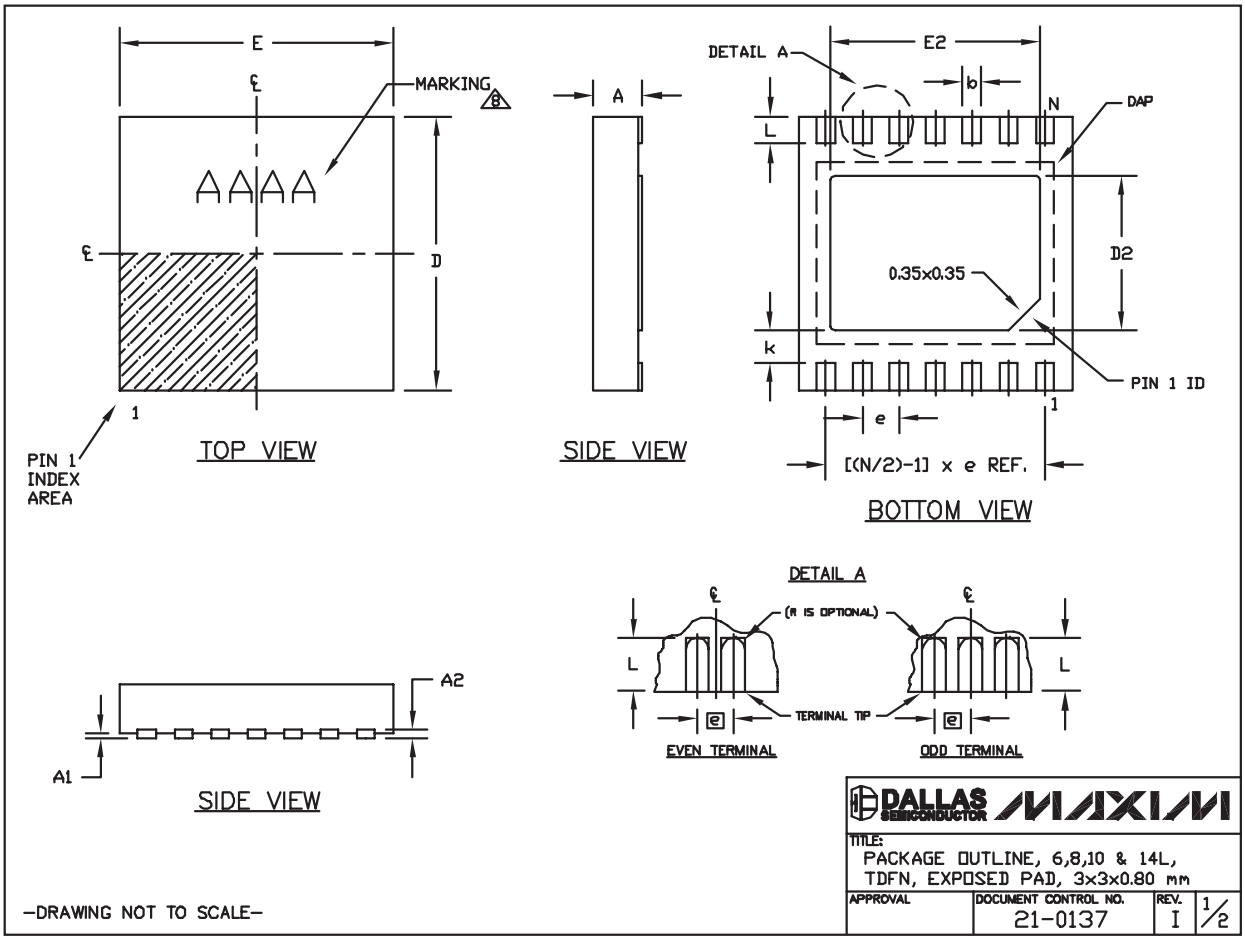
Chip Information

TRANSISTOR COUNT: 7817

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

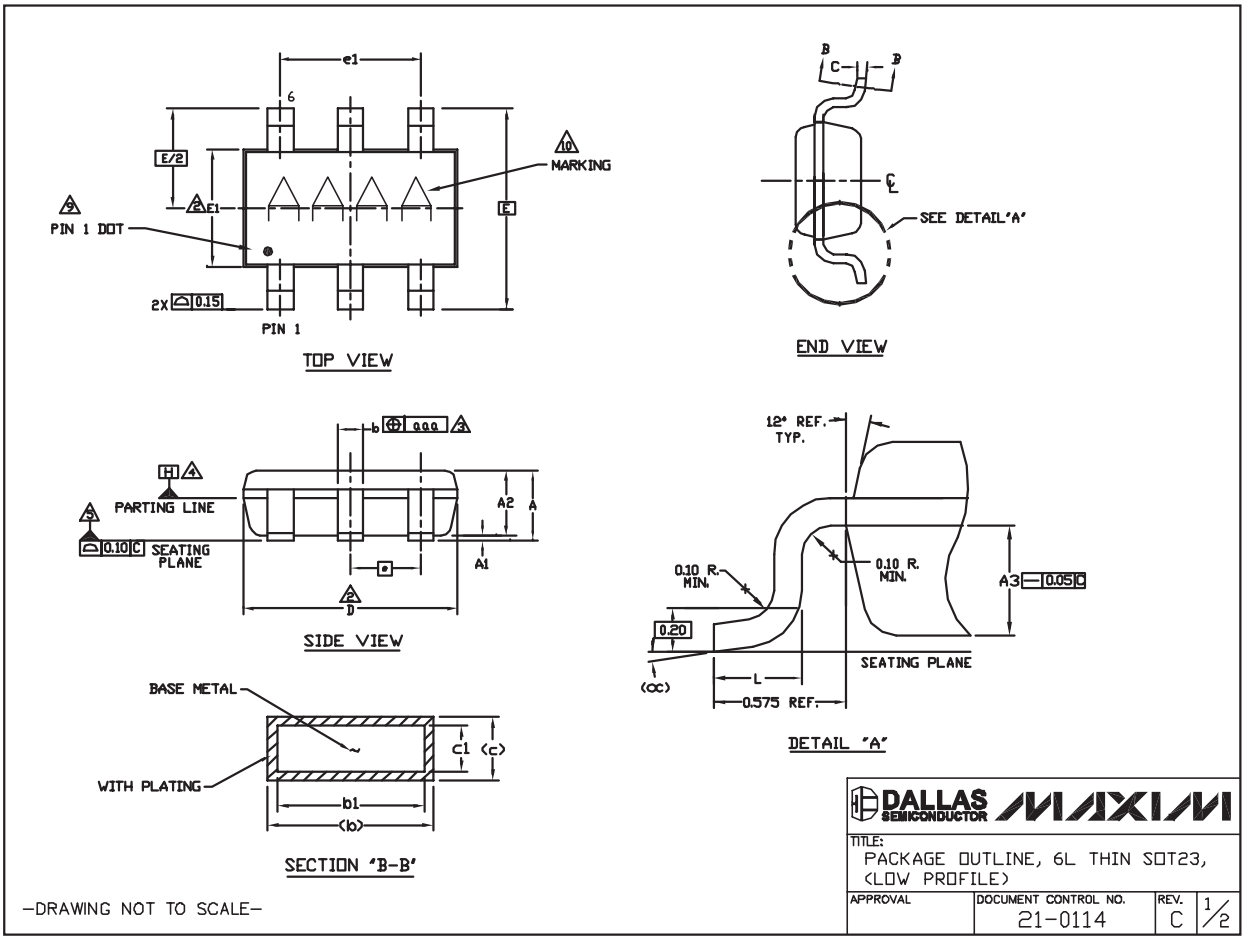
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6L THIN SOT23.EPS



32-Tap, Nonvolatile, I²C, Linear, Digital Potentiometers

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS			
	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3		0.50 BSC	
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E		2.75 BSC	
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1		1.90 BSC	
e		0.95 BSC	
∝	0°	4°	8°
aaa		0.20	

Pkg. codes: Z6-1, Z6-2

—DRAWING NOT TO SCALE—

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6L THIN SOT23, (LOW PROFILE)

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0114	C	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	11/07	Eliminated address options, added lead-free option, updated information in Table 1b	1, 9, 14