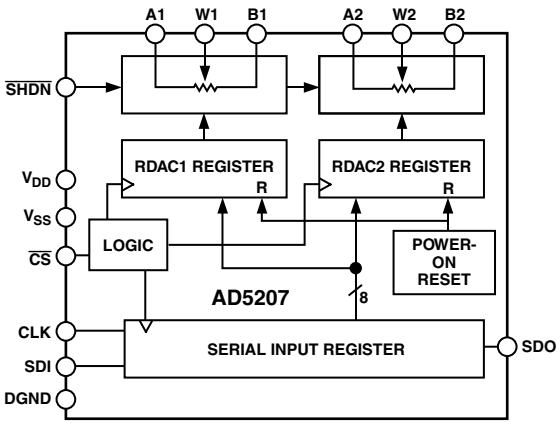
2-Channel, 256-Position Digital Potentiometer

AD5207

FEATURES
256-Position, 2-Channel
Potentiometer Replacement
10 kΩ, 50 kΩ, 100 kΩ
Power Shut-Down, Less than 5 μA
2.7 V to 5.5 V Single Supply
±2.7 V Dual Supply
3-Wire SPI-Compatible Serial Data Input
Midscale Preset During Power-On

APPLICATIONS
Mechanical Potentiometer Replacement
Stereo Channel Audio Level Control
Instrumentation: Gain, Offset Adjustment
Programmable Voltage-to-Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching
Automotive Electronics Adjustment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD5207 provides dual channel, 256-position, digitally controlled variable resistor (VR) devices that perform the same electronic adjustment function as a potentiometer or variable resistor. Each channel of the AD5207 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI-compatible serial-input register. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance, between the A Terminal and the wiper or the B Terminal and the wiper. The fixed A-to-B terminal resistance of 10 kΩ, 50 kΩ or 100 kΩ has a ±1% channel-to-channel matching tolerance with a nominal temperature coefficient of 500 ppm/°C. A unique switching circuit minimizes the high glitch inherent in traditional switched resistor designs and avoids any make-before-break or break-before-make operation.

Each VR has its own VR latch, which holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register, which is loaded from a standard 3-wire serial-input digital interface. Ten bits, to make up the data word, are required and clocked into the serial input register. The first two bits are address bits. The following eight bits are the data bits that represent the 256 steps of the resistance value. The reason for two address bits instead of one is to be compatible with similar products such as AD8402 so that drop-in replacement is possible. The address bit determines the corresponding VR latch to be loaded with the data bits during the returned positive edge of $\overline{CS}$ strobe. A serial data output pin at the opposite end of the serial register allows simple daisy chaining in multiple VR applications without additional external decoding logic.

An internal reset block will force the wiper to the midscale position during every power-up condition. The $\overline{SHDN}$ pin forces an open circuit on the A Terminal and at the same time shorts the wiper to the B Terminal, achieving a microwatt power shutdown state. When $\overline{SHDN}$ is returned to logic high, the previous latch settings put the wiper in the same resistance setting prior to shutdown. The digital interface remains active during shutdown; code changes can be made to produce new wiper positions when the device is resumed from shutdown.

The AD5207 is available in 1.1 mm thin TSSOP-14 package, which is suitable for PCMCIA applications. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +125°C.

REV. 0

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AD5207–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS 10 kΩ, 50 kΩ, 100 kΩ VERSION (V_{DD} = 5 V, V_{SS} = 0, V_A = 5 V, V_B = 0, –40°C < T_A < +125°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE						
Specifications Apply to All VRs						
Resistor Differential Nonlinearity[2]	R-DNL	R_{WB}, V_A = NC	–1		+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–1.5		+1.5	LSB
Nominal Resistor Tolerance[3]	ΔR		–30		+30	%
Resistance Temperature Coefficient	$R_{AB}/\Delta T$	V_{AB} = V_{DD}, Wiper = No Connect		500		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R, V_{DD} = 5 V		50	100	Ω
Nominal Resistance Match	$\Delta R/R_O$	Ch 1 to 2, V_{AB} = V_{DD}, T_A = 25°C		0.2	1	%
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE						
Specifications Apply to All VRs						
Resolution	N		8			Bits
Integral Nonlinearity[4]	INL		–1.5		+1.5	LSB
Differential Nonlinearity[4]	DNL	V_{DD} = 5 V, V_{SS} = 0 V	–1		+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80_H		15		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–1.5			LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H			+1.5	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$	$\|V_{DD}\| + \|V_{SS}\| \le 5.5$ V	V_{SS}		V_{DD}	V
Capacitance[6] A_X, B_X	$C_{A,B}$	f = 1 MHz, Measured to GND, Code = 80_H		45		pF
Capacitance[6] W_X	C_W	f = 1 MHz, Measured to GND, Code = 80_H		70		pF
Shutdown Current[7]	I_{A_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0			5	μA
Shutdown Wiper Resistance	R_{W_SD}	V_A = V_{DD}, V_B = 0 V, $\overline{SHDN}$ = 0, V_{DD} = 5 V			200	Ω
Common-Mode Leakage	I_{CM}	V_A = V_B = $V_{DD}/2$		1		nA
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}	V_{DD} = 5 V, V_{SS} = 0 V	2.4			V
Input Logic Low	V_{IL}	V_{DD} = 5 V, V_{SS} = 0 V			0.8	V
Input Logic High	V_{IH}	V_{DD} = 3 V, V_{SS} = 0 V	2.1			V
Input Logic Low	V_{IL}	V_{DD} = 3 V, V_{SS} = 0 V			0.6	V
Output Logic High	V_{OH}	R_L = 1 kΩ to V_{DD}	V_{DD} – 0.1			V
Output Logic Low	V_{OL}	I_{OL} = 1.6 mA, V_{DD} = 5 V			0.4	V
Input Current	I_{IL}	V_{IN} = 0 V or 5 V			±10	μA
Input Capacitance[6]	C_{IL}			10		pF
POWER SUPPLIES						
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	2.7		5.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±2.2		±2.7	V
Positive Supply Current	I_{DD}	V_{IH} = V_{DD} or V_{IL} = GND, V_{SS} = 0 V			40	μA
Negative Supply Current	I_{SS}	V_{IH} = V_{DD} or V_{IL} = GND V_{SS} = –2.5 V			40	μA
Power Dissipation[8]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V			0.2	mW
Power Supply Sensitivity, V_{DD}	PSS	ΔV_{DD} = 5 V ± 10%, V_{SS} = 0 V, Code = 80_H			0.01	%/%
Power Supply Sensitivity, V_{SS}	PSS	ΔV_{SS} = –2.5 V ± 10%, V_{DD} = 2.5 V, Code = 80_H			0.03	%/%
DYNAMIC CHARACTERISTICS[6, 9]						
Bandwidth –3 dB	BW_10 kΩ	R_{AB} = 10 kΩ		600		kHz
Bandwidth –3 dB	BW_50 kΩ	R_{AB} = 50 kΩ		125		kHz
Bandwidth –3 dB	BW_100 kΩ	R_{AB} = 100 kΩ		71		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V rms, V_B = 0 V, f = 1 kHz, R_{AB} = 10 kΩ		0.003		%
V_W Settling Time	t_S	R_{AB} = 10 kΩ/50 kΩ/100 kΩ, ±1 LSB Error Band		2/9/18		μs
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz, RS = 0		9		$nV\sqrt{Hz}$
Crosstalk[10]	C_T	V_A = 5 V, V_B = 0 V		–65		dB

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
INTERFACE TIMING CHARACTERISTICS Applies to All Parts[6, 11]						
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock Level High or Low	10			ns
Data Setup Time	t_{DS}		5			ns
Data Hold Time	t_{DH}		5			ns
CLK to SDO Propagation Delay[12]	t_{PD}	R_L = 1 kΩ to 5 V, C_L < 20 pF	1		25	ns
$\overline{CS}$ Setup Time	t_{CSS}		10			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		10			ns
CLK Fall to $\overline{CS}$ Fall Hold Time	t_{CSH0}		0			ns
CLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH1}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES
[1] Typicals represent average readings at 25°C and V_{DD} = 5 V, V_{SS} = 0 V.
[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. $I_W = V_{DD}/R$ for both V_{DD} = 5 V, V_{SS} = 0 V.
[3] $V_{AB} = V_{DD}$, Wiper (V_W) = No connect.
[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. $V_A = V_{DD}$ and V_B = 0 V. DNL specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions.
[5] Resistor Terminals A, B, W have no limitations on polarity with respect to each other.
[6] Guaranteed by design and not subject to production test.
[7] Measured at the A_X terminals. All A_X terminals are open-circuited in shut-down mode.
[8] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.
[9] All dynamic characteristics use V_{DD} = 5 V, V_{SS} = 0 V.
[10] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.
[11] See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using V_{DD} = 5 V.
[12] Propagation delay depends on value of V_{DD}, R_L, and C_L; see applications text.

The AD5207 contains 474 transistors. Die Size: 67 mil × 69 mil, 4623 sq. mil.
Specifications subject to change without notice.

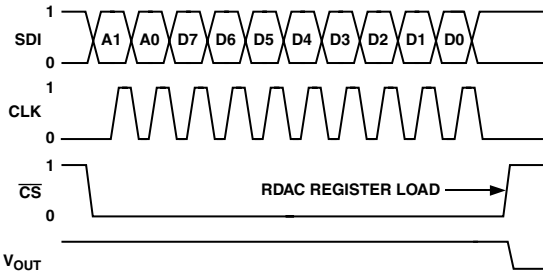


Figure 1a. Timing Diagram

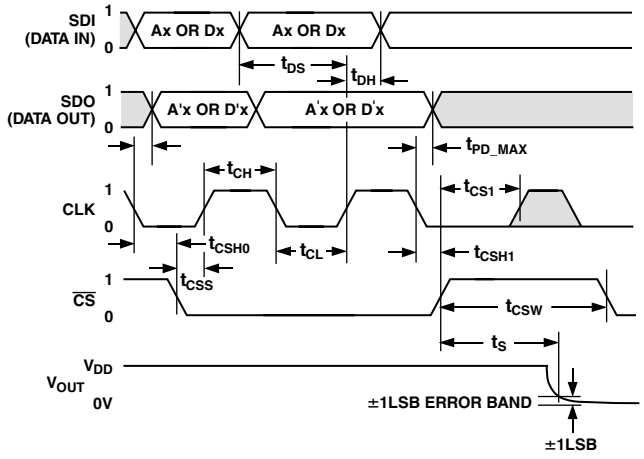


Figure 1b. Detail Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted)

V_{DD} to GND . . . . . –0.3, +7 V
V_{SS} to GND . . . . . 0, –3 V
V_{DD} to V_{SS} . . . . . 7 V
V_A, V_B, V_W to GND . . . . . V_{SS}, V_{DD}
I_{MAX}[2] (A, B, W) . . . . . ±20 mA
Digital Inputs and Output Voltage to GND . . 0 V, V_{DD} + 0.3 V
Operating Temperature Range . . . . . –40°C to +125°C
Maximum Junction Temperature (T_J Max) . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Thermal Resistance[3] θ_{JA}, TSSOP-14 . . . . . 206°C/W

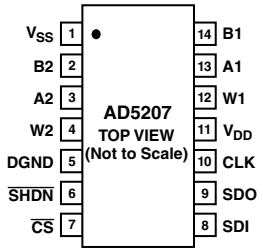
NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Max current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W Terminals at a given resistance. Please refer to TPC 22 for detail.

[3] Package Power Dissipation = (T_J Max–T_A)/θ_{JA}.

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	V_{SS}	Negative Power Supply, specified for operation from 0 V to –2.7 V.
2	B2	Terminal B of RDAC#2.
3	A2	Terminal A of RDAC#2.
4	W2	Wiper, RDAC#2, addr = 1_2
5	DGND	Digital Ground.
6	$\overline{SHDN}$	Active Low Input. Terminal A open-circuit and Terminal B shorted to Wiper. Shutdown controls both RDACs #1 and #2.
7	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded, based on the address bit, and loaded into the corresponding RDAC register.
8	SDI	Serial Data Input. MSB is loaded first.
9	SDO	Serial Data Output. Open Drain transistor requires pull-up resistor.
10	CLK	Serial Clock Input. Positive Edge Triggered.
11	V_{DD}	Positive Power Supply. Specified for operation at 2.7 V to 5.5 V.
12	W1	Wiper, RDAC #1, addr = 0_2.
13	A1	Terminal A of RDAC #1.
14	B1	Terminal B of RDAC #1.

Table I. Serial-Data Word Format

ADDR		DATA							
B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
		MSB							LSB
2^9	2^8	2^7							2^0

NOTES
ADDR(RDAC1) = 00; ADDR(RDAC2 = 01).
Data loads B9 first into SDI pin.

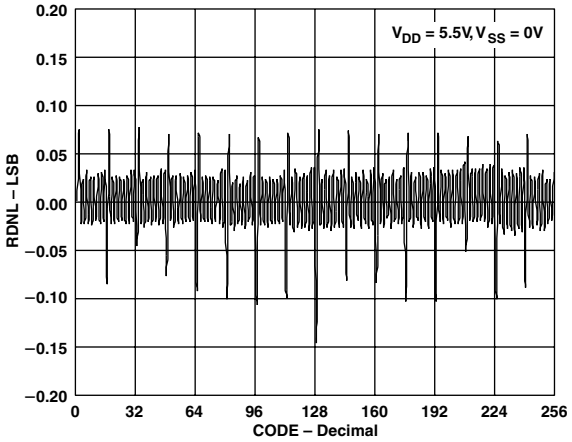
ORDERING GUIDE

Model	kΩ	Temperature Range	Package Description	Package Option	Qty Per Container	Branding Information*
AD5207BRU10-REEL7	10	–40°C to +125°C	TSSOP-14	RU-14	1,000	B10
AD5207BRU50-REEL7	50	–40°C to +125°C	TSSOP-14	RU-14	1,000	B50
AD5207BRU100-REEL7	100	–40°C to +125°C	TSSOP-14	RU-14	1,000	B100

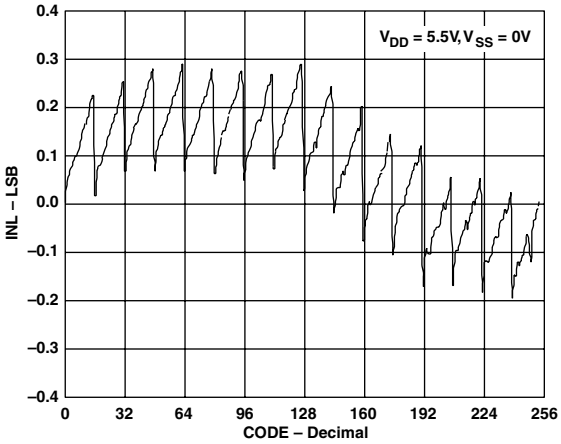
*Three lines of information appear on the device. Line 1 lists the part number; Line 2 includes branding information and the ADI logo, and Line 3 contains the date code YYWW.

CAUTION

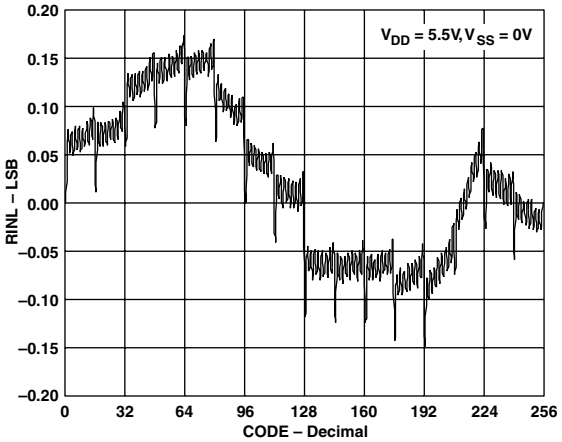
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5207 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



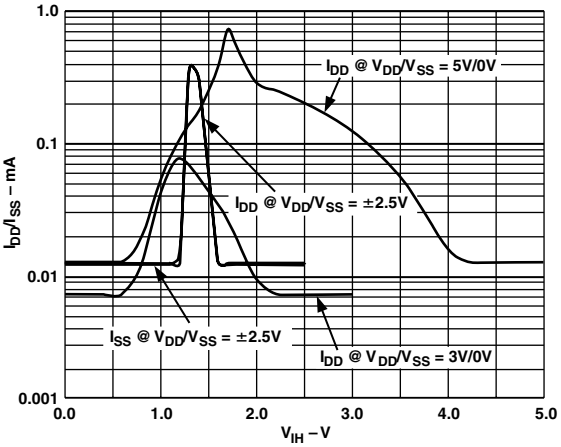
TPC 1. 10 kΩ RDNL vs. Code



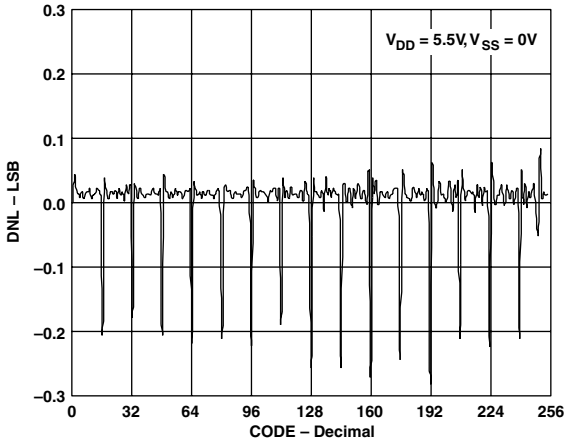
TPC 4. 10 kΩ INL vs. Code



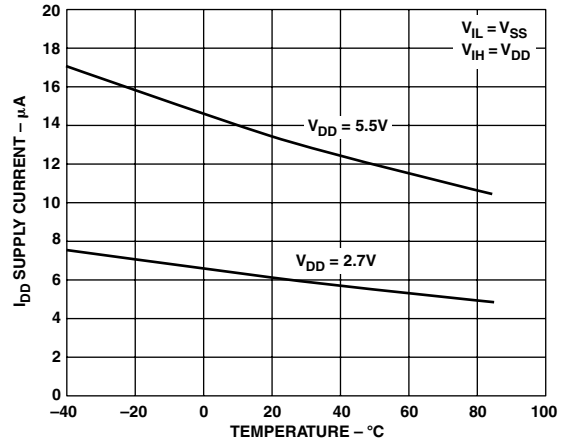
TPC 2. 10 kΩ RINL vs. Code



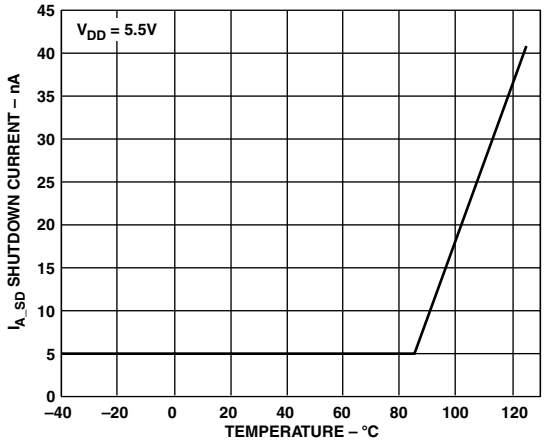
TPC 5. Supply Current vs. Logic Input Voltage



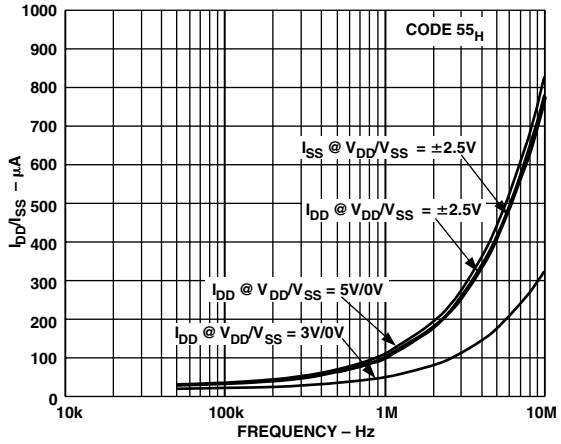
TPC 3. 10 kΩ DNL vs. Code



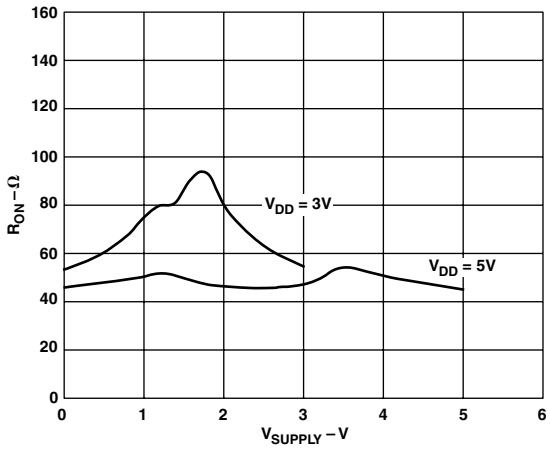
TPC 6. Supply Current vs. Temperature



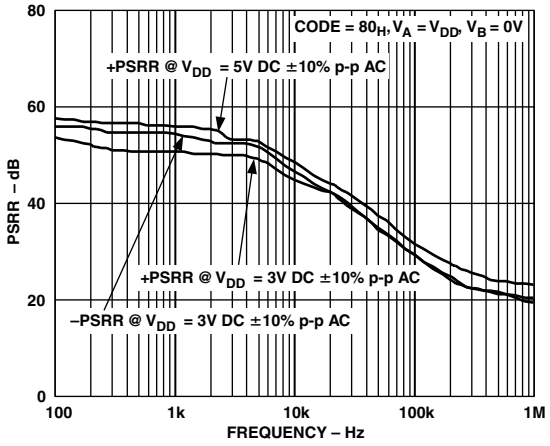
TPC 7. Shutdown Current vs. Temperature



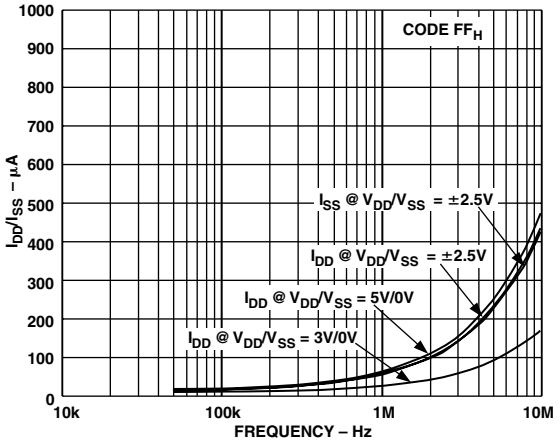
TPC 10. 10 kΩ Supply Current vs. Clock Frequency



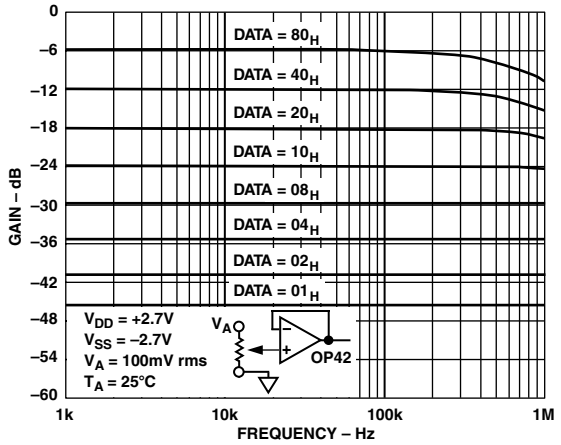
TPC 8. Wiper ON Resistance vs. V_{SUPPLY}



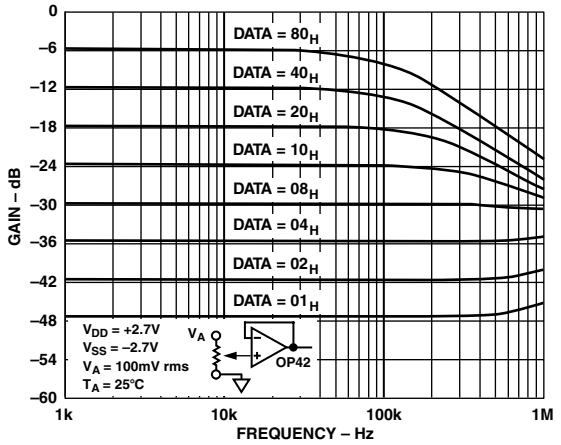
TPC 11. Power Supply Rejection Ratio vs. Frequency



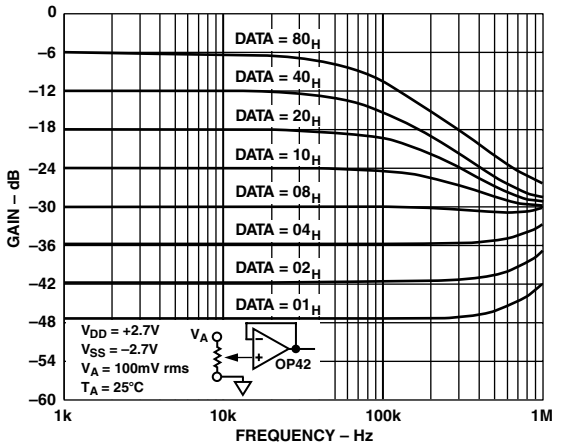
TPC 9. 10 kΩ Supply Current vs. Clock Frequency



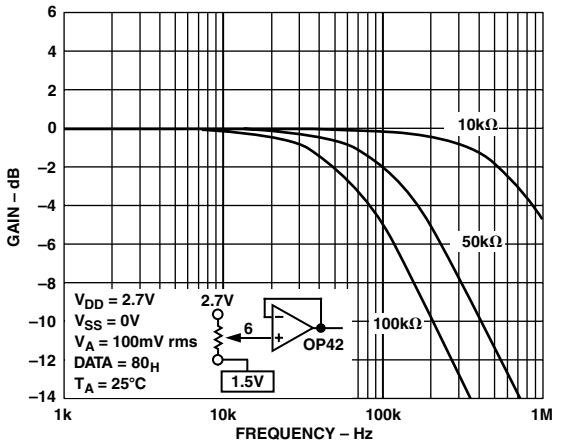
TPC 12. 10 kΩ Gain vs. Frequency vs. Code



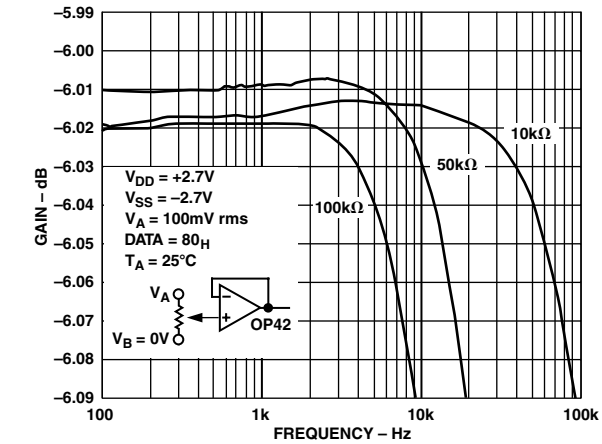
TPC 13. 50 kΩ Gain vs. Frequency vs. Code



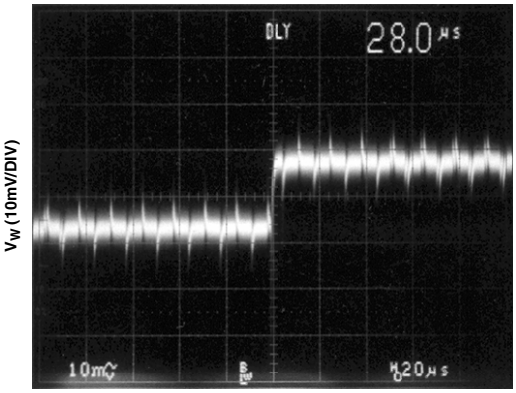
TPC 14. 100 kΩ Gain vs. Frequency vs. Code



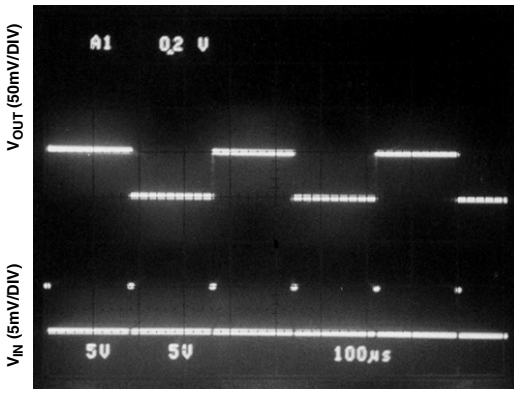
TPC 15. –3 dB Bandwidth



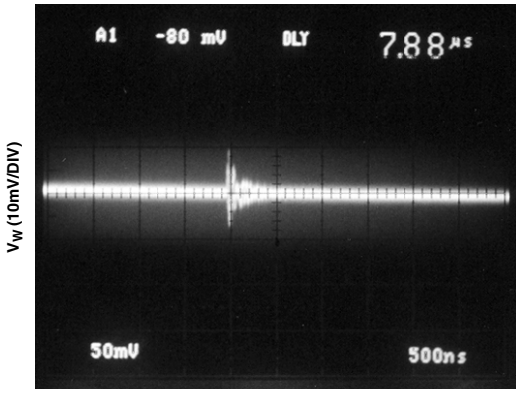
TPC 16. Normalized Gain Flatness vs. Frequency



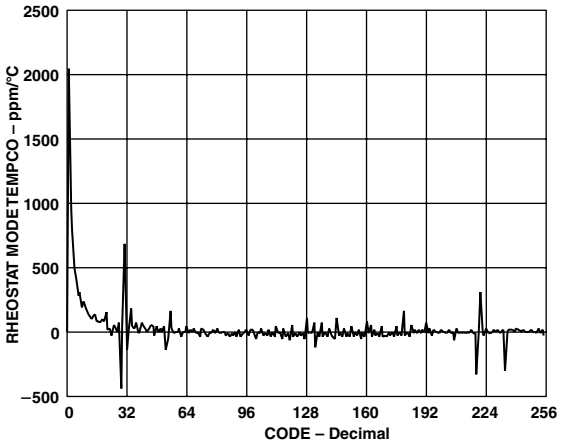
TPC 17. One Position Step Change at Half Scale



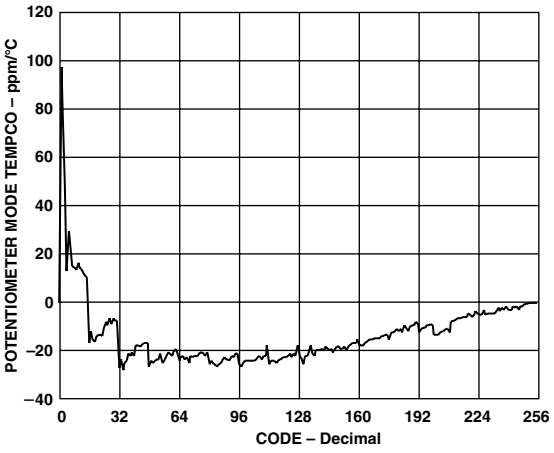
TPC 18. Large Signal Settling Time



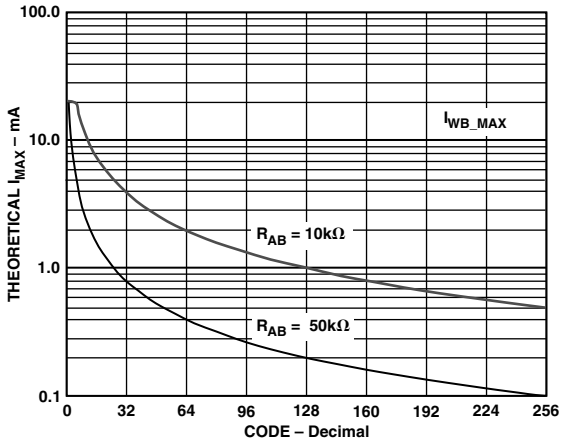
TPC 19. Digital Feedthrough vs. Time



TPC 21. $\Delta R_{WB}/\Delta T$ Rheostat Mode Temperature Coefficient



TPC 20. $\Delta V_{WB}/\Delta T$ Potentiometer Mode Temperature Coefficient



TPC 22. I_{MAX} vs. Code

OPERATION

The AD5207 provides a dual channel, 256-position digitally controlled variable resistor (VR) device. The terms VR, RDAC, and digital potentiometer are sometimes used interchangeably. Changing the programmable VR settings is accomplished by clocking in a 10-bit serial data word into the SDI (Serial Data Input) pin. The format of this data word is two address Bits, A1 and A0. With A1 and A2 are first and second bits respectively, followed by eight data bits B7–B0 with MSB first. Table I provides the serial register data word format. See Table III for the AD5207 address assignments to decode the location of VR latch receiving the serial register data in Bits B7 through B0. VR settings can be changed one at a time in random sequence. The AD5207 presets to a midscale during power-on condition. AD5207 contains a power shutdown $\overline{SHDN}$ pin. When activated in logic low. Terminals A on both RDACs will be open-circuited while the wiper terminals W_X are shorted to B_X. As a result, a minimum amount of leakage current will be consumed in both RDACs, and the power dissipation is negligible. During the shutdown mode, the VR latch settings are maintained. Thus the previous resistance values remain when the devices are resumed from the shutdown.

DIGITAL INTERFACING

The AD5207 contains a standard three-wire serial input control interface. The three inputs are clock (CLK), chip select ($\overline{CS}$), and serial data input (SDI). The positive edge-sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. Figure 2 shows more detail of the internal digital circuitry. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge; see Table II.

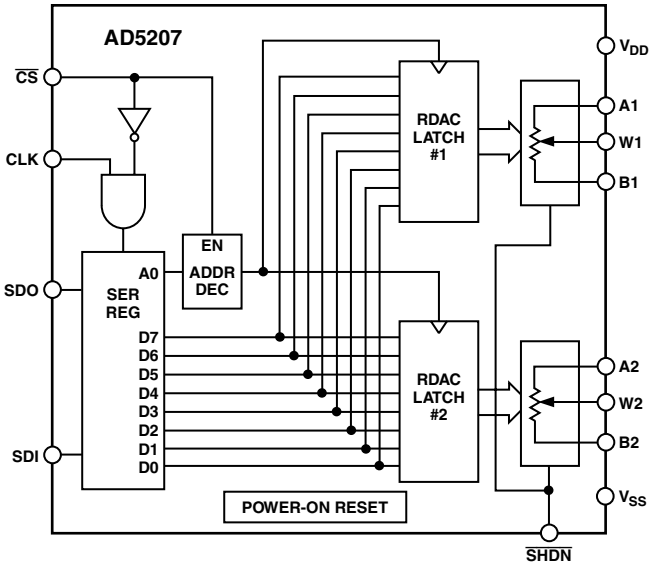


Figure 2. Block Diagram

The serial-data-output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor in order to transfer data to the next package's SDI pin. The pull-up resistor termination voltage may be larger than the V_{DD} supply of the AD5207 SDO output device, e.g., the AD5207 could operate at V_{DD} = 3.3 V and the pull-up for interface to the next device could be set at 5 V. This allows for daisy chaining several RDACs from a single processor serial-data line. The clock period may need to be increased when using a pull-up resistor to the SDI pin of the following devices in series. Capacitive loading at the daisy chain node SDO–SDI between devices may add time delay to subsequent devices. User should be aware of this potential problem in order to successfully achieve data transfer. See Figure 3. When configuring devices for daisy-chaining, the $\overline{CS}$ should be kept low until all the bits of every package are clocked into their respective serial registers, ensuring that the address bit and data bits are in the proper decoding location. This requires 20 bits of address and data complying with the data word in Table I if two AD5207 RDACs are daisy chained. During shutdown $\overline{SHDN}$, the SDO output pin is forced to OFF (logic high state) to disable power dissipation in the pull-up resistor. See Figure 4 for equivalent SDO output circuit schematic.

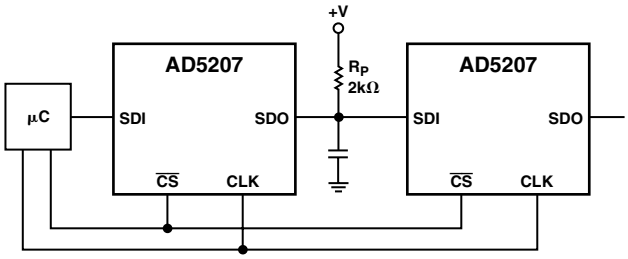


Figure 3. Daisy-Chain Configuration Using SDO

Table II. Input Logic Control Truth Table

CLK	$\overline{CS}$	$\overline{SHDN}$	Register Activity
L	L	H	No SR effect, enables SDO pin.
P	L	H	Shift one bit in from the SDI pin. MSB first. The tenth previously entered bit is shifted out of the SDO pin.
X	P	H	Load SR data into RDAC latch based on A0 decode (Table III).
X	H	H	No Operation.
X	H	L	Open circuits all resistor A Terminals, connects W to B, turns off SDO output transistor.

NOTE
P = positive edge, X = don't care, SR = shift register.

Table III. Address Decode Table

A1	A0	Latch Loaded
0	0	RDAC #1
0	1	RDAC #2

The data setup and data hold times in the specification table determine the data valid time requirements. The last ten bits of the data word entered into the serial register are held when $\overline{CS}$ returns high and any extra bits are ignored. At the same time, when $\overline{CS}$ goes high, it gates the address decoder enabling one of two positive edge-triggered AD5207 RDAC latches; see Figure 5 detail.

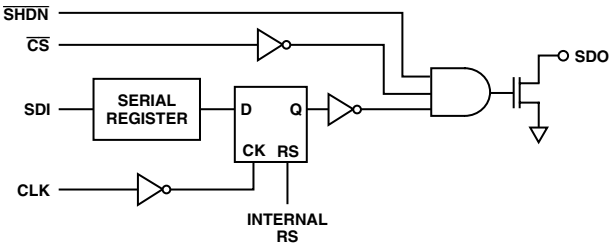


Figure 4. Detail SDO Output Schematic of the AD5207

The target RDAC latch is loaded with the last eight bits of the data word to complete one RDAC update. For AD5207, it cannot update both channels simultaneously and therefore, two separate 10-bit data words must be clocked in to change both VR settings.

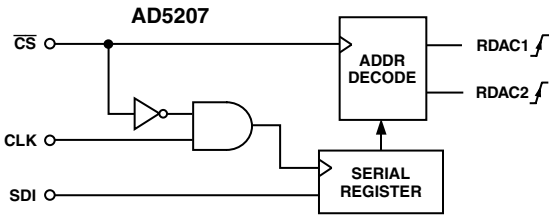


Figure 5. Equivalent Input Control Logic

All digital inputs are protected with a series input resistor and parallel Zener ESD structure shown in Figures 6 and 7. Applies to digital input pins $\overline{CS}$, SDI, SDO, $\overline{SHDN}$, and CLK. Digital input level for Logic 1 can be anywhere from 2.4 V to 5 V regardless of whether it is in single or dual supplies.

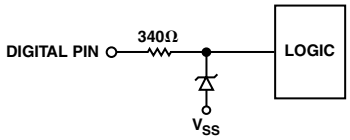


Figure 6. ESD Protection of Digital Pins

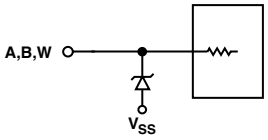


Figure 7. ESD Protection of Resistor Terminals

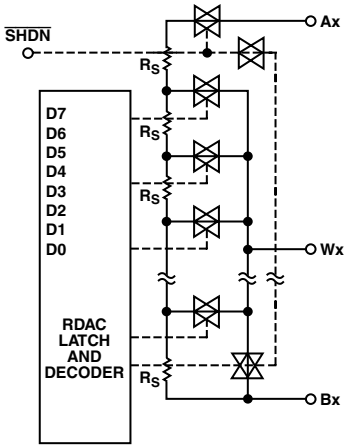


Figure 8. Equivalent RDAC Circuit

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance of the RDAC between Terminals A and B is available with values of 10 kΩ, 50 kΩ, and 100 kΩ. The last few digits of the part number determine the nominal resistance value, e.g., 10 kΩ = 10; 50 kΩ = 50; and 100 kΩ = 100. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B Terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assume a 10 kΩ part is used, the wiper's first connection starts at the B Terminal for data 00_H. Since there is a 45 Ω wiper contact resistance, such connection yields a minimum of 45 Ω resistance between Terminals W and B. The second connection is the first tap point corresponds to 84 Ω (R_{WB} = R_{AB}/256 + R_W = 39 Ω + 45 Ω) for data 01_H. The third connection is the next tap point representing 123 Ω (39 × 2 + 45) for data 02_H and so on. Each LSB value increase moves the wiper up the resistor ladder until the last tap point is reached at 10006 Ω (R_{AB} – 1 LSB + R_W). Figure 8 shows a simplified diagram of the equivalent RDAC circuit.

The general equation determining the programmable output resistance between W and B is:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where D is the data contained in the 8-bit RDAC latch, and R_{AB} is the nominal end-to-end resistance.

For example, R_{AB} =10 kΩ, A Terminal can be open-circuit or tied to W. The following output resistance R_{WB} will be set for the following RDAC latch codes.

Table IV.

D (DEC)	R_{WB} (Ω)	Output State
255	10006	Full-Scale (R_{AB} – 1 LSB + R_W)
128	5045	Midscale
1	84	1 LSB
0	45	Zero-Scale (Wiper Contact Resistance)

Note that in the zero-scale condition a finite wiper resistance of 45 Ω is present. Care should be taken to limit the current flow between W and B in this state to a maximum current of no more than 5 mA. Otherwise, degradation or possibly destruction of the internal switch contacts can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between the wiper W and Terminal A also produces a digitally controlled resistance R_{WA}. When these terminals are used, the B Terminal should be let open or tied to the wiper terminal. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For example, when R_{AB} = 10 kΩ, B terminal is either open or tied to W, the following output resistance, R_{WA}, will be set for the following RDAC latch codes.

Table V.

D (DEC)	R_{WA} (Ω)	Output State
255	84	Full-Scale (R_{AB}/256 + R_W)
128	5045	Midscale
1	10006	1 LSB
0	10045	Zero-Scale

The typical distribution of R_{AB} from channel to channel matches within ±1%. Device-to-device matching is process-lot dependent and is possible to have ±30% variation. The change in R_{AB} with temperature has a 500 ppm/°C temperature coefficient.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates an output voltage proportional to the input voltage. Let's ignore the effect of the wiper resistance for the moment. For example, when connecting A Terminal to 5 V and B Terminal to ground, it produces a programmable output voltage at the wiper starting at zero volts up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 position of the potentiometer divider. Since AD5207 is capable for dual supplies, the general equation defining the output voltage with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent on the ratio of R_{WA} and R_{WB} and not the absolute values; therefore, the drift reduces to 15 ppm/°C. There is no voltage polarity constraint between Terminals A, B, and W as long as the terminal voltage stays within $V_{SS} < V_{TERM} < V_{DD}$.

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider the –3 dB bandwidth of the AD5207BRU10 (10 kΩ resistor) measures 600 kHz at half scale. TPC 16 provides the large signal BODE plot characteristics of the three available resistor versions 10 kΩ and 50 kΩ. The gain flatness versus frequency graph, TPC 16, predicts filter applications performance. A parasitic simulation model has been developed and is shown in Figure 9. Listing I provides a macro model net list for the 10 kΩ RDAC:

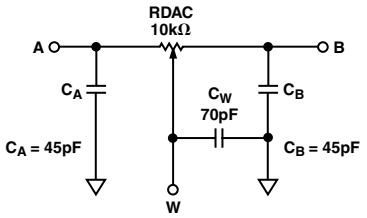


Figure 9. RDAC Circuit Simulation Model for RDAC = 10 kΩ

Listing I. Macro Model Net List for RDAC

```
.PARAM D=255, RDAC=10E3
*
.SUBCKT DPOT (A,W)
*
CA A 0 45E-12
RAW A W {(1-D/256)*RDAC+50}
CW W 0 70E-12
RBW W B {D/256*RDAC+50}
CB B 0 45E-12
*
.ENDS DPOT
```

TEST CIRCUITS

Figures 10 to 18 define the test conditions used in product Specification table.

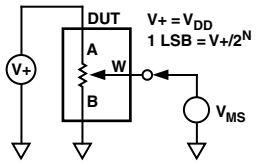


Figure 10. Potentiometer Divider Nonlinearity Error Test Circuit (INL, DNL)

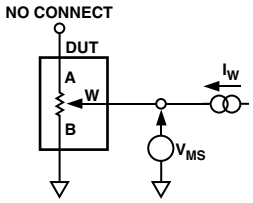


Figure 11. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

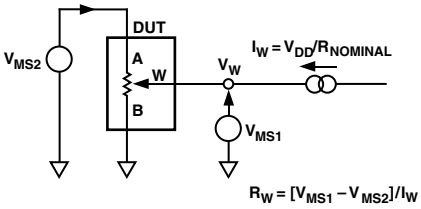


Figure 12. Wiper Resistance Test Circuit

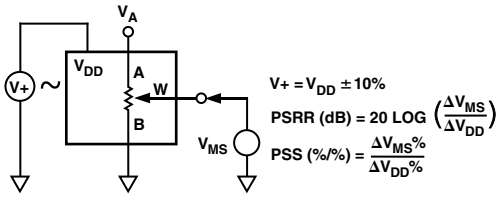


Figure 13. Power Supply Sensitivity Test Circuit (PSS, PSSR)

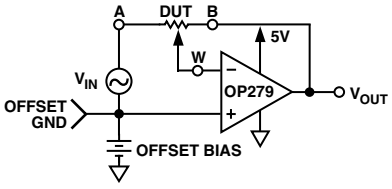


Figure 14. Inverting Gain Test Circuit

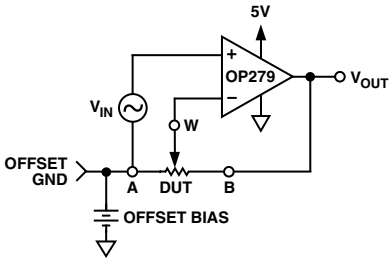


Figure 15. Noninverting Gain Test Circuit

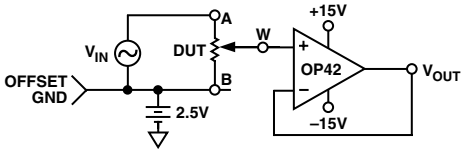


Figure 16. Gain vs. Frequency Test Circuit

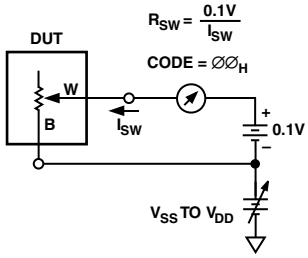


Figure 17. Incremental ON Resistance Test Circuit

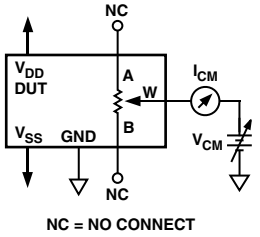


Figure 18. Common-Mode Leakage Current Test Circuit

DIGITAL POTENTIOMETER FAMILY SELECTION GUIDE

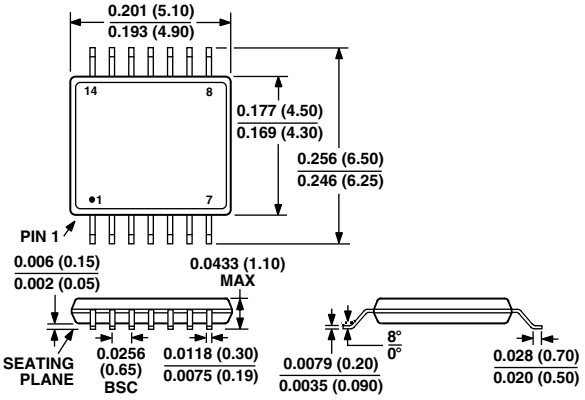
Part Number	Number of VRs per Package	Terminal Voltage Range	Interface Data Control	Nominal Resistance (kΩ)	Resolution (Number of Wiper Positions)	Power Supply Current (I_{DD})	Packages	Comments
AD5201	1	±3 V, +5.5 V	3-Wire	10, 50	33	40 µA	µSOIC-10	Full AC Specs, Dual Supply, Pwr-On-Reset, Low Cost
AD5220	1	5.5 V	Up/Down	10, 50, 100	128	40 µA	PDIP, SO-8, µSOIC-8	No Rollover, Pwr-On-Reset
AD7376	1	±15 V, +28 V	3-Wire	10, 50, 100, 1000	128	100 µA	PDIP-14, SOL-16, TSSOP-14	Single +28 V or Dual ±15 V Supply Operation
AD5200	1	±3 V, +5.5 V	3-Wire	10, 50	256	40 µA	µSOIC-10	Full AC Specs, Dual Supply, Pwr-On-Reset
AD8400	1	5.5 V	3-Wire	1, 10, 50, 100	256	5 µA	SO-8	Full AC Specs
AD5260	1	±5 V, +15 V	3-Wire	20, 50, 200	256	60 µA	TSSOP-14	15 V or ±5 V, TC < 50 ppm/°C
AD5241	1	±3 V, +5.5 V	2-Wire	10, 100, 1000	256	50 µA	SO-14, TSSOP-14	I^2C-Compatible, TC < 50 ppm/°C
AD5231*	1	±3 V, +5.5 V	3-Wire	10, 50, 100	1024	20 µA	TSSOP-16	*Nonvolatile* Memory, Direct Program, I/D, ±6 dB Settability
AD5222	2	±3 V, +5.5 V	Up/Down	10, 50, 100, 1000	128	80 µA	SO-14, TSSOP-14	No Rollover, Stereo, Pwr-On-Reset, TC < 50 ppm/°C
AD8402	2	5.5 V	3-Wire	1, 10, 50, 100	256	5 µA	PDIP, SO-14, TSSOP-14	Full AC Specs, nA Shutdown Current
AD5207	2	±3 V, +5.5 V	3-Wire	10, 50, 100	256	40 µA	TSSOP-14	Full AC specs, Dual Supply, Pwr-On-Reset, SDO
AD5232*	2	±3 V, +5.5 V	3-Wire	10, 50, 100	256	20 µA	TSSOP-16	*Nonvolatile* Memory, Direct Program, I/D, ±6 dB Settability
AD5235*	2	±3 V, +5.5 V	3-Wire	25, 250	1024	20 µA	TSSOP-16	*Nonvolatile* Memory, Direct Program, TC < 50 ppm/°C
AD5242	2	±3 V, +5.5 V	2-Wire	10, 100, 1000	256	50 µA	SO-16, TSSOP-16	I^2C-Compatible, TC < 50 ppm/°C
AD5262*	2	±5 V, +15 V	3-Wire	20, 50, 200	256	60 µA	TSSOP-16	±15 V or ±5 V, Pwr-On-Reset, TC < 50 ppm/°C
AD5203	4	5.5 V	3-Wire	10, 100	64	5 µA	PDIP, SOL-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5233*	4	±3 V, +5.5 V	3-Wire	10, 50, 100	64	20 µA	TSSOP-16	*Nonvolatile* Memory, Direct Program, I/D, ±6 dB Settability
AD5204	4	±3 V, +5.5 V	3-Wire	10, 50, 100	256	60 µA	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Pwr-On-Reset
AD8403	4	5.5 V	3-Wire	1, 10, 50, 100	256	5 µA	PDIP, SOL-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5206	6	±3 V, +5.5 V	3-Wire	10, 50, 100	256	60 µA	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Pwr-On-Reset

*Future product, consult factory for latest status.
Latest Digital Potentiometer Information available at www.analog.com/support/standard_linear/selection_guides/dig_pot.html

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

14-Lead TSSOP
(RU-14)



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