National Semiconductor

November 1994

ADC12441 Dynamically-Tested Self-Calibrating 12-Bit Plus Sign A/D Converter with Sample-and-Hold

General Description

The ADC12441 is a CMOS 12-bit plus sign successive approximation analog-to-digital converter whose dynamic specifications (S/N, THD, etc.) are tested and guaranteed. On request, the ADC12441 goes through a self-calibration cycle that adjusts positive linearity and full-scale errors to less than ±½ LSB each and zero error to less than ±1 LSB. The ADC12441 also has the ability to go through an Auto-Zero cycle that corrects the zero error during every conversion.

The analog input to the ADC12441 is tracked and held by the internal circuitry, and therefore does not require an external sample-and-hold. A unipolar analog input voltage range (0V to +5V) or a bipolar range (−5V to +5V) can be accommodated with ±5V supplies.

The 13-bit word on the outputs of the ADC12441 gives a 2's complement representation of negative numbers. The digital inputs and outputs are compatible with TTL or CMOS logic levels.

Applications

- Digital signal processing
- Telecommunications
- Audio
- High resolution process control
- Instrumentation

Key Specifications

■ Resolution	12 bits plus sign
■ Conversion Time	13.8 μs (max)
■ Bipolar Signal/Noise	76.5 dB (min)
■ Total Harmonic Distortion	−75 dB (max)
■ Aperture Time	100 ns
■ Aperture Jitter	100 ps_{rms}
■ Zero Error	±1 LSB (max)
■ Positive Full Scale Error	±1 LSB (max)
■ Power Consumption @ ±5V	70 mW (max)
■ Sampling rate	55 kHz (max)

Features

- Self-calibration provides excellent temperature stability
- Internal sample-and-hold
- Bipolar input range with single +5V reference

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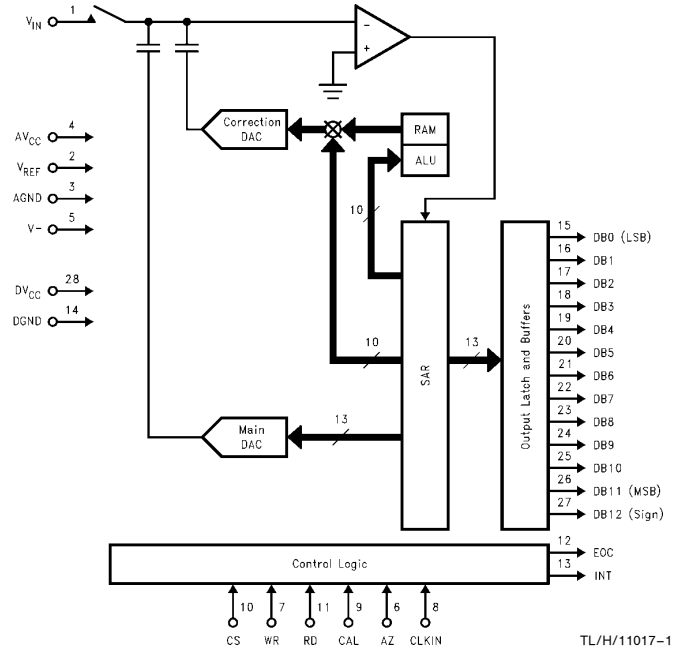
Simplified Block Diagram



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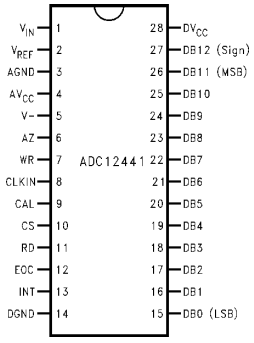
Connection Diagram

Dual-In-Line Package



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Top View

Order Number
ADC12441CMJ, ADC12441CMJ/883
or ADC12441CIJ
See NS Package Number J28A

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC} = DV_{CC} = AV_{CC})	6.5V
Negative Supply Voltage (V^-)	−6.5V
Voltage at Logic Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Analog Inputs (V_{IN} and V_{REF})	(V^- − 0.3V) to (V_{CC} + 0.3V)
AV_{CC}−DV_{CC} (Note 7)	0.3V
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation at 25°C (Note 4)	875 mW
Storage Temperature Range	−65°C to +150°C
ESD Susceptability (Note 5)	2000V
Soldering Information J Package (10 sec.)	300°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC12441CIJ	−40°C ≤ T_A ≤ +85°C
ADC12441CMJ, ADC12441CMJ/883	−55°C ≤ T_A ≤ +125°C
DV_{CC} and AV_{CC} Voltage (Notes 6 & 7)	4.5V to 5.5V
Negative Supply Voltage (V^-)	−4.5V to −5.5V
Reference Voltage (V_{REF}, Notes 6 & 7)	3.5V to AV_{CC} + 50 mV

Converter Electrical Characteristics

The following specifications apply for V_{CC} = DV_{CC} = AV_{CC} = +5.0V, V^- = −5.0V, V_{REF} = +5.0V, Analog Input Source Impedance = 600Ω, and f_{CLK} = 2.0 MHz unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C. (Notes 6, 7 and 8)

Symbol	Parameter		Conditions	Typical (Note 9)	Limit (Note 10)	Units (Limit)
STATIC CHARACTERISTICS						
	Positive Integral Linearity Error		After Auto-Cal (Notes 11 & 12)	±½		LSB
	Negative Integral Linearity Error		After Auto-Cal (Notes 11 & 12)	±¾		LSB
	Positive or Negative Differential Linearity		After Auto-Cal (Notes 11 & 12)	12		Bits
	Zero Error		After Auto-Zero or Auto-Cal (Notes 12 & 13)		**±1**	LSB (max)
	Positive Full-Scale Error		After Auto-Cal (Note 12)	±½	**±1**	LSB (max)
	Negative Full-Scale Error		After Auto-Cal (Note 12)		±1 / **±2**	LSB (max)
V_{IN}	Analog Input Voltage				**V^- − 0.05** **V_{CC} + 0.05**	V(min) V(max)
	Power Supply Sensitivity	Zero Error (Note 14)	AV_{CC} = DV_{CC} = 5V ±5%, V_{REF} = 4.75V, V^- = −5V ±5%	±⅛		LSB
		Full-Scale Error		±⅛		LSB
		Linearity Error		±⅛		LSB
C_{REF}	V_{REF} Input Capacitance (Note 18)			80		pF
C_{IN}	Analog Input Capacitance			65		pF
DYNAMIC CHARACTERISTICS						
	Bipolar Effective Bits (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85V	12.6		Bits
			f_{IN} = 20 kHz, V_{IN} = ±4.85V	12.6	**12.4**	Bits (min)
	Unipolar Effective Bits (Note 17)		f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	11.8		Bits
			f_{IN} = 20 kHz, V_{IN} = 4.85 V_{p-p}	11.8	**11.6**	Bits (min)
S/N	Bipolar Signal-to-Noise Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = ±4.85V	78		dB
			f_{IN} = 10 kHz, V_{IN} = ±4.85V	78		dB
			f_{IN} = 20 kHz, V_{IN} = ±4.85V	78	**76.5**	dB (min)
S/N	Unipolar Signal-to-Noise Ratio (Note 17)		f_{IN} = 1 kHz, V_{IN} = 4.85 V_{p-p}	73		dB
			f_{IN} = 10 kHz, V_{IN} = 4.85 V_{p-p}	73		dB
			f_{IN} = 20 kHz, V_{IN} = 4.85 V_{p-p}	73	**71.5**	dB (min)

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Converter Electrical Characteristics

The following specifications apply for $V_{CC} = DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, Analog Input Source Impedance = 600Ω, and $f_{CLK} = 2.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6, 7 and 8) (Continued)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limit)
DYNAMIC CHARACTERISTICS (Continued)					
THD	Bipolar Total Harmonic Distortion (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = \pm 4.85V$	−82		dB
		$f_{IN} = 19.688$ kHz, $V_{IN} = \pm 4.85V$	−80	**−75**	dB (max)
THD	Unipolar Total Harmonic Distortion (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−82		dB
		$f_{IN} = 19.688$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−80	**−75**	dB (max)
	Bipolar Peak Harmonic or Spurious Noise (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = \pm 4.85V$	−88		dB
		$f_{IN} = 10$ kHz, $V_{IN} = \pm 4.85V$	−84		dB
		$f_{IN} = 20$ kHz, $V_{IN} = \pm 4.85V$	−80		dB
	Unipolar Peak Harmonic or Spurious Noise (Note 17)	$f_{IN} = 1$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−90		dB
		$f_{IN} = 10$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−86		dB
		$f_{IN} = 20$ kHz, $V_{IN} = 4.85\ V_{p-p}$	−82		dB
	Bipolar Two Tone Intermodulation Distortion (Note 17)	$V_{IN} = \pm 4.85V$, $f_{IN1} = 19.375$ kHz, $f_{IN2} = 20.625$ kHz	−78	**−74**	dB (max)
	Unipolar Two Tone Intermodulation Distortion (Note 17)	$V_{IN} = 4.85\ V_{p-p}$, $f_{IN1} = 19.375$ kHz, $f_{IN2} = 20.625$ kHz	−78	**−73**	dB (max)
	−3 dB Bipolar Full Power Bandwidth	$V_{IN} = \pm 4.85V$ (Note 17)	25	**20**	kHz (Min)
	−3 dB Unipolar Full Power Bandwidth	$V_{IN} = 4.85\ V_{p-p}$ (Note 17)	30	**20**	kHz (Min)
	Aperture Time		100		ns
	Aperture Jitter		100		ps_{rms}

Digital and DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and $f_{CLK} = 2.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limits)
$V_{IN(1)}$	Logical "1" Input Voltage for All Inputs except CLK IN	$V_{CC} = 5.25V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage for All Inputs except CLK IN	$V_{CC} = 4.75V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$	0.005	**1**	μA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1**	μA (max)
V_T^+	CLK IN Positive-Going Threshold Voltage		2.8	**2.7**	V (min)
V_T^-	CLK IN Negative-Going Threshold Voltage		2.1	**2.3**	V (max)
V_H	CLK IN Hysteresis $[V_T^+ (min) - V_T^- (max)]$		0.7	**0.4**	V (min)
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 4.75V$: $I_{OUT} = -360\ \mu A$ $I_{OUT} = -10\ \mu A$		 **2.4** **4.5**	 V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 4.75V$, $I_{OUT} = 1.6$ mA		**0.4**	V (max)

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Digital and DC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $V_{REF} = +5.0V$, and $f_{CLK} = 2.0$ MHz unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7) (Continued)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limits)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$	−0.01	**−3**	μA (max)
		$V_{OUT} = 5V$	0.01	**3**	μA (max)
I_{SOURCE}	Output Source Current	$V_{OUT} = 0V$	−20	**−6.0**	mA (min)
I_{SINK}	Output Sink Current	$V_{OUT} = 5V$	20	**8.0**	mA (min)
DI_{CC}	DV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	1	**2**	mA (max)
AI_{CC}	AV_{CC} Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA (max)
I^-	V^- Supply Current	$f_{CLK} = 2$ MHz, $\overline{CS}$ = "1"	2.8	**6**	mA (max)

AC Electrical Characteristics

The following specifications apply for $DV_{CC} = AV_{CC} = +5.0V$, $V^- = -5.0V$, $t_r = t_f = 20$ ns unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$. (Notes 6 and 7)

Symbol	Parameter	Conditions	Typical (Note 9)	Limit (Notes 10, 19)	Units (Limits)
f_{CLK}	Clock Frequency		0.5 4.0	 **2.0**	MHz (min) MHz (max)
	Clock Duty Cycle		50	 **40** **60**	% % (min) % (max)
t_C	Conversion Time		$27(1/f_{CLK})$	$\mathbf{27(1/f_{CLK}) + 300\ ns}$	(max)
		$f_{CLK} = 2.0$ MHz	13.5		μs
t_A	Acquisition Time (Note 15)	$R_{SOURCE} = 50\Omega$, $f_{CLK} = 2.0$ MHz	$7(1/f_{CLK})$	$\mathbf{7(1/f_{CLK}) + 300\ ns}$	(max)
			3.5		μs
t_Z	Auto Zero Time		$26(1/f_{CLK})$	$\mathbf{26(1/f_{CLK})}$	(max)
		$f_{CLK} = 2.0$ MHz	13		μs
t_{CAL}	Calibration Time		$1396(1/f_{CLK})$		max
		$f_{CLK} = 2.0$ MHz	698	**706**	μs (max)
$t_{W(CAL)L}$	Calibration Pulse Width	(Note 16)	60	**200**	ns (min)
$t_{W(WR)L}$	Minimum $\overline{WR}$ Pulse Width		60	**200**	ns (min)
t_{ACC}	Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100$ pF	50	85	ns (max)
t_{0H}, t_{1H}	TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1$ kΩ, $C_L = 100$ pF	30	90	ns (max)
$t_{PD(INT)}$	Maximum Delay from Falling Edge of $\overline{RD}$ or $\overline{WR}$ to Reset of $\overline{INT}$		100	**175**	ns (max)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to AGND and DGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > (AV_{CC}$ or $DV_{CC})$, the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.

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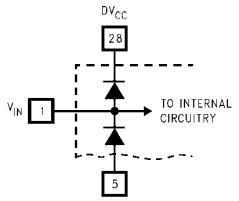
AC Electrical Characteristics (Continued)

Note 4: The power dissipation of this device under normal operation should never exceed 169 mW (Quiescent Power Dissipation + TTL Loads on the digital outputs). Caution should be taken not to exceed absolute maximum power rating when the device is operating in a severe fault condition (ex. when any inputs or outputs exceed the power supply). The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{Jmax} = 125°C$, and the typical thermal resistance (θ_{JA}) of the ADC12441 with CMJ and CIJ suffixes when board mounted is 47°C/W.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to the analog input as shown below. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV.



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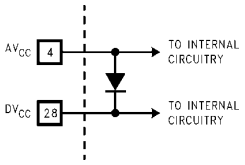
This means that if AV_{CC} and DV_{CC} are minimum (4.75 V_{DC}) and V^- is maximum (−4.75 V_{DC}), full-scale must be ≤ 4.8 V_{DC}.

Note 7: A diode exists between AV_{CC} and DV_{CC} as shown below.



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To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.

Note 8: Accuracy is guaranteed at $f_{CLK} = 2.0$ MHz. At higher and lower clock frequencies accuracy may degrade. See curves in the Typical Performance Characteristics section.

Note 9: Typicals are at $T_J = 25°C$ and represent most likely parametric norm.

Note 10: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero. (See *Figures 1b* and *1c*.)

Note 12: The ADC12441's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

Note 13: If T_A changes then an Auto-Zero or Auto-Cal cycle will have to be re-started (see the Typical Performance Characteristic curves).

Note 14: After an Auto-Zero or Auto-Cal cycle at the specified power supply extremes.

Note 15: If the clock is asynchronous to the falling edge of $\overline{WR}$ an uncertainty of one clock period will exist in the interval of t_A, therefore making the minimum $t_A = 6$ clock periods and the maximum $t_A = 7$ clock periods. If the falling edge of the clock is synchronous to the rising edge of $\overline{WR}$ then t_A will be exactly 6.5 clock periods.

Note 16: The $\overline{CAL}$ line must be high before a conversion is started.

Note 17: The specifications for these parameters are valid after an Auto-Cal cycle has been completed.

Note 18: The ADC12441 reference ladder is composed solely of capacitors.

Note 19: A Military RETS Electrical Test Specification is available on request. At time of printing the ADC12441CMJ/883 RETS complies fully with the **boldface** limits in this column.

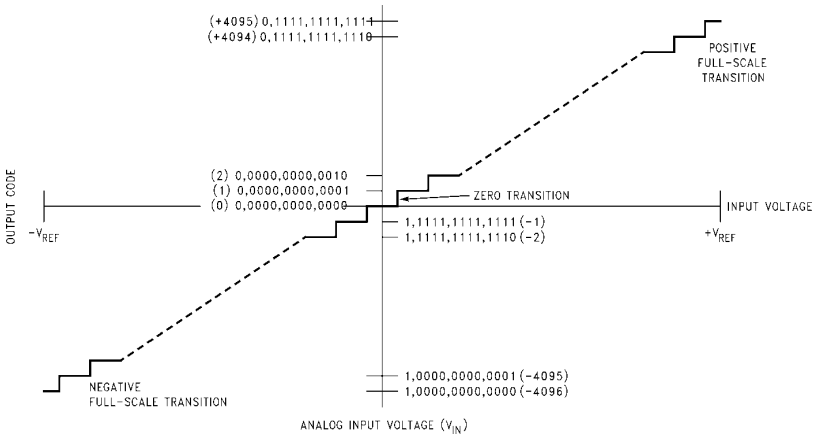

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FIGURE 1a. Transfer Characteristic

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Electrical Characteristics (Continued)

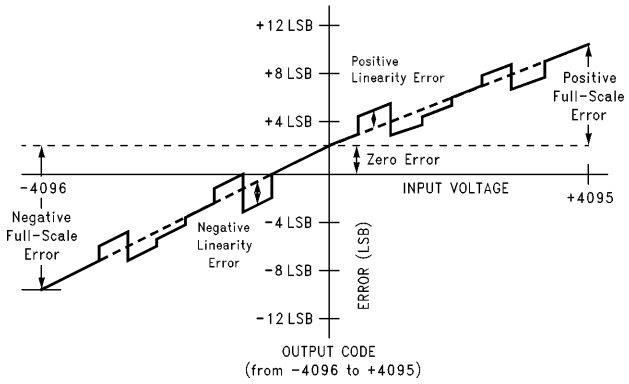

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FIGURE 1b. Simplified Error Curve vs Output Code without Auto-Cal or Auto-Zero Cycles

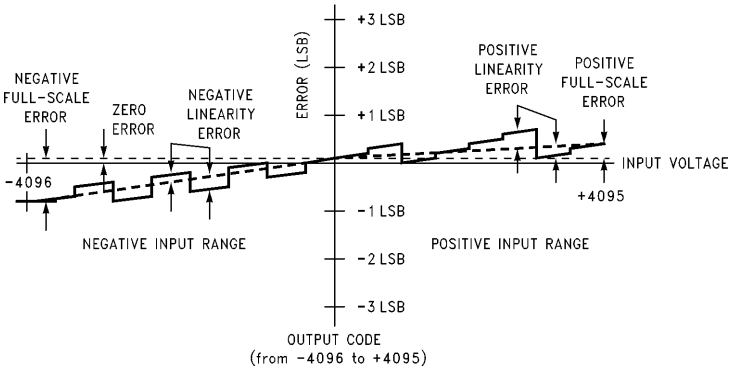

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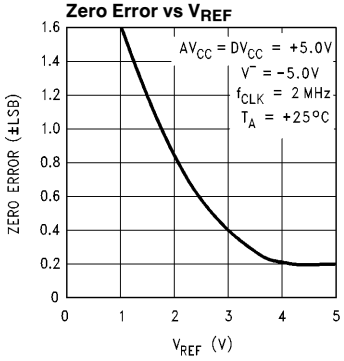
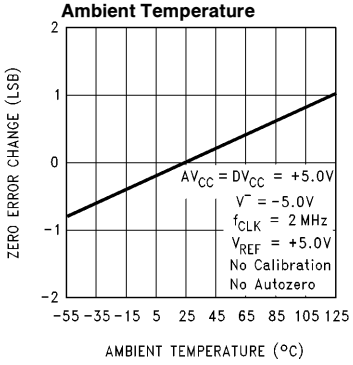
FIGURE 1c. Simplified Error Curve vs Output Code after Auto-Cal Cycle

Typical Performance Characteristics

Zero Error vs V_{REF}



Zero Error Change vs Ambient Temperature



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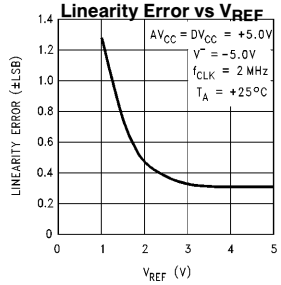
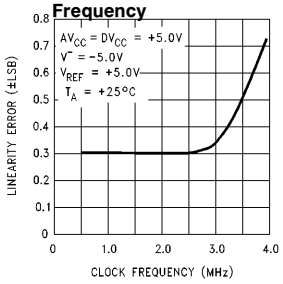
Typical Performance Characteristics (Continued)

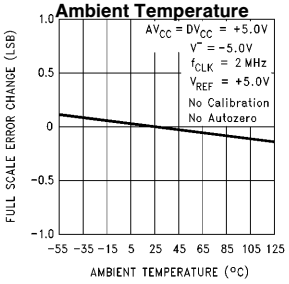
Linearity Error vs V_{REF}



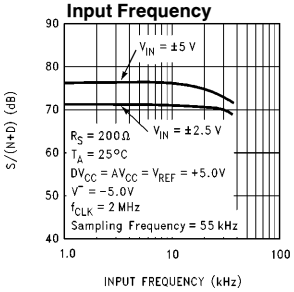
Linearity Error vs Clock Frequency



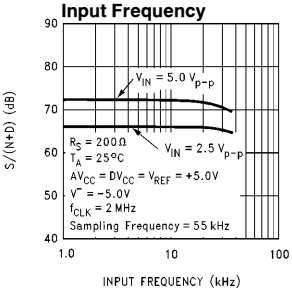
Full Scale Error Change vs Ambient Temperature



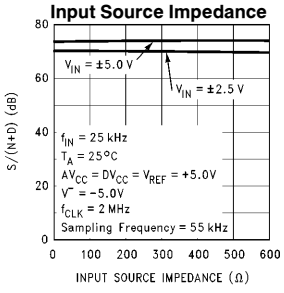
Bipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



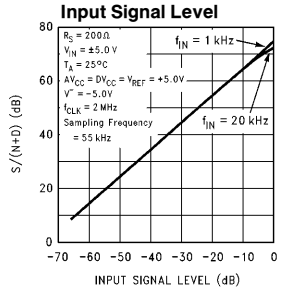
Unipolar Signal-to-Noise + Distortion Ratio vs Input Frequency



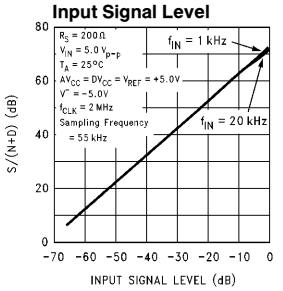
Bipolar Signal-to-Noise + Distortion Ratio vs Input Source Impedance



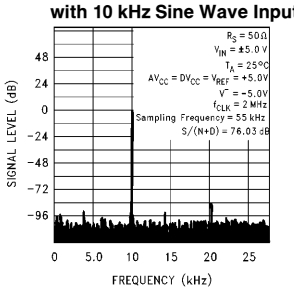
Bipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



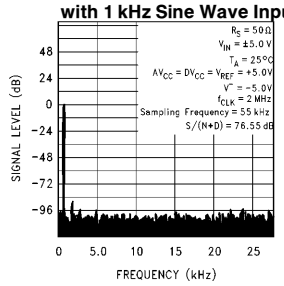
Unipolar Signal-to-Noise + Distortion Ratio vs Input Signal Level



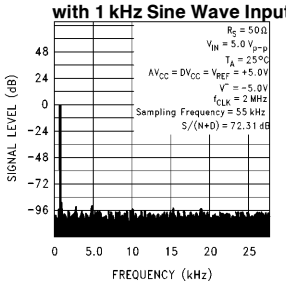
Bipolar Spectral Response with 10 kHz Sine Wave Input



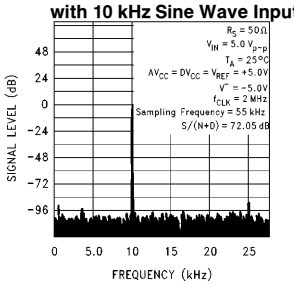
Bipolar Spectral Response with 1 kHz Sine Wave Input



Unipolar Spectral Response with 1 kHz Sine Wave Input



Unipolar Spectral Response with 10 kHz Sine Wave Input



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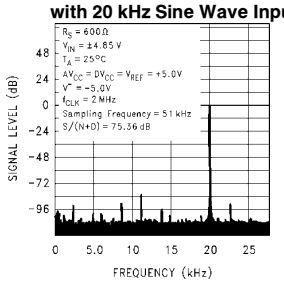
Typical Performance Characteristics (Continued)

Bipolar Spectral Response with 20 kHz Sine Wave Input



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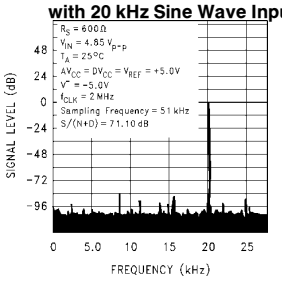
Unipolar Spectral Response with 20 kHz Sine Wave Input



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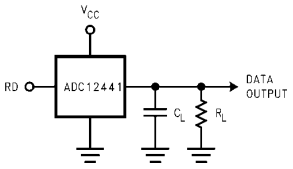
Test Circuits



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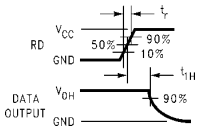

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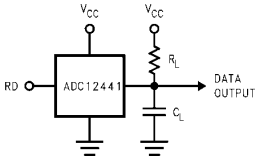

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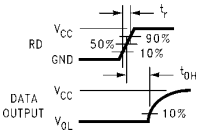

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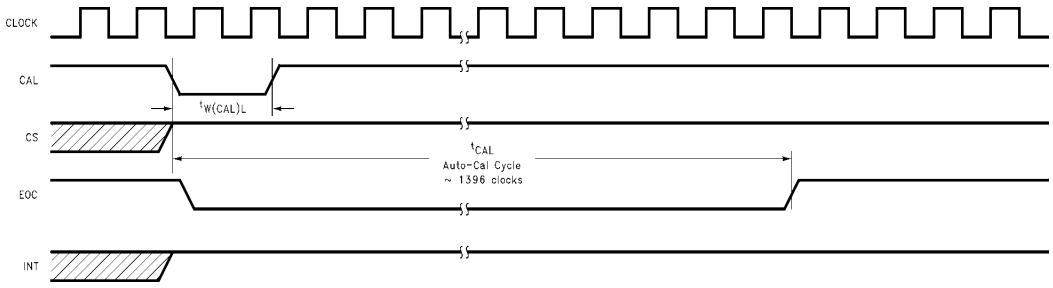
FIGURE 2. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

Auto-Cal Cycle ($\overline{CS}$ = 1, $\overline{WR}$ = X, $\overline{RD}$ = X, $\overline{AZ}$ = X, X = Don't Care)



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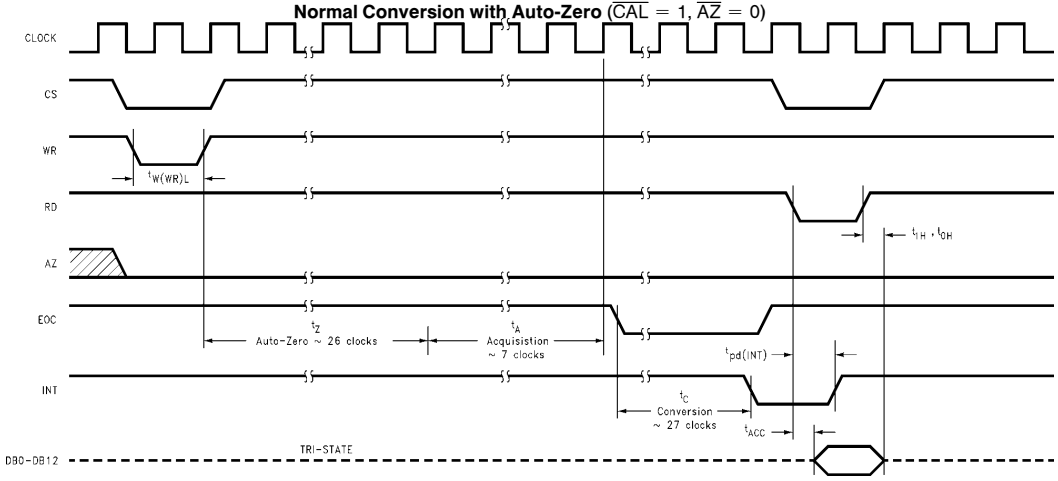
Timing Diagrams (Continued)

Normal Conversion with Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 0)



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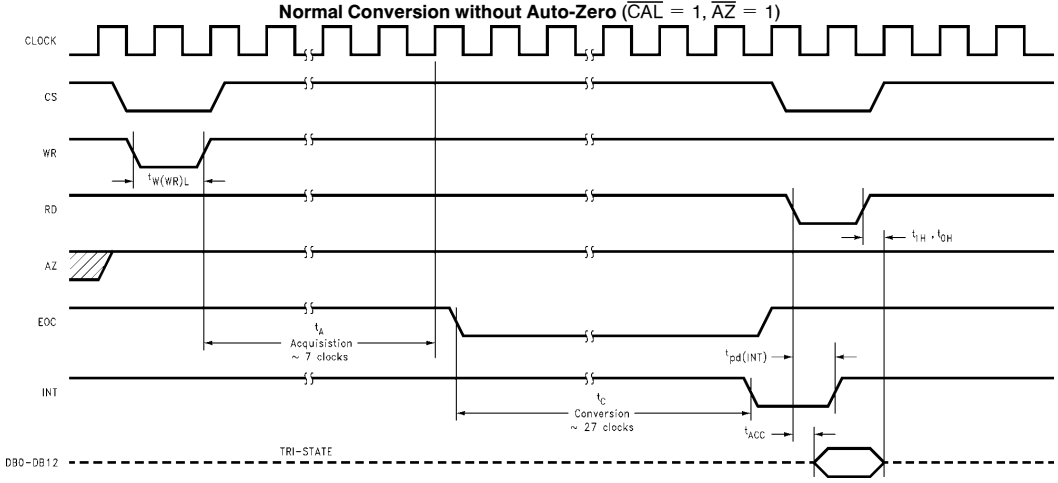
Normal Conversion without Auto-Zero ($\overline{CAL}$ = 1, $\overline{AZ}$ = 1)



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1.0 Pin Descriptions

DV_{CC} (28), AV_{CC} (4) — The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC12441 is +4.5V to +5.5V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass filters (10 μF tantalum in parallel with a 0.1 μF ceramic) at each V_{CC} pin.

V^- (5) — The analog negative supply voltage pin. V^- has a range of −4.5V to −5.5V and needs a bypass filter of 10 μF tantalum in parallel with a 0.1 μF ceramic.

DGND (14), AGND (3) — The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.

V_{REF} (2) — The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed the AV_{CC} or DV_{CC} by more than 50 mV or go below 3.5 VDC.

V_{IN} (1) — The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V^- by more than 50 mV.

$\overline{CS}$ (10) — The Chip Select control input. This input is active low and enables the $\overline{WR}$ and $\overline{RD}$ functions.

$\overline{RD}$ (11) — The Read control input. With both $\overline{CS}$ and $\overline{RD}$ low the TRI-STATE output buffers are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ (7) — The Write control input. The converison is started on the rising edge of the $\overline{WR}$ pulse when $\overline{CS}$ is low.

CLK (8) — The external clock input pin. The clock frequency range is 500 kHz to 4 MHz.

$\overline{CAL}$ (9) — The Auto-Calibration control input. When $\overline{CAL}$ is low the ADC12441 is reset and a calibration cycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.

$\overline{AZ}$ (6) — The Auto-Zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC12441 goes into an auto-zero cycle before the actual A/D conversion is started. This Auto-Zero cycle corrects for the comparator offset voltage. The total conversion time (t_C) is increased by 26 clock periods when Auto-Zero is used.

EOC (12) — The End-of-Conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{INT}$ (13) — The Interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

DB0–DB12 (15–27) — The TRI-STATE output pins. The output is in two's complement format with DB12 the sign bit, DB11 the MSB and DB0 the LSB.

2.0 Functional Description

The ADC12441 is a 12-bit plus sign A/D converter with the capability of doing Auto-Zero or Auto-Cal routines to minimize zero, full-scale and linearity errors. It is a successive-approximation A/D converter consisting of a DAC, comparator and a successive-approximation register (SAR). Auto-Zero is an internal calibration sequence that corrects for the A/D's zero error caused by the comparator's offset voltage. Auto-Cal is a calibration cycle that not only corrects zero error but also corrects for full-scale and linearity errors caused by DAC inaccuracies. Auto-Cal minimizes the errors of the ADC12441 without the need of trimming during its fabrication. An Auto-Cal cycle can restore the accuracy of the ADC12441 at any time, which ensures its long term stability.

2.1 DIGITAL INTERFACE

On power up, a calibration sequence should be initiated by pulsing $\overline{CAL}$ low with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ high. To acknowledge the $\overline{CAL}$ signal, EOC goes low after the falling edge of $\overline{CAL}$, and remains low during the calibration cycle of 1396 clock periods. During the calibration sequence, first the comparator's offset is determined, then the capacitive DAC's mismatch error is found. Correction factors for these errors are then stored in internal RAM.

A conversion is initiated by taking $\overline{CS}$ and $\overline{WR}$ low. The $\overline{AZ}$ (Auto Zero) signal line should be tied high or low during the conversion process. If $\overline{AZ}$ is low an auto zero cycle, which takes approximately 26 clock periods, occurs before the actual conversion is started. The auto zero cycle determines the correction factors for the comparator's offset voltage. If $\overline{AZ}$ is high, the auto zero cycle is skipped. Next the analog input is sampled for 7 clock periods, and held in the capacitive DAC's ladder structure. The EOC then goes low, signaling that the analog input is no longer being sampled and that the A/D successive approximation conversion has started.

During a conversion, the sampled input voltage is successively compared to the output of the DAC. First, the acquired input voltage is compared to analog ground to determine its polarity. The sign bit is set low for positive input voltages and high for negative. Next the MSB of the DAC is set high with the rest of the bits low. If the input voltage is greater than the output of the DAC, then the MSB is left high; otherwise it is set low. The next bit is set high, making the output of the DAC three quarters or one quarter of full scale. A comparison is done and if the input is greater than the new DAC value this bit remains high; if the input is less than the new DAC value the bit is set low. This process continues until each bit has been tested. The result is then stored in the output latch of the ADC12441. Next EOC goes high, and $\overline{INT}$ goes low to signal the end of the conversion. The result can now be read by taking $\overline{CS}$ and $\overline{RD}$ low to enable the DB0–DB12 output buffers.

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2.0 Functional Description (Continued)

Digital Control Inputs					A/D Function
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⌐¬	⌐¬	1	1	1	Start Conversion without Auto-Zero
⌐¬	1	⌐¬	1	1	Read Conversion Result without Auto-Zero
⌐¬	⌐¬	1	1	0	Start Conversion with Auto-Zero
⌐¬	1	⌐¬	1	0	Read Conversion Result with Auto-Zero
1	X	X	⌐¬	X	Start Calibration Cycle
0	X	1	0	X	Test Mode (DB2, DB3, DB5 and DB6 become active)

FIGURE 1. Function of the A/D Control Inputs

The table in *Figure 1* summarizes the effect of the digital control inputs on the function of the ADC12441. The Test Mode, where $\overline{RD}$ is high and $\overline{CS}$ and $\overline{CAL}$ are low, is used during manufacture to thoroughly check out the operation of the ADC12441. Care should be taken not to inadvertently be in this mode, since DB2, DB3, DB5, and DB6 become active outputs, which may cause data bus contention.

2.2 RESETTING THE A/D

All internal logic can be reset, which will abort any conversion in process. The A/D is reset whenever a new conversion is started by taking $\overline{CS}$ and $\overline{WR}$ low. If this is done when the analog input is being sampled or when EOC is low, the Auto-Cal correction factors may be corrupted, therefore requiring an Auto-Cal cycle before the next conversion. This is true with or without Auto-Zero. The Calibration Cycle cannot be reset once started. On power-up the ADC12441 automatically goes through a Calibration Cycle that takes typically 1396 clock cycles. For reasons that will be discussed in Section 3.7, a new calibration cycle needs to be started after the completion of the automatic one.

3.0 Analog Considerations

3.1 REFERENCE VOLTAGE

The voltage applied to the reference input of the converter defines the voltage span of the analog input (the difference between V_{IN} and AGND), over which 4095 positive output codes and 4096 negative output codes exist. The A-to-D can be used in either ratiometric or absolute reference applications. The voltage source driving V_{REF} must have a very low output impedance and very low noise. The circuit in *Figure 2a* is an example of a very stable reference that is appropriate for use with the ADC12441. The simple reference circuit of *Figure 2b* may be used when the application does not require low full scale errors.

In a ratiometric system, the analog input voltage is proportional to the voltage used for the A/D reference. When this voltage is the system power supply, the V_{REF} pin can be tied to V_{CC}. This technique relaxes the stability requirement of the system reference as the analog input and A/D reference move together maintaining the same output code for given input condition.

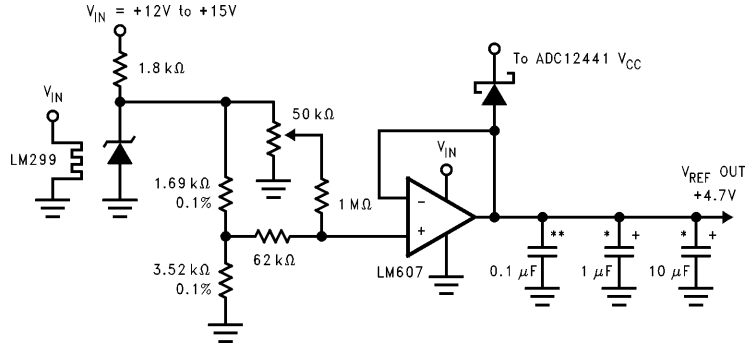
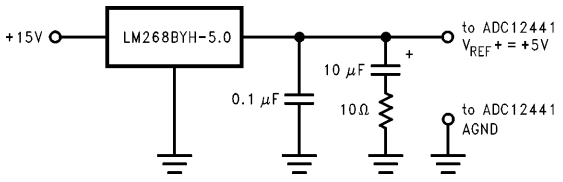


FIGURE 2a. Low Drift Extremely Stable Reference Circuit



Errors without any trims:	25°C	−40°C to +85°C
Full Scale	±0.075%	±0.2%
Zero	±0.024%	±0.024%
Linearity	±½ LSB	±½ LSB

FIGURE 2b. Simple Reference Circuit

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3.0 Analog Considerations (Continued)

For absolute accuracy, where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. In general, the magnitude of the reference voltage will require an initial adjustment to null out full-scale errors.

3.2 INPUT CURRENT

Because the input network of the ADC12441 is made up of a switch and a network of capacitors, a charging current will flow into or out of (depending on the input voltage polarity) of the analog input pin (V_{IN}) on the start of the analog input sampling period (t_A). The peak value of this current will depend on the actual input voltage applied.

3.3 NOISE

The leads to the analog input pin should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to this input can cause errors. Input filtering can be used to reduce the effects of these noise sources.

3.4 INPUT BYPASS CAPACITORS

An external capacitor can be used to filter out any noise due to inductive pickup by a long input lead and will not degrade the accuracy of the conversion result.

3.5 INPUT SOURCE RESISTANCE

The analog input can be modeled as shown in *Figure 3*. External R_S will lengthen the time period necessary for the voltage on C_{REF} to settle to within ½ LSB of the analog input voltage. With $f_{CLK} = 2$ MHz $t_A = 7$ clock periods $= 3.5\ \mu s$, $R_S \leq 1\ k\Omega$ will allow a 5V analog input voltage to settle properly.

3.6 POWER SUPPLIES

Noise spikes on the V_{CC} and V^- supply lines can cause conversion errors as the comparator will respond to this noise. The A/D is especially sensitive during the auto-zero or auto-cal procedures to any power supply spikes. Low inductance tantalum capacitors of 10 μF or greater paralleled with 0.1 μF ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors whould be placed close to the DV_{CC}, AV_{CC} and V^- pins. If an unregulated voltage source is available in the system, a separate LM340LAZ-5.0 voltage regulator for the A-to-D's V_{CC} (and other analog circuitry) will greatly reduce digital noise on the supply line.

3.7 THE CALIBRATION CYCLE

On power up the ADC12441 goes through an Auto-Cal cycle which cannot be interrupted. Since the power supply, reference, and clock will not be stable at power up, this first calibration cycle will not result in an accurate calibration of the A/D. A new calibration cycle needs to be started after the power supplies, reference, and clock have been given enough time to stabilize. During the calibration cycle, correction values are determined for the offset voltage of the sampled data comparator and any linearity and gain errors. These values are stored in internal RAM and used during an analog-to-digital conversion to bring the overall full scale, offset, and linearity errors down to the specified limits. Full scale error typically changes ± 0.1 LSB over temperature and linearity error changes even less; therefore it should be necessary to go through the calibration cycle only once after power up, if auto-zero is used to correct the zero error change.

3.8 THE AUTO-ZERO CYCLE

To correct for any change in the zero (offset) error of the A/D, the auto-zero cycle can be used. It may be necessary to do an auto-zero cycle whenever the ambient temperature changes significantly. (See the curved titled ''Zero Error Change vs Ambient Temperature'' in the Typical Performance Characteristics.) A change in the ambient temperature will cause the V_{OS} of the sampled data comparator to change, which may cause the zero error of the A/D to be greater than ± 1 LSB. An auto-zero cycle will maintain the zero error to ± 1 LSB or less.

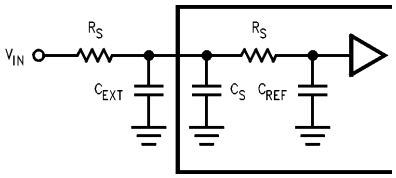

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FIGURE 3. Analog Input Equivalent Circuit

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4.0 Dynamic Performance

Many applications require the A/D converter to digitize ac signals, but the standard dc integral and differential nonlinearity specifications will not accurately predict the A/D converter's performance with ac input signals. The important specifications for ac applications reflect the converter's ability to digitize ac signals without significant spectral errors and without adding noise to the digitized signal. Dynamic characteristics such as signal-to-noise ratio (S/N), signal-to-noise + distortion ratio (S/(N + D)), effective bits, full power bandwidth, aperture time and aperture jitter are quantitative measures of the A/D converter's capability.

An A/D converter's ac performance can be measured using Fast Fourier Transform (FFT) methods. A sinusoidal waveform is applied to the A/D converter's input, and the transform is then performed on the digitized waveform. S/(N + D) and S/N are calculated from the resulting FFT data, and a spectral plot may also be obtained. Typical values for S/N are shown in the table of Electrical Characteristics, and spectral plots of S/(N + D) are included in the typical performance curves.

The A/D converter's noise and distortion levels will change with the frequency of the input signal, with more distortion and noise occurring at higher signal frequencies. This can be seen in the S/(N + D) versus frequency curves. These curves will also give an indication of the full power bandwidth (the frequency at which the S/(N + D) or S/N drops 3 dB).

Effective number of bits can also be useful in describing the A/D's noise performance. An ideal A/D converter will have some amount of quantization noise, determined by its resolution, which will yield an optimum S/N ratio given by the following equation:

$$S/N = (6.02 \times n + 1.8)dB$$

where n is the A/D's resolution in bits.

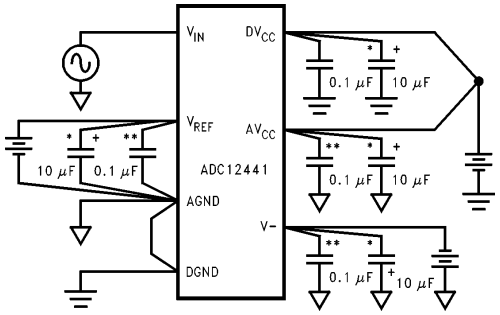
The effective bits of a real A/D converter, therefore, can be found by:

$$n(\text{effective}) = \frac{S/N(dB) - 1.8}{6.02}$$

As an example, an ADC12441 with a ±5V, 10 kHz sine wave input signal will typically have a S/N of 78 dB, which is equivalent to 12.6 effective bits.

Two sample/hold specifications, aperture time and aperture jitter, are included in the Dynamic Characteristics table since the ADC12441 has the ability to track and hold the analog input voltage. Aperture time is the delay for the A/D to respond to the hold command. In the case of the ADC12441, the hold command is internally generated. When the Auto-Zero function is not being used, the hold command occurs at the end of the acquisition window, or seven clock periods after the rising edge of the $\overline{WR}$. The delay between the internally generated hold command and the time that the ADC12441 actually holds the input signal is the aperture time. For the ADC12441, this time is typically 100 ns. Aperture jitter is the change in the aperture time from sample to sample. Aperture jitter is useful in determining the maximum slew rate of the input signal for a given accuracy. For example, an ADC12441 with 100 ps of aperture jitter operating with a 5V reference can have an effective gain variation of about 1 LSB with an input signal whose slew rate is 12 V/μs.

Power Supply Bypassing



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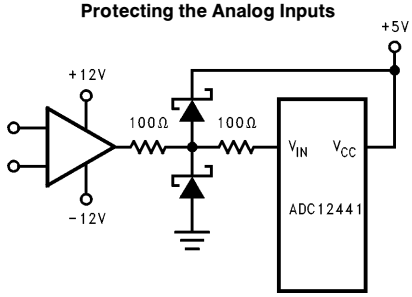
*Tantalum
**Ceramic

Protecting the Analog Inputs



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Note: External protection diodes should be able to withstand the op amp current limit.

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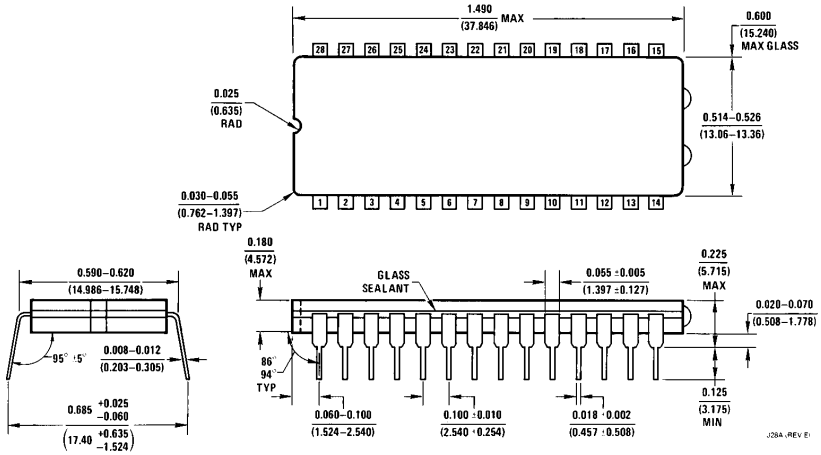
Physical Dimensions inches (millimeters)



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NS Package Number J28A

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