

### FEATURES

- 2 Matched ADCs on Single Chip
- 50 MSPS Conversion Speed
- On-Board Voltage Reference
- Low Power (<1 W)
- Low Input Capacitance (10 pF)
- 65 V Power Supplies
- Flexible Input Range

### APPLICATIONS

- Quadrature Demodulation for Communications
- Digital Oscilloscopes
- Electronic Warfare
- Radar

### GENERAL DESCRIPTION

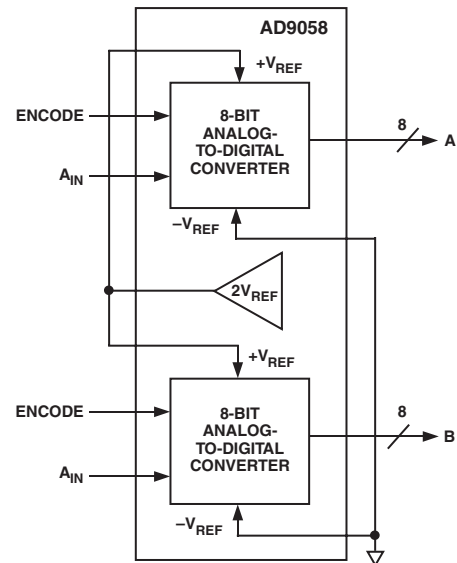
The AD9058 combines two independent, high performance, 8-bit analog-to-digital converters (ADCs) on a single monolithic IC. Combined with an optional on-board voltage reference, the AD9058 provides a cost-effective alternative for systems requiring two or more ADCs.

Dynamic performance (SNR, ENOB) is optimized to provide up to 50 MSPS conversion rates. The unique architecture results in low input capacitance while maintaining high performance and low power (<0.5 W/channel). Digital inputs and outputs are TTL compatible.

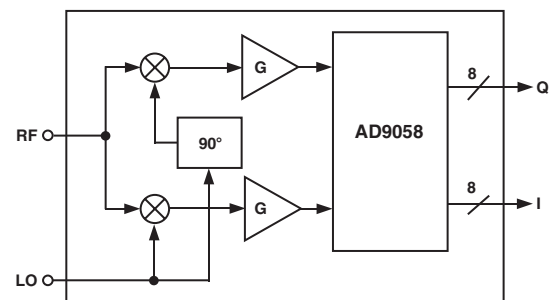
Performance has been optimized for an analog input of 2 V p-p ( $\pm 1$  V; 0 V to 2 V). Using the on-board 2 V voltage reference, the AD9058 can be set up for unipolar positive operation (0 V to 2 V). This internal voltage reference can drive both ADCs.

Commercial (0°C to 70°C) and military (-55°C to +125°C) temperature range parts are available. Parts are supplied in hermetic 48-lead DIP and 44-lead "J" lead packages.

### FUNCTIONAL BLOCK DIAGRAM



### QUADRATURE RECEIVER



### REV. D

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# AD9058—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS [ $\pm V_S = \pm 5\text{ V}$ ; $V_{REF} = 2\text{ V}$ (internal); ENCODE = 40 MSPS; $A_{IN} = 0\text{ V}$ to $2\text{ V}$ ; $-V_{REF} = \text{GROUND}$ , unless otherwise noted.] All specifications apply to either of the two ADCs.

Parameter	Temp	Test Level	AD9058AJD/AJJ			AD9058AKD/AKJ			Unit
			Min	Typ	Max	Min	Typ	Max	
RESOLUTION			8			8			Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		0.25	0.65		0.25	0.5	LSB
	Full	VI			0.8			0.7	LSB
Integral Nonlinearity	25°C	I		0.5	1.3		0.5	1.0	LSB
	Full	VI			1.4			1.25	LSB
No Missing Codes	Full	VI	Guaranteed			Guaranteed			
ANALOG INPUT									
Input Bias Current	25°C	I		75	170		75	170	$\mu\text{A}$
	Full	VI			340			340	$\mu\text{A}$
Input Resistance	25°C	I	12	28		12	28		k $\Omega$
Input Capacitance	25°C	IV		10	15		10	15	pF
Analog Bandwidth	25°C	V		175			175		MHz
REFERENCE INPUT									
Reference Ladder Resistance	25°C	I	120	170	220	120	170	220	$\Omega$
	Full	VI	80		270	80		270	$\Omega$
Ladder Tempco	Full	V		0.45			0.45		$\Omega/^\circ\text{C}$
Reference Ladder Offset (Top)	25°C	I		8	16		8	16	mV
	Full	VI			24			24	mV
Reference Ladder Offset (Bottom)	25°C	I		8	23		8	23	mV
	Full	VI			33			33	mV
Offset Drift Coefficient	Full	V		50			50		$\mu\text{V}/^\circ\text{C}$
INTERNAL VOLTAGE REFERENCE									
Reference Voltage	25°C	I	1.95	2.0	2.20	1.95	2.0	2.20	V
	Full	VI	1.90		2.25	1.90		2.25	V
Temperature Coefficient	Full	V		150			150		$\mu\text{V}/^\circ\text{C}$
Power Supply Rejection Ratio (PSRR)	25°C	I		10	25		10	25	mV/V
SWITCHING PERFORMANCE									
Maximum Conversion Rate <sup>2</sup>	25°C	I		50		50	60		MSPS
Aperture Delay ( $t_A$ )	25°C	IV	0.1	0.8	1.5	0.1	0.8	1.5	ns
Aperture Delay Matching	25°C	IV		0.2	0.5		0.2	0.5	ns
Aperture Uncertainty (Jitter)	25°C	V		10			10		ps, rms
Output Delay (Valid) ( $t_V$ ) <sup>2</sup>	25°C	I		8		5	8		ns
Output Delay ( $t_V$ ) Tempco	Full	V		16			16		ps/ $^\circ\text{C}$
Propagation Delay ( $t_{PD}$ ) <sup>2</sup>	25°C	I		12			12	19	ns
Propagation Delay ( $t_{PD}$ ) Tempco	Full	V		-16			-16		ps/ $^\circ\text{C}$
Output Time Skew	25°C	V		1			1		ns
ENCODE INPUT									
Logic "1" Voltage	Full	VI	2			2			V
Logic "0" Voltage	Full	VI			0.8			0.8	V
Logic "1" Current	Full	VI			600			600	$\mu\text{A}$
Logic "0" Current	Full	VI			1000			1000	$\mu\text{A}$
Input Capacitance	25°C	V		5			5		pF
Pulsewidth (High)	25°C	I		8		8			ns
Pulsewidth (Low)	25°C	I		8		8			ns

Parameter	Temp	Test Level	AD9058AJD/AJJ			AD9058AKD/AKJ			Unit
			Min	Typ	Max	Min	Typ	Max	
<b>DYNAMIC PERFORMANCE</b>									
Transient Response	25°C	V		2			2		ns
Overvoltage Recovery Time	25°C	V		2			2		ns
Effective Number of Bits (ENOB) <sup>3</sup>									
Analog Input @ 2.3 MHz	25°C	I		7.7		7.2	7.7		Bits
@ 10.3 MHz	25°C	I		7.4		7.1	7.4		Bits
Signal-to-Noise Ratio <sup>3</sup>									
Analog Input @ 2.3 MHz	25°C	I		48		45	48		dB
@ 10.3 MHz	25°C	I		46		44	46		dB
Signal-to-Noise Ratio <sup>3</sup> (Without Harmonics)									
Analog Input @ 2.3 MHz	25°C	I		48		46	48		dB
@ 10.3 MHz	25°C	I		47		45	47		dB
Second Harmonic Distortion									
Analog Input @ 2.3 MHz	25°C	I		58		48	58		dBc
@ 10.3 MHz	25°C	I		58		48	58		dBc
Third Harmonic Distortion									
Analog Input @ 2.3 MHz	25°C	I		58		50	58		dBc
@ 10.3 MHz	25°C	I		58		50	58		dBc
Crosstalk Rejection <sup>4</sup>	25°C	IV		60		48	60		dBc
<b>DIGITAL OUTPUTS</b>									
Logic "1" Voltage ( $I_{OH} = 2\text{ mA}$ )	Full	VI	2.4			2.4			V
Logic "0" Voltage ( $I_{OL} = 2\text{ mA}$ )	Full	VI			0.4			0.4	V
<b>POWER SUPPLY<sup>5</sup></b>									
+V <sub>S</sub> Supply Current	Full	VI		127	154		127	154	mA
-V <sub>S</sub> Supply Current	Full	VI		27	38		27	38	mA
Power Dissipation	Full	VI		770	960		770	960	mW

NOTES

<sup>1</sup>For applications in which +V<sub>S</sub> may be applied before -V<sub>S</sub>, or +V<sub>S</sub> current is not limited to 500 mA, a reverse-biased clamping diode should be inserted between ground and -V<sub>S</sub> to prevent destructive latch up. See section entitled "Using the AD9058."

<sup>2</sup>To achieve guaranteed conversion rate, connect each data output to ground through a 2 kΩ pull-down resistor.

<sup>3</sup>SNR performance limits for the 48-lead DIP "D" package are 1 dB less than shown. ENOB limits are degraded by 0.3 dB. SNR and ENOB measured with analog input signal 1 dB below full scale at specified frequency.

<sup>4</sup>Crosstalk rejection measured with full-scale signals of different frequencies (2.3 MHz and 3.5 MHz) applied to each channel. With both signals synchronously encoded at 40 MSPS, isolation of the undesired frequency is measured with an FFT.

<sup>5</sup>Applies to both A/Ss and includes internal ladder dissipation.

Specifications subject to change without notice.

# AD9058

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Analog Input	-1.5 V to +2.5 V
+V <sub>S</sub>	6 V
-V <sub>S</sub>	+0.8 V to -6 V <sup>2</sup>
Digital Inputs	-0.5 V to +V <sub>S</sub>
Digital Output Current	20 mA
Voltage Reference Current	53 mA
+V <sub>REF</sub>	2.5 V
-V <sub>REF</sub>	-1.5 V
Operating Temperature Range	
AD9058AJD/AJJ/AKD/AKJ	0°C to 70°C
Maximum Junction Temperature <sup>3</sup>	
AD9058AJD/AJJ/AKD/AKJ	150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

## NOTES

<sup>1</sup>Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

<sup>2</sup>For applications in which +V<sub>S</sub> may be applied before -V<sub>S</sub>, or +V<sub>S</sub> current is not limited to 500 mA, a reverse-biased clamping diode should be inserted between ground and -V<sub>S</sub> to prevent destructive latch up. See section entitled "Using the AD9058."

<sup>3</sup>Typical thermal impedances: 44-lead hermetic J-leaded ceramic package:  $\theta_{JA} = 86.4^{\circ}\text{C}/\text{W}$ ;  $\theta_{JC} = 24.9^{\circ}\text{C}/\text{W}$ ; 48-lead hermetic: DIP  $\theta_{JA} = 40^{\circ}\text{C}/\text{W}$ ;  $\theta_{JC} = 12^{\circ}\text{C}/\text{W}$ .

## EXPLANATION OF TEST LEVELS

### Test Level

- I. 100% production tested.
- II. 100% production tested at 25°C, and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. All devices are 100% production tested at 25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9058 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## ORDERING GUIDE

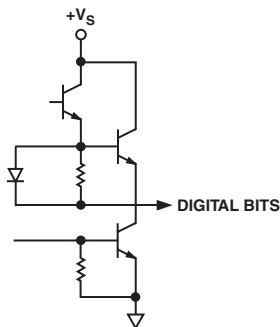
Model	Temperature Range	Description	Package Option <sup>1</sup>
AD9058AJJ	0°C to 70°C	44-Lead J-Leaded Ceramic <sup>2</sup>	J-44
AD9058AJJ-REEL	0°C to 70°C	44-Lead J-Leaded Ceramic <sup>2</sup>	J-44
AD9058AKJ	0°C to 70°C	44-Lead J-Leaded Ceramic, AC Tested	J-44
AD9058ATJ/883 <sup>3</sup>	-55°C to +125°C	44-Lead J-Leaded Ceramic, AC Tested	J-44
AD9058AJD	0°C to 70°C	48-Lead Ceramic DIP	D-48
AD9058AKD	0°C to 70°C	48-Lead Ceramic DIP, AC Tested	D-48
AD9058ATD/883 <sup>3</sup>	-55°C to +125°C	48-Lead Ceramic DIP, AC Tested	D-48

## NOTES

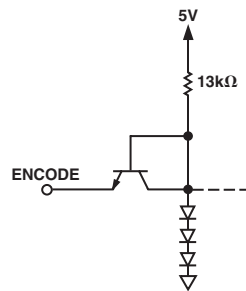
<sup>1</sup>D = Hermetic ceramic DIP package; J = leaded ceramic package.

<sup>2</sup>Hermetically sealed ceramic package; footprint equivalent to PLCC.

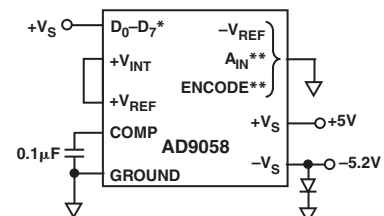
<sup>3</sup>For specifications, refer to Analog Devices Military Products Databook.



Equivalent Digital Outputs



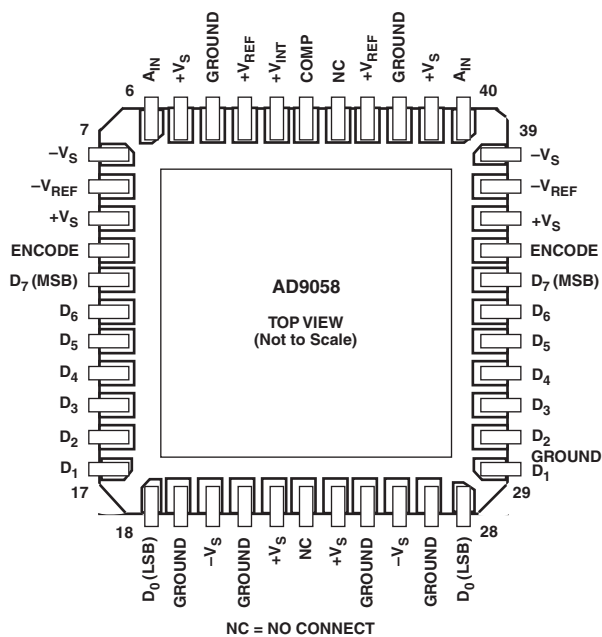
Equivalent Encode Circuit



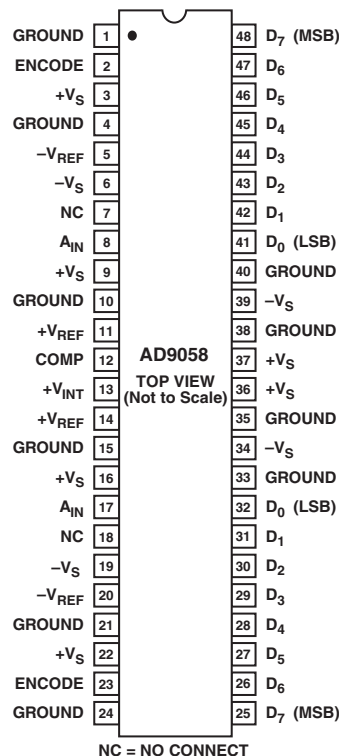
\* INDICATES EACH PIN IS CONNECTED THROUGH 2kΩ  
 \*\* INDICATES EACH PIN IS CONNECTED THROUGH 100Ω



## PIN CONFIGURATIONS



AD9058AJJ/AKJ Pinouts



AD9058AJD/AKD Pinouts

## PIN FUNCTION DESCRIPTIONS

J-Lead Pin Number		Mnemonic	Function	Ceramic DIP Pin Number	
ADC-A	ADC-B			ADC-A	ADC-B
3	43	+V <sub>REF</sub>	Top of Internal Voltage Reference Ladder	14	11
4	42	GROUND	Analog Ground Return	15	10
5	41	+V <sub>S</sub>	Positive 5 V Analog Supply Voltage	16	9
6	40	A <sub>IN</sub>	Analog Input Voltage	17	8
7	39	-V <sub>S</sub>	Negative 5 V Supply Voltage	19	6
8	38	-V <sub>REF</sub>	Bottom of Internal Voltage Reference Ladder	20	5
9	37	+V <sub>S</sub>	Positive 5 V Digital Supply Voltage	22	3
10	36	ENCODE	TTL Compatible Convert Command	23	2
11	35	D <sub>7</sub> (MSB)	Most Significant Bit of TTL Digital Output	25	48
12-17	34-29	D <sub>6</sub> -D <sub>1</sub>	TTL Compatible Digital Output Bits	26-31	47-42
18	28	D <sub>0</sub> (LSB)	Least Significant Bit of TTL Digital Output	32	41
19	27	GROUND	Digital Ground Return	21, 24, 33	1, 4, 40
20	26	-V <sub>S</sub>	Negative 5 V Supply Voltage	34	39
21	25	GROUND	Analog Ground Return	35	38
22	24	+V <sub>S</sub>	Positive 5 V Analog Supply Voltage	36	37
COMMON PINS				COMMON PINS	
1		COMP	Connection for External (0.1 μF) Compensation Capacitor	12	
2		+V <sub>INT</sub>	Internal 2 V Reference; Can Drive +V <sub>REF</sub> for Both ADCs	13	

# AD9058

## THEORY OF OPERATION

The AD9058 contains two separate 8-bit analog-to-digital converters (ADCs) on a single silicon die. The two devices can be operated independently with separate analog inputs, voltage references, and clocks.

In a traditional flash converter, 256 input comparators are required to make the parallel conversion for 8-bit resolution. This is in marked contrast to the scheme used in the AD9058, as shown in Figure 1.

Unlike traditional “flash,” or parallel, converters, each of the two ADCs in the AD9058 utilizes a patented interpolating architecture to reduce circuit complexity, die size, and input capacitance. These advantages accrue because, compared to a conventional flash design, only half the normal number of input comparator cells is required to accomplish the conversion.

In this unit, each of the two independent ADCs uses only 128 ( $2^7$ ) comparators to make the conversion. The conversion for the seven most significant bits (MSBs) is performed by the 128 comparators. The value of the least significant bit (LSB) is determined by interpolation between adjacent comparators in the decoding register. A proprietary decoding scheme processes the comparator outputs and provides an 8-bit code to the output register of each ADC; the scheme also minimizes error codes.

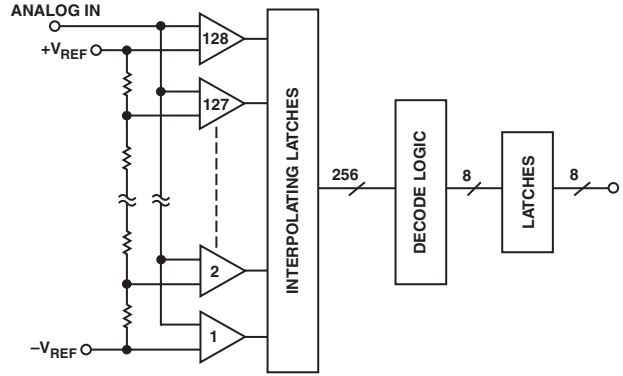


Figure 1. Comparator Block Diagram

Analog input range is established by the voltages applied at the voltage reference inputs ( $+V_{REF}$  and  $-V_{REF}$ ). The AD9058 can operate from 0 V to 2 V using the internal voltage reference, or anywhere between -1 V and +2 V using external references. Input range is limited to 2 V p-p when using external references. The internal resistor ladder divides the applied voltage reference into 128 steps, with each step representing two 8-bit quantization levels.

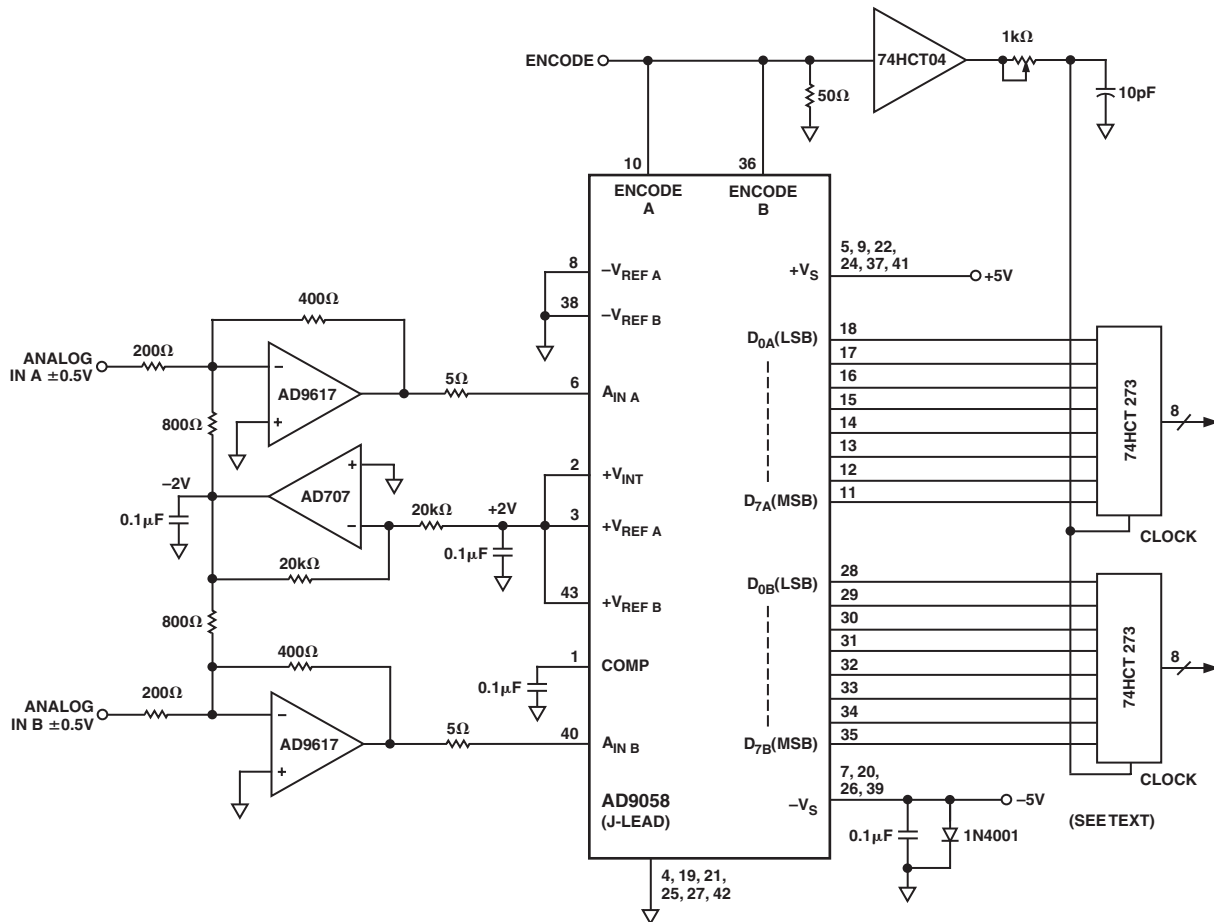


Figure 2. AD9058 Using Internal 2 V Voltage Reference

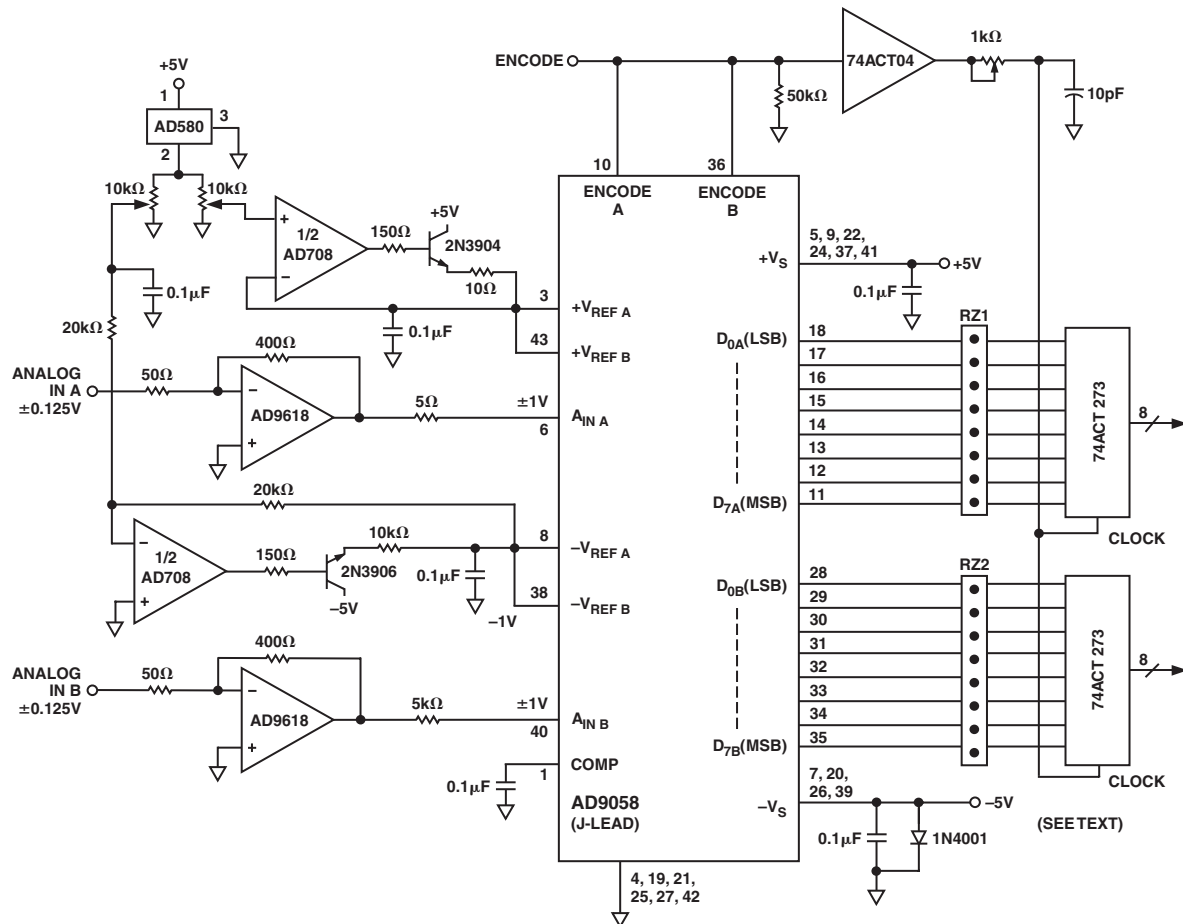


Figure 3. AD9058 Using External Voltage References

The on-board voltage reference,  $+V_{INT}$ , is a band gap reference that has sufficient drive capability for both reference ladders. It provides a 2 V reference that can drive both ADCs in the AD9058 for unipolar positive operation (0 V to 2 V).

#### USING THE AD9058

Refer to Figure 2. Using the internal voltage reference connected to both ADCs as shown reduces the number of external components required to create a complete data acquisition system. The input ranges of the ADCs are positive unipolar in this configuration, ranging from 0 V to 2 V. Bipolar input signals are buffered, amplified, and offset into the proper input range of the ADC using a good low distortion amplifier such as the AD9617 or AD9618.

The AD9058 offers considerable flexibility in selecting the analog input ranges of the ADCs; the two independent ADCs can even have different input ranges if required. In Figure 3, the AD9058 is shown configured for  $\pm 1$  V operation.

The “Reference Ladder Offset” shown in the specifications table refers to the error between the voltage applied to the  $+V_{REF}$  (top) or  $-V_{REF}$  (bottom) of the reference ladder and the voltage required at the analog input to achieve a 1111 1111 or 0000 0000 transition. This indicates the amount of adjustment range that must be designed into the reference circuit for the AD9058.

The diode shown between ground and  $-V_S$  is normally reverse-biased and is used to prevent latch-up. Its use is recommended for applications in which power supply sequencing might allow  $+V_S$  to be applied before  $-V_S$ ; or the  $+V_S$  supply is not current

limited. If the negative supply is allowed to float (the +5 V supply is powered up before the -5 V supply), substantial +5 V supply current will attempt to flow through the substrate ( $V_S$  supply contact) to ground. If this current is not limited to <500 mA, the part may be destroyed. The diode prevents this potentially destructive condition from occurring.

#### Timing

Refer to the AD9058 Timing Diagram, Figure 4. The AD9058 provides latched data outputs with no pipeline delay. To conserve power, the data outputs have relatively slow rise and fall times. When designing system timing, it is important to observe (1) setup and hold times; and (2) the intervals when data is changing.

Figure 3 shows 2 k $\Omega$  pull-down resistors on each of the  $D_0$ - $D_7$  output data bits. When operating at conversion rates higher than 40 MSPS, these resistors help equalize rise and fall times and ease latching the output data into external latches. The 74ACT logic family devices have short setup and hold times and are the recommended choices for speeds of 40 MSPS or more.

#### Layout

To ensure optimum performance, a single low impedance ground plane is recommended. Analog and digital grounds should be connected together and to the ground plane at the AD9058 device. Analog and digital power supplies should be bypassed to ground through 0.1  $\mu$ F ceramic capacitors as close to the unit as possible.

For prototyping or evaluation, surface-mount sockets are available from Methode Electronics, Inc. (Part No. 213-0320602) for evaluating AD9058 surface-mount packages. To evaluate the

# AD9058

AD9058 in through-hole PCB designs, use the AD9058AJD/AKD with individual pin sockets (AMP Part No. 6-330808-0). Alternatively, surface-mount AD9058 units can be mounted in a through-hole socket (Circuit Assembly Corporation, Irvine, California Part No. CA-44SPC-T).

## AD9058 APPLICATIONS

Combining two ADCs in a single package is an attractive alternative in a variety of systems when cost, reliability, and space are important considerations. Different systems emphasize particular specifications, depending on how the part is used.

In high density digital radio communications, a pair of high speed ADCs are used to digitize the in-phase (I) and quadrature (Q) components of a modulated signal. The signal presented to each ADC in this type of system consists of message-dependent amplitudes varying at the symbol rate, which is equal to the sample rates of the converters.

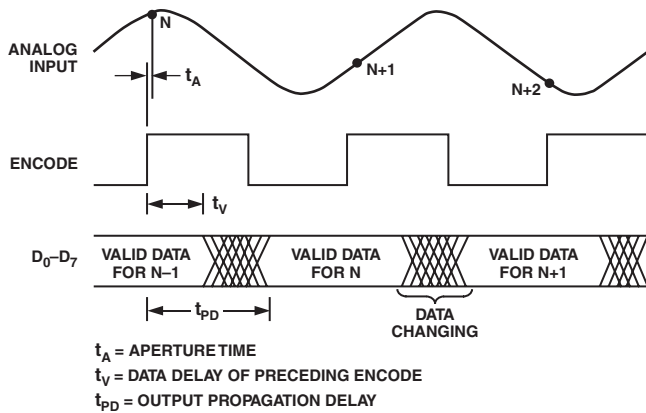


Figure 4. Timing Diagram

Figure 5 shows what the analog input to the AD9058 would look like when observed relative to the sample clock. Signal-to-noise ratio (SNR), transient response, and sample rate are all critical specifications in digitizing this “eye pattern.”

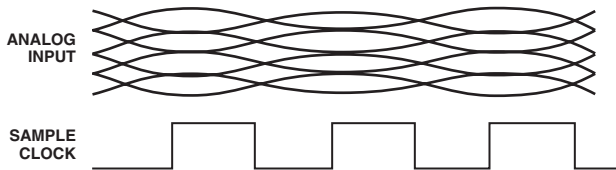


Figure 5. I and Q Input Signals

Receiver sensitivity is limited by the SNR of the system. For the ADC, SNR is measured in the frequency domain and calculated with a Fast Fourier Transform (FFT). The signal-to-noise ratio equals the ratio of the fundamental component of the signal (rms amplitude) to the rms level of the noise. Noise is the sum of all other spectral components, including harmonic distortion, but excluding dc.

Although the signal being sampled does not have a significant slew rate at the instant it is encoded, dynamic performance of the ADC and the system is still critical. Transient response is

the time required for the AD9058 to achieve full accuracy when a step function input is applied. Overvoltage recovery time is the interval required for the AD9058 to recover to full accuracy after an overdriven analog input signal is reduced to its input range.

Time domain performance of the ADC is also extremely important in digital oscilloscopes. When a track-/sample-and-hold is used ahead of the ADC, its operation becomes similar to that described above for receivers.

The dynamic response to high frequency inputs can be described by the effective number of bits (ENOB). The effective number of bits is calculated with a sine wave curve fit and is expressed as:

$$ENOB = N - \text{LOG}_2 \left[ \frac{\text{Error}(\text{measured})}{\text{Error}(\text{ideal})} \right]$$

where  $N$  is the resolution (number of bits) and measured error is actual rms error calculated from the converter's outputs with a pure sine wave applied as the input.

Maximum conversion rate is defined as the encode (sample) rate at which SNR of the lowest frequency analog test signal drops no more than 3 dB below the guaranteed limit.

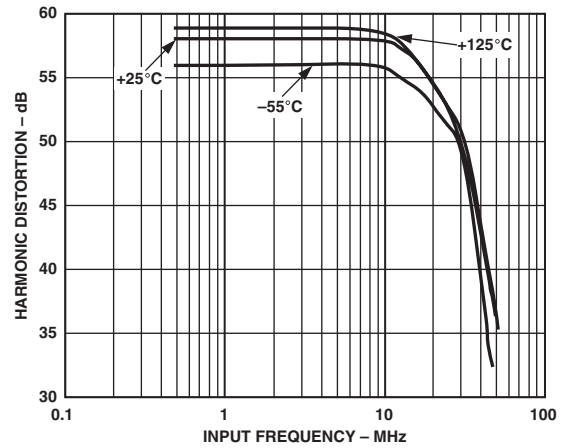


Figure 6. Harmonic Distortion vs. Analog Input Frequency

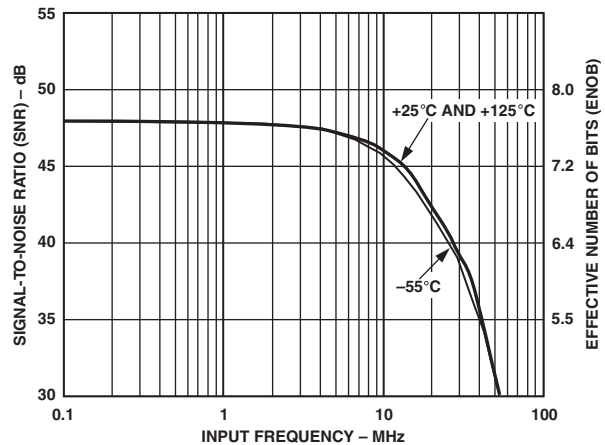
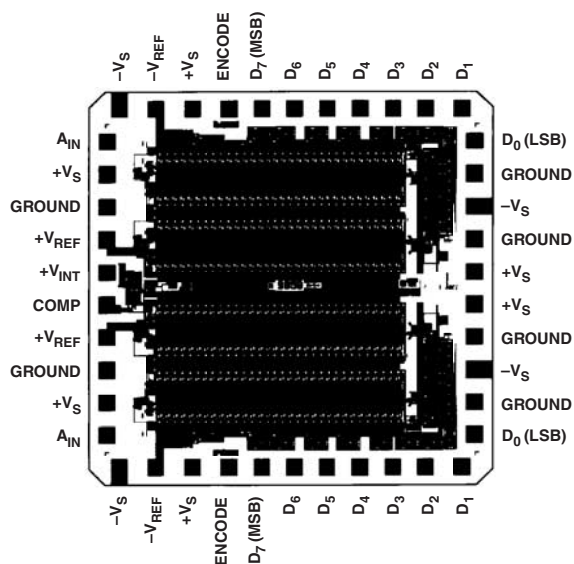


Figure 7. Dynamic Performance vs. Analog Input Frequency



MECHANICAL INFORMATION

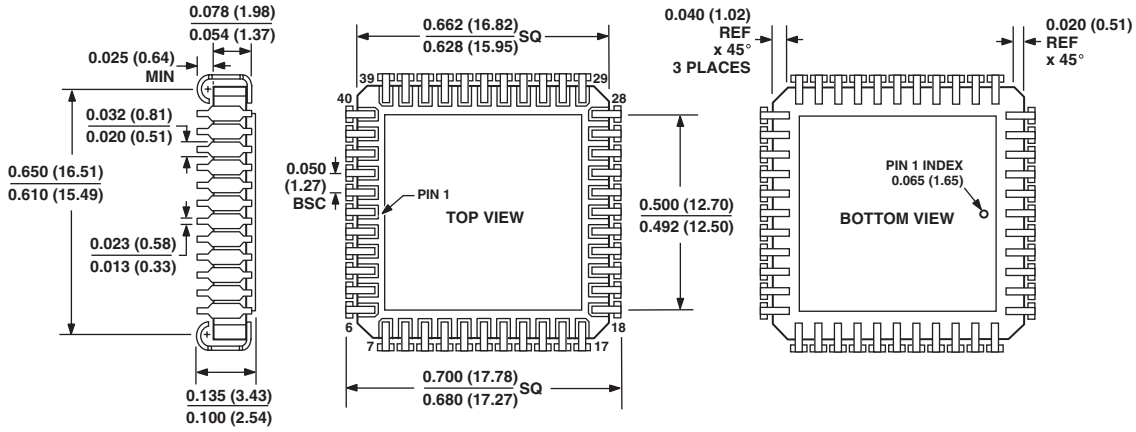
Die Dimensions . . . . . 106 mils × 108 mils × 15 (±2) mils  
 Pad Dimensions . . . . . 4 mils × 4 mils  
 Metallization . . . . . Gold  
 Backing . . . . . None  
 Substrate Potential . . . . .  $-V_S$   
 Passivation . . . . . Nitride  
 Die Attach . . . . . Gold Eutectic (Ceramic)  
 Bond Wire . . . . . 1 mil–1.3 mil, Gold; Gold Ball Bonding



OUTLINE DIMENSIONS

44-Lead Ceramic Leaded Chip Carrier — J-Formed Leads [JLCC]  
(J-44)

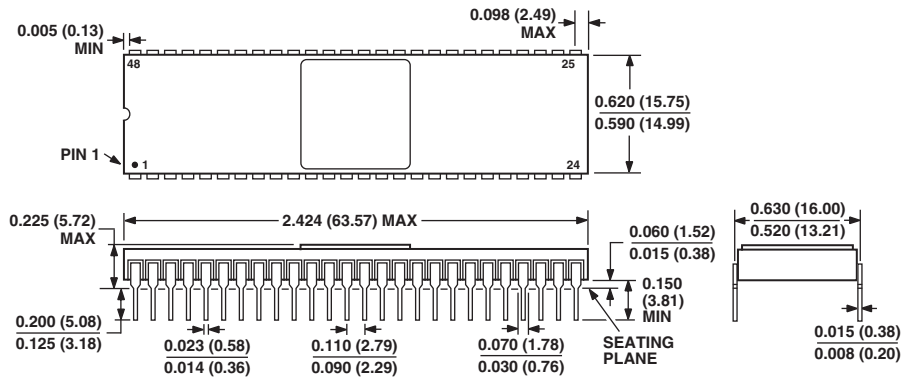
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

48-Lead Side-Brazed Solder Lid Ceramic DIP [DIP/SB]  
(D-48)

Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

## Revision History

Location	Page
<b>5/03—Data Sheet changed from REV. C to REV. D</b>	
Changes to ORDERING GUIDE .....	4
Changes to OUTLINE DIMENSIONS .....	10
<b>6/01—Data Sheet changed from REV. B to REV. C</b>	
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