

### FEATURES

**SNR = 59.4 dBFS @  $f_{IN}$  up to 70 MHz @ 250 MSPS**  
**ENOB of 9.7 @  $f_{IN}$  up to 70 MHz @ 250 MSPS (-1.0 dBFS)**  
**SFDR = 81 dBc @  $f_{IN}$  up to 70 MHz @ 250 MSPS (-1.0 dBFS)**  
**Excellent linearity**  
**DNL = 0.2 LSB typical**  
**INL = 0.2 LSB typical**  
**CMOS outputs**  
**Single data port at up to 250 MHz**  
**Demultiplexed dual port at up to  $2 \times 125$  MHz**  
**700 MHz full power analog bandwidth**  
**On-chip reference, no external decoupling required**  
**Integrated input buffer and track-and-hold**  
**Low power dissipation**  
**274 mW @ 200 MSPS**  
**322 mW @ 250 MSPS**  
**Programmable input voltage range**  
**1.0 V to 1.5 V, 1.25 V nominal**  
**1.8 V analog and digital supply operation**  
**Selectable output data format (offset binary, twos complement, Gray code)**  
**Clock duty cycle stabilizer**  
**Integrated data capture clock**

### GENERAL DESCRIPTION

The AD9601 is a 10-bit monolithic sampling analog-to-digital converter optimized for high performance, low power, and ease of use. The product operates at up to a 250 MSPS conversion rate and is optimized for outstanding dynamic performance in wideband carrier and broadband systems. All necessary functions, including a track-and-hold (T/H) and voltage reference, are included on the chip to provide a complete signal conversion solution.

The ADC requires a 1.8 V analog voltage supply and a differential clock for full performance operation. The digital outputs are CMOS compatible and support either twos complement, offset binary format, or Gray code. A data clock output is available for proper output data timing.

Fabricated on an advanced CMOS process, the AD9601 is available in a 56-lead LFCSP, specified over the industrial temperature range (-40°C to +85°C).

#### Rev. 0

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### APPLICATIONS

**Wireless and wired broadband communications**  
**Cable reverse path**  
**Communications test equipment**  
**Radar and satellite subsystems**  
**Power amplifier linearization**

### FUNCTIONAL BLOCK DIAGRAM

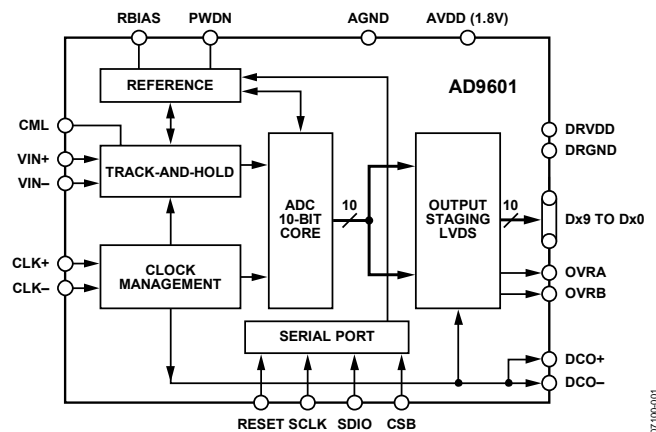


Figure 1.

### PRODUCT HIGHLIGHTS

1. High Performance—Maintains 59.4 dBFS SNR @ 250 MSPS with a 70 MHz input.
2. Low Power—Consumes only 322 mW @ 250 MSPS.
3. Ease of Use—CMOS output data and output clock signal allow interface to current FPGA technology. The on-chip reference and sample-and-hold provide flexibility in system design. Use of a single 1.8 V supply simplifies system power supply design.
4. Serial Port Control—Standard serial port interface supports various product functions, such as data formatting, power-down, gain adjust, and output test pattern generation.
5. Pin-Compatible Family—12-bit pin-compatible family offered as the AD9626.

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## REVISION HISTORY

11/07—Revision 0: Initial Version

## SPECIFICATIONS

### DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T<sub>MIN</sub> = -40°C, T<sub>MAX</sub> = +85°C, f<sub>IN</sub> = -1.0 dBFS, full scale = 1.25 V, single port output mode, DCS enabled, unless otherwise noted.

Table 1.

Parameter <sup>1</sup>	Temp	AD9601-200			AD9601-250			Unit
		Min	Typ	Max	Min	Typ	Max	
RESOLUTION		10			10			Bits
ACCURACY		Guaranteed			Guaranteed			
No Missing Codes	Full	Guaranteed			Guaranteed			
Offset Error	25°C	4.0			4.0			mV
Gain Error	Full	-12		+12	-12		+12	mV
	25°C	1.4			1.4			% FS
Differential Nonlinearity (DNL)	Full	-2.1		+4.5	-2.1		+4.5	% FS
	25°C	0.2			0.2			LSB
Integral Nonlinearity (INL)	Full	-0.5		+0.5	-0.5		+0.5	LSB
	25°C	0.2			0.2			LSB
	Full	-0.5		+0.5	-0.5		+0.5	LSB
TEMPERATURE DRIFT								
Offset Error	Full	8			8			μV/°C
Gain Error	Full	0.021			0.021			%/°C
ANALOG INPUTS (VIN+, VIN-)								
Differential Input Voltage Range <sup>2</sup>	Full	0.98	1.25	1.5	0.98	1.25	1.5	V p-p
Input Common-Mode Voltage	Full	1.4			1.4			V
Input Resistance (Differential)	Full	4.3			4.3			kΩ
Input Capacitance	25°C	2			2			pF
POWER SUPPLY								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Currents								
I <sub>AVDD</sub> <sup>3</sup>	Full	133		142	157		167	mA
I <sub>DRVDD</sub> <sup>3</sup> /Single Port Mode <sup>4</sup>	Full	19		20	22		24	mA
I <sub>DRVDD</sub> <sup>3</sup> /Interleaved Mode <sup>5</sup>	Full	16			18			mA
Power Dissipation <sup>3</sup>	Full							mW
Single Port Mode <sup>4</sup>	Full	274		291	322		344	mW
Interleaved Mode <sup>5</sup>	Full	268			315			mW
Power-Down Mode Supply Currents								
I <sub>AVDD</sub>	Full	40			40			μA
I <sub>DRVDD</sub>	Full	170			170		22	μA
Standby Mode Supply Currents								
I <sub>AVDD</sub>	Full	19			19			mA
I <sub>DRVDD</sub>	Full	170			170		22	μA

<sup>1</sup> See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

<sup>2</sup> The input range is programmable through the SPI, and the range specified reflects the nominal values of each setting. See the Memory Map section.

<sup>3</sup> I<sub>AVDD</sub> and I<sub>DRVDD</sub> are measured with a -1 dBFS, 10.3 MHz sine input at rated sample rate.

<sup>4</sup> Single data rate mode; this is the default mode of the AD9601.

<sup>5</sup> Interleaved mode; user-programmable feature. See the Memory Map section.

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## AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T<sub>MIN</sub> = -40°C, T<sub>MAX</sub> = +85°C, f<sub>IN</sub> = -1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted. <sup>1</sup>

Table 2.

Parameter <sup>2</sup>	Temp	AD9601-200			AD9601-250			Unit
		Min	Typ	Max	Min	Typ	Max	
SNR								
f <sub>IN</sub> = 10 MHz	25°C		59.5			59.4		dB
	Full			58.5				dB
f <sub>IN</sub> = 70 MHz	25°C		59.3			59.4		dB
SINAD								
f <sub>IN</sub> = 10 MHz	25°C		59.5			59.4		dB
	Full			58.5				dB
f <sub>IN</sub> = 70 MHz	25°C		59.3			59.4		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f <sub>IN</sub> = 10 MHz	25°C		9.6			9.7		Bits
f <sub>IN</sub> = 70 MHz	25°C		9.6			9.7		Bits
WORST HARMONIC (SECOND OR THIRD)								
f <sub>IN</sub> = 10 MHz	25°C		84			84		dBc
	Full			77				dBc
f <sub>IN</sub> = 70 MHz	25°C		78			81		dBc
WORST OTHER (SFDR EXCLUDING SECOND AND THIRD)								
f <sub>IN</sub> = 10 MHz	25°C		88			86		dBc
	Full			80				dBc
f <sub>IN</sub> = 70 MHz	25°C		87			85		dBc
TWO-TONE IMD								
170.2 MHz/171.3 MHz @ -7 dBFS	25°C		81			81		dBFS
ANALOG INPUT BANDWIDTH	25°C		700			700		MHz

<sup>1</sup> All ac specifications tested by driving CLK+ and CLK- differentially.

<sup>2</sup> See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

**DIGITAL SPECIFICATIONS**

AVDD = 1.8 V, DRVDD = 1.8 V, T<sub>MIN</sub> = -40°C, T<sub>MAX</sub> = +85°C, f<sub>IN</sub> = -1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

**Table 3.**

Parameter <sup>1</sup>	Temp	AD9601-200			AD9601-250			Unit
		Min	Typ	Max	Min	Typ	Max	
<b>CLOCK INPUTS</b>								
Logic Compliance	Full	CMOS/LVDS/LVPECL			CMOS/LVDS/LVPECL			
Internal Common-Mode Bias	Full	1.2			1.2			V
Differential Input Voltage	Full	0.2		6	0.2		6	V p-p
Input Voltage Range	Full	AVDD - 0.3		AVDD + 1.6	AVDD - 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	1.1		AVDD	V
High Level Input Voltage (V <sub>IH</sub> )	Full	1.2		3.6	1.2		3.6	V
Low Level Input Voltage (V <sub>IL</sub> )	Full	0		0.8	0		0.8	V
Input Resistance (Differential)	Full	16	20	24	16	20	24	kΩ
Input Capacitance	Full	4			4			pF
<b>LOGIC INPUTS</b>								
Logic 1 Voltage	Full	0.8 × VDD			0.8 × VDD			V
Logic 0 Voltage	Full				0.2 × AVDD			V
Logic 1 Input Current (SDIO)	Full	0			0			μA
Logic 0 Input Current (SDIO)	Full	-60			-60			μA
Logic 1 Input Current (SCLK, PDWN, CSB, RESET)	Full	55			50			μA
Logic 0 Input Current (SCLK, PDWN, CSB, RESET)	Full	0			0			μA
Input Capacitance	25°C	4			4			pF
<b>LOGIC OUTPUTS</b>								
High Level Output Voltage	Full	DRVDD - 0.05			DRVDD - 0.05			V
Low Level Output Voltage	Full	GND + 0.05			GND + 0.05			V
Output Coding		Twos complement, Gray code, or offset binary (default)						

<sup>1</sup> See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.

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## SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, T<sub>MIN</sub> = -40°C, T<sub>MAX</sub> = +85°C, f<sub>IN</sub> = -1.0 dBFS, full scale = 1.25 V, DCS enabled, unless otherwise noted.

Table 4.

Parameter (Conditions)	Temp	AD9601-200			AD9601-250			Unit
		Min	Typ	Max	Min	Typ	Max	
Maximum Conversion Rate	Full	200			250			MSPS
Minimum Conversion Rate	Full			40			40	MSPS
CLK+ Pulse Width High (t <sub>CH</sub> )	Full	2.15	2.4		1.8	2.0		ns
CLK+ Pulse Width Low (t <sub>CL</sub> )	Full	2.15	2.4		1.8	2.0		ns
Output, Single Data Port Mode <sup>1</sup>								
Data Propagation Delay (t <sub>PD</sub> )	25°C		3.7			3.7		ns
DCO Propagation Delay (t <sub>CPD</sub> )	25°C		3.4			3.4		ns
Data to DCO Skew (t <sub>SKEW</sub> )	Full	0	0.3	0.55	0	0.3	0.55	ns
Latency	Full		6			6		Cycles
Output, Interleaved Mode <sup>2</sup>								
Data Propagation Delay (t <sub>PDA</sub> , t <sub>PDB</sub> )	25°C		3.5			3.5		ns
DCO Propagation Delay (t <sub>CPDA</sub> , t <sub>CPDB</sub> )	25°C		3.0			3.0		ns
Data to DCO Skew (t <sub>SKEWA</sub> , t <sub>SKEWB</sub> )	Full	0	0.5	1.1	0	0.5	1.1	ns
Latency	Full		6			6		Cycles
Standby Recovery	25°C		250			250		ns
Power-Down Recovery			50			50		μs
Aperture Delay (t <sub>A</sub> )	25°C		0.1			0.1		ns
Aperture Uncertainty (Jitter, t <sub>j</sub> )	25°C		0.2			0.2		ps rms

<sup>1</sup> See Figure 2.

<sup>2</sup> See Figure 3.

TIMING DIAGRAMS

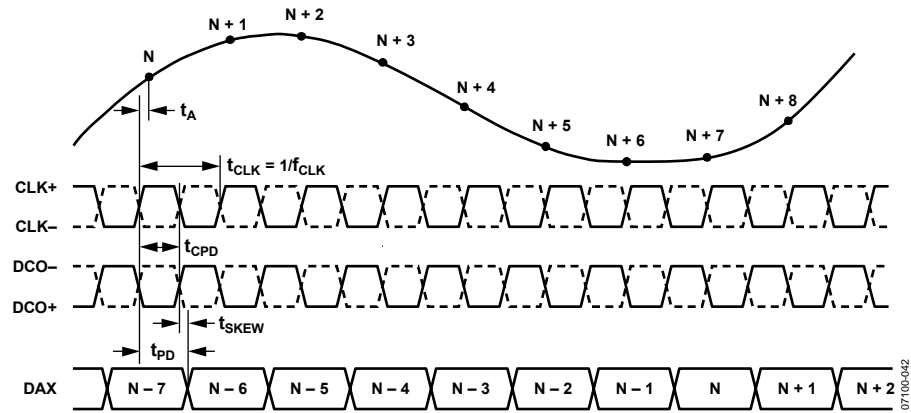


Figure 2. Single Port Mode

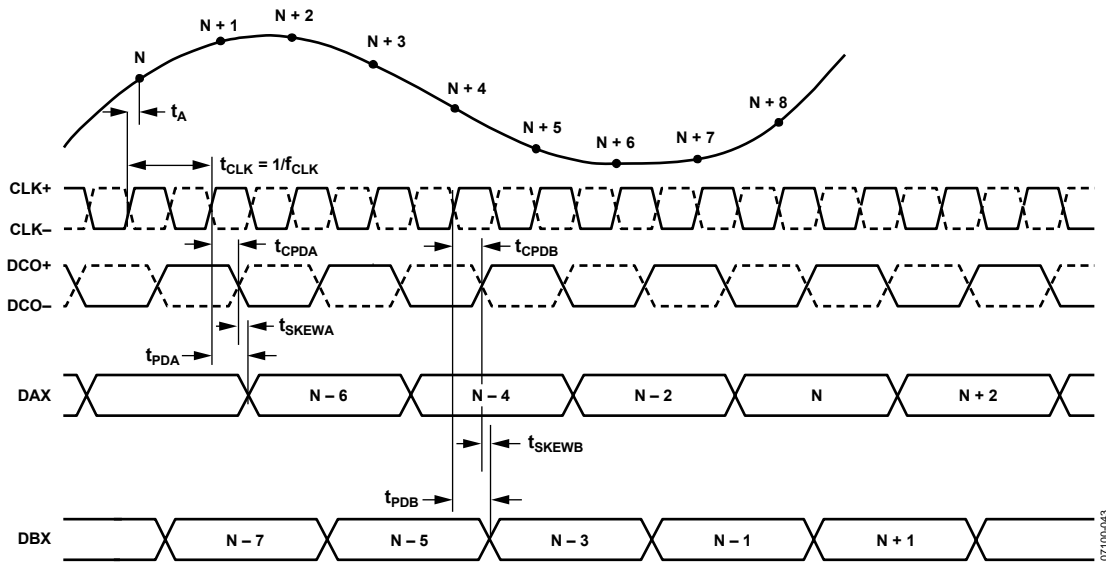


Figure 3. Interleaved Mode

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +2.0 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−2.0 V to +2.0 V
Dx0 Through Dx9 to DRGND	−0.3 V to DRVDD + 0.3 V
DCO+/DCO− to DRGND	−0.3 V to DRVDD + 0.3 V
OVRA/OVRB to DGND	−0.3 V to DRVDD + 0.3 V
CLK+ to AGND	−0.3 V to +3.6 V
CLK− to AGND	−0.3 V to +3.6 V
VIN+ to AGND	−0.3 V to AVDD + 0.2 V
VIN− to AGND	−0.3 V to AVDD + 0.2 V
SDIO/DCS to DGND	−0.3 V to DRVDD + 0.3 V
PDWN to AGND	−0.3 V to +3.6 V
CSB to AGND	−0.3 V to +3.6 V
SCLK/DFS to AGND	−0.3 V to +3.6 V
ENVIRONMENTAL	
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 6.

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
56-Lead LFCSP (CP-56-2)	30.4	2.9	°C/W

Typical  $\theta_{JA}$  and  $\theta_{JC}$  are specified for a 4-layer board in still air. Airflow increases heat dissipation, effectively reducing  $\theta_{JA}$ . In addition, metal in direct contact with the package leads from metal traces, and through holes, ground, and power planes reduces the  $\theta_{JA}$ .

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

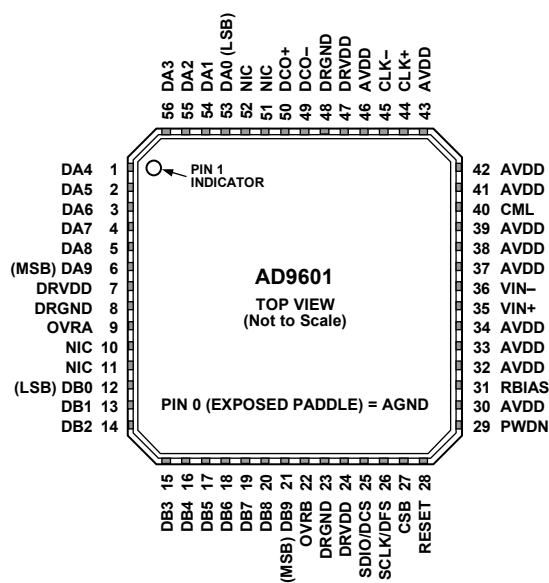


Figure 4. Pin Configuration

Table 7. Single Data Rate Mode Pin Function Descriptions

Pin No.	Mnemonic	Description
30, 32, 33, 34, 37, 38, 39, 41, 42, 43, 46	AVDD	1.8 V Analog Supply.
7, 24, 47	DRVDD	1.8 V Digital Output Supply.
0	AGND <sup>1</sup>	Analog Ground.
8, 23, 48	DRGND <sup>1</sup>	Digital Output Ground.
35	VIN+	Analog Input—True.
36	VIN–	Analog Input—Complement.
40	CML	Common-Mode Output Pin. Enabled through the SPI, this pin provides a reference for the optimized internal bias voltage for VIN+/VIN–.
44	CLK+	Clock Input—True.
45	CLK–	Clock Input—Complement.
31	RBIAS	Set Pin for Chip Bias Current. (Place 1% 10 kΩ resistor terminated to ground.) Nominally 0.5 V.
28	RESET	CMOS-Compatible Chip Reset (Active Low).
25	SDIO/DCS	Serial Port Interface (SPI) Data Input/Output (Serial Port Mode); Duty Cycle Stabilizer Select (External Pin Mode).
26	SCLK/DFS	Serial Port Interface Clock (Serial Port Mode); Data Format Select Pin (External Pin Mode).
27	CSB	Serial Port Chip Select (Active Low).
29	PWDN	Chip Power-Down.
49	DCO–	Data Clock Output—Complement.
50	DCO+	Data Clock Output—True.
53	DA0 (LSB)	Output Port A Output Bit 0 (LSB).
54	DA1	Output Port A Output Bit 1.
55	DA2	Output Port A Output Bit 2.
56	DA3	Output Port A Output Bit 3.
1	DA4	Output Port A Output Bit 4.
2	DA5	Output Port A Output Bit 5.
3	DA6	Output Port A Output Bit 6.

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Pin No.	Mnemonic	Description
4	DA7	Output Port A Output Bit 7.
5	DA8	Output Port A Output Bit 8.
6	DA9 (MSB)	Output Port A Output Bit 9 (MSB).
10, 11, 51, 52	NIC	Not internally connected.
9	OVRA	Output Port A Overrange Output Bit.
12	DB0 (LSB)	Output Port B Output Bit 0 (LSB).
13	DB1	Output Port B Output Bit 1.
14	DB2	Output Port B Output Bit 2.
15	DB3	Output Port B Output Bit 3.
16	DB4	Output Port B Output Bit 4.
17	DB5	Output Port B Output Bit 5.
18	DB6	Output Port B Output Bit 6.
19	DB7	Output Port B Output Bit 7.
20	DB8	Output Port B Output Bit 8.
21	DB9 (MSB)	Output Port B Output Bit 9 (MSB).
22	OVRA	Output Port B Overrange Output Bit.

<sup>1</sup> AGND and DRGND should be tied to a common quiet ground plane.

# EQUIVALENT CIRCUITS

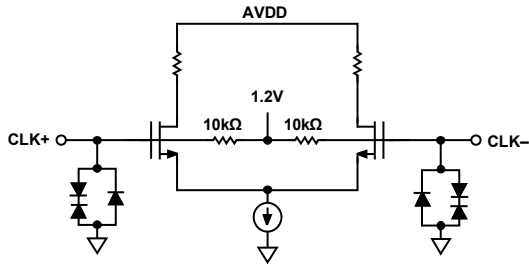


Figure 5. Clock Inputs

07100-003

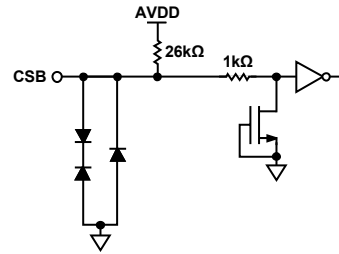


Figure 8. Equivalent CSB Input Circuit

07100-006

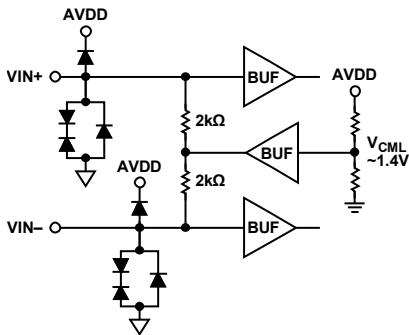


Figure 6. Analog Inputs ( $V_{CML} \approx 1.4V$ )

07100-004

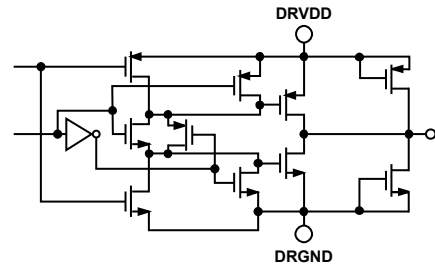


Figure 9. CMOS Outputs (Dx, OVRA, OVRB, DCO+, DCO-)

07100-044

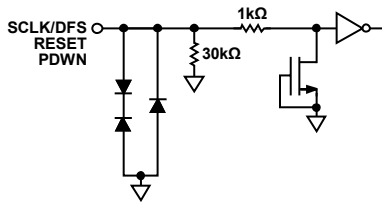


Figure 7. Equivalent SCLK/DFS, RESET, PDWN Input Circuit

07100-005

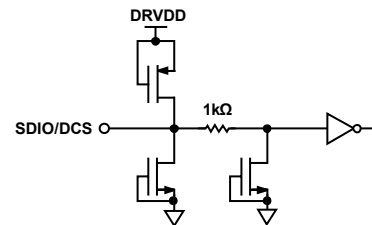


Figure 10. Equivalent SDIO/DCS Input Circuit

07100-007

## TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, rated sample rate, DCS enabled,  $T_A = 25^\circ\text{C}$ , 1.25 V p-p differential input, AIN = -1 dBFS, unless otherwise noted.

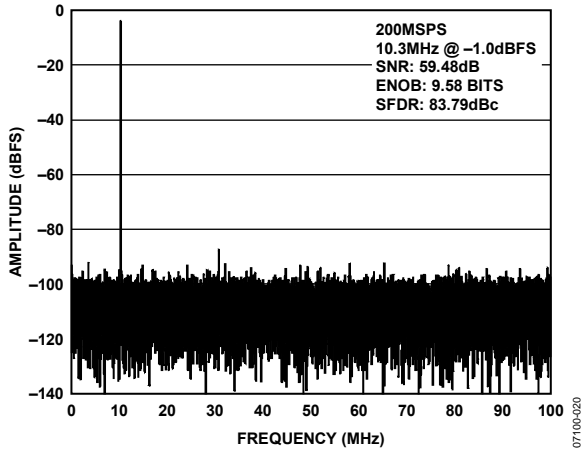


Figure 11. AD9601-200 64k Point Single-Tone FFT; 200 MSPS, 10.3 MHz

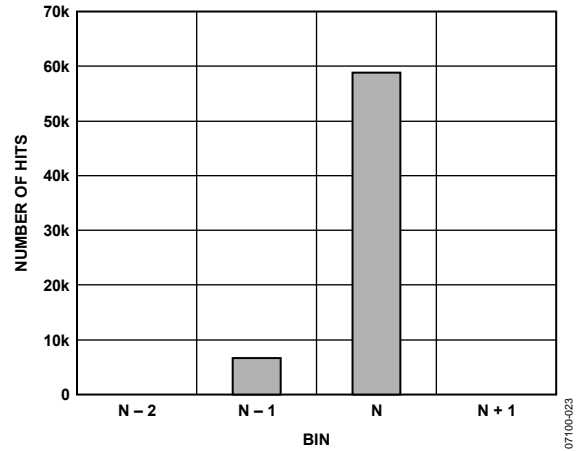


Figure 14. AD9601-200 Grounded Input Histogram; 200 MSPS

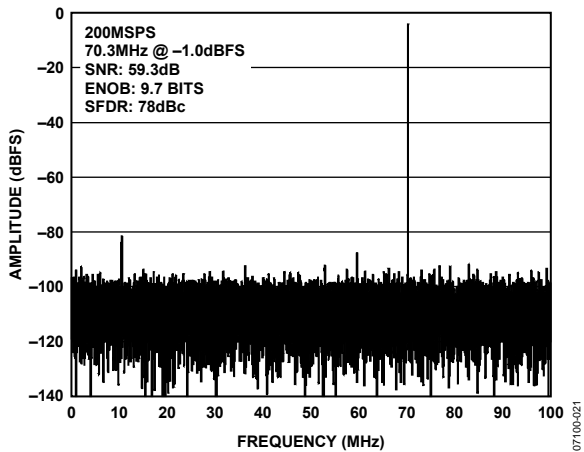


Figure 12. AD9601-200 64k Point Single-Tone FFT; 200 MSPS, 70.3 MHz

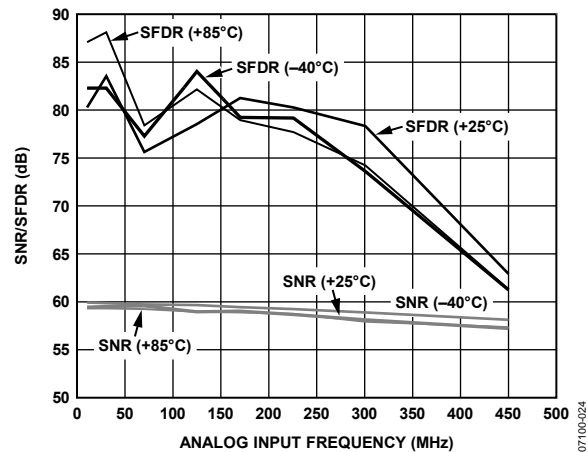


Figure 15. AD9601-200 Single-Tone SNR/SFDR vs. Input Frequency ( $f_{in}$ ) and Temperature with 1.25 V p-p Full Scale; 200 MSPS

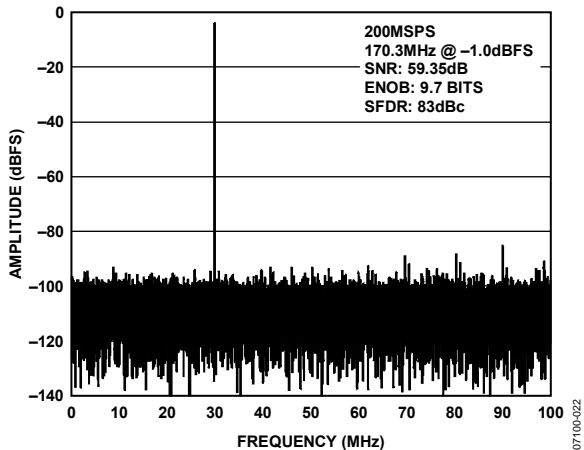


Figure 13. AD9601-200 64k Point Single-Tone FFT; 200 MSPS, 170.3 MHz

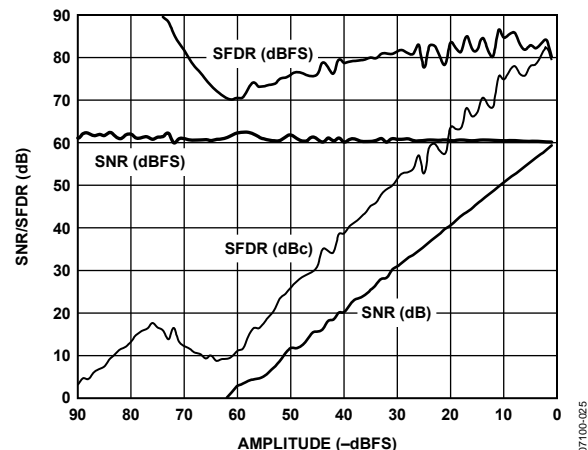


Figure 16. AD9601-200 SNR/SFDR vs. Input Amplitude; 170.3 MHz

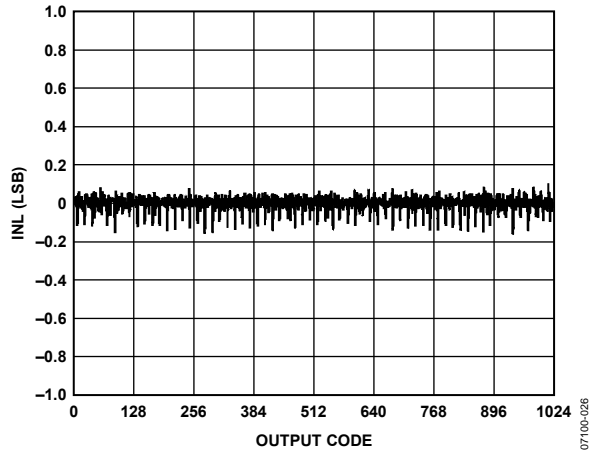


Figure 17. AD9601-200 INL; 200 MSPS

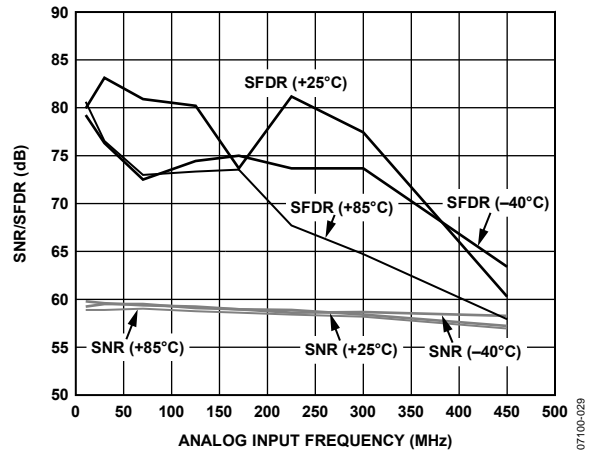


Figure 20. SNR/SFDR vs. Analog Input Frequency, Interleaved Mode vs. Temperature

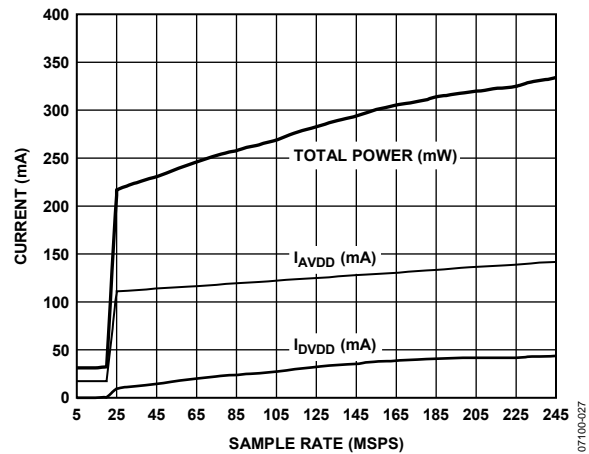


Figure 18. AD9601-200 Power Supply Current vs. Sample Rate

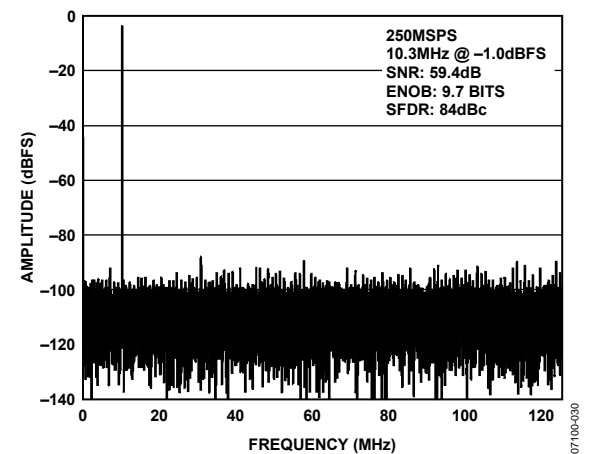


Figure 21. AD9601-250 64k Point Single-Tone FFT; 250 MSPS, 10.3 MHz

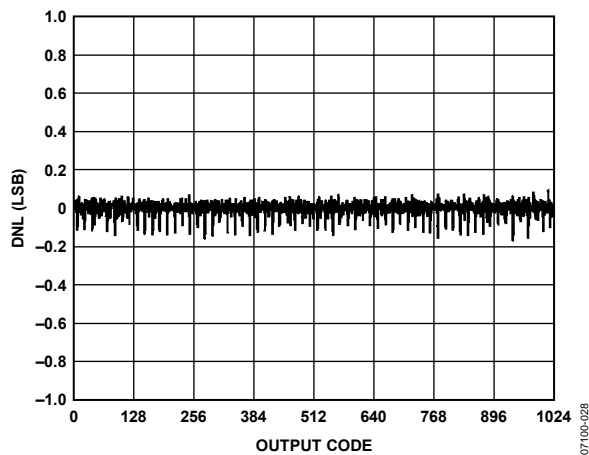


Figure 19. AD9601-200 DNL; 200 MSPS

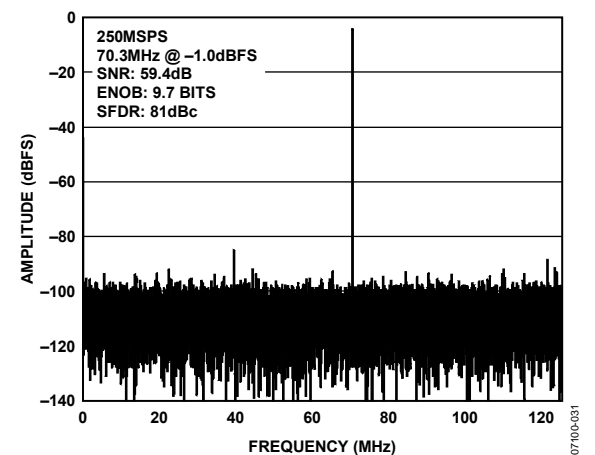


Figure 22. AD9601-250 64k Point Single-Tone FFT; 250 MSPS, 70.3 MHz

# AD9601

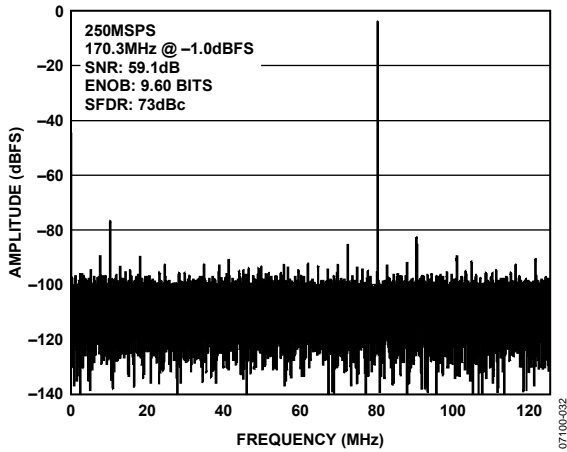


Figure 23. AD9601-250 64k Point Single-Tone FFT; 250 MSPS, 170.3 MHz

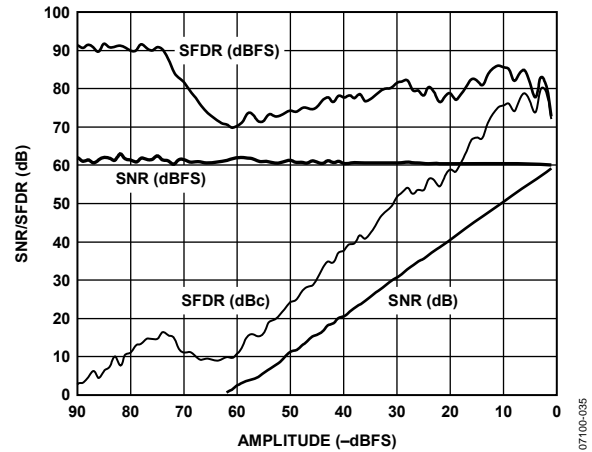


Figure 26. AD9601-250 SNR/SFDR vs. Input Amplitude; 250 MSPS, 170.3 MHz

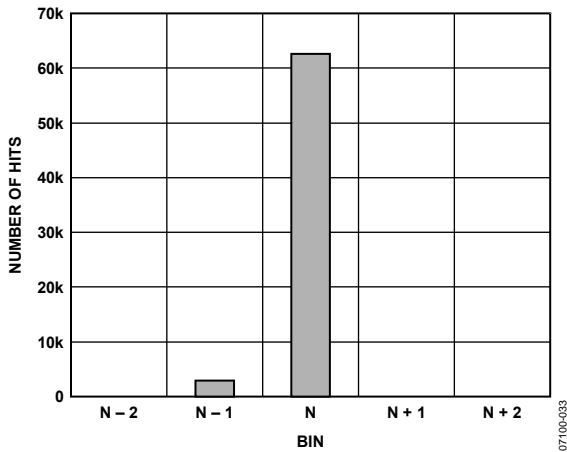


Figure 24. AD9601-250 Grounded Input Histogram; 250 MSPS

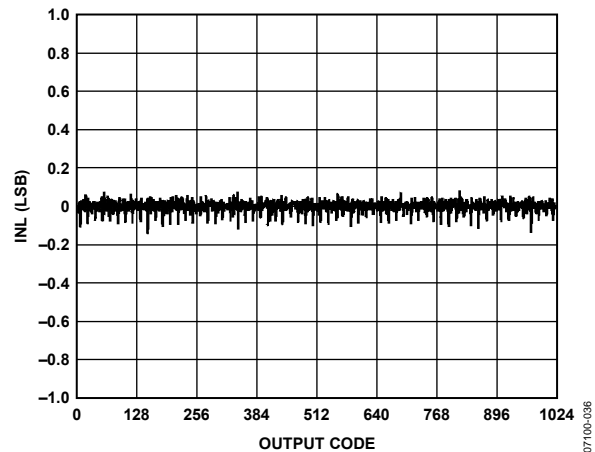


Figure 27. AD9601-250 DNL; 250 MSPS

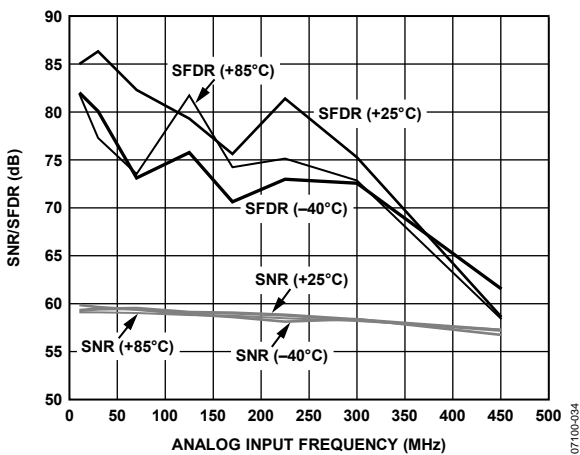


Figure 25. AD9601-250 Single-Tone SNR/SFDR vs. Input Frequency ( $f_{IN}$ ) and Temperature with 1.25 V p-p Full Scale; 250 MSPS

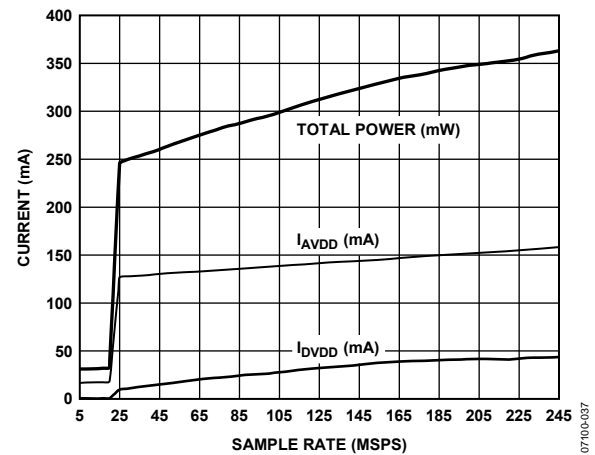


Figure 28. AD9601 Power Supply Current vs. Sample Rate

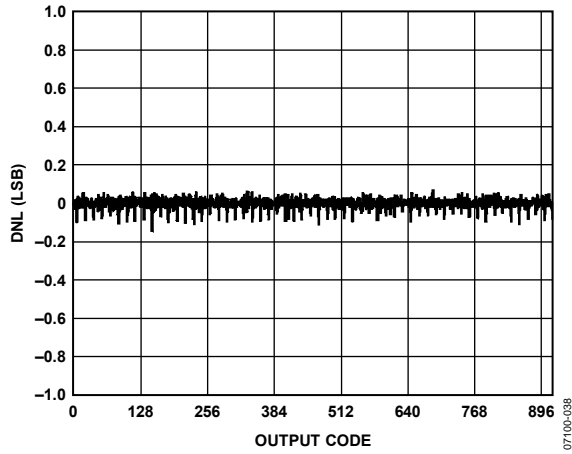


Figure 29. AD9601-250 DNL; 250 MSPS

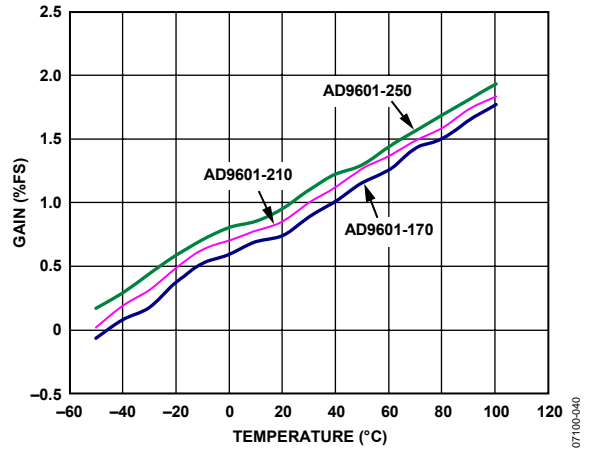


Figure 31. Gain vs. Temperature

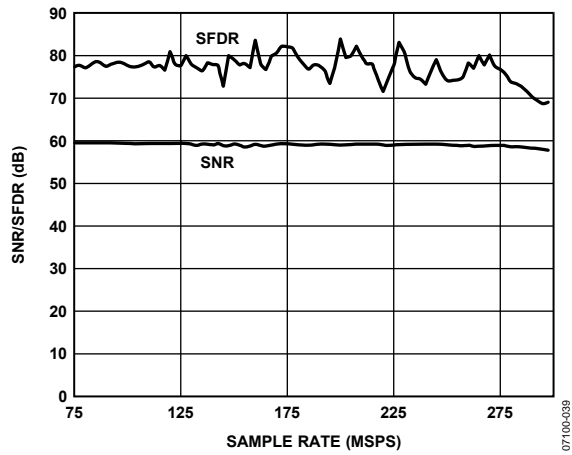


Figure 30. SNR/SFDR vs. Sample Rate; AD9601-250, 170.3 MHz @ -1 dBFS

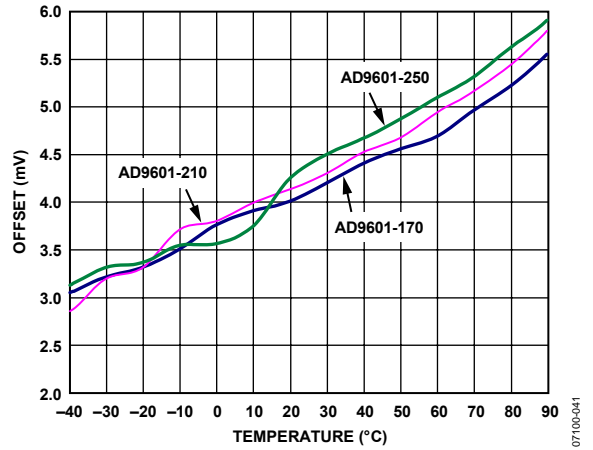


Figure 32. Offset vs. Temperature

## THEORY OF OPERATION

The AD9601 architecture consists of a front-end sample-and-hold amplifier (SHA) followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 10-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

### ANALOG INPUT AND VOLTAGE REFERENCE

The analog input to the AD9601 is a differential buffer. For best dynamic performance, the source impedances driving VIN+ and VIN- should be matched such that common-mode settling errors are symmetrical. The analog input is optimized to provide superior wideband performance and requires that the analog inputs be driven differentially.

A wideband transformer, such as Mini-Circuits® ADT1-1WT, can provide the differential analog inputs for applications that require a single-ended-to-differential conversion. Both analog inputs are self-biased by an on-chip resistor divider to a nominal 1.4 V.

An internal differential voltage reference creates positive and negative reference voltages that define the 1.25 V p-p fixed span of the ADC core. This internal voltage reference can be adjusted by means of SPI control. See the AD9601 Configuration Using the SPI section for more details.

### Differential Input Configurations

Optimum performance is achieved while driving the AD9601 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to  $AVDD/2 + 0.5$  V, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

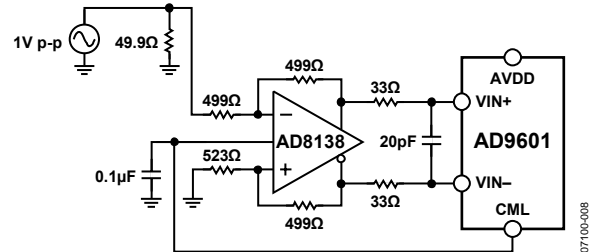


Figure 33. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers may not be adequate to achieve the true performance of the AD9601. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration. The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few millihertz, and excessive signal power can also cause core saturation, which leads to distortion.

In any configuration, the value of the shunt capacitor, C, is dependent on the input frequency and may need to be reduced or removed.

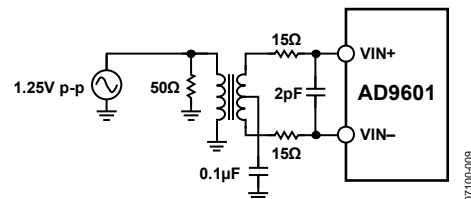


Figure 34. Differential Transformer-Coupled Configuration

As an alternative to using a transformer-coupled input at frequencies in the second Nyquist zone, the AD8352 differential driver can be used (see Figure 35).

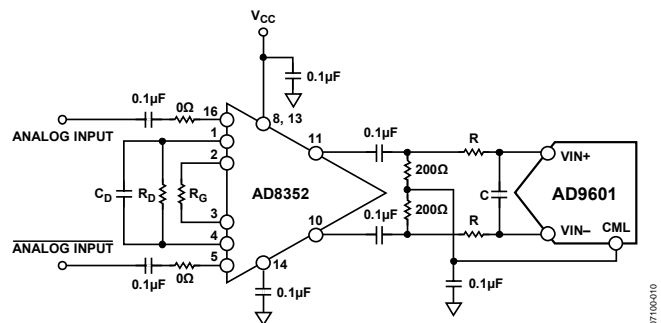


Figure 35. Differential Input Configuration Using the AD8352



**CLOCK INPUT CONSIDERATIONS**

For optimum performance, the AD9601 sample clock inputs (CLK+ and CLK-) should be clocked with a differential signal. This signal is typically ac-coupled into the CLK+ pin and the CLK- pin via a transformer or capacitors. These pins are biased internally and require no additional bias.

Figure 36 shows one preferred method for clocking the AD9601. The low jitter clock source is converted from single-ended to differential using an RF transformer. The back-to-back Schottky diodes across the secondary transformer limit clock excursions into the AD9601 to approximately 0.8 V p-p differential. This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9601 and preserves the fast rise and fall times of the signal, which are critical to low jitter performance.

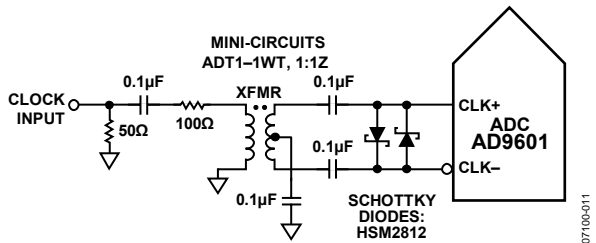
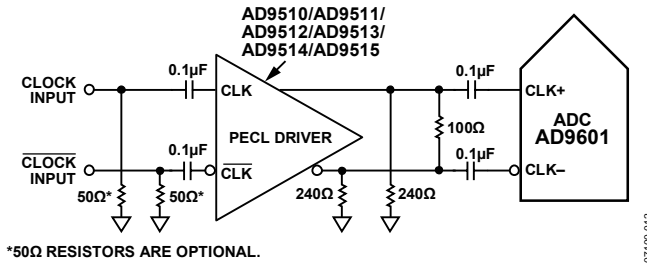


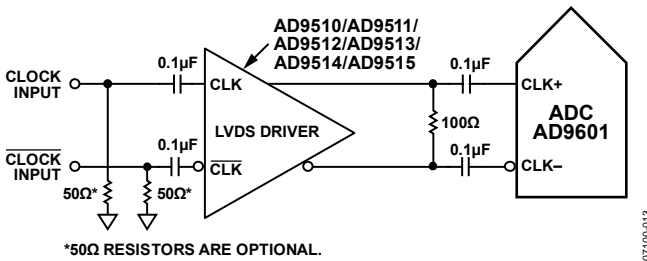
Figure 36. Transformer-Coupled Differential Clock

If a low jitter clock is available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 37. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515 family of clock drivers offers excellent jitter performance.



\*50Ω RESISTORS ARE OPTIONAL.

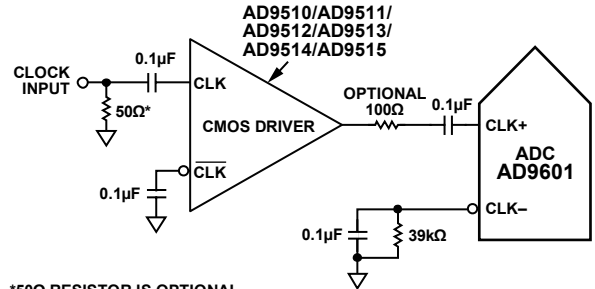
Figure 37. Differential PECL Sample Clock



\*50Ω RESISTORS ARE OPTIONAL.

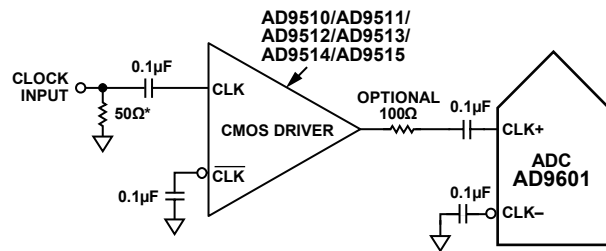
Figure 38. Differential LVDS Sample Clock

In some applications, it is acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, and the CLK- pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 39). Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.3 V, making the selection of the drive logic voltage very flexible.



\*50Ω RESISTOR IS OPTIONAL.

Figure 39. Single-Ended 1.8 V CMOS Sample Clock



\*50Ω RESISTOR IS OPTIONAL.

Figure 40. Single-Ended 3.3 V CMOS Sample Clock

**Clock Duty Cycle Considerations**

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals. As a result, these ADCs may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9601 contains a duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9601. When the DCS is on, noise and distortion performance are nearly flat for a wide range of duty cycles. However, some applications may require the DCS function to be off. If so, keep in mind that the dynamic range performance can be affected when operated in this mode. See the AD9601 Configuration Using the SPI section for more details on using this feature.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately eight clock cycles to allow the DLL to acquire and lock to the new rate.

## Clock Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR for a full-scale input signal at a given input frequency ( $f_A$ ) due only to aperture jitter ( $t_j$ ) can be calculated by

$$SNR \text{ Degradation} = 20 \times \log_{10}[1/2 \times \pi \times f_A \times t_j]$$

In this equation, the rms aperture jitter represents the root mean square of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter (see Figure 41).

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9601. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note for more in-depth information about jitter performance as it relates to ADCs (visit [www.analog.com](http://www.analog.com)).

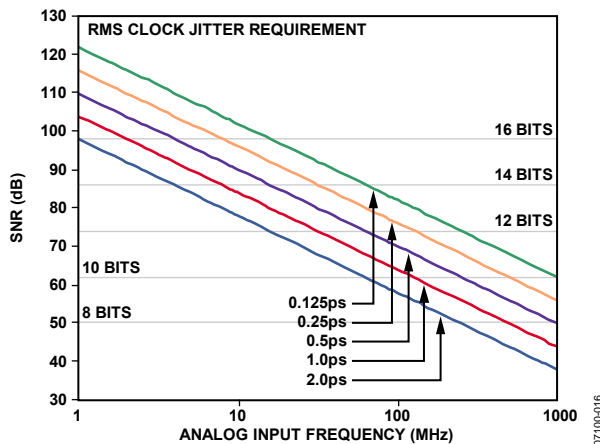


Figure 41. Ideal SNR vs. Input Frequency and Jitter for 0 dBFS Input Signal

## POWER DISSIPATION AND POWER-DOWN MODE

As shown in Figure 28, the power dissipated by the AD9601 is proportional to its sample rate. The digital power dissipation does not vary much because it is determined primarily by the DRVDD supply and bias current of the LVDS output drivers.

By asserting PDWN (Pin 29) high, the AD9601 is placed in standby mode or full power-down mode, as determined by the contents of Serial Port Register 08. Reasserting the PDWN pin low returns the AD9601 into its normal operational mode.

An additional standby mode is supported by means of varying the clock input. When the clock rate falls below 20 MHz, the AD9601 assumes a standby state. In this case, the biasing network

and internal reference remain on, but digital circuitry is powered down. Upon reactivating the clock, the AD9601 resumes normal operation after allowing for the pipeline latency.

## DIGITAL OUTPUTS

### Digital Outputs and Timing

The off-chip drivers on the AD9601 are CMOS-compatible output levels. The outputs are biased from a separate supply (DRVDD), allowing isolation from the analog supply and easy interface to external logic. The outputs are CMOS devices that swing from ground to DRVDD (with no dc load). It is recommended to minimize the capacitive load the ADC drives by keeping the output traces short (<1 inch, for a total  $C_{LOAD} < 5$  pF). When operating in CMOS mode, it is also recommended to place low value (20  $\Omega$ ) series damping resistors on the data lines to reduce switching transient effects on performance.

The format of the output data is offset binary by default. An example of the output coding format can be found in Table 11. If it is desired to change the output data format to twos complement, see the AD9601 Configuration Using the SPI section.

An output clock signal is provided to assist in capturing data from the AD9601. The DCO+/DCO- signal is used to clock the output data and is equal to the sampling clock (CLK) rate in single port mode, and one-half the clock rate in interleaved output mode. See the timing diagrams shown in Figure 2 and Figure 3 for more information.

### Out-of-Range

An out-of-range condition exists when the analog input voltage is beyond the input range of the ADC. OVRA/OVRB is a digital output that is updated along with the data output corresponding to the particular sampled input voltage. Thus, OVRA/OVRB has the same pipeline latency as the digital data. OVRA/OVRB is low when the analog input voltage is within the analog input range and high when the analog input voltage exceeds the input range, as shown in Figure 42. OVRA/OVRB remains high until the analog input returns to within the input range and another conversion is completed. By logically AND-ing OVRA/OVRB with the MSB and its complement, overrange high or under-range low conditions can be detected.

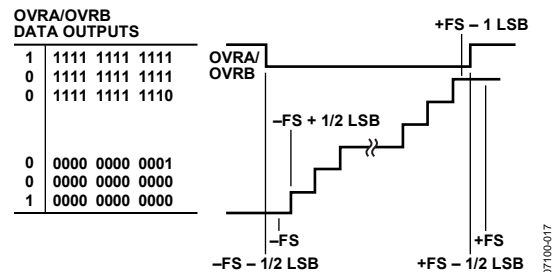


Figure 42. OVRA/OVRB Relation to Input Voltage and Output Data

### TIMING—SINGLE PORT MODE

In single port mode, the CMOS output data is available from Data Port A (DA0 to DA9). The outputs for Port B (DB0 to DB9) are unused, and are high impedance in this mode. The Port A outputs and the differential output data clock (DCO+/DCO-) switch nearly simultaneously during the rising edge of DCO+. In this mode, it is recommended to use the rising edge of DCO- to capture the data from Port A. The setup and hold time depends on the input sample clock period, and is approximately  $1/f_{\text{CLK}} \pm t_{\text{SKEW}}$ .

### TIMING—INTERLEAVED MODE

In interleaved mode, the output data of the AD9601 is demultiplexed onto two data port buses, Port A (DA0 to DA9) and Port B (DB0 to DB9). The output data and differential data capture clock switch at one-half the rate of the sample clock input (CLK+/CLK-), increasing the setup and hold time for the external data capture circuit relative to single port mode (see Figure 3, interleaved mode timing diagram). The two ports switch on alternating sample clock cycles, with the data for Port A being valid during the rising edge of DCO+, and the data for Port B being valid during the rising edge of DCO-. The pipeline latency for both ports is six sample clock cycles. Due to the random nature of the  $\div 2$  circuit that generates the timing for the output stage in interleaved mode, the first data sample during power-up can be assigned to either Data Port A or Port B. The user cannot control the polarity of the output data clock relative to the input sample clock. In this mode, it is recom-

mended to use the rising edge of DCO+ to capture the data from Port A, and the rising edge of DCO- to capture the data from Port B. In both cases, the setup and hold time depends on the input sample clock period, and both are approximately  $2/f_s \pm t_{\text{SKEW}}$ .

### $f_s/2$ Spurious

Because the AD9601 output data rate is at one-half the sampling frequency in interleaved output mode, there is significant  $f_s/2$  energy in the outputs of the part, and there is significant energy in the ADC output spectrum at  $f_s/2$ . Care must be taken to be certain that this  $f_s/2$  energy does not couple into either the clock circuit or the analog inputs of the AD9601. When  $f_s/2$  energy is coupled in this fashion, it appears as a spurious tone reflected around  $f_s/4$ ,  $3f_s/4$ ,  $5f_s/4$ , and so on. For example, in a 125 MSPS sampling application with a 90 MHz single-tone analog input, this energy generates a tone at 97.5 MHz.

$$[(3 \times 125 \text{ MSPS}/4 - 90 \text{ MHz}) + 3 \times 125 \text{ MSPS}/4]$$

Depending on the relationship of the IF frequency to the center of the Nyquist zone, this spurious tone may or may not be in the user's band of interest. Some residual  $f_s/2$  energy is present in the AD9601, and the level of this spur is typically below the level of the harmonics at clock rates. Figure 20 shows a plot of the  $f_s/2$  spur level vs. the analog input frequency for the AD9601-250. For the specifications provided in Table 2, the  $f_s/2$  spur effect is not a factor, as the device is specified in single port output mode.

## LAYOUT CONSIDERATIONS

### POWER AND GROUND RECOMMENDATIONS

When connecting power to the AD9601, it is recommended that two separate supplies be used: one for analog (AVDD, 1.8 V nominal) and one for digital (DRVDD, 1.8 V nominal). If only a single 1.8 V supply is available, it is routed to AVDD first, then tapped off and isolated with a ferrite bead or filter choke with decoupling capacitors preceding connection to DRVDD. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the parts with minimal trace length.

A single PC board ground plane is sufficient when using the AD9601. With proper decoupling and smart partitioning of analog, digital, and clock sections of the PC board, optimum performance is easily achieved.

### Exposed Paddle Thermal Heat Slug Recommendations

It is required that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance of the AD9601. An exposed, continuous copper plane on the PCB should mate to the AD9601 exposed paddle, Pin 0. The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be solder-filled or plugged.

To maximize the coverage and adhesion between the ADC and PCB, partition the continuous plane by overlaying a silkscreen on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and PCB. See Figure 43 for a PCB layout example. For detailed information on packaging and the PCB layout of chip scale packages, see Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package*.

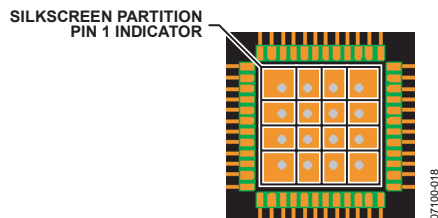


Figure 43. Typical PCB Layout

### CML

The CML pin should be decoupled to ground with a 0.1  $\mu\text{F}$  capacitor, as shown in Figure 45.

### RBIAS

The AD9601 requires the user to place a 10 k $\Omega$  resistor between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

### AD9601 CONFIGURATION USING THE SPI

The AD9601 SPI allows the user to configure the converter for specific functions or operations through a structured register space inside the ADC. This gives the user added flexibility to customize device operation depending on the application. Addresses are accessed (programmed or read back) serially in one-byte words. Each byte can be further divided down into fields, which are documented in the Memory Map section.

There are three pins that define the serial port interface or SPI to this particular ADC. They are the SPI SCLK/DFS, SPI SDIO/DCS, and CSB pins. The SCLK/DFS (serial clock) is used to synchronize the read and write data presented the ADC. The SDIO/DCS (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB is an active low control that enables or disables the read and write cycles (see Table 8).

Table 8. Serial Port Pins

Mnemonic	Function
SCLK	SCLK (Serial Clock) is the serial shift clock in. SCLK is used to synchronize serial interface reads and writes.
SDIO	SDIO (Serial Data Input/Output) is a dual-purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	CSB (Chip Select Bar) is an active low control that gates the read and write cycles.
RESET	Master Device Reset. When asserted, device assumes default settings. Active low.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 44 and Table 10.

During an instruction phase, a 16-bit instruction is transmitted. Data then follows the instruction phase and is determined by the W0 and W1 bits, which is 1 or more bytes of data. All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether this is a read or write command. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

Data can be sent in MSB or in LSB first mode. MSB first is default on power-up and can be changed by changing the configuration register. For more information about this feature and others, see *Interfacing to High Speed ADCs via SPI* at [www.analog.com](http://www.analog.com).

## HARDWARE INTERFACE

The pins described in Table 8 comprise the physical interface between the user's programming device and the serial port of the AD9601. All serial pins are inputs, which is an open-drain output and should be tied to an external pull-up or pull-down resistor (suggested value of 10 k $\Omega$ ).

This interface is flexible enough to be controlled by either PROMS or PIC microcontrollers as well. This provides the user with an alternate method to program the ADC other than a SPI controller.

If the user chooses not to use the SPI interface, some pins serve a dual function and are associated with a specific function when strapped externally to AVDD or ground during device power-on. The Configuration Without the SPI section describes the strappable functions supported on the AD9601.

## CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SPI SDIO/DCS and SPI SCLK/DFS pins can alternately serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer. In this mode, the SPI CSB chip select should be connected to ground, which disables the serial port interface.

**Table 9. Mode Selection**

Mnemonic	External Voltage	Configuration
SPI SDIO/DCS	AVDD	Duty cycle stabilizer enabled
	AGND	Duty cycle stabilizer disabled
SPI SCLK/DFS	AVDD	Twos complement enabled
	AGND	Offset binary enabled

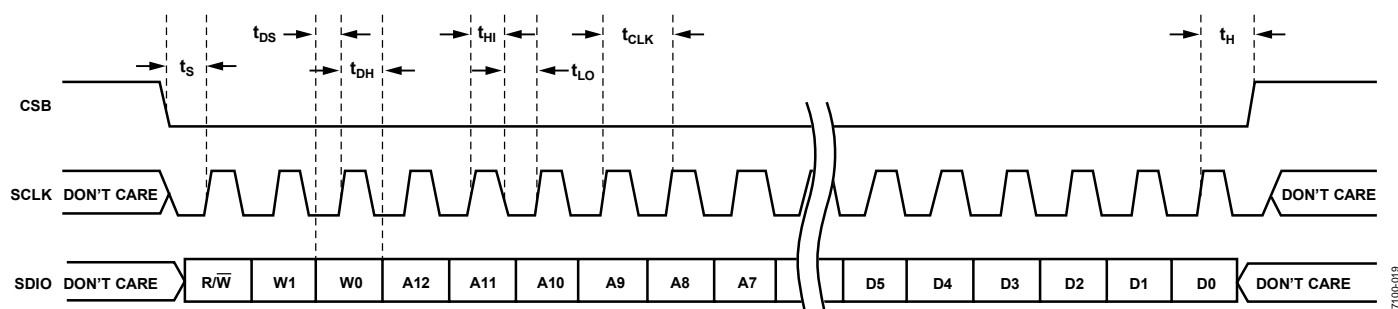


Figure 44. Serial Port Interface Timing Diagram

07100-019

# AD9601

**Table 10. Serial Timing Definitions**

Parameter	Timing (minimum, ns)	Description
t <sub>DS</sub>	5	Setup time between the data and the rising edge of SCLK
t <sub>DH</sub>	2	Hold time between the data and the rising edge of SCLK
t <sub>CLK</sub>	40	Period of the clock
t <sub>S</sub>	5	Setup time between CSB and SCLK
t <sub>H</sub>	2	Hold time between CSB and SCLK
t <sub>HI</sub>	16	Minimum period that SCLK should be in a logic high state
t <sub>LO</sub>	16	Minimum period that SCLK should be in a logic low state
t <sub>EN_SDIO</sub>	1	Minimum time for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in Figure 44)
t <sub>DIS_SDIO</sub>	5	Minimum time for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in Figure 44)

**Table 11. Output Data Format**

Input (V)	Condition (V)	Offset Binary Output Mode D11 to D0	Twos Complement Mode D11 to D0	Gray Code Mode (SPI Accessible) D11 to D0	OR
VIN+ – VIN–	< 0.62	0000 0000 0000	0000 0000 0000	0000 0000 0000	1
VIN+ – VIN–	= 0.62	0000 0000 0000	0000 0000 0000	0000 0000 0000	0
VIN+ – VIN–	= 0	0000 0000 0000	0000 0000 0000	0000 0000 0000	0
VIN+ – VIN–	= 0.62	1111 1111 1111	1111 1111 1111	0000 0000 0000	0
VIN+ – VIN–	> 0.62 + 0.5 LSB	1111 1111 1111	1111 1111 1111	0000 0000 0000	1

## MEMORY MAP

### READING THE MEMORY MAP TABLE

Each row in the memory map table has eight address locations. The memory map is roughly divided into three sections: chip configuration register map (Address 0x00 to Address 0x02), transfer register map (Address 0xFF), and program register map (Address 0x08 to Address 0x2A).

The Addr (Hex) column of the memory map indicates the register address in hexadecimal, and the Default Value (Hex) column shows the default hexadecimal value that is already written into the register. The Bit 7 (MSB) column is the start of the default hexadecimal value given. For example, Hexadecimal Address 0x09, clock, has a hexadecimal default value of 0x01. This means Bit 7 = 0, Bit 6 = 0, Bit 5 = 0, Bit 4 = 0, Bit 3 = 0, Bit 2 = 0, Bit 1 = 0, and Bit 0 = 1, or 0000 0001 in binary. The default value enables the duty cycle stabilizer. Overwriting this default so that Bit 0 = 0 disables the duty cycle stabilizer. For more information on this and other functions, consult the *Interfacing to High Speed ADCs via SPI* user manual at [www.analog.com](http://www.analog.com).

### RESERVED LOCATIONS

Undefined memory locations should not be written to other than their default values suggested in this data sheet. Addresses that have values marked as 0 should be considered reserved and have a 0 written into their registers during power-up.

### DEFAULT VALUES

Coming out of reset, critical registers are preloaded with default values. These values are indicated in Table 12. Other registers do not have default values and retain the previous value when exiting reset.

### LOGIC LEVELS

An explanation of various registers follows: “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.” Similarly, “clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

Table 12. Memory Map Register

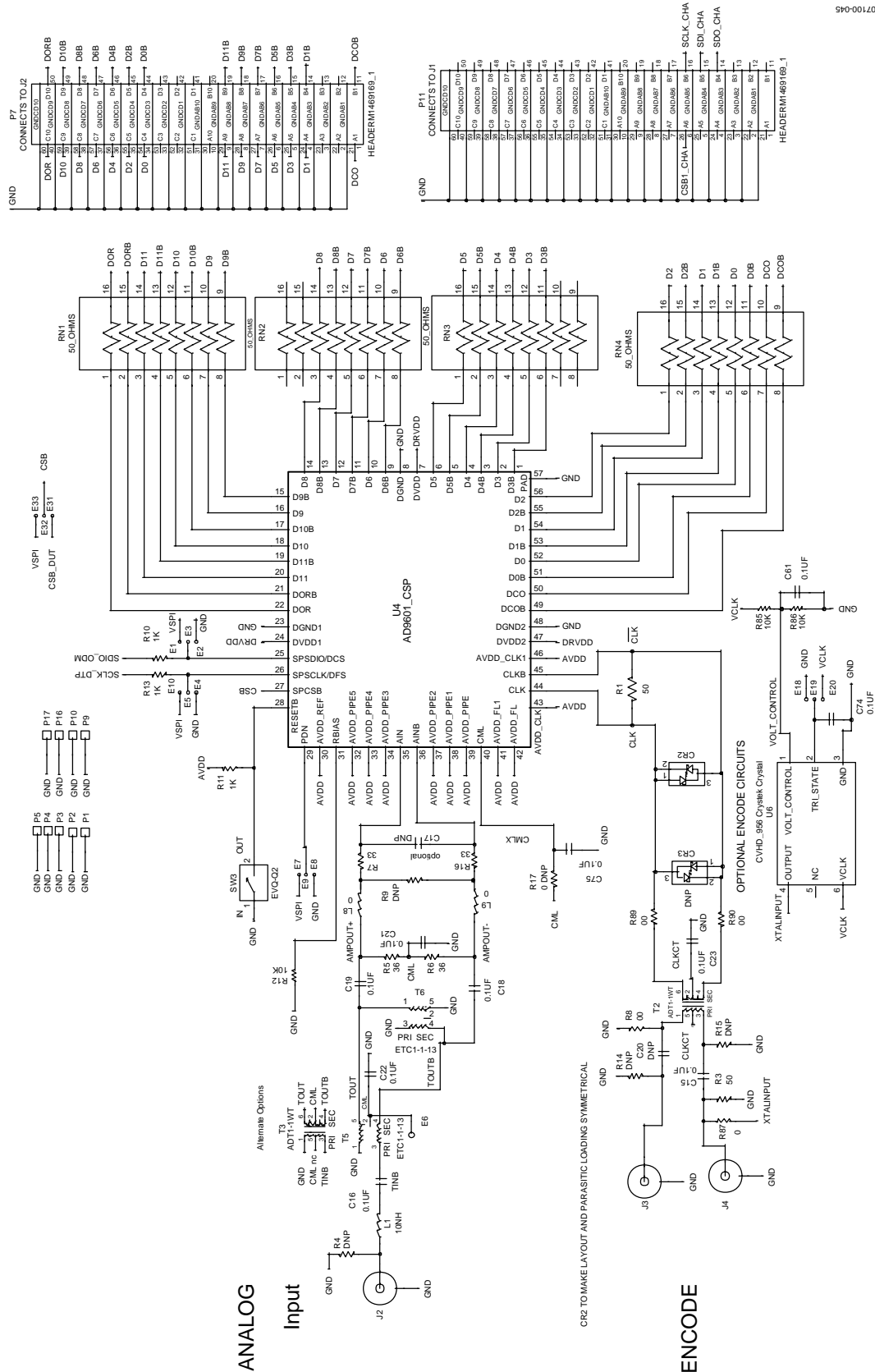
Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/Comments
<b>Chip Configuration Registers</b>											
00	chip_port_config	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	The nibbles should be mirrored by the user so that LSB or MSB first mode registers correctly, regardless of shift mode.
01	chip_id	8-bit chip ID, Bits[7:0] AD9601 = 0x36								Read-only	Default is unique chip ID, different for each device. This is a read-only register.
02	chip_grade	0	0	0	Speed grade: 01 = 200 MSPS 10 = 250 MSPS		X	X	X	Read-only	Child ID used to differentiate graded devices.
<b>Transfer Register</b>											
FF	device_update	0	0	0	0	0	0	0	SW transfer	0x00	Synchronously transfers data from the master shift register to the slave.
<b>ADC Functions</b>											
08	modes	0	0	PDWN: 0 = full (default) 1 = standby	0	0	Internal power-down mode: 000 = normal (power-up, default) 001 = full power-down 010 = standby 011 = normal (power-up) Note: external PDWN pin overrides this setting			0x00	Determines various generic modes of chip operation.

# AD9601

Addr (Hex)	Parameter Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/Comments
09	clock	0	0	0	0	0	0	0	Duty cycle stabilizer: 0 = disabled 1 = enabled (default)	0x01	
0D	test_io			Reset PN23 gen: 1 = on 0 = off (default)	Reset PN9 gen: 1 = on 0 = off (default)		Output test mode: 0000 = off (default) 0001 = midscale short 0010 = +FS short 0011 = -FS short 0100 = checker board output 0101 = PN 23 sequence 0110 = PN 9 0111 = one/zero word toggle 1000 = unused 1001 = unused 1010 = unused 1011 = unused 1100 = unused (Format determined by output_mode)			0x00	When set, the test data is placed on the output pins in place of normal data.
0F	ain_config	0	0	0	0	0	Analog input disable: 1 = on 0 = off (default)	CML enable: 1 = on 0 = off (default)	0	0x00	
14	output_mode	0	0	Interleave output mode: 1 = enabled 0 = disabled (default)	Output enable: 0 = enable (default) 1 = disable	0	Output invert: 1 = on 0 = off (default)	Data format select: 00 = offset binary (default) 01 = twos complement 10 = Gray code		0x00	
16	output_phase	Output clock polarity 1 = inverted 0 = normal (default)		0	0					0x03	
17	flex_output_delay	Output delay enable: 0 = enable 1 = disable					Output clock delay: 00000 = 0.1 ns 00001 = 0.2 ns 00010 = 0.3 ns ... 11101 = 3.0 ns 11110 = 3.1 ns 11111 = 3.2 ns			0x00	
18	flex_vref						Input voltage range setting: 10000 = 0.98 V 10001 = 1.00 V 10010 = 1.02 V 10011 = 1.04 V ... 11111 = 1.23 V 00000 = 1.25 V 00001 = 1.27 V ... 01110 = 1.48 V 01111 = 1.50 V			0x00	



EVALUATION BOARD



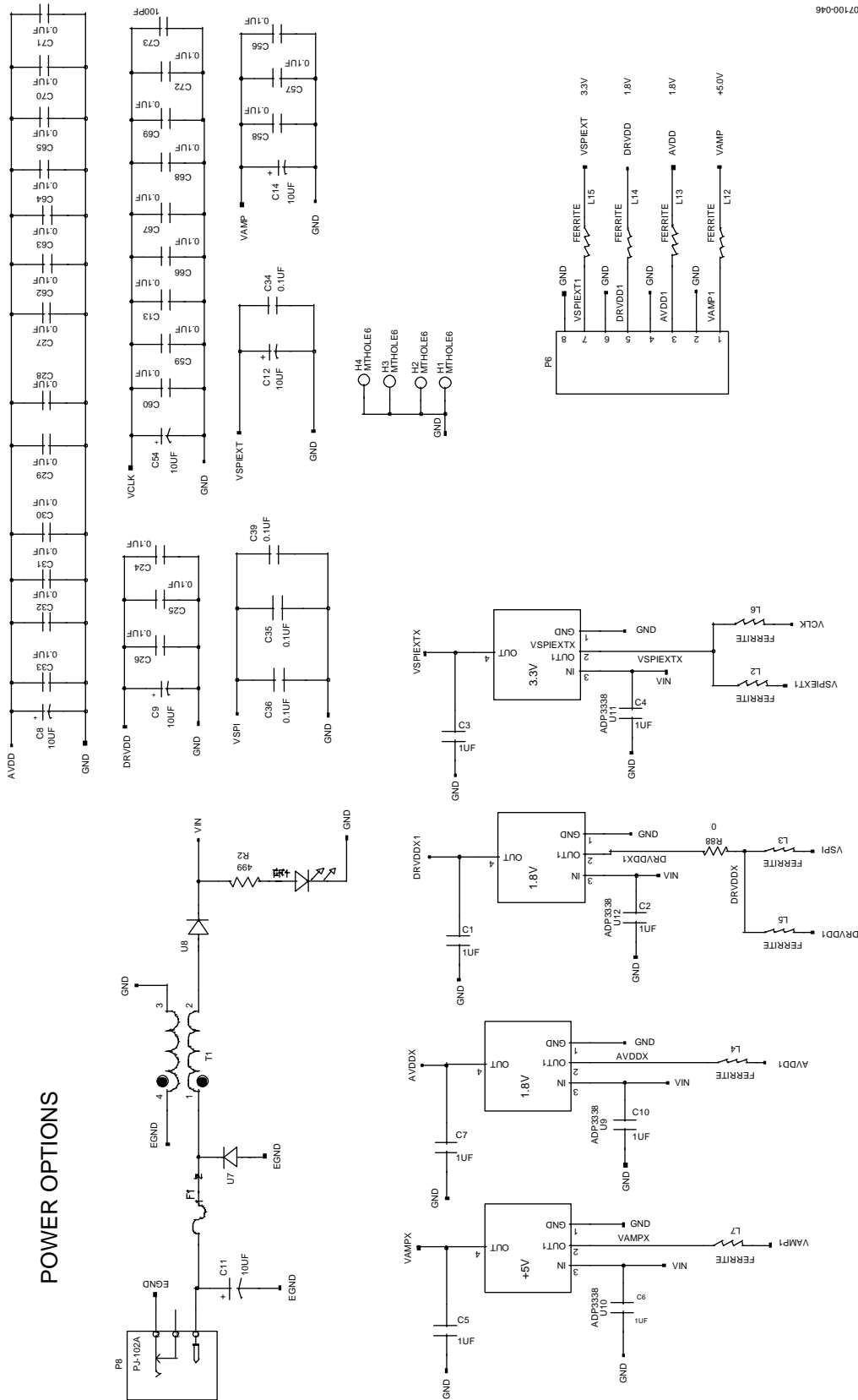


Figure 46. AD9601 Evaluation Board Schematic Page 2

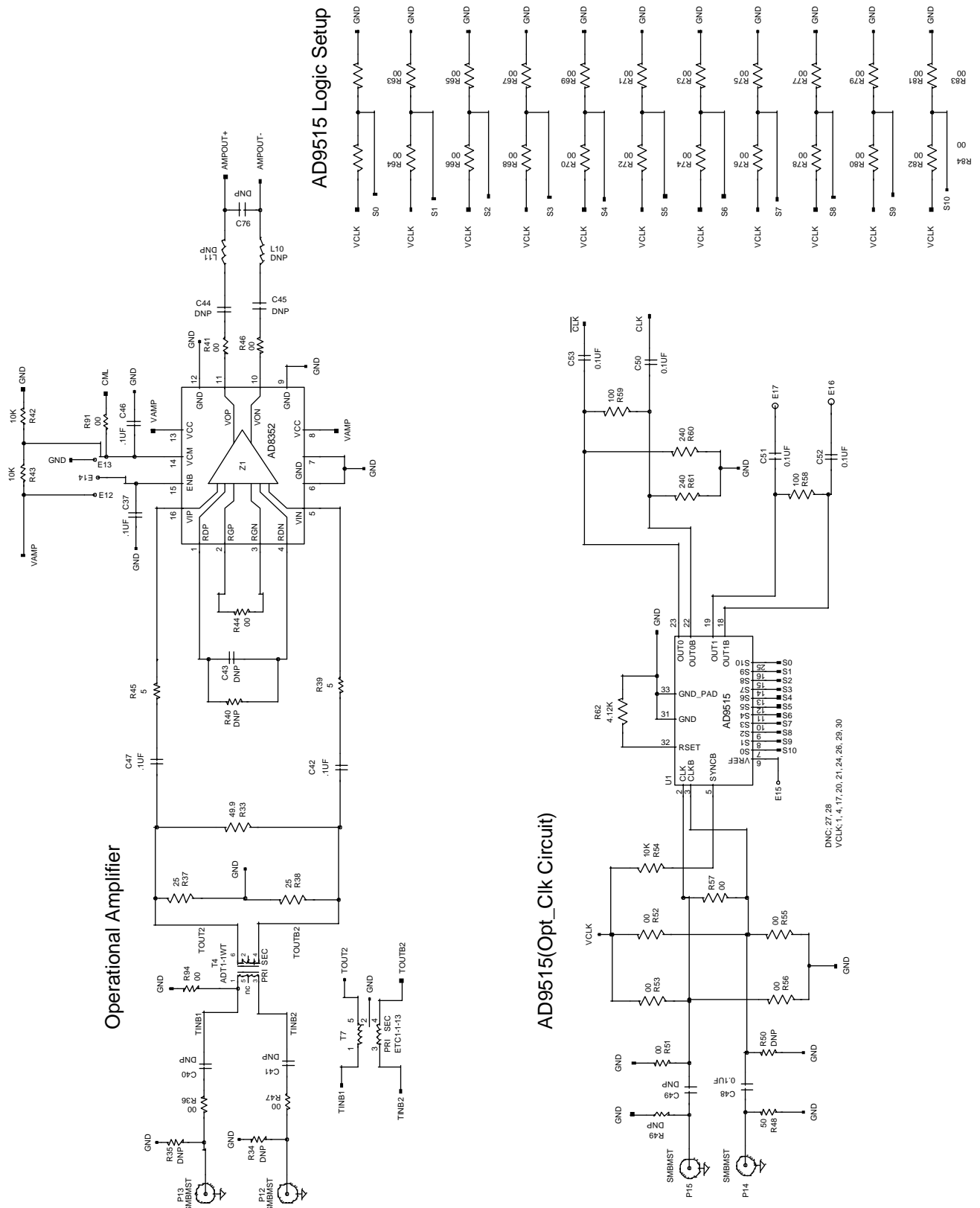


Figure 47. AD9601 Evaluation Board Schematic Page 3

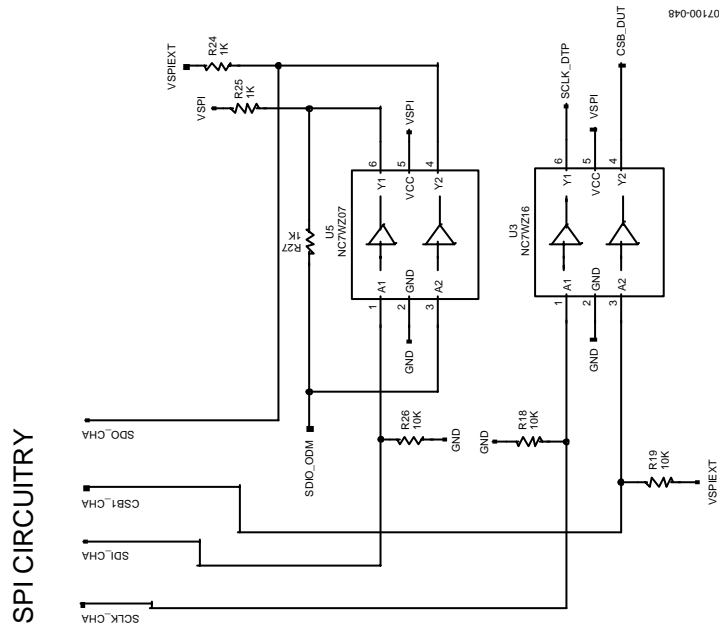


Figure 48. AD9601 Evaluation Board Schematic Page 4

Table 13. Bill of Materials

Qty	Reference Designator	Package	Description	Vendor	Part Number
1		PCB	PCB, AD9230 customer evaluation board, Rev. G	Moog	AD9230revG
7	C1, C3, C4, C5, C6, C7, C10	603	Capacitor, 1 $\mu$ F, 0603, X5R, ceramic, 6.3 V, 10%	Panasonic	ECJ-1VB0J105K
6	C8, C9, C11, C12, C14, C55	6032-28	Capacitor, 10 $\mu$ F, tantalum, 16 V, 10%	Kemet	T491C106K016AS
1	C17	402	Capacitor, 2.0 pF, 50 V, ceramic, 0402, SMD	Murata	GRM1555C1H2R0GZ01D
7	C27, C32, C33, C62, C63, C64, C71	402	Capacitor, 0.33 $\mu$ F, ceramic, X5R, 10 V, 10%	Murata	GRM155R61A334KE15D
6	C28, C29, C30, C31, C65, C70	402	Capacitor, 120 pF, ceramic, C0G, 25 V, 5%	Murata	GRM1555C1H121JA01J
10	C21, C22, C23, C24, C25, C26, C34, C35, C36, C39	402	Capacitor, 0.1 $\mu$ F, ceramic, X5R, 10 V, 10%	Murata	GRM155R71C104KA88D
1	CR4	603	LED green, SMT, 0603, SS-TYPE	Panasonic	LNJ314G8TRA
1	CR2	Mini 3P	Diode, 30 V, 20 mA	Agilent	HSMS2812
1	F1	1210	Fuse, 6.0 V, 2.2 A trip current resettable fuse	Tyco/Raychem	NANOSMDC110F-2
15	E1, E2, E3, E4, E5, E7, E8, E9, E10, E12, E13, E14, E31, E32, E33		Connector, header, 0.1"	Samtec	TSW-150-08-G-S
2	J2, J3	SMA end launch	Connector, SMA PCB coax end launch, Johnson 142	Johnson	142-0701-851
10	L2, L3, L4, L5, L7, L12, L13, L14, L15, R88	1206	Ferrite bead, BLM, 3 A, 50 $\Omega$ @ 100 MHz	Murata	BLM31PG500SN1L
1	P8		Power jack, male, 2.1 mm power jack dc	CUI Inc	CP-102A-ND
1	R1	201	Resistor, 100 $\Omega$ , 0201, 1/20 W, 1%	NIC Components	NRC02F1000TRF
1	R2	603	Resistor, 499 $\Omega$ , 0603, 1/10 W, 1%	NIC Components	NRC06F4990TRF

Qty	Reference Designator	Package	Description	Vendor	Part Number
2	R5, R6	402	Resistor, 36 $\Omega$ , 0402, 1/16 W, 1%	Panasonic	ERJ-2GEJ360X
2	R7, R16	402	Resistor, 15 $\Omega$ , 0402, 1/16 W, 5%	Panasonic	ERJ-2RKF15R0X
6	R10, R11, R13, R24, R25, R27	402	Resistor, 1 k $\Omega$ , 0402, 1/16 W, 1%	NIC Components	NRC04F1001TRF
4	R12, R18, R19, R26,	402	Resistor, 10 k $\Omega$ , 0402, 1/16 W, 5%	NIC Components	NRC04J103TRF
7	R15, C16, C18, C19, C20, R89, R90	402	Resistor, 0 $\Omega$ , 0402, 1/16 W, 5%	NIC Components	NRC04ZOTRF
4	RN1, RN2, RN3, RN4	0402x8	Resistor array, SMT 0402; 0 $\Omega$ , 1/4 W, 5%, RESNEXB-2HV	Panasonic	EXB2HV050JV
3	L1, L8, L9	603	Resistor, 0 $\Omega$ , 0603, 1/10 W, 5%	NIC Components	NRC06ZOTRF
1	P9, P10	805	Resistor, 0 $\Omega$ , 0805, 1/8 W, 1%	NIC Components	NRC10ZOTRF
1	SW3	EVQ-Q2F03W	Switch, light touch SMD	Panasonic	P12937SCT-ND
1	T1	2020	Ferrite bead, 5 A, 50 V, 190 $\Omega$ @ 100 MHz	Murata	DLW5BSN191SQ2L
2	T2,T3	CD542	Transformer, 0.5 W, 30 mA	Mini-Circuits	ADT1-1WT+
1	U3	6-SC70	IC, buffer, inverter, UHS dual SC70-6	Fairchild	NC7WZ16P6X
1	U5	6-SC70	IC, buffer, inverter, UHS dual OD out SC70-6	Fairchild	NC7WZ07P6X
1	U7	DO-214AA	Diode, 50 V, 2 A	Micro Commercial	S2A-TPMSTR-ND
1	U8	DO-214AB	Diode, 30 V, 3 A (SMC)	Micro Commercial	SK33-TPMSCT-ND
1	U11	SOT-223	Voltage regulator, 3.3 V, 1.5 A	Analog Devices	ADP3339AKCZ-3.3
2	U9, U12	SOT-223	Voltage regulator, 1.8 V, 1.5 A	Analog Devices	ADP3339AKCZ-1.8
1	U4	LFCSP56	AD9230 12-bit, 170 MSPS/210 MSPS/250 MSPS, 1.8 V ADC, LFCSP-56	Analog Devices	AD9230BCPZ-xxx
2	P7, P11	HM-Zd PCB	Connector, 2-Pr, 10-column, high speed, HM-Zd, PCB-mounted	Tyco	6469169-1

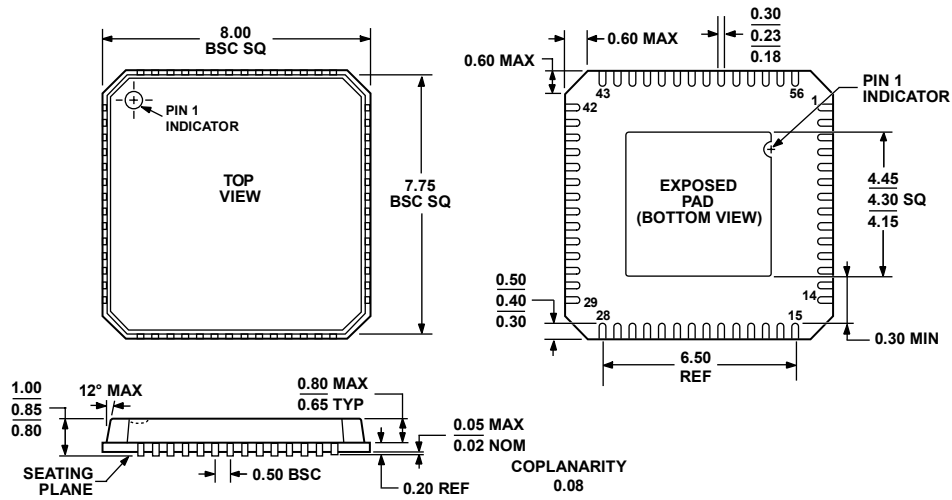
**Do not install the following:**

0	C2, C54	TAJD	Capacitor, tantalum, SMT 6032, 10 $\mu$ F, 16 V, 10%	Kemet	T491C106K016AS
0	C15, C37, C38, C40, C41, C61, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C39, C56, C57, C58, C59, C74, C75, C60, C66, C67, C68, C69, C72	402	Capacitor, 0.1 $\mu$ F, ceramic, 10%	Murata	GRM155R71C104KA88D
0	CR1	Led_ss	LED green, USS type 0603	Panasonic	LNJ314G8TRA
0	CR3	Diode	Schottky diode	Agilent	HSMS2812
0		805		Tyco/Raychem	NANOSMDC110F-2
0	E6, E15, E16, E17, E18, E19, E20		Connector, header, 0.1"	Samtec	TSW-150-08-G-S
0	J1	10-pin header	TSW-110-08-G-D	Samtec	TSW-110-08-G-D
0	J4	SMA	Connector, PCB coax SMA end launch, Johnson 142	Johnson	142-0701-851
0	L6	1206	Inductor, 10 nH	Murata	BLM31P500S
0	P12, P13, P14, P15		SMA	Amphenol RF	ARFX1231-ND

# AD9601

Qty	Reference Designator	Package	Description	Vendor	Part Number
0	R3, R14, R33, R34, R35, R48, R49	402	Resistor, 49.9 $\Omega$	Susumu	RR0510R-49R9-D
0	R42, R43, R54, R85, R86	402	Resistor, 10 k $\Omega$	NIC Components	NRC04J103TRF
0	R28, R29, R30, R31, R32	402	Resistor, 5 k $\Omega$	NIC Components	NRC04F4991TRF
0	R37, R38	402	Resistor, 25 $\Omega$	NIC Components	NRC04F24R9TRF
0	R39, R45	402	Resistor, 5 $\Omega$	NIC Components	NRC04J5R1TRF
0	R58, R59	402	Resistor, 100 $\Omega$	NIC Components	NRC04F1000TRF
0	R60, R61	402	Resistor, 240 $\Omega$	NIC Components	NRC04J241TRF
0	R8, R9, R17, R36, R40, R41, R44, R46, R47, R87, R50, R51, R52, R53, R55, R56, R57, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84	402	Resistor, 0 $\Omega$	NIC Components	NRC04ZOTRF
0	P1, P2, P16, P17	805	Resistor, 0 $\Omega$	NIC Components	NRC10ZOTRF
0	SW1	EVQ-Q2F03W	Switch, light touch SMD	Panasonic	P12937SCT-ND
0	T4		Transformer, RF, 0.4 MHz to 800 MHz, SMD case style CD542	Mini-Circuits	ADT1-1WT+
0	T5, T6	sm-22	Balun	M/A-Com	MABA007159-0000
0	U2	SOIC-8	PIC12F629	Microchip Tech	PIC12F629-I/SN
0	U6	Crystal	Cvhd_956 crystal		CVHD_956
0	U10	SOT-223	Regulator		ADP3339AKCZ-5.0
0	Z1	16CSP4X4	AD8352		
0	U1	16CSP8X8	AD9515		
0	P6		8-pin power connector post	Wieland	Z5.530.0825.0
0	P6		8-pin power connector top	Wieland	Z5.602.2853.0

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VLLD-2

Figure 49. 56-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
 8 mm × 8 mm Body, Very Thin Quad  
 (CP-56-2)  
 Dimensions shown in millimeters

112805-0

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9601BCPZ-200 <sup>1</sup>	-40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9601BCPZ-250 <sup>1</sup>	-40°C to +85°C	56-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-56-2
AD9601-250EBZ <sup>1</sup>		CMOS Evaluation Board with AD9601BCPZ-250	

<sup>1</sup> Z = RoHS Compliant Part.

**AD9601**

**NOTES**