12-Bit, 170Msps ADC

FEATURES

- **Pin Compatible with the AD9430**
- **Sample Rate: 170Msps**
- **66.2dB SNR, 84dB SFDR**
- **No Missing Codes**
- **Single 3.3V supply**
- **Power Dissipation: 1050mW**
- LVDS Digital Outputs
- 1.536V_{PP} Input Range
- Clock Duty Cycle Stabilizer
- Out-of-Range Indicator
- Data Ready Output Clock
- Integrated Bypass Capacitors
- 100-Pin SiPLGA Package

APPLICATIONS

- Wireless and Wired Broadband Communication
- Spectral Analysis

DESCRIPTION

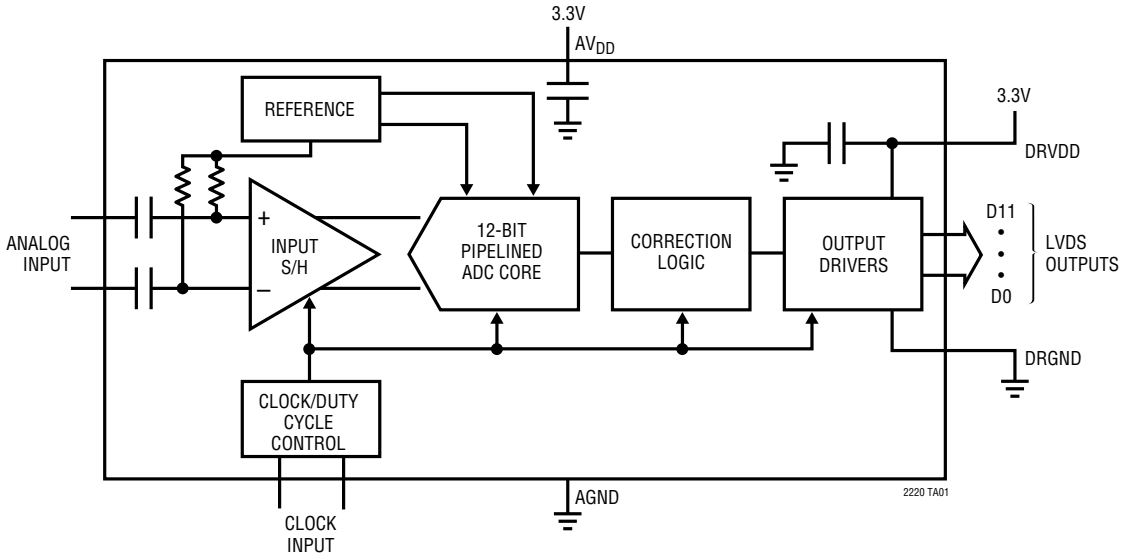
The LTM®2220-AA is a 170Msps sampling 12-bit A/D converter designed for digitizing high frequency, wide dynamic range signals. The LTM2220-AA is perfect for demanding communications applications with AC performance that includes 66.2dB SNR and 84dB spurious free dynamic range.

DC specs include ±0.5LSB INL (typ), ±0.3LSB DNL (typ) and no missing codes over temperature.

The CLK+ and CLK- inputs may be driven differentially or single ended with a sine wave, PECL, TTL or CMOS inputs. A clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

The LTM2220-AA is pin compatible with the AD9430 when used with LVDS outputs, 2's complement output format and the 1.536V_{PP} input range.

TYPICAL APPLICATION



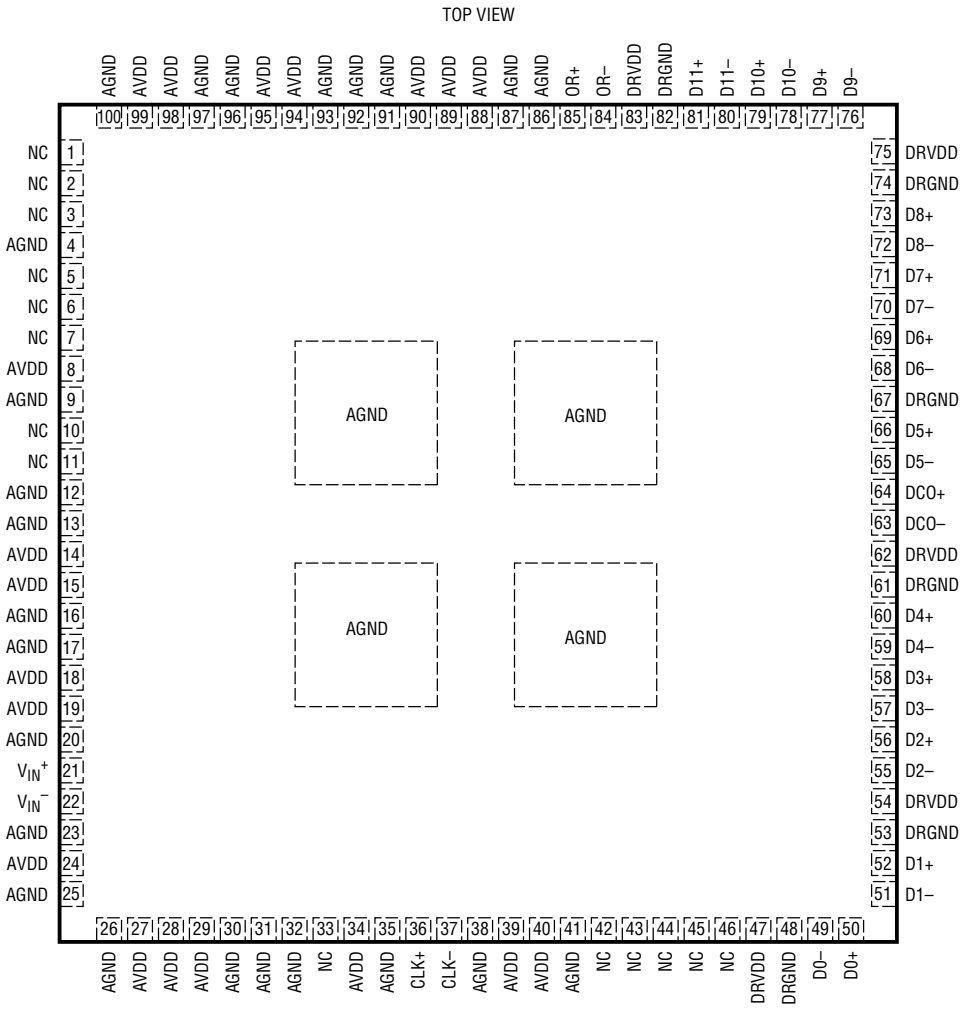
ABSOLUTE MAXIMUM RATINGS

AVDD = DRVDD (Notes 1, 2)

Supply Voltage (AVDD, DRVDD) 4V
Analog Input Voltage (Note 3) .... -0.3V to (AVDD + 0.3V)
Digital Input Voltage ..... -0.3V to (AVDD + 0.3V)
Digital Output Voltage ..... -0.3V to (DRVDD + 0.3V)

Power Dissipation 1500mW
Operating Temperature Range ..... -40°C to 85°C
Storage Temperature Range ..... -65°C to 125°C

PACKAGE/ORDER INFORMATION



SiPLGA PACKAGE
100-LEAD (16mm × 16mm)

T_{JMAX} = 125°C, θ_{JA} = 20°C/W
EXPOSED PADS ARE AGND

ORDER PART NUMBER	LGA PART MARKING
LTM2220IV-AA#PBF	LTM2220V-AA

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 5)	●	–1.5	±0.5	1.5	LSB
Differential Linearity Error		●	–1	±0.3	1	LSB
Offset Error	(Note 6)		–35	±3	35	mV
Gain Error				±0.5		%FS

ANALOG INPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Differential Input Range	$V_{IN}^+ – V_{IN}^–$	●		1.536		V
$V_{IN, CM}$	Common Mode Input Range	$(V_{IN}^+ + V_{IN}^–)/2$	●	0		3.6	V
f_L	Lower –3dB Frequency				1.6		kHz
f_H	Upper –3dB Frequency	R_S = 75Ω			195		MHz
t_{JITTER}	Sample and Hold Jitter				0.2		ps_{RMS}

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	10MHz Input			66.2		dB
		70MHz Input	●	63.5	66.1		dB
SINAD	Signal to Noise Plus Distortion Ratio	10MHz Input			66.1		dB
		70MHz Input	●	63.2	65.9		dB
SFDR	Spurious Free Dynamic Range: 2nd or 3rd Harmonic	10MHz Input			84		dB
		70MHz Input	●	70	84		dB
SFDR	Spurious Free Dynamic Range: 4th Harmonic or Higher	10MHz Input			90		dB
		70MHz Input	●	78	90		dB
IMD	Intermodulation Distortion	f_{IN1} = 138MHz, f_{IN2} = 140MHz			81		dB

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLK+, CLK–)							
V_{ID}	Differential Input Voltage		●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set			1.6		V
		Externally Set	●	1.1	1.6	2.5	V
R_{IN}	Input Resistance				6		kΩ
C_{IN}	Input Capacitance	(Note 7)			3		pF
DIGITAL LOGIC OUTPUTS							
V_{OD}	Differential Output Voltage	100Ω Load	●	247	350	454	mV
V_{OS}	Output Common Mode Voltage		●	1.125	1.250	1.375	V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AVDD	Analog Supply Voltage	(Note 8)	●	3.1	3.3	3.5	V
DRVDD	Digital Supply Voltage	(Note 8)	●	3.0	3.3	3.6	V
IAVDD	Analog Supply Current		●		264	288	mA
IDVDD	Digital Supply Current		●		55	70	mA
PDISS	Power Dissipation		●		1050	1182	mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S	Sampling Frequency		●	1		170	MHz
t_L	CLK Low Time	(Note 7)	●	2	2.94	500	ns
t_H	CLK High Time	(Note 7)	●	2	2.94	500	ns
t_{AP}	Sample-and-Hold Aperture Delay				0		ns
t_D	CLK to DATA Delay	(Note 7)	●	1.5	3	4.3	ns
t_C	CLK to DCO Delay	(Note 7)	●	1.5	3	4.3	ns
	DATA to DCO Skew	(t_C – t_D), (Note 7)	●	–0.6	0	0.6	ns
	Rise Time				0.5		ns
	Fall Time				0.5		ns
	Pipeline Latency				5		Cycles

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground with AGND and DRGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: AVDD = DRVDD = 3.3V, f_{SAMPLE} =170MHz, differential CLK+/CLK- = 2Vpp sine wave, differential analog inputs, unless otherwise noted.

Note 5: Integral nonlinearity is defined as the deviation of a code from a "best fit straight line" fit to the transfer curve. The deviation is measured from the center of the quantization band.

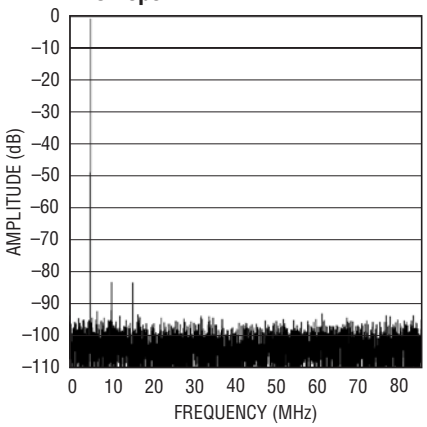
Note 6: Offset error is the offset voltage measured from -0.5 LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 7: Guaranteed by design, not subject to test.

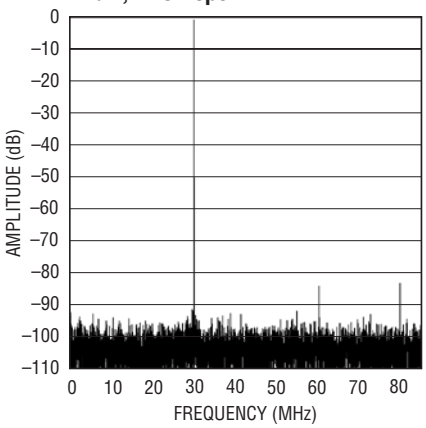
Note 8: Recommended operating conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

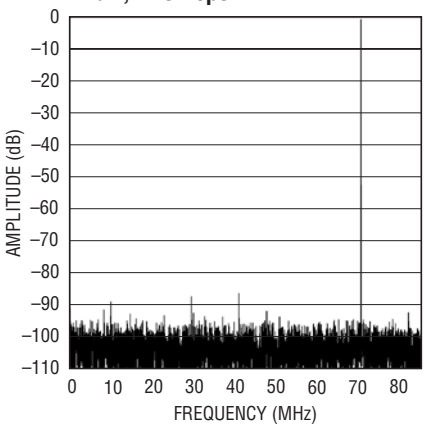
8192 Point FFT, f_{IN} = 5MHz, –1dB, 170Msps



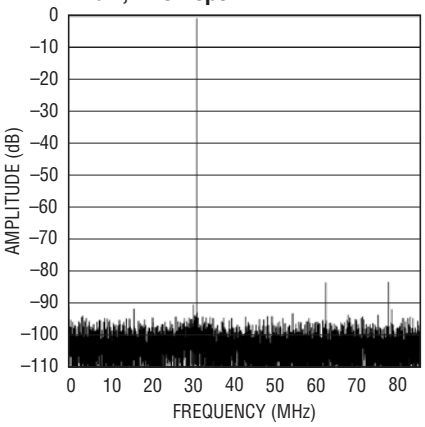
8192 Point FFT, f_{IN} = 30MHz, –1dB, 170Msps



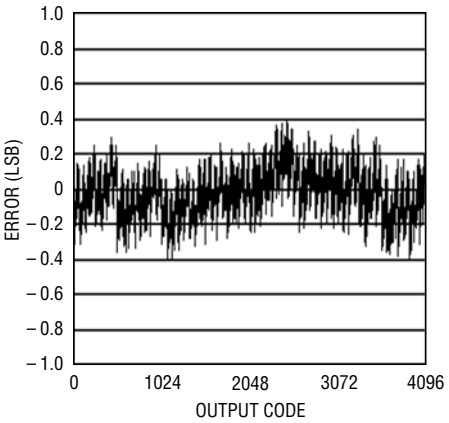
8192 Point FFT, f_{IN} = 70MHz, –1dB, 170Msps



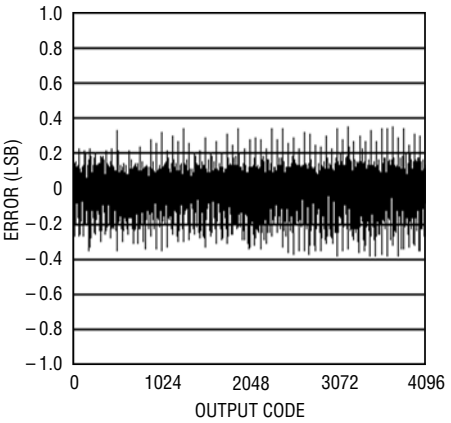
8192 Point FFT, f_{IN} = 140MHz, –1dB, 170Msps



INL Error



DNL Error



PIN FUNCTIONS

NC (Pins 1, 2, 3, 5, 6, 7, 10, 11, 33, 42, 43, 44, 45, 46): Pin is not connected internally.

AGND (Pins 4, 9, 12, 13, 16, 17, 20, 23, 25, 26, 30, 31, 32, 35, 38, 41, 86, 87, 91, 92, 93, 96, 97, 100): Analog Ground.

AVDD (Pins 8, 14, 15, 18, 19, 24, 27, 28, 29, 34, 39, 40, 88, 89, 90, 94, 95, 98, 99): 3.3V Analog Supply.

V_{IN}^+ (Pin 21): Positive Analog Input.

V_{IN}^- (Pin 22): Negative Analog Input.

CLK+ (Pin 36): Clock Input. The input sample starts on the positive edge.

CLK- (Pin 37): Clock Complement Input. Conversion starts on the negative edge. Bypass to ground with a 0.1µF ceramic for a single-ended clock.

DRVDD (Pins 47, 54, 62, 75, 83): 3.3V Digital Output Driver Supply.

DRGND (Pins 48, 53, 61, 67, 74, 82): Digital Output Driver Ground.

D0- (Pin 49): D0 Complement Output Bit (LSB).

D0+ (Pin 50): D0 True Output Bit (LSB).

D1- (Pin 51): D1 Complement Output Bit.

D1+ (Pin 52): D1 True Output Bit.

D2- (Pin 55): D2 Complement Output Bit.

D2+ (Pin 56): D2 True Output Bit.

D3- (Pin 57): D3 Complement Output Bit.

D3+ (Pin 58): D3 True Output Bit.

D4- (Pin 59): D4 Complement Output Bit.

D4+ (Pin 60): D4 True Output Bit.

DCO- (Pin 63): Data Clock Output Complement.

DCO+ (Pin 64): Data Clock Output True.

D5- (Pin 65): D5 Complement Output Bit.

D5+ (Pin 66): D5 True Output Bit.

D6- (Pin 68): D6 Complement Output Bit.

D6+ (Pin 69): D6 True Output Bit.

D7- (Pin 70): D7 Complement Output Bit.

D7+ (Pin 71): D7 True Output Bit.

D8- (Pin 72): D8 Complement Output Bit.

D8+ (Pin 73): D8 True Output Bit.

D9- (Pin 76): D9 Complement Output Bit.

D9+ (Pin 77): D9 True Output Bit.

D10- (Pin 78): D10 Complement Output Bit.

D10+ (Pin 79): D10 True Output Bit.

D11- (Pin 80): D11 Complement Output Bit (MSB).

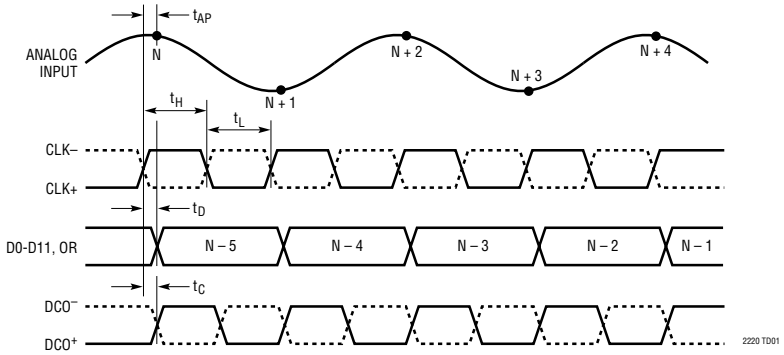
D11+ (Pin 81): D11 True Output Bit (MSB).

OR- (Pin 84): Overrange Output Complement.

OR+ (Pin 85): Overrange Output True.

GND (Exposed Pads): The exposed pads on the bottom of the package need to be soldered to Analog Ground.

TIMING DIAGRAM



2220aaf

APPLICATIONS INFORMATION

DYNAMIC PERFORMANCE

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to Total Harmonic Distortion (THD). IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. The 3rd order intermodulation products are 2fa + fb, 2fb + fa, 2fa – fb and 2fb – fa. The intermodulation distortion is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order intermodulation product.

Spurious Free Dynamic Range (SFDR)

Spurious free dynamic range is the peak harmonic or spurious noise that is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Lower and Upper –3dB Frequencies

The input frequencies at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal. Note that the analog input has a bandpass response.

Aperture Delay Time

The time from when a rising CLK+ equals the CLK– voltage to the instant that the input signal is held by the sample and hold circuit.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log(2\pi \bullet f_{IN} \bullet t_{JITTER})$$

CONVERTER OPERATION

The LTM2220-AA is a CMOS pipelined multistep converter. The converter has five pipelined ADC stages; a sampled analog input will result in a digitized value five cycles later (see the Timing Diagram section). For optimal AC performance the analog inputs should be driven differentially. For cost sensitive applications, the analog inputs can be driven single-ended with slightly worse harmonic distortion. The clock input is differential for improved common mode noise immunity.

The LTM2220-AA is pin compatible with the AD9430 when used with LVDS outputs, 2's complement output format and the $1.536V_{PP}$ input range.

The LTM2220-AA package contains power supply bypass capacitors, which makes the part easy to use since it is insensitive to the PC board layout.

APPLICATIONS INFORMATION

SAMPLE/HOLD OPERATION AND INPUT DRIVE

Sample/Hold Operation

Figure 1 shows an equivalent circuit for the LTM2220-AA CMOS differential sample-and-hold. The analog inputs are AC coupled to the sample and hold circuit through 0.1µF capacitors and 1k bias resistors. The 25Ω resistor and 0.5pF capacitor serve two purposes: isolating the drive circuitry from the sample and hold charging glitches and limiting the wideband noise at the converter input.

Single-Ended Input

For cost sensitive applications, the analog inputs can be driven single-ended. With a single-ended input the harmonic distortion and INL will degrade, but the SNR and DNL will remain unchanged.

Common Mode Bias

For optimal performance the analog inputs should be driven differentially. Each input should swing ±0.384V around a common mode voltage of between 0V and 3.6V.

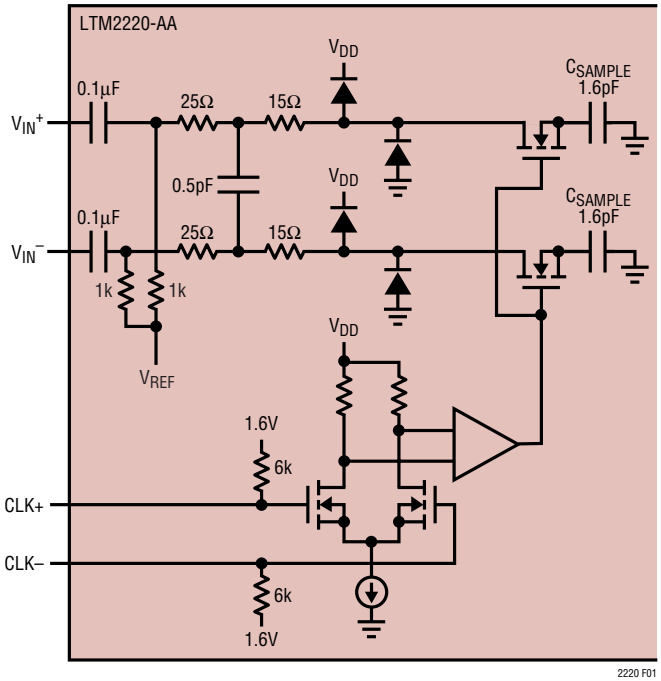


Figure 1. Equivalent Input Circuit

Input Drive Impedance

As with all high performance, high speed ADCs, the dynamic performance of the LTM2220-AA can be influenced by the input drive circuitry, particularly the second and third harmonics. Source impedance and input reactance can influence SFDR.

The source impedance should be matched for the differential inputs. Poor matching will result in higher even order harmonics, especially the second.

Input Drive Circuits

Figure 2 shows the LTM2220-AA being driven by an RF transformer with a center tapped secondary. The secondary center tap is grounded as shown, but it can also be connected to any DC bias voltage from 0V to 3.6V. Terminating on the transformer secondary is desirable, as this provides a common mode path for charging glitches caused by the sample and hold.

Driving the Clock Inputs

The noise performance of the LTM2220-AA can depend on the encode signal quality as much as on the analog input. The CLK+/CLK– inputs are intended to be driven differentially, primarily for noise immunity from common mode noise sources. Each input is biased through a 6k resistor to a 1.6V bias. The bias resistors set the DC operating point for transformer coupled drive circuits and can set the logic threshold for single-ended drive circuits.

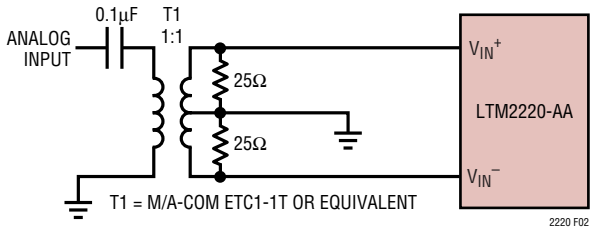


Figure 2. Single-Ended to Differential Conversion Using a Transformer

APPLICATIONS INFORMATION

Any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter.

In applications where jitter is critical (high input frequencies) take the following into consideration:

1. Differential drive should be used.

2. Use as large an amplitude as possible; if transformer coupled use a higher turns ratio to increase the amplitude.

3. If the ADC is clocked with a sinusoidal signal, filter the encode signal to reduce wideband noise.

4. Balance the capacitance and series resistance at both encode inputs so that any coupled noise will appear at both inputs as common mode noise. The clock inputs have a common mode range of 1.1V to 2.5V. Each input may be driven from ground to VDD for single-ended drive.

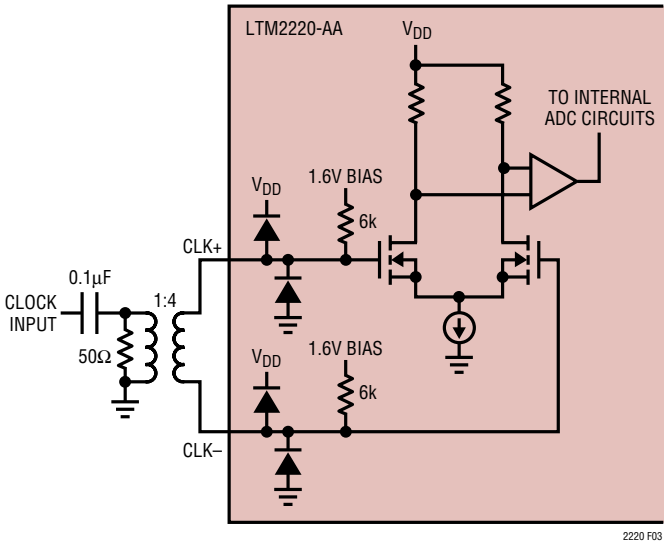


Figure 3. Transformer Driven CLK+/CLK–

Maximum and Minimum Encode Rates

The maximum encode rate for the LTM2220-AA is 170Msps. For the ADC to operate properly, the encode signal should have a 50% (±20%) duty cycle. Each half cycle must have at least 2ns for the ADC internal circuitry to have enough settling time for proper operation.

If the clock is turned off for a long period of time, the duty cycle stabilizer circuit will require one hundred clock cycles for the PLL to lock onto the input clock.

The lower limit of the LTM2220-AA sample rate is determined by droop of the sample-and-hold circuits. The pipelined architecture of this ADC relies on storing analog signals on small valued capacitors. Junction leakage will discharge the capacitors. The specified minimum operating frequency for the LTM2220-AA is 1Msps.

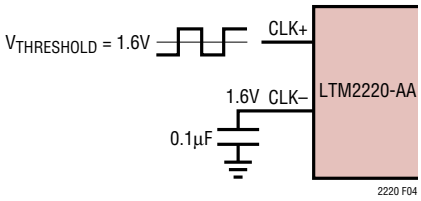


Figure 4. Single-Ended CLK Drive, Not Recommended for Low Jitter

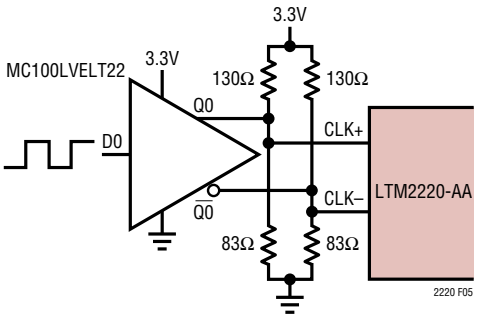


Figure 5. CLK Drive Using a CMOS to PECL Translator

APPLICATIONS INFORMATION

DIGITAL OUTPUTS

Table 1. Output Codes vs Input Voltage

$VIN^+ – VIN^–$	OR	D11 – D0
>+0.768000V	1	0111 1111 1111
+0.768000V	0	0111 1111 1111
+0.767625V	0	0111 1111 1110
+0.000375V	0	0000 0000 0001
0.000000V	0	0000 0000 0000
–0.000375V	0	1111 1111 1111
–0.000750V	0	1111 1111 1110
–0.767625V	0	1000 0000 0001
–0.768000V	0	1000 0000 0000
<–0.768000V	1	1000 0000 0000

Digital Output Buffers

Figure 6 shows an equivalent circuit for a differential output pair in the LVDS output mode. A 3.5mA current is steered from OUT^+ to $OUT^–$ or vice versa which creates a ±350mV differential voltage across the 100Ω termination resistor at the LVDS receiver. A feedback loop regulates the common mode output voltage to 1.25V. For proper operation each LVDS output pair needs an external 100Ω termination resistor, even if the signal is not used (such as OR+/OR– or DCO+/DCO–). To minimize noise the PC board traces for each LVDS output pair should be routed close together. To minimize clock skew all LVDS PC board traces should have about the same length.

Data Format

The LTM2220-AA parallel digital output has 2's complement format. Table 1 shows the relationship between the analog input voltage, the digital data bits and the overrange bit.

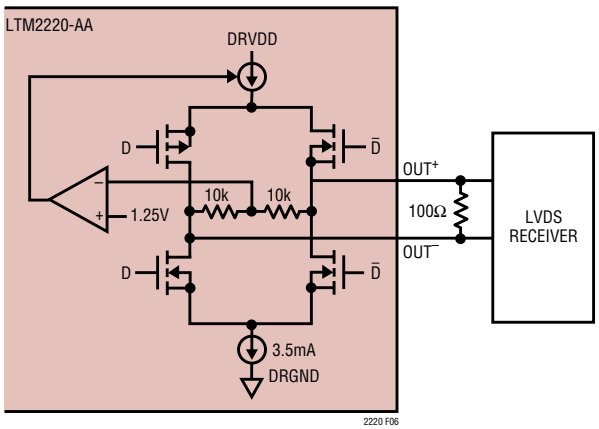


Figure 6. Digital Output

Output Clock

The ADC has a delayed version of the CLK+ input available as a digital output, DCO. The DCO pin can be used to synchronize the converter data to the digital system. This is necessary when using a sinusoidal clock. Data will be updated as DCO+/DCO– rises and can be latched on the falling edge of DCO+/DCO–.

Output Driver Power

Separate output power and ground pins allow the output drivers to be isolated from the analog circuitry. DRVDD should be connected to a 3.3V supply and DRGND should be connected to GND.

GROUNDING AND BYPASSING

The LTM2220-AA requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital signal alongside an analog signal or underneath the ADC.

The LTM2220-AA differential inputs should run parallel and close to each other. The input traces should be as short as possible to minimize capacitance and to minimize noise pickup.

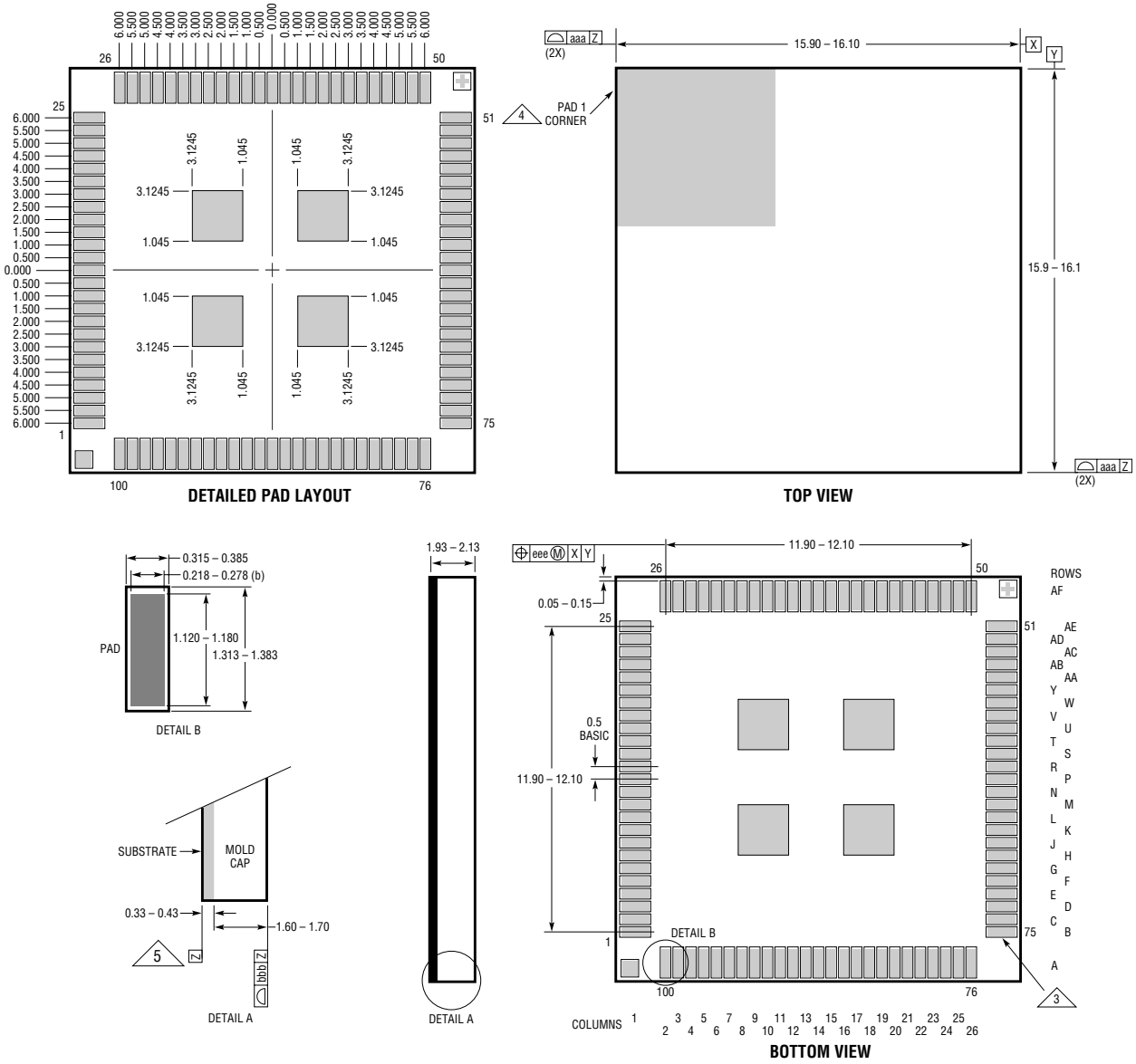
The LTM2220-AA package contains power supply bypass capacitors on AVDD and DRVDD. External bypass capacitors can be added for additional low-frequency noise rejection, but they are not required if the power supplies come from quiet linear voltage regulators.

HEAT TRANSFER

Most of the heat generated by the LTM2220-AA is transferred from the die through the bottom-side exposed pads and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pads should be soldered to a large grounded pad on the PC board. It is critical that all ground pins are connected to a ground plane of sufficient area.

PACKAGE DESCRIPTION

SiPLGA Package
100-Lead (16mm × 16mm)
(Reference LTC DWG # 05-08-1802 Rev Ø)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. DIMENSION (b) IS MEASURED AT THE MAXIMUM LAND WIDTH, PARALLEL TO PRIMARY DATUM -Z-
7. TOTAL NUMBER OF PADS: 104 TOTAL (100 PERIPHERAL + 4 COMMON CENTER)

SYMBOL	TOLERANCE
aaa	0.10
bbb	0.10
eee	0.03

10_10_06

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2220	12-Bit, 170Msps, 3.3V ADC, LVDS Outputs	890mW, 67.7dB SNR, 84dB SFDR, 64-Pin QFN Package
LTC2242-12	12-Bit, 250Msps, 2.5V ADC, LVDS Outputs	740mW, 65.4dB SNR, 84dB SFDR, 64-Pin QFN Package
LT1993-2	High Speed Differential Op Amp	800MHz BW, 70dBc Distortion at 70MHz, 6dB Gain

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT 0107 • PRINTED IN USA