1 MSPS 16-/14-Bit Analog I/O Port

AD15700

FEATURES

16-Bit A/D Converter
- 1 MSPS
- S/(N + D): 90 dB Typ @ 250 kHz
- No Pipeline Delay

14-Bit D/A Converter
- Settling Time: 1 μs
- S/N: 92 dB Typ

2 80 MHz Amplifiers
- 30 V/μs Slew Rate
- Rail-to-Rail Input and Output
- Output Current 15 mA

2 Gain Setting Center Tapped Resistors
- Resistor Ratio Tracking: 2 ppm/°C

Unipolar Operation

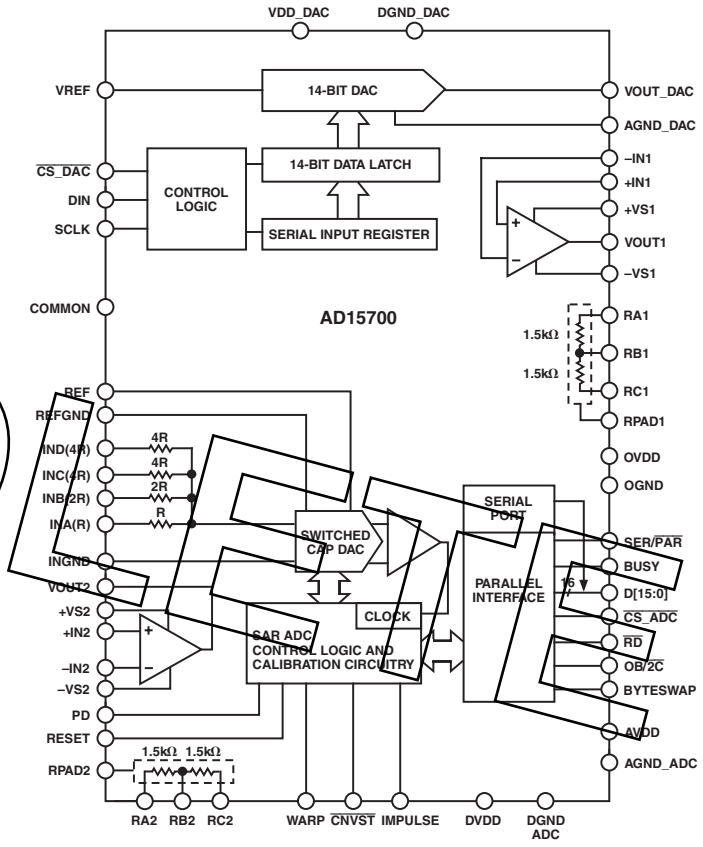
SPI®/QSPI™/MICROWIRE™/DSP Compatible

132 mW Typical Power Dissipation

APPLICATIONS

Optical MEMS Mirror Control
Industrial Process Control
Data Acquisition
Instrumentation
Communication

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD15700 is a precision component to interface analog input and output channels to a digital processor. It is ideal for area-limited applications that require maximum circuit density. The AD15700 contains the functionality of a 16-bit, 1 MSPS charge redistribution SAR analog-to-digital converter that operates from a 5 V power supply. The high speed 16-bit sampling ADC incorporates a resistor input scaler that allows various input ranges, an internal conversion clock, error correction circuits, and both serial and parallel system interface ports. The AD15700 also contains a 14-bit, serial input, voltage output DAC that operates from a 5 V supply and has a settling time of 1 μs. Two single- or split-supply voltage feedback amplifiers with rail-to-rail input and output characteristics featuring 80 MHz of small signal bandwidth and 10 μV/°C offset drift provide ADC and DAC buffering capability. The center tapped 3 kΩ resistors are precision resistor networks with 2 ppm/°C ratio tracking that provide low gain drift when used for scaling.

The ADC, DAC, and amp functions are electrically isolated from each other to provide maximum design flexibility. Input and output signal conditioning circuits for the converters can be easily configured with short interconnects under the device at the board level. The AD15700 is available in a 10 mm CSPBGA package.

PRODUCT HIGHLIGHTS

1. Fast Throughput ADC.
   The AD15700 incorporates a high speed, 1 MSPS, 16-bit SAR ADC.
2. Superior ADC INL.
   The 16-bit ADC has a maximum integral nonlineariy of 2.5 LSB with no missing codes.
3. Two Precision Resistor Networks with 2 ppm/°C Ratio Tracking for Gain Setting.
4. Low Power Consumption.
   Typically 132 mW at maximum performance levels.
5. Industrial Temperature Range: –40°C to +85°C.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD15700–SPECIFICATIONS

16-BIT ADC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Voltage Range	VIND – VINGND	±4 REF, 0 V to 4 REF, ±2 REF (See Table I)			
Common-Mode Input Voltage	VINGND	–0.1		+0.5	V
Analog Input CMRR	f_{IN} = 100 kHz		74		dB
Input Impedance			See Table I		
THROUGHPUT SPEED					
Complete Cycle	In Warp Mode			1	µs
Throughput Rate	In Warp Mode	1		1000	kSPS
Time between Conversions	In Warp Mode			1	ms
Complete Cycle	In Normal Mode			1.25	µs
Throughput Rate	In Normal Mode	0		800	kSPS
Complete Cycle	In Impulse Mode			1.5	µs
Throughput Rate	In Impulse Mode	0		666	kSPS
DC ACCURACY					
Integral Linearity Error		–2.5		+2.5	LSB[1]
No Missing Codes		16			Bits
Transition Noise			0.7		LSB
Bipolar Zero Error[2], T_{MIN} to T_{MAX}	±5 V Range, Normal or Impulse Modes	–45		+45	LSB
	Other Range or Mode		±0.1%		% of FSR
Bipolar Full-Scale Error[2], T_{MIN} to T_{MAX}		–0.38		+0.38	% of FSR
Unipolar Zero Error[2], T_{MIN} to T_{MAX}		–0.18		+0.18	% of FSR
Unipolar Full-Scale Error[2], T_{MIN} to T_{MAX}		–0.76		+0.76	% of FSR
Power Supply Sensitivity	AVDD = 5 V ± 5%		±9.5		LSB
AC ACCURACY					
Signal-to-Noise	f_{IN} = 20 kHz	89	90		dB[3]
	f_{IN} = 250 kHz		90		dB
Spurious-Free Dynamic Range	f_{IN} = 250 kHz		100		dB
Total Harmonic Distortion	f_{IN} = 20 kHz		–100	–96	dB
	f_{IN} = 250 kHz		–100		dB
Signal-to-(Noise + Distortion)	f_{IN} = 20 kHz	88.5	90		dB
	f_{IN} = 250 kHz, –60 dB Input		30		dB
–3 dB Input Bandwidth			9.6		MHz
SAMPLING DYNAMICS					
Aperture Delay			2		ns
Aperture Jitter			5		ps rms
Transient Response	Full-Scale Step			250	ns
REFERENCE					
External Reference Voltage Range		2.3	2.5	3.0	V
External Reference Current Drain	1 MSPS Throughput		200		µA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.0		DVDD + 0.3	V
I_{IL}		–1		+1	µA
I_{IH}		–1		+1	µA

Parameter	Condition	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
Data Format			Parallel or Serial 16-Bit		
Pipeline Delay			Conversion Results Available Immediately after Completed Conversion		
V_{OL}	I_{SINK} = 1.6 mA			0.4	V
V_{OH}	I_{SOURCE} = –570 µA	OVDD – 0.6			V
POWER SUPPLIES					
Specified Performance					
AVDD		4.75	5	5.25	V
DVDD		4.75	5	5.25	V
OVDD		2.7		5.25	V
Operating Current[4]					
AVDD			15		mA
DVDD[5]			7.2		mA
OVDD[5]			37		µA
Power Dissipation[5, 6]	666 kSPS Throughput[7]		84	95	mW
	100 SPS Throughput[7]		15		µW
	1 MSPS Throughput[4]		112	125	mW
In Power-Down Mode[8]				1	mW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	–40		+85	°C

NOTES
[1]LSB means Least Significant Bit. With the ±5 V input range, one LSB is 152.588 µV.
[2]These specifications do not include the error contribution from the external reference.
[3]All specifications in dB are referred to a full-scale input FS. Tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[4]In Warp Mode.
[5]Tested in Parallel Reading Mode.
[6]Tested with the 0 V to 5 V range and VIN – VINGND = 0 V.
[7]In Impulse Mode.
[8]With OVDD below DVDD + 0.3 V and all digital inputs forced to OVDD or OGND, respectively.

Specifications subject to change without notice.

Table I. Analog Input Configuration

Input Voltage Range	IND(4R)	INC(4R)	INB(2R)	INA(R)	Input Impedance[1]
±4 REF	V_{IN}	INGND	INGND	REF	1.63 kΩ
±2 REF	V_{IN}	V_{IN}	INGND	REF	948 Ω
± REF	V_{IN}	V_{IN}	V_{IN}	REF	711 Ω
0 V to 4 REF	V_{IN}	V_{IN}	INGND	INGND	948 Ω
0 V to 2 REF	V_{IN}	V_{IN}	V_{IN}	INGND	711 Ω
0 V to REF	V_{IN}	V_{IN}	V_{IN}	V_{IN}	Note 2

NOTES
[1]Typical analog input impedance.
[2]For this range, the input is high impedance.

16-BIT ADC TIMING CHARACTERISTICS (–40°C to +85°C, AVDD = DVDD = 5 V, OVDD = 2.7 V to 5.25 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
Refer to Figures 14 and 15					
Convert Pulsewidth	t_1	5			ns
Time between Conversions (Warp Mode/Normal Mode/Impulse Mode)	t_2	1/1.25/1.5		Note 1	µs
CNVST LOW to BUSY HIGH Delay	t_3			30	ns
BUSY HIGH All Modes Except in Master Serial Read after Convert Mode (Warp Mode/Normal Mode/Impulse Mode)	t_4			0.75/1/1.25	µs
Aperture Delay	t_5		2		ns
End of Conversion to BUSY LOW Delay	t_6	10			ns
Conversion Time (Warp Mode/Normal Mode/Impulse Mode)	t_7			0.75/1/1.25	µs
Acquisition Time	t_8	1			µs
RESET Pulsewidth	t_9	10			ns
Refer to Figures 16, 17, and 18 (Parallel Interface Modes)					
CNVST LOW to DATA Valid Delay (Warp Mode/Normal Mode/Impulse Mode)	t_{10}			0.75/1/1.25	µs
DATA Valid to BUSY LOW Delay	t_{11}	20			ns
Bus Access Request to DATA Valid	t_{12}			40	ns
Bus Relinquish Time	t_{13}	5		15	ns
Refer to Figures 20 and 21 (Master Serial Interface Modes)[2]					
CS_ADC LOW to SYNC Valid Delay	t_{14}			10	ns
CS_ADC LOW to Internal SCLK Valid Delay	t_{15}			10	ns
CS_ADC LOW to SDOUT Delay	t_{16}			10	ns
CNVST LOW to SYNC Delay (Read During Convert) (Warp Mode/Normal Mode/Impulse Mode)	t_{17}		25/275/525		ns
SYNC Asserted to SCLK First Edge Delay[3]	t_{18}	4			ns
Internal SCLK Period[3]	t_{19}	25		40	ns
Internal SCLK HIGH[3]	t_{20}	15			ns
Internal SCLK LOW[3]	t_{21}	9			ns
SDOUT Valid Setup Time[3]	t_{22}	4.5			ns
SDOUT Valid Hold Time[3]	t_{23}	2			ns
SCLK Last Edge to SYNC Delay[3]	t_{24}	3			ns
CS_ADC HIGH to SYNC HI-Z	t_{25}			10	ns
CS_ADC HIGH to Internal SCLK HI-Z	t_{26}			10	ns
CS_ADC HIGH to SDOUT HI-Z	t_{27}			10	ns
BUSY HIGH in Master Serial Read after Convert[3]	t_{28}		See Table II		µs
CNVST LOW to SYNC Asserted Delay	t_{29}		0.75/1/1.25		µs
Master Serial Read after Convert					
SYNC Deasserted to BUSY LOW Delay	t_{30}		25		ns
Refer to Figures 22 and 24 (Slave Serial Interface Modes)					
External SCLK Setup Time	t_{31}	5			ns
External SCLK Active Edge to SDOUT Delay	t_{32}	3		16	ns
SDIN Setup Time	t_{33}	5			ns
SDIN Hold Time	t_{34}	5			ns
External SCLK Period	t_{35}	25			ns
External SCLK HIGH	t_{36}	10			ns
External SCLK LOW	t_{37}	10			ns

NOTES

[1]In Warp Mode only, the maximum time between conversions is 1 ms; otherwise, there is no required maximum time.

[2]In Serial Interface Modes, the SYNC, SCLK, and SDOUT timings are defined with a maximum load C_L of 10 pF; otherwise, the load is 60 pF maximum.

[3]In serial master Read during Convert Mode. See Table II.

Specifications subject to change without notice.

Table II. Serial Clock Timings in Master Read after Convert

DIVSCLK[1] DIVSCLK[0]	Symbol	0 0	0 1	1 0	1 1	Unit
SYNC to SCLK First Edge Delay Minimum	t_{18}	4	20	20	20	ns
Internal SCLK Period Minimum	t_{19}	25	50	100	200	ns
Internal SCLK Period Maximum	t_{19}	40	70	140	280	ns
Internal SCLK HIGH Minimum	t_{20}	15	25	50	100	ns
Internal SCLK LOW Minimum	t_{21}	9	24	49	99	ns
SDOUT Valid Setup Time Minimum	t_{22}	4.5	22	22	22	ns
SDOUT Valid Hold Time Minimum	t_{23}	2	4	30	89	ns
SCLK Last Edge to SYNC Delay Minimum	t_{24}	3	60	140	300	ns
BUSY HIGH Width Maximum (Warp)	t_{28}	1.5	2	3	5.25	µs
BUSY HIGH Width Maximum (Normal)	t_{28}	1.75	2.25	3.25	5.5	µs
BUSY HIGH Width Maximum (Impulse)	t_{28}	2	2.5	3.5	5.75	µs

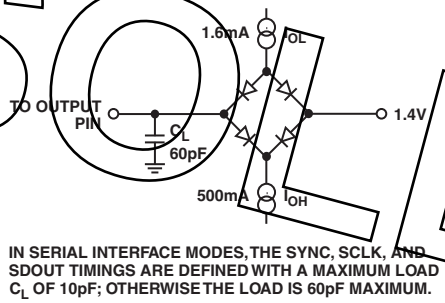


Figure 1. Load Circuit for Digital Interface Timing, SDOUT, SYNC, SCLK Outputs, C_L = 10 pF

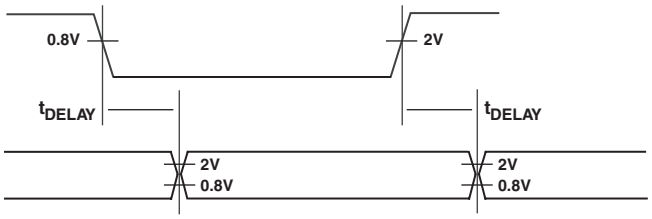


Figure 2. Voltage Reference Levels for Timing

14-BIT DAC ELECTRICAL CHARACTERISTICS (T_A = –40°C to +85°C, V_{DD}_DAC = 5 V, V_{REF} = 2.5 V, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
STATIC PERFORMANCE					
Resolution	1 LSB = $V_{REF}/2^{14}$ = 153 µV when V_{REF} = 2.5 V	14			Bits
Relative Accuracy, INL			±0.15	±1.0	LSB
Differential Nonlinearity	Guaranteed Monotonic		±0.15	±0.8	LSB
Gain Error		–1.75	–0.3	0	LSB
Gain Error Temperature Coefficient			±0.1		ppm/°C
Zero Code Error		0	0.1	0.5	LSB
Zero Code Temperature Coefficient			±0.05		ppm/°C
OUTPUT CHARACTERISTICS					
Output Voltage Range		0		V_{REF} –1 LSB	V
Output Voltage Settling Time	To 1/2 LSB of FS, C_L = 10 pF		1		µs
Digital-to-Analog Glitch Impulse	1 LSB Change around the Major Carry		10		nV–s
Digital Feedthrough	All 1s Loaded to DAC, V_{REF} = 2.5 V		0.05		nV–s
DAC Output Impedance	Tolerance Typically 20%		6.25		kΩ
Power Supply Rejection Ratio	ΔV_{DD} ±10%			±1.0	LSB
DAC REFERENCE INPUT					
Reference Input Range		2		V_{DD}	V
Reference Input Resistance*		9			kΩ
LOGIC INPUTS					
Input Current				±1.0	µA
VINL, Input Low Voltage				0.8	V
VINH, Input High Voltage		2.4			V
Input Capacitance				10	pF
Hysteresis Voltage			0.4		V
REFERENCE					
Reference –3 dB Bandwidth	All 1s Loaded		1.3		MHz
Reference Feedthrough	All 0s Loaded, V_{REF} = 1 V p-p at 100 kHz		1		mV p-p
Signal-to-Noise Ratio			92		dB
Reference Input Capacitance	Code 0000_H		75		pF
	Code $3FFF_H$		120		pF
POWER REQUIREMENTS					
V_{DD}		4.5		5.50	V
I_{DD}			0.3	1.1	mA
Power Dissipation			1.5	6.05	mW

*Reference input resistance is code-dependent, minimum at 2555_H.

Specifications subject to change without notice.

14-BIT DAC TIMING CHARACTERISTICS[1, 2] (V_{DD} = 5 V, ±5%, V_{REF} = 2.5 V, AGND = DGND = 0 V. All Specifications $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted).

Parameter	Limit at T_{MIN}, T_{MAX} All Versions	Unit	Description
f_{SCLK}	25	MHz max	SCLK Cycle Frequency
t_1	40	ns min	SCLK Cycle Time
t_2	20	ns min	SCLK High Time
t_3	20	ns min	SCLK Low Time
t_4	15	ns min	$\overline{CS\_DAC}$ Low to SCLK High Setup
t_5	15	ns min	$\overline{CS\_DAC}$ High to SCLK High Setup
t_6	35	ns min	SCLK High to $\overline{CS\_DAC}$ Low Hold Time
t_7	20	ns min	SCLK High to $\overline{CS\_DAC}$ High Hold Time
t_8	15	ns min	Data Setup Time
t_9	0	ns min	Data Hold Time
t_{10}	30	ns min	$\overline{CS\_DAC}$ High Time between Active Periods

NOTES

[1]Guaranteed by design. Not production tested.

[2]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are measured with tr = tf = 5 ns (10% to 90% of 3 V and timed from a voltage level of 1.6 V).

Specifications subject to change without notice.

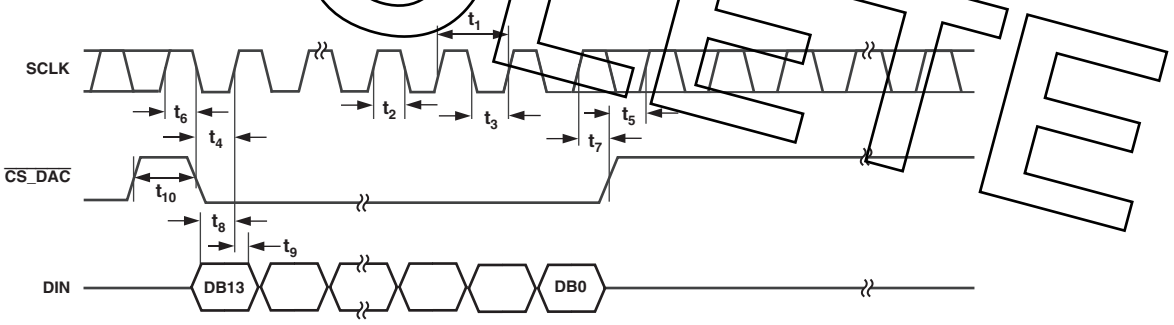


Figure 3. Timing Diagram

AMPLIFIER ELECTRICAL CHARACTERISTICS

[5 V Supply (T_A = 25°C, V_S = 5 V, R_L = 1 kΩ to 2.5 V, R_F = 2.5 kΩ, unless otherwise noted.)]

Parameter	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, V_O < 0.4 V p-p	54	80		MHz
Slew Rate	G = –1, V_O = 2 V Step	27	32		V/µs
Settling Time to 0.1%	G = –1, V_O = 2 V Step, C_L = 10 pF		125		ns
DISTORTION/NOISE PERFORMANCE					
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p, G = +2		–62		dBc
	f_C = 100 kHz, V_O = 2 V p-p, G = +2		–86		dBc
Input Voltage Noise	f = 1 kHz		15		nV/√Hz
Input Current Noise	f = 100 kHz		2.4		pA/√Hz
	f = 1 kHz		5		pA/√Hz
Differential Gain	R_L = 1 kΩ		0.17		%
Differential Phase	R_L = 1 kΩ		0.11		Degrees
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = V_{CC}/2; V_{OUT} = 2.5 V		±1	±6	mV
	T_{MIN} to T_{MAX}		±6	±10	mV
Offset Drift	V_{CM} = V_{CC}/2; V_{OUT} = 2.5 V		5		µV/°C
Input Bias Current	V_{CM} = V_{CC}/2; V_{OUT} = 2.5 V		0.45	1.2	µA
	T_{MIN} to T_{MAX}			2.0	µA
Input Offset Current			50	350	nA
Open-Loop Gain	V_{CM} = V_{CC}/2; V_{OUT} = 1.5 V to 3.5 V	76	82		dB
	T_{MIN} to T_{MAX}	74			dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			40		MΩ
Differential Input Resistance			280		kΩ
Input Capacitance			1.6		pF
Input Voltage Range			–0.5 to +5.5		V
Input Common-Mode Voltage Range			–0.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 5 V	56	70		dB
	V_{CM} = 0 V to 3.8 V	66	80		dB
Differential/Input Voltage				3.4	V
OUTPUT CHARACTERISTICS					
Output Voltage Swing Low	R_L = 10 kΩ	0.05	0.02		V
Output Voltage Swing High		4.95	4.98		V
Output Voltage Swing Low	R_L = 1 kΩ	0.2	0.1		V
Output Voltage Swing High		4.8	4.9		V
Output Current			15		mA
Short Circuit Current	Sourcing		28		mA
	Sinking		–46		mA
Capacitive Load Drive	G = +2		15		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current per Amplifier			800	1400	µA
Power Supply Rejection Ratio	V_S– = 0 V to –1 V or V_S+ = 5 V to 6 V	75	86		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

AMPLIFIER ELECTRICAL CHARACTERISTICS [±5 V Supply (T_A = 25°C, V_S = ±5 V, R_L = 1 kΩ to 0 V, R_F = 2.5 kΩ, unless otherwise noted.)]

Parameter	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = +1, V_O < 0.4 V p-p	54	80		MHz
Slew Rate	G = –1, V_O = 2 V Step	30	35		V/µs
Settling Time to 0.1%	G = –1, V_O = 2 V Step, C_L = 10 pF		125		ns
DISTORTION/NOISE PERFORMANCE					
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p, G = +2		–62		dBc
	f_C = 100 kHz, V_O = 2 V p-p, G = +2		–86		dBc
Input Voltage Noise	f = 1 kHz		15		nV/√Hz
Input Current Noise	f = 100 kHz		2.4		pA/√Hz
	f = 1 kHz		5		pA/√Hz
Differential Gain	R_L = 1 kΩ		0.15		%
Differential Phase	R_L = 1 kΩ		0.15		Degrees
DC PERFORMANCE					
Input Offset Voltage	V_{CM} = 0 V; V_{OUT} = 0 V		±1	±6	mV
	T_{MIN} to T_{MAX}		±6	±10	mV
Offset Drift	V_{CM} = 0 V; V_{OUT} = 0 V		5		µV/°C
Input Bias Current	V_{CM} = 0 V; V_{OUT} = 0 V		0.45	1.2	µA
	T_{MIN} to T_{MAX}			2.0	µA
Input Offset Current			50	350	nA
Open-Loop Gain	V_{CM} = 0 V; V_{OUT} = ±2 V	76	80		dB
	T_{MIN} to T_{MAX}	74			dB
INPUT CHARACTERISTICS					
Common-Mode Input Resistance			40		MΩ
Differential Input Resistance			280		kΩ
Input Capacitance			1.6		pF
Input Voltage Range			–5.5 to +5.5		V
Input Common-Mode Voltage Range			–5.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = –5 V to +5 V	60	80		dB
	V_{CM} = –5 V to +3.5 V	66	90		dB
Differential/Input Voltage				3.4	V
OUTPUT CHARACTERISTICS					
Output Voltage Swing Low	R_L = 10 kΩ	–4.94	–4.98		V
Output Voltage Swing High		+4.94	+4.98		V
Output Voltage Swing Low	R_L = 1 kΩ	–4.7	–4.85		V
Output Voltage Swing High		+4.7	+4.75		V
Output Current			15		mA
Short Circuit Current	Sourcing		+35		mA
	Sinking		–50		mA
Capacitive Load Drive	G = +2		15		pF
POWER SUPPLY					
Operating Range		±1.35		±6	V
Quiescent Current per Amplifier			900	1600	µA
Power Supply Rejection Ratio	V_S– = –5 V to –6 V or V_S+ = +5 V to +6 V	76	86		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

RESISTOR DIVIDER ELECTRICAL CHARACTERISTICS (@ T_A = 25°C, unless otherwise noted.)

Parameter	Condition	Min	Typ	Max	Unit
Resistance		2.97	3.00	3.03	kΩ
Temperature Coefficient of Resistance			50		ppm/°C
Resistance Ratio of Two Halves		0.99	1.0	1.01	
Resistance Ratio Tracking				2	ppm/°C
Power Dissipation	T_A = 70°C			250*	mW

*At higher temperatures, linearly derates to 0 mW at 175°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Analog Inputs
- IND, INC, INB . . . . . –11 V to +30 V
- INA, REF, INGND, REFGND, AGND . . . –0.3 V to AVDD + 0.3 V

ADC Ground Voltage Differences
- AGND_ADC, DGND_ADC, OGND . . . . . ±0.3 V

ADC Supply Voltages
- AVDD, DVDD, OVDD . . . . . 7 V
- AVDD to DVDD, AVDD to OVDD . . . . . ±7 V
- DVDD to OVDD . . . . . ±7 V

ADC Digital Inputs . . . . . –0.3 V to DVDD + 0.3 V
VDD_DAC to AGND_DAC . . . . . –0.3 V to +6 V
DAC Digital Input Voltage to
- DGND_DAC . . . . . –0.3 V to DVDD + 0.3 V

VOUT_DAC to AGND_DAC . . . . –0.3 V to DVDD + 0.3 V
AGND_DAC to DGND_DAC . . . . . –0.3 V to +0.3 V
DAC Input Current to Any DAC Pin Except Supplies . . ±10 mA
Amplifier Supply Voltage (VS1, VS2) . . . . . 12.6 V
Amplifier Input Voltage (Common Mode) . . . . . $\pm V_S$ ±0.5 V
Amplifier Differential Input Voltage . . . . . ±3.4 V
Amplifier Output Short Circuit
- Duration . . . . . Observe Power Derating Curves

Resistor Instantaneous Voltage Drop . . . . . ±50 V
Internal Power Dissipation . . . . . $(T_J \text{ Max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
- 10 mm CSPBGA . . . . . 42°C/W

Maximum Junction Temperature (T_J Max) . . . . . 150°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature . . . . . 225°C, 15 sec

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD15700BCA	–40°C to +85°C	144-Lead CSPBGA
AD15700/PCB	25°C	Evaluation Board
ADDS-2191-EZLITE™	25°C	Evaluation Kit*
ADDS-21535-EZLITE		
ADDS-21160M-EZLITE		
ADDS-21161N-EZLITE		

*One of the DSP Evaluation Kits is required for operation of the AD15700/PCB Evaluation Board.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD15700 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADC PIN FUNCTION DESCRIPTIONS (See Pinout, page 42)

Pin No.	Mnemonic	Type	Description
H9, J8, J9, M12	AGND_ADC	P	Analog Power Ground Pin
M6	AVDD	P	Input Analog Power Pin. Nominally 5 V.
L7	BYTESWAP	DI	Parallel Mode Selection (8-/16-Bit). When LOW, the LSB is output on D[7:0] and the MSB is output on D[15:8]. When HIGH, the LSB is output on D[15:8] and the MSB is output on D[7:0].
L8	OB/$\overline{2C}$	DI	Straight Binary/Binary Twos Complement. When OB/$\overline{2C}$ is HIGH, the digital output is straight binary; when LOW, the MSB is inverted, resulting in a twos complement output from its internal shift register.
M7	WARP	DI	Mode Selection. When HIGH and IMPULSE LOW, this input selects the fastest mode, the maximum throughput is achievable, and a minimum conversion rate must be applied in order to guarantee full specified accuracy. When LOW, full accuracy is maintained independent of the minimum conversion rate.
L9	IMPULSE	DI	Mode Selection. When HIGH and WARP LOW, this input selects a reduced power mode. In this mode, the power dissipation is approximately proportional to the sampling rate.
M8	SER/$\overline{PAR}$	DI	Serial/Parallel Selection Input. When LOW, the Parallel Port is selected; when HIGH, the Serial Interface Mode is selected and some bits of the DATA bus are used as a serial port.
M9, L10	D[0:1]	DO	Bit 0 and Bit 1 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, these outputs are in high impedance.
M10, L11	D[2:3] or DIVSCLK[0:1]	DI/O	When SER/$\overline{PAR}$ is HIGH, EXT/$\overline{INT}$ is LOW and/RDC/SDIN is LOW, which is the serial master read DIVSCLK[0:1] after Convert Mode. These inputs, part of the Serial Port, are used to slow down, if desired, the internal serial clock that clocks the data output. In the other serial modes, these inputs are not used.
M11	D[4] or EXT/$\overline{INT}$	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 4 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used as a digital select input for choosing the internal or an external data clock, called, respectively, Master and Slave Mode. With EXT/$\overline{INT}$ tied LOW, the internal clock is selected on SCLK output. With EXT/$\overline{INT}$ set to a logic HIGH, output data is synchronized to an external clock signal connected to the SCLK input and the external clock is gated by $\overline{CS\_ADC}$.
L12	D[5] or INVSYNC	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 5 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used to select the active state of the SYNC signal. When LOW, SYNC is active HIGH. When HIGH, SYNC is active LOW.
K11	D[6] or INVSCLK	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 6 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the Serial Port, is used to invert the SCLK signal. It is active in both Master and Slave Mode.
K12	D[7] or RDC/SDIN	DI/O	When SER/$\overline{PAR}$ is LOW, this output is used as Bit 7 of the Parallel Port Data Output Bus. When SER/$\overline{PAR}$ is HIGH, this input, part of the serial port, is used as either an external data input or a read mode selection input, depending on the state of EXT/$\overline{INT}$. When EXT/$\overline{INT}$ is HIGH, RDC/SDIN could be used as a data input to daisy-chain the conversion results from two or more ADCs onto a single SDOUT line. The digital data level on SDIN is output on DATA with a delay of 16 SCLK periods after the initiation of the read sequence. When EXT/$\overline{INT}$ is LOW, RDC/SDIN is used to select the read mode. When RDC/SDIN is HIGH, the previous data is output on SDOUT during conversion. When RDC/SDIN is LOW, the data can be output on SDOUT only when the conversion is complete.
J10	OGND	P	Input/Output Interface Digital Power Ground
J11	OVDD	P	Input/Output Interface Digital Power. Nominally at the same supply as the supply of the host interface (5 V or 3.3 V).
J12	DVDD	P	Digital Power. Nominally at 5 V.

ADC PIN FUNCTION DESCRIPTIONS (continued)

Pin No.	Mnemonic	Type	Description
H10	DGND_ADC	P	Digital Power Ground
H12	D[8] or SDOUT	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 8 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the serial port, is used as a serial data output synchronized to SCLK. Conversion results are stored in an on-chip register. The ADC provides the conversion result, MSB first, from its internal shift register. The DATA format is determined by the logic level of OB/$\overline{\text{2C}}$. In Serial Mode, when EXT/$\overline{\text{INT}}$ is LOW, SDOUT is valid on both edges of SCLK. In Serial Mode, when EXT/$\overline{\text{INT}}$ is HIGH: If INVSCLK is LOW, SDOUT is updated on SCLK rising edge and valid on the next falling edge. If INVSCLK is HIGH, SDOUT is updated on SCLK falling edge and valid on the next rising edge.
H11	D[9] or SCLK	DI/O	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 9 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the Serial Port, is used as a serial data clock input or output, dependent upon the logic state of the EXT/$\overline{\text{INT}}$ pin. The active edge where the data SDOUT is updated depends upon the logic state of the INVSCLK pin.
G12	D[10] or SYNC	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 10 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, this input, part of the Serial Port, is used as a digital output frame synchronization for use with the internal data clock (EXT/$\overline{\text{INT}}$ = Logic LOW). When a read sequence is initiated and INVSYNC is LOW, SYNC is driven HIGH and remains HIGH while SDOUT output is valid. When a read sequence is initiated and INVSYNC is High, SYNC is driven LOW and remains LOW while SDOUT output is valid.
G11	D[11] or RDERROR	DO	When SER/$\overline{\text{PAR}}$ is LOW, this output is used as Bit 11 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH and EXT/$\overline{\text{INT}}$ is HIGH, this output, part of the Serial Port, is used as an incomplete read error flag. In Slave Mode, when a data read is started and not complete when the following conversion is complete, the current data is lost and RDERROR is pulsed high.
F12, F11, E12, E11	D[12:15]	DO	Bit 12 to Bit 15 of the Parallel Port Data Output Bus. When SER/$\overline{\text{PAR}}$ is HIGH, these outputs are in high impedance.
G10	BUSY	DO	Busy Output. Transitions HIGH when a conversion is started, and remains HIGH until the conversion is complete and the data is latched into the on-chip shift register. The falling edge of BUSY could be used as a data ready clock signal.
G9	DGND_ADC	P	Must be Tied to Digital Ground
E10	$\overline{\text{RD}}$	DI	Read Data. When $\overline{\text{CS\_ADC}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled.
K10	$\overline{\text{CS\_ADC}}$	DI	Chip Select. When $\overline{\text{CS\_ADC}}$ and $\overline{\text{RD}}$ are both LOW, the interface parallel or serial output bus is enabled. $\overline{\text{CS\_ADC}}$ is also used to gate the external serial clock.
D12	RESET	DI	Reset Input. When set to a logic HIGH, reset the ADC. Current conversion, if any, is aborted. If not used, this pin could be tied to DGND.
K9	PD	DI	Power-Down Input. When set to a logic HIGH, power consumption is reduced and conversions are inhibited after the current one is completed.
E7	$\overline{\text{CNVST}}$	DI	Start Conversion. A falling edge on $\overline{\text{CNVST}}$ puts the internal sample/hold into the hold state and initiates a conversion. In impulse mode (IMPULSE HIGH and WARP LOW), if $\overline{\text{CNVST}}$ is held low when the acquisition phase (t_8) is complete, the internal sample/hold is put into the hold state and a conversion is immediately started.
H8	AGND_ADC	P	Must be Tied to Analog Ground
G5	REF	AI	Reference Input Voltage
H5	REFGND	AI	Reference Input Analog Ground
J7	INGND	P	Analog Input Ground
J5, K5, L5, M5	INA, INB, INC, IND	AI	Analog Inputs. Refer to Table I for input range configuration.

DAC PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
A6	VOUT_DAC	AO	Analog Output Voltage from the DAC
A3, C3, C4	AGND_DAC	P	Ground Reference Point for Analog Circuitry
A2	VREF	AI	This is the voltage reference input for the DAC. Connect to external reference ranges from 2 V to VDD.
B1	$\overline{\text{CS\_DAC}}$	DI	This is an active low logic input signal. The chip select signal is used to frame the serial data input.
E1	SCLK	DI	Clock Input. Data is clocked into the input register on the rising edge of SCLK. Duty cycle must be between 40% and 60%.
E2	DIN	DI	Serial Data Input. This device accepts 14-bit words. Data is clocked into the input register on the rising edge of SCLK.
E3	DGND_DAC	P	Digital Ground. Ground reference for digital circuitry.
C6	VDD_DAC	P	Analog Supply Voltage, 5 V ± 10%

AMPLIFIER PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
C9 (J1)	+IN1(2)	AI	Positive Input Voltage
A9 (G1)	–IN1(2)	AI	Negative Input Voltage
B12 (K4)	VOUT1(2)	AO	Amplifier Output Voltage
A11 (F3)	+VS1(2)	P	Analog Positive Supply Voltage
B10, B11 (G3, H3)	–VS1(2)	P	Analog Negative Supply Voltage

RESISTOR PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
B9 (L4)	RA1(2)	AI/O	Resistor End Terminal
A8 (M4)	RB1(2)	AI/O	Resistor Center Tap
D9 (L1)	RC1(2)	AI/O	Resistor End Terminal
A7 (M3)	RPAD1(2)	P	Resistor Die Pad. Tie to Analog Ground.

COMMON PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
A1, A4, A5, A10, A12, B2–B8, C1, C2, C5, C7, C8, C10–C12, D1–D8, D10, D11, E4–E6, E8, E9, F1, F2, F4–F10, G2, G4, G6–G8, H1, H2, H4, H6, H7, J2–J4, J6, K1–K3, K6–K8, L2, L3, L6, M1, M2	COMMON	P	Common Floating Net Connecting 69 Pins. Not electrically connected within the module. Tie at least one of these pins to Analog Ground.

NOTES
AI = Analog Input
AI/O = Bidirectional Analog
AO = Analog Output
DI = Digital Input
DI/O = Bidirectional Digital
DO = Digital Output
P = Power

ADC DEFINITION OF SPECIFICATIONS

Integral Nonlinearity Error (INL)
Linearity error refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)
In an ideal ADC, code transitions are 1 LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

Full-Scale Error
The last transition (from 011...10 to 011...11 in twos complement coding) should occur for an analog voltage 1 1/2 LSB below the nominal full scale (2.499886 V for the ±2.5 V range). The full-scale error is the deviation of the actual level of the last transition from the ideal level.

Bipolar Zero Error
The difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

Unipolar Zero Error
In unipolar mode, the first transition should occur at a level 1/2 LSB above analog ground. The unipolar zero error is the deviation of the actual transition from that point.

Spurious Free Dynamic Range (SFDR)
The difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Effective Number of Bits (ENOB)
A measurement of the resolution with a sine wave input. It is related to S/(N + D) by the following formula:

$$ENOB = \left(\left(S / \left[N + D \right]_{dB} - 1.76 \right) / 6.02 \right)$$

and is expressed in bits.

Total Harmonic Distortion (THD)
The rms sum of the first five harmonic components to the rms value of a full-scale input signal; expressed in decibels.

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Signal-to-(Noise + Distortion) Ratio (S/[N + D])
The ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N + D) is expressed in decibels.

Aperture Delay
A measure of the acquisition performance, measured from the falling edge of the $\overline{\text{CNVST}}$ input to when the input signal is held for a conversion.

Transient Response
The time required for the ADC to achieve its rated accuracy after a full-scale step function is applied to its input.

DAC DEFINITION OF SPECIFICATIONS

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. A typical INL versus code plot can be seen in TPC 16.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. TPC 19 illustrates a typical DNL versus code plot.

Gain Error
Gain error is the difference between the actual and ideal analog output range, expressed as a percent of the full-scale range. It is the deviation in slope of the DAC transfer characteristic from ideal.

Gain Error Temperature Coefficient
This is a measure of the change in gain error with changes in temperature. It is expressed in ppm/°C.

Zero Code Error
Zero code error is a measure of the output error when zero code is loaded to the DAC register.

Zero Code Temperature Coefficient
This is a measure of the change in zero code error with a change in temperature. It is expressed in mV/°C.

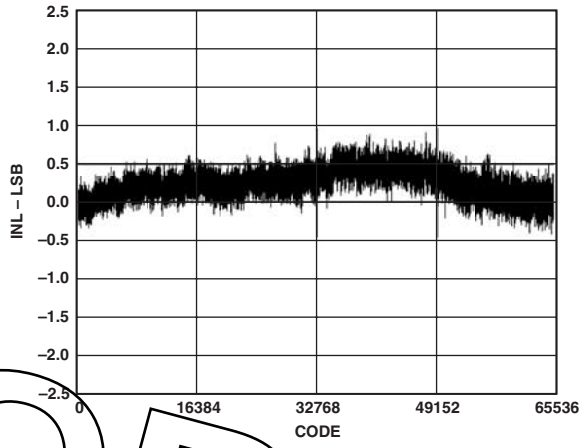
Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV–s and is measured when the digital input code is changed by 1 LSB at the major carry transition. A plot of the glitch impulse is shown in Figure 28.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. $\overline{\text{CS\_DAC}}$ is held high, while the CLK and DIN signals are toggled. It is specified in nV–s and is measured with a full-scale code change on the data bus, i.e., from all 0s to all 1s and vice versa. A typical plot of digital feedthrough is shown in Figure 27.

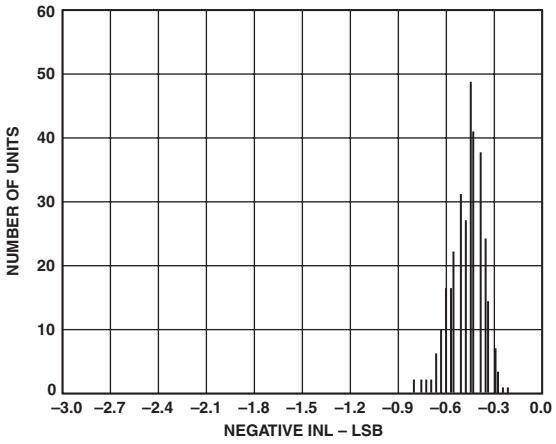
Power Supply Rejection Ratio
This specification indicates how the output of the DAC is affected by changes in the power supply voltage. Power supply rejection ratio is quoted in terms of percent change in output per percent change in V_{DD} for full-scale output of the DAC. V_{DD} is varied by ±10%.

Reference Feedthrough
This is a measure of the feedthrough from the V_{REF} input to the DAC output when the DAC is loaded with all 0s. A 100 kHz, 1 V p-p is applied to V_{REF}. Reference feedthrough is expressed in mV p-p.

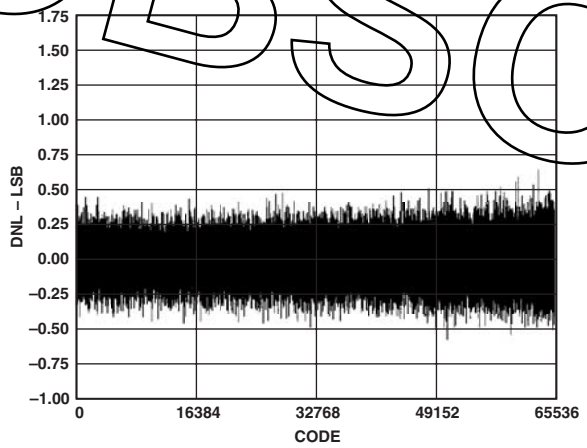
16-BIT D/A CONVERTER



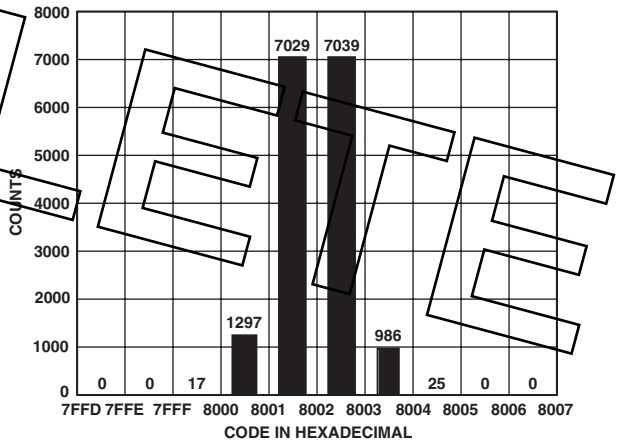
TPC 1. Integral Nonlinearity vs. Code



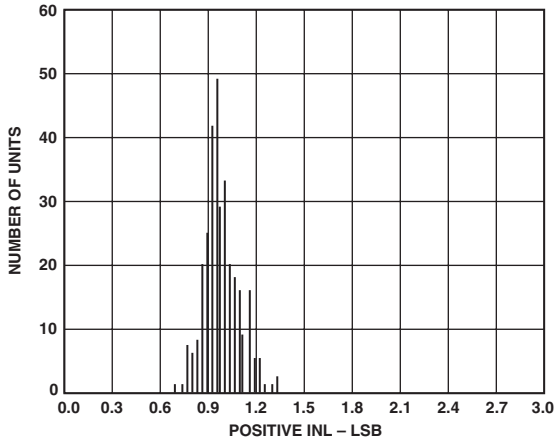
TPC 4. Typical Negative INL Distribution (314 Units)



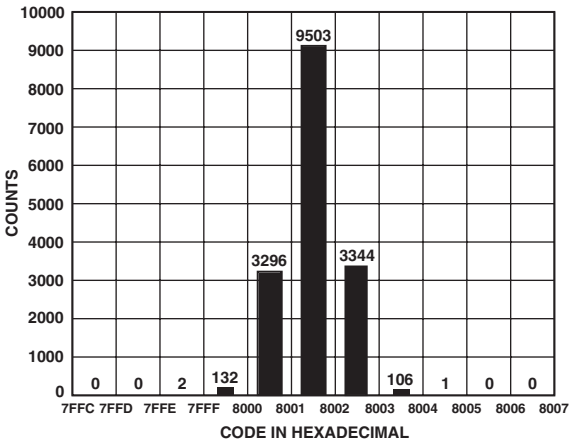
TPC 2. Differential Nonlinearity vs. Code



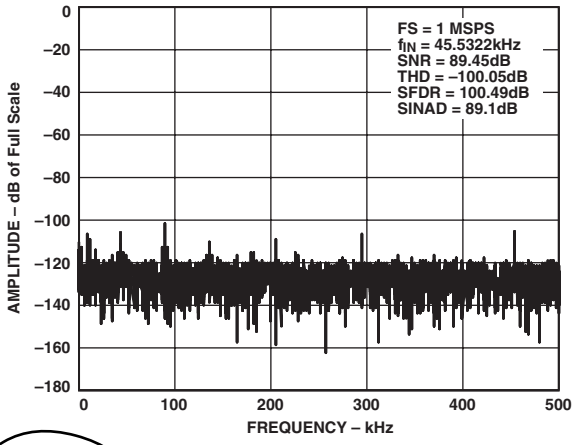
TPC 5. Histogram of 16,384 Conversions of a DC Input at the Code Transition



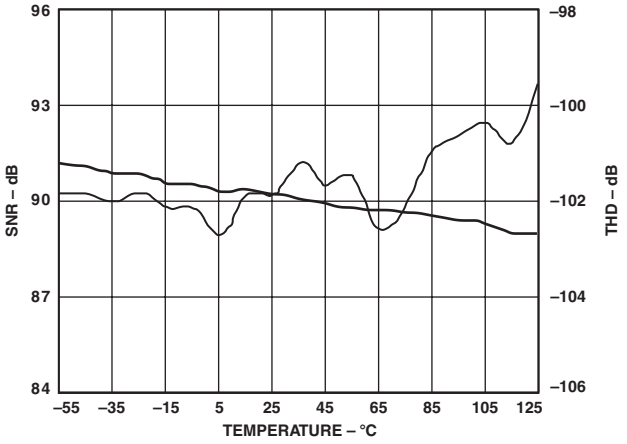
TPC 3. Typical Positive INL Distribution (314 Units)



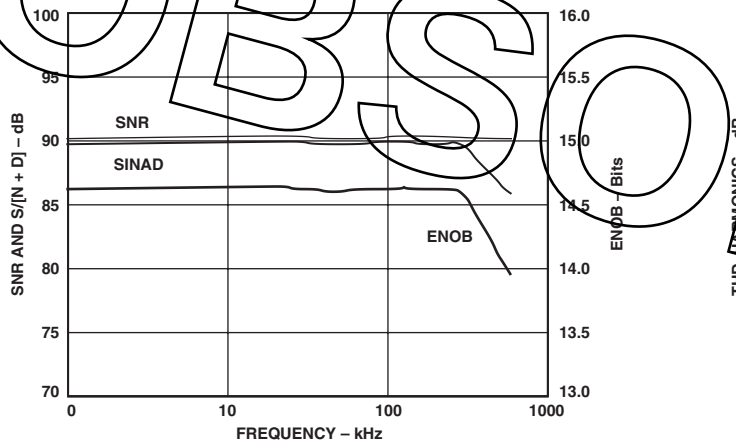
TPC 6. Histogram of 16,384 Conversions of a DC Input at the Code Center



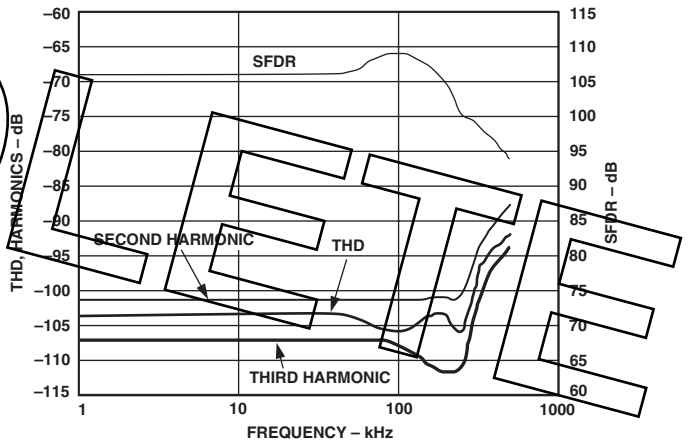
TPC 7. FFT Plot



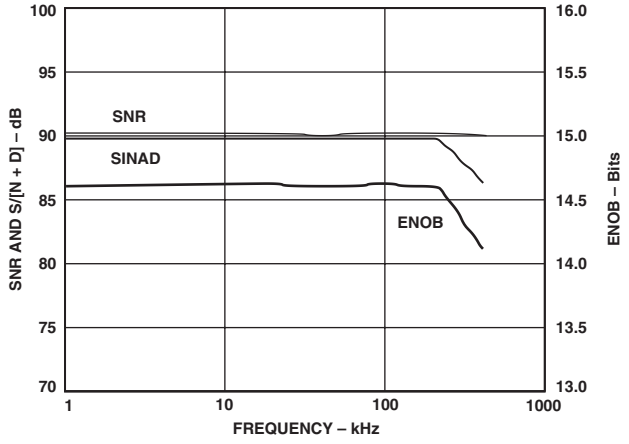
TPC 10. SNR, THD vs. Temperature



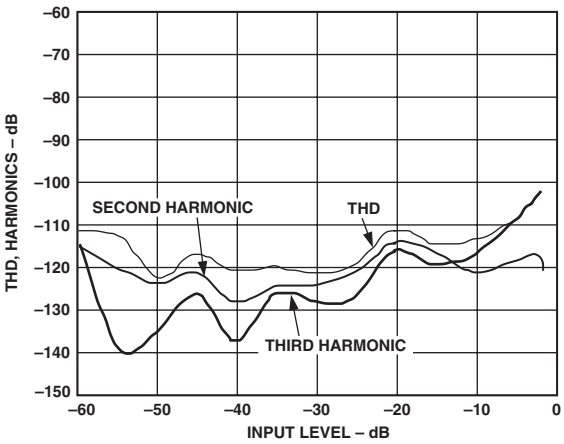
TPC 8. SNR, S/(N + D), and ENOB vs. Frequency



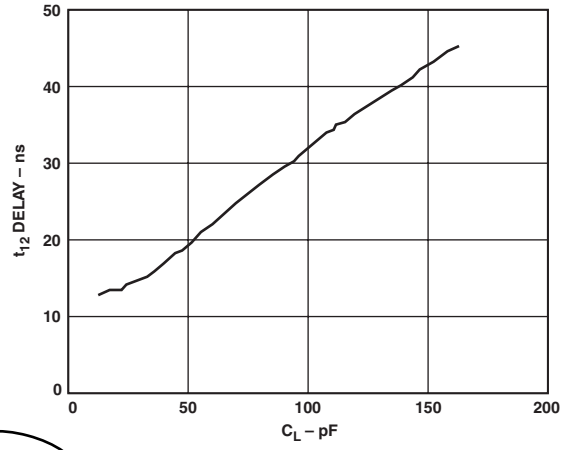
TPC 11. THD, Harmonics, and SFDR vs. Frequency



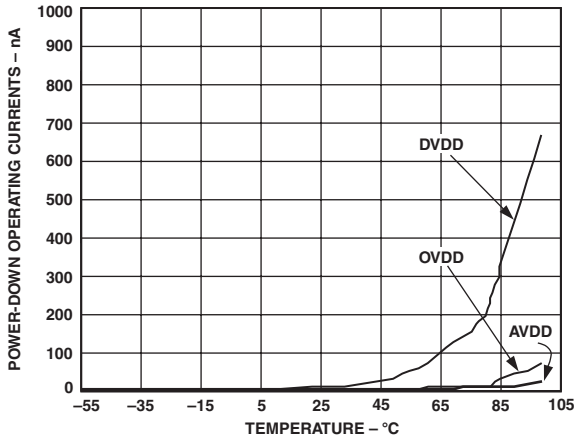
TPC 9. SNR vs. Input Frequency



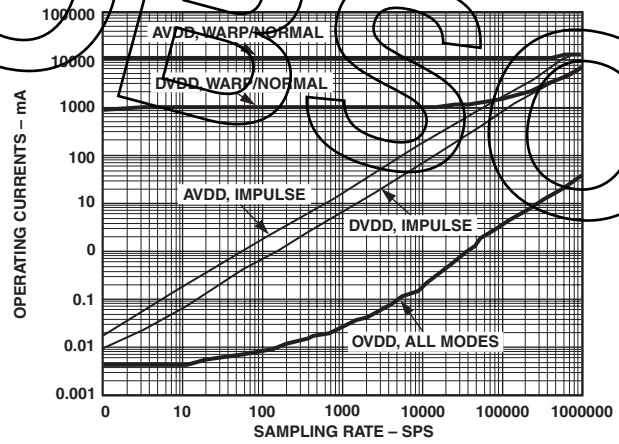
TPC 12. THD, Harmonics vs. Input Level



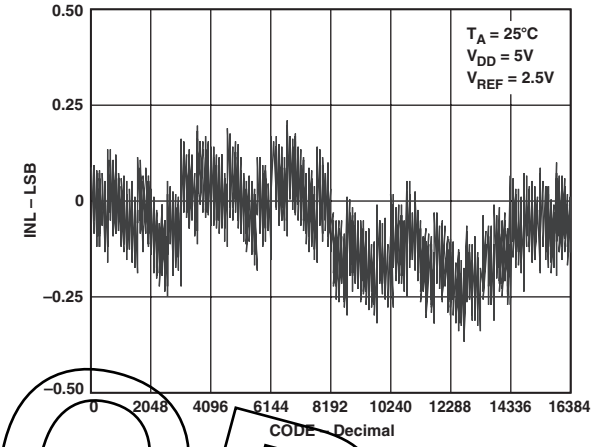
TPC 13. Typical Delay vs. Load Capacitance C_L



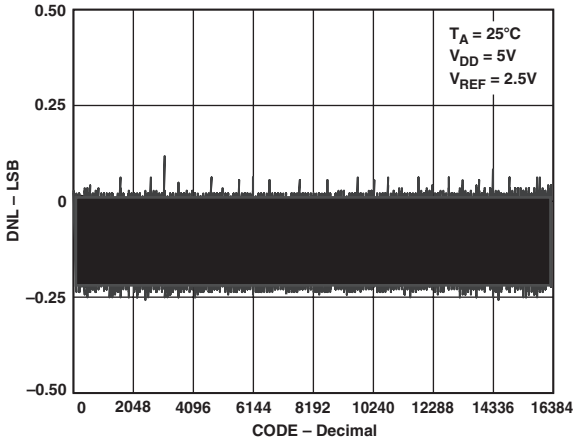
TPC 15. Power-Down Operating Currents vs. Temperature



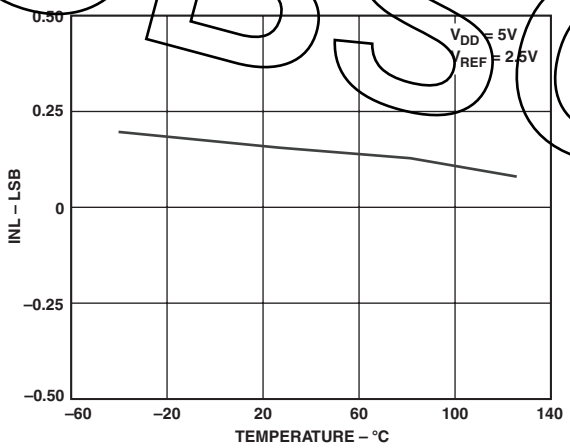
TPC 14. Operating Currents vs. Sample Rate



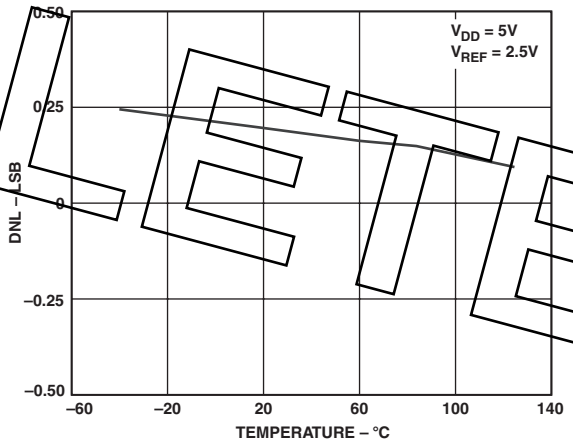
TPC 16. Integral Nonlinearity vs. Code



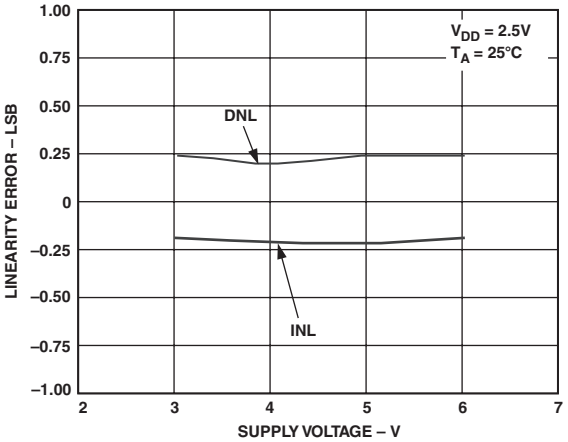
TPC 19. Differential Nonlinearity vs. Code



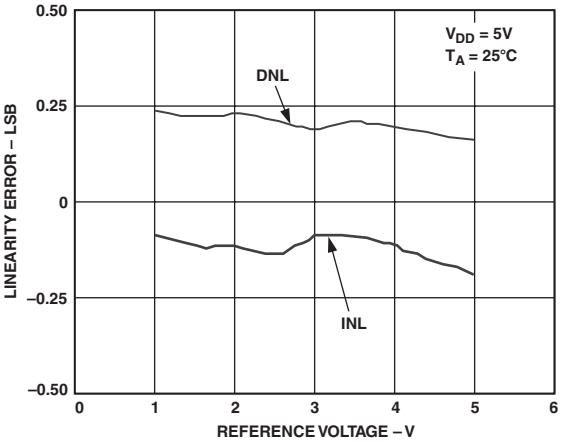
TPC 17. Integral Nonlinearity vs. Temperature



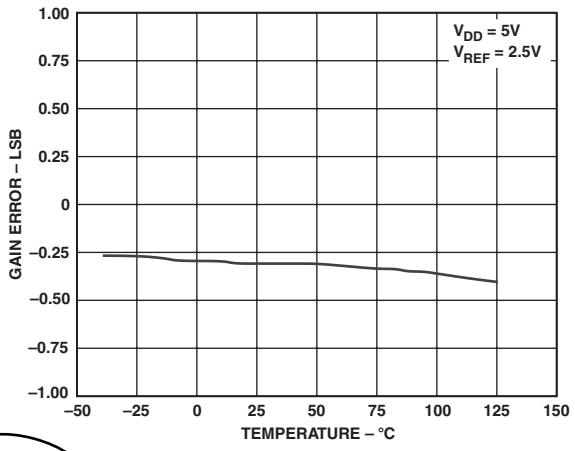
TPC 20. Differential Nonlinearity vs. Temperature



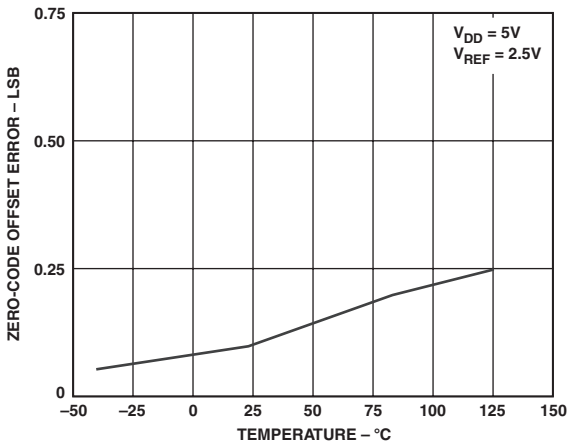
TPC 18. Linearity Error vs. Supply Voltage



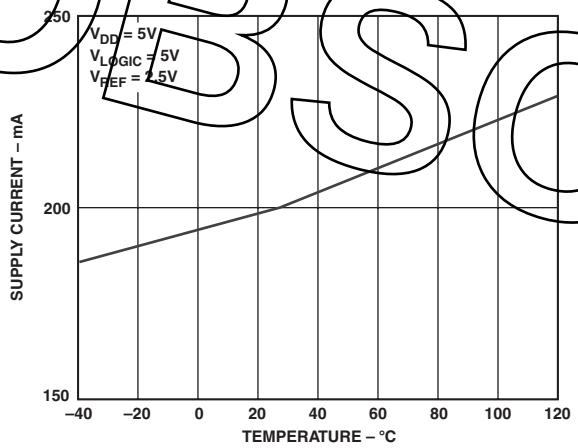
TPC 21. Linearity Error vs. Reference Voltage



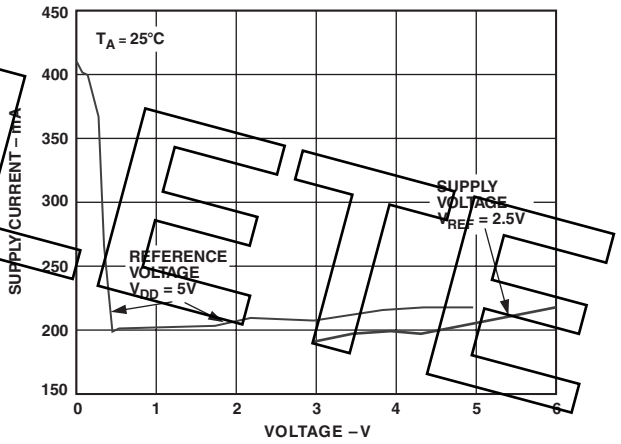
TPC 22. Gain Error vs. Temperature



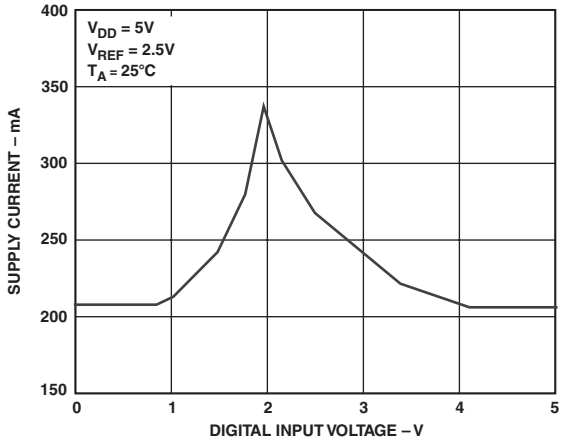
TPC 25. Zero-Code Error vs. Temperature



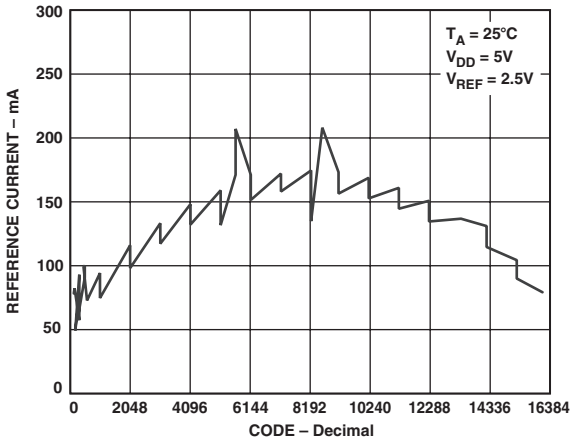
TPC 23. Supply Current vs. Temperature



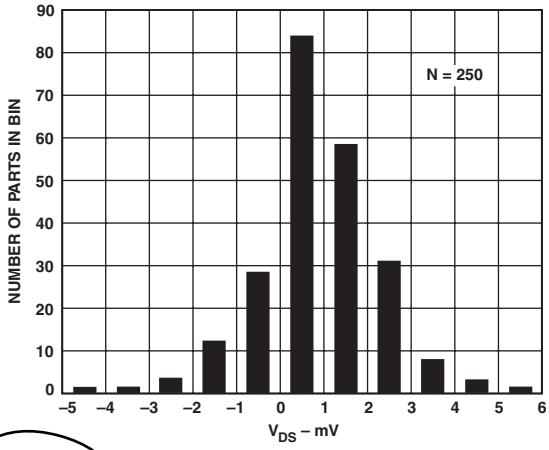
TPC 26. Supply Current vs. Reference Voltage or Supply Voltage



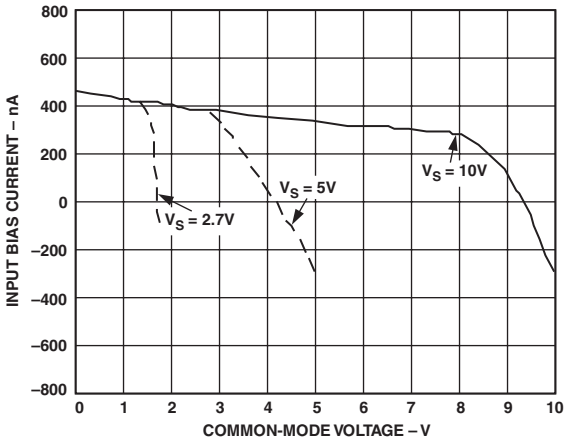
TPC 24. Supply Current vs. Digital Input Voltage



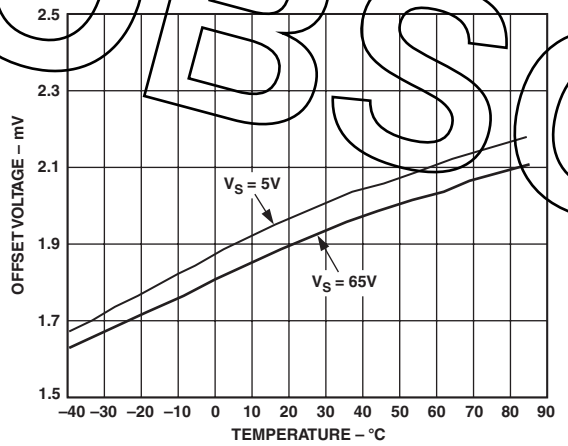
TPC 27. Reference Current vs. Code



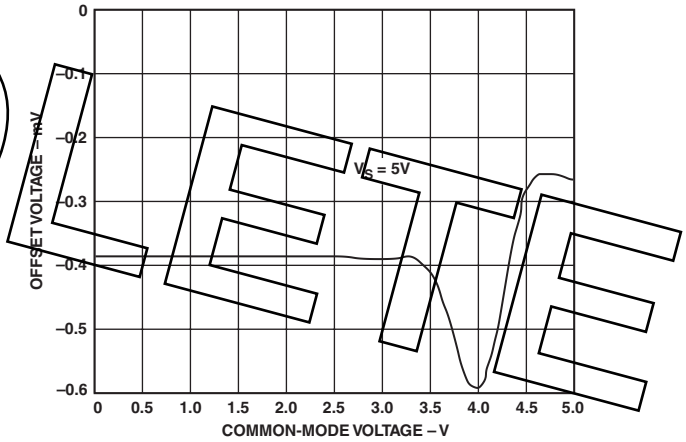
TPC 28. Typical V_{OS} Distribution @ V_S = 5 V



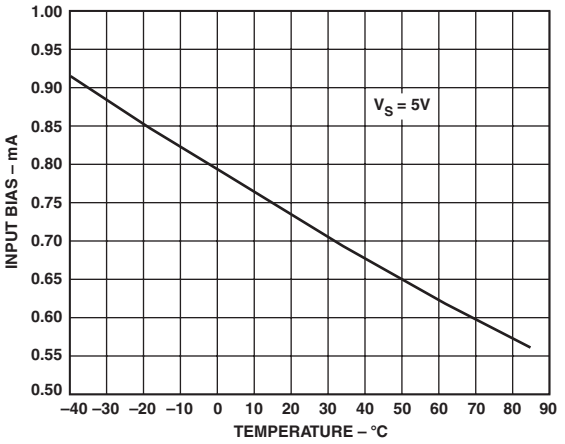
TPC 31. Input Bias Current vs. Common-Mode Voltage



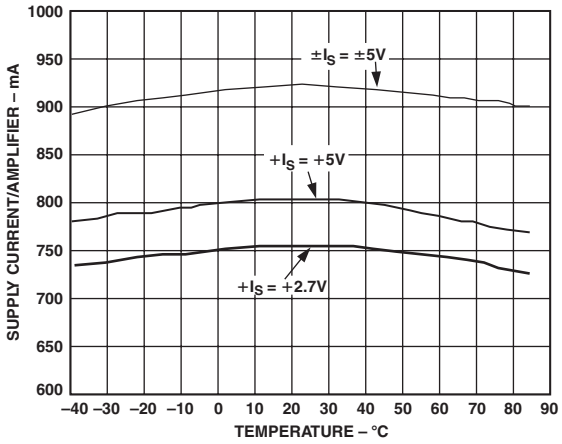
TPC 29. Input Offset Voltage vs. Temperature



TPC 32. V_{OS} vs. Common-Mode Voltage

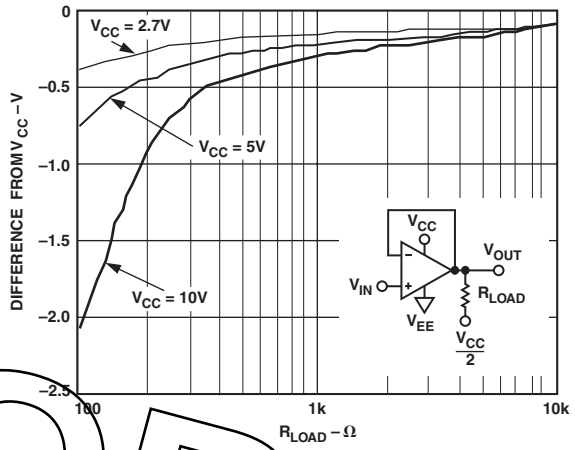


TPC 30. Input Bias Current vs. Temperature

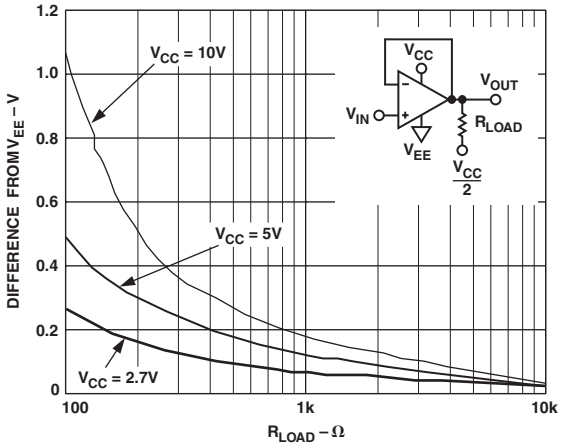


TPC 33. Supply Current vs. Temperature

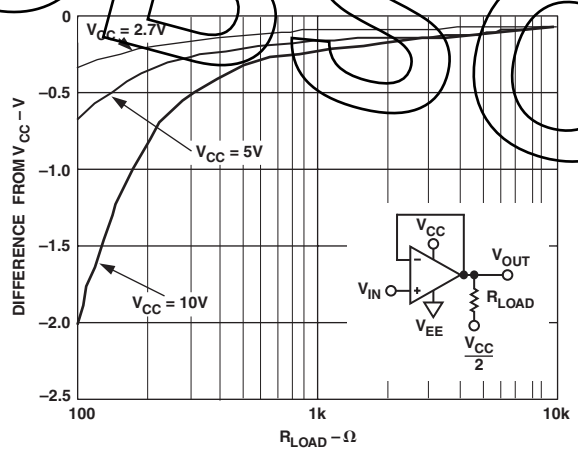
AMPLIFIER



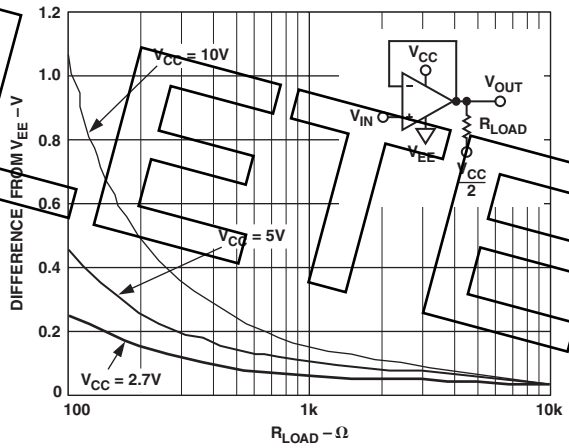
TPC 34. +Output Saturation Voltage vs. R_{LOAD} @ 85°C



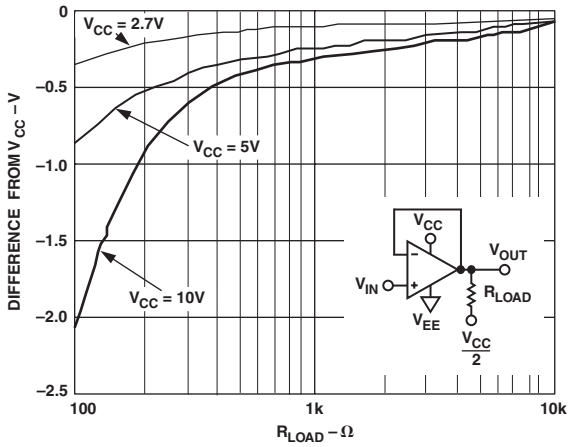
TPC 37. –Output Saturation Voltage vs. R_{LOAD} @ 85°C



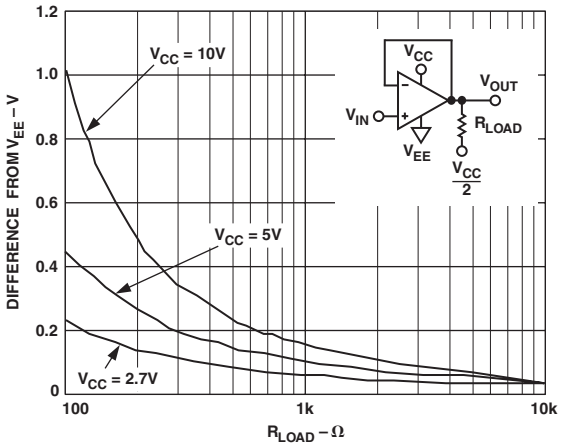
TPC 35. +Output Saturation Voltage vs. R_{LOAD} @ 25°C



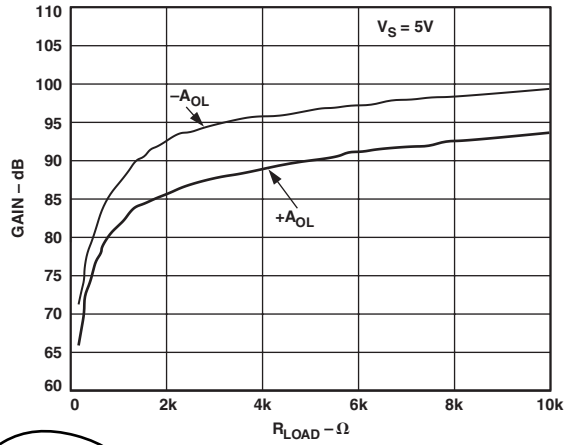
TPC 38. –Output Saturation Voltage vs. R_{LOAD} @ 25°C



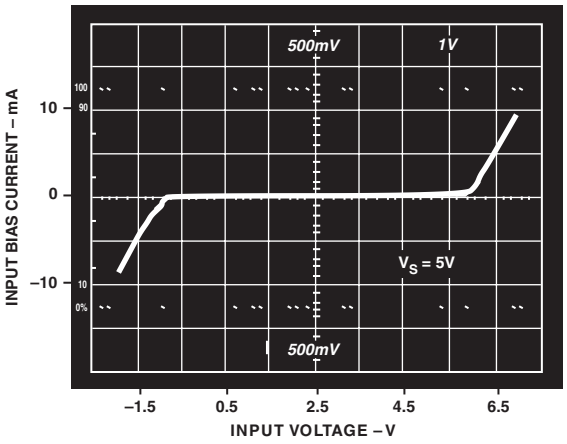
TPC. 36 +Output Saturation Voltage vs. R_{LOAD} @ –40°C



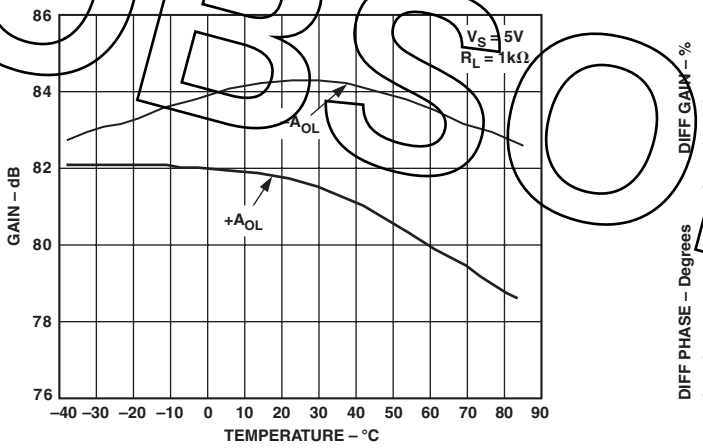
TPC. 39 –Output Saturation Voltage vs. R_{LOAD} @ –40°C



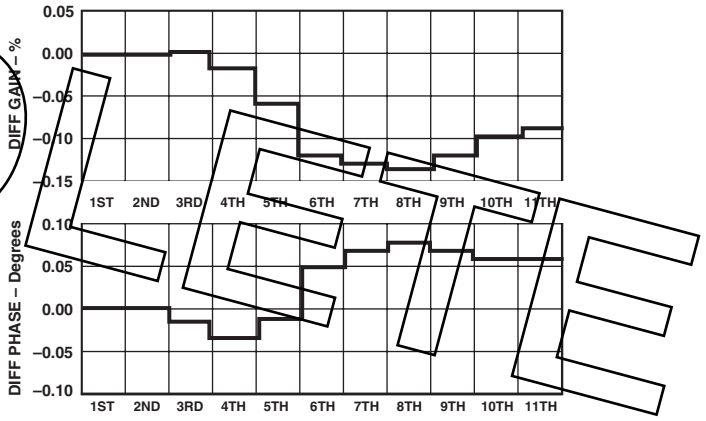
TPC 40. Open-Loop Gain (A_{OL}) vs. R_{LOAD}



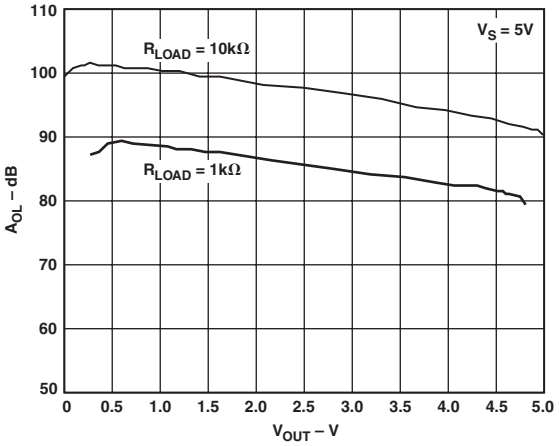
TPC 43. Differential Input Voltage 1 V Characteristics



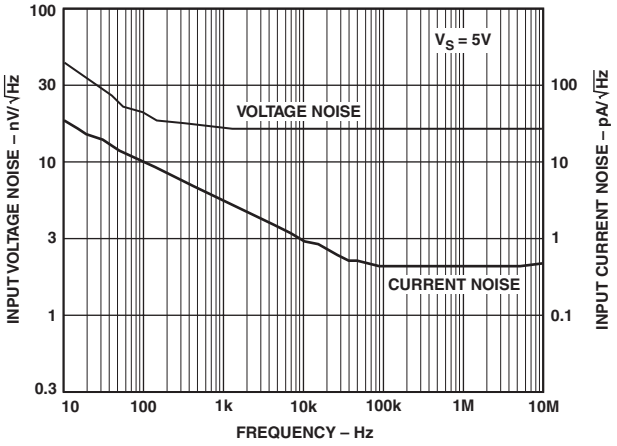
TPC 41. Open-Loop Gain (A_{OL}) vs. Temperature



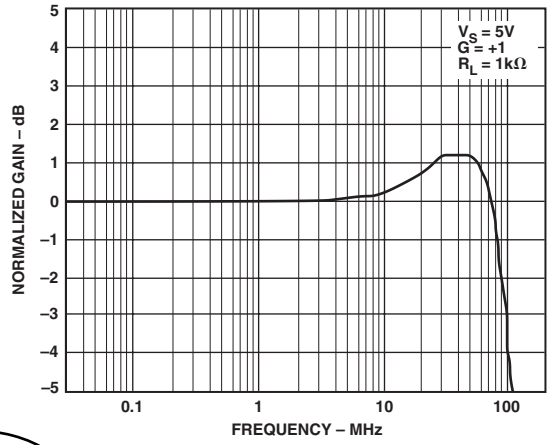
TPC 44. Differential Gain and Phase @ V_S = ±5 V; R_L = 1 kΩ



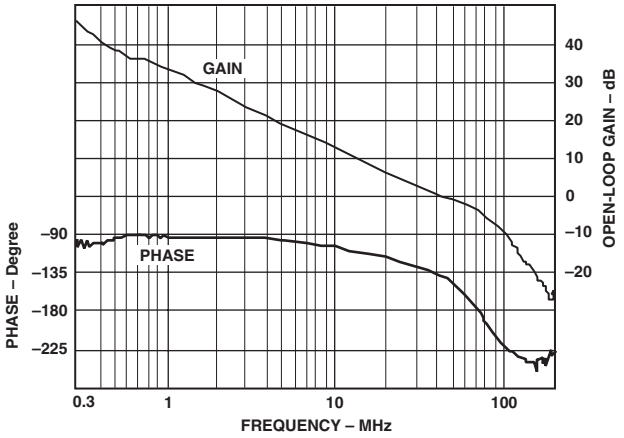
TPC 42. Open-Loop Gain (A_{OL}) vs. V_{OUT}



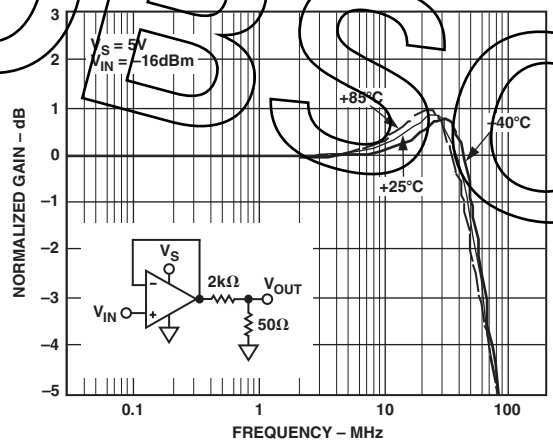
TPC 45. Input Voltage Noise vs. Frequency



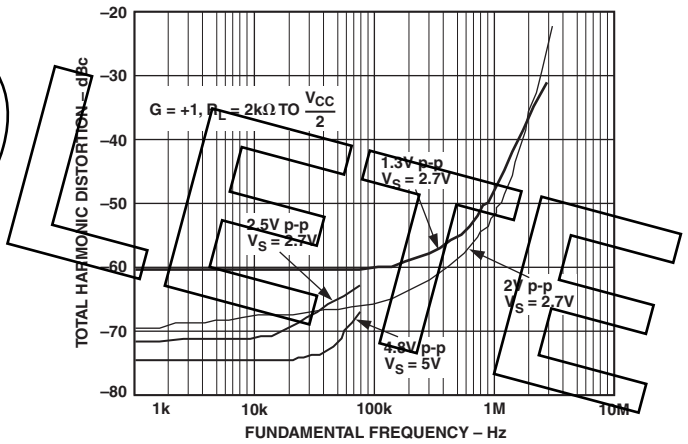
TPC 46. Unity Gain, –3 dB Bandwidth



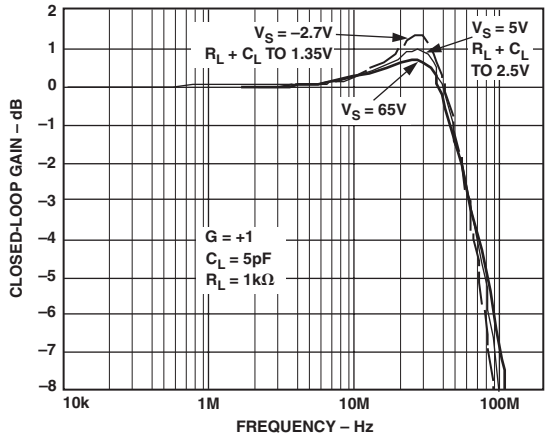
TPC 49. Open-Loop Frequency Response



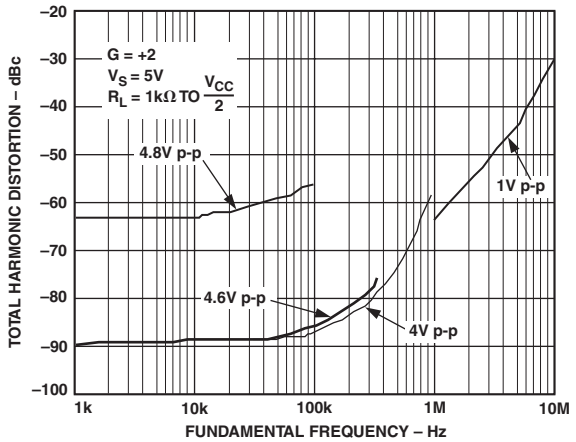
TPC 47. Closed-Loop Gain vs. Temperature



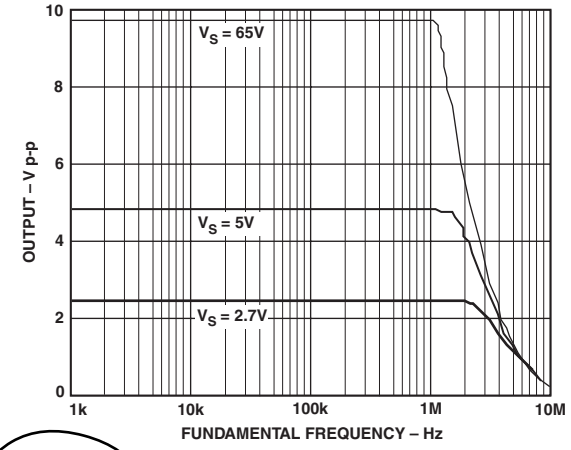
TPC 50. Total Harmonic Distortion vs. Frequency; G = +1



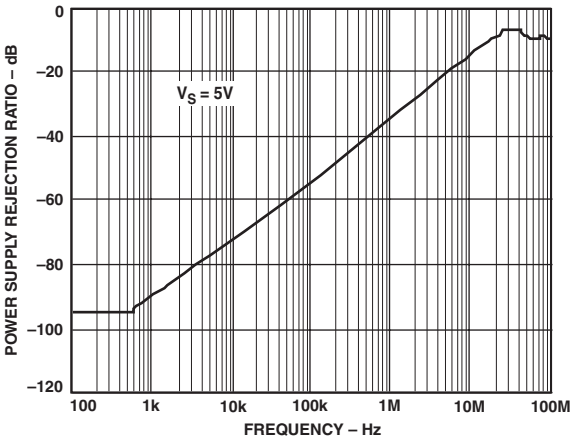
TPC 48. Closed-Loop Gain vs. Supply Voltage



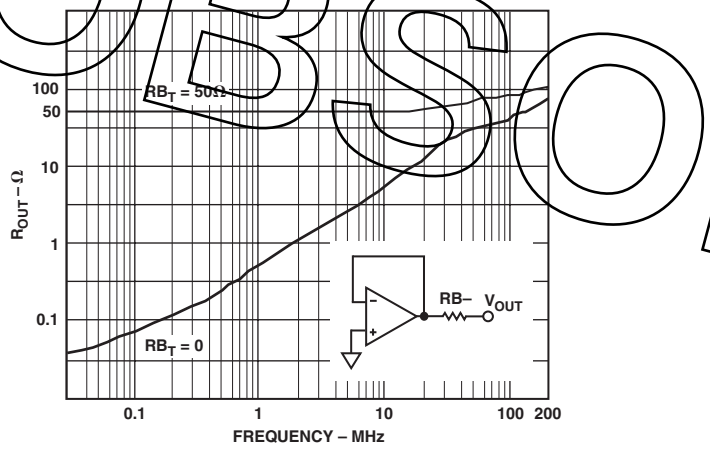
TPC 51. Total Harmonic Distortion vs. Frequency; G = +2



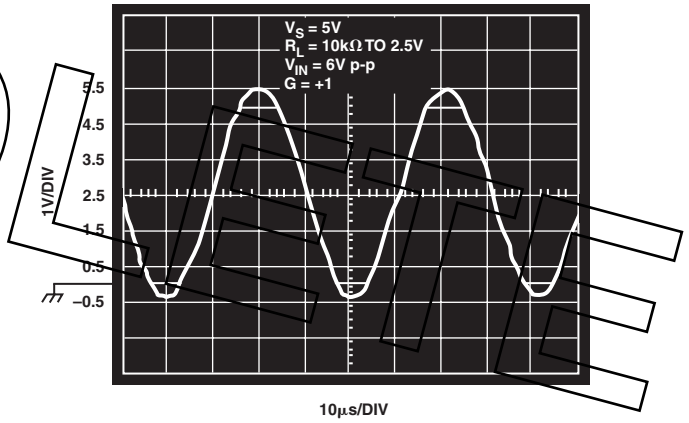
TPC 52. Large Signal Response



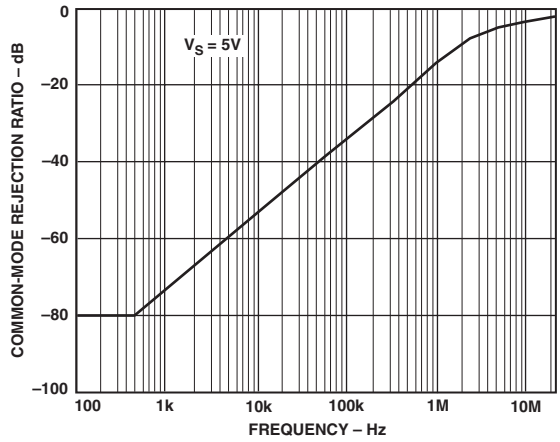
TPC 55. PSRR vs. Frequency



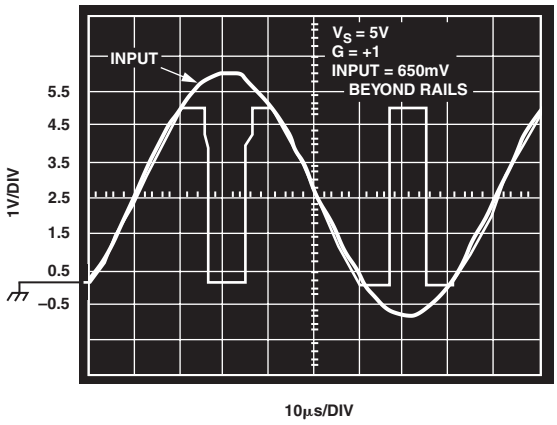
TPC 53. R_{OUT} vs. Frequency



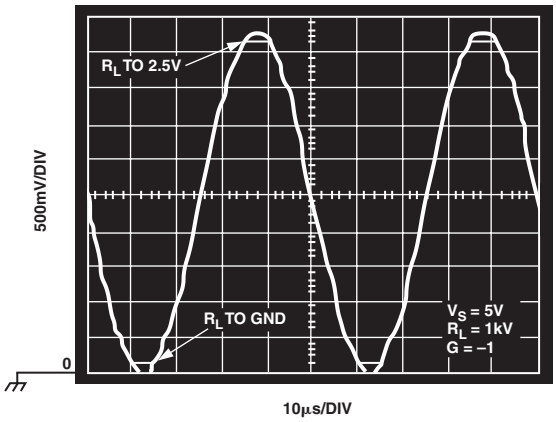
TPC 56. Output Voltage



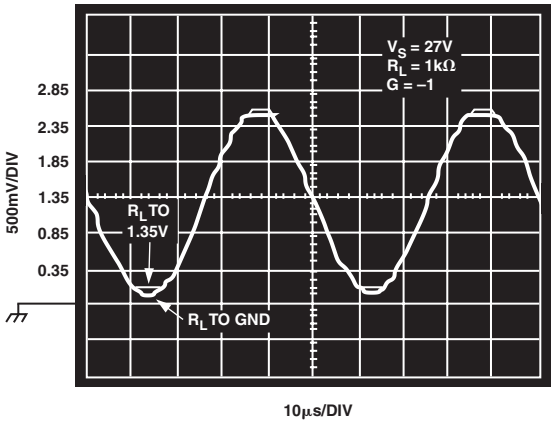
TPC 54. CMRR vs. Frequency



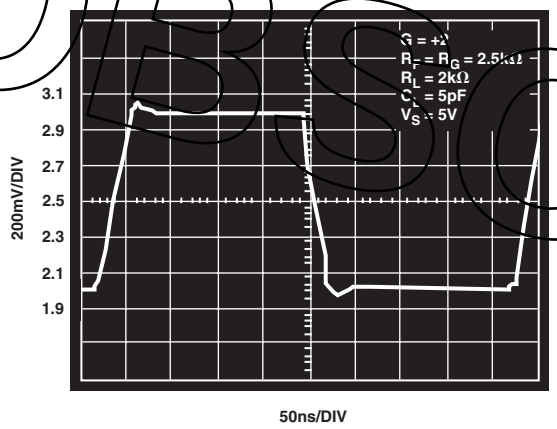
TPC 57. Output Voltage Phase Reversal Behavior



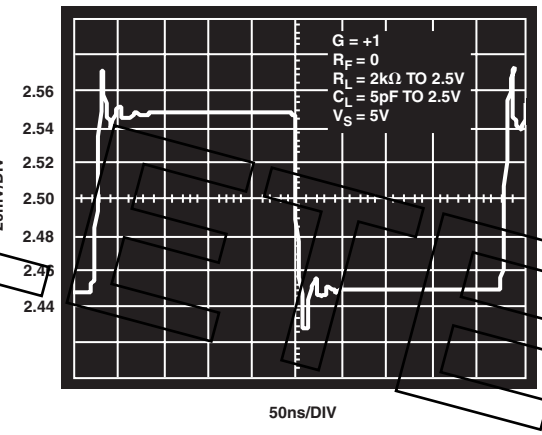
TPC 58. Output Swing



TPC 60. Output Swing



TPC 59. 1 V Step Response



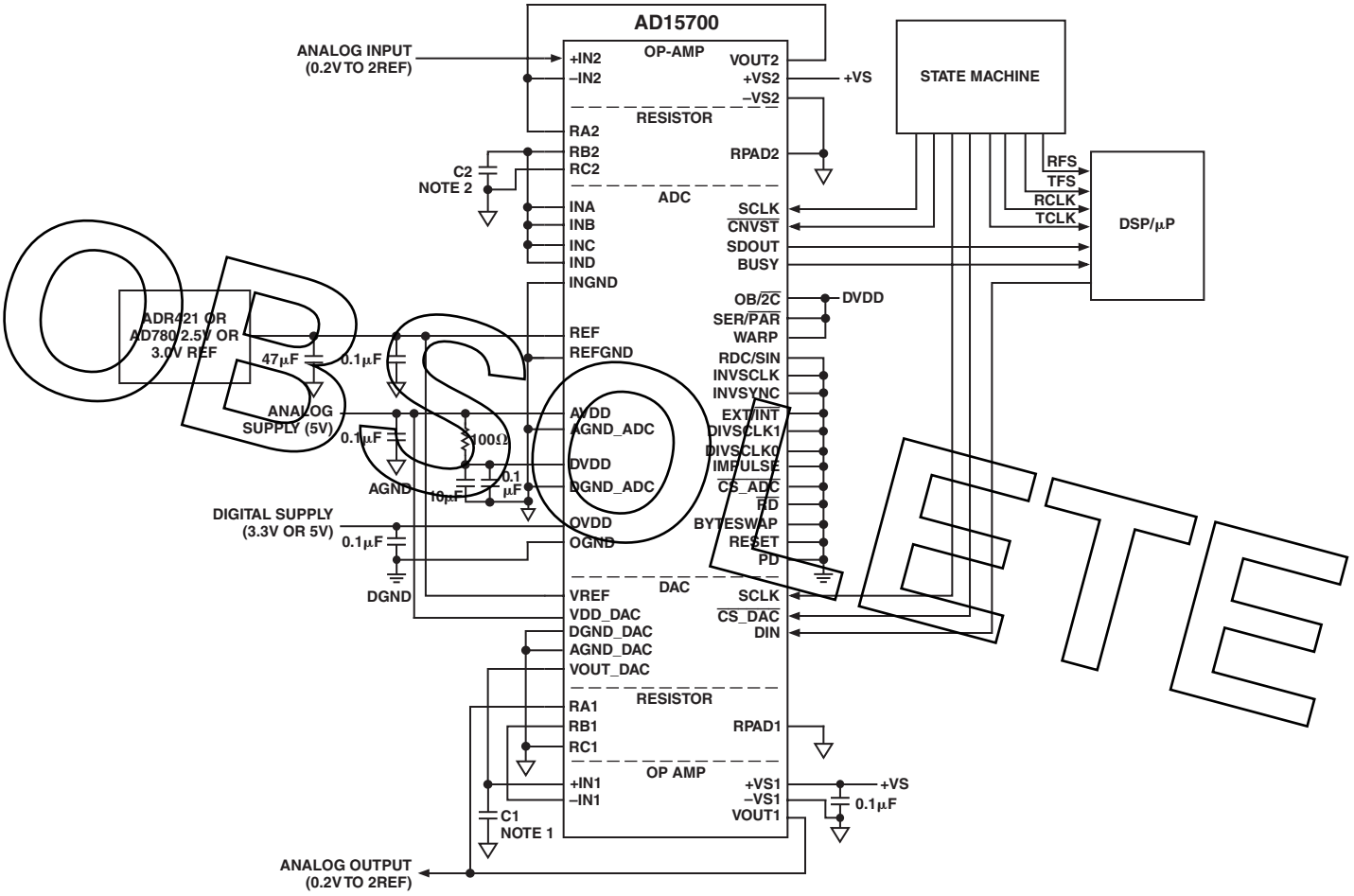
TPC 61. 100 mV Step Response

CIRCUIT OPERATION

The AD15700 contains precision components for interfacing analog I/O to a processor. Configuration for particular applications can be made with short external interconnects under the device.

TYPICAL CONNECTION DIAGRAM

Figure 4 shows how, using a minimum of external devices, the components within the AD15700 can be interconnected to form a complete analog interface to a processor. The circuit implements signal conditioning that includes buffering, filtering, and voltage scaling.



NOTES
1. C1 FORMS AN R-C FILTER WITH THE 6.25kΩ NOMINAL OUTPUT RESISTANCE OF THE DAC
2. C2 FORMS PART OF THE ADC INPUT FILTER. SEE ANALOG INPUT SECTION.

Figure 4. Typical Connection Diagram

Analog Input Section

Made up of a buffer amplifier, an RC filter, and an ADC, the analog input circuit allows measurement of voltages ranging from 0.2 V to 2 REF V. When placed in the 0 V to REF input range, the circuit has the configuration shown in Figure 5a.

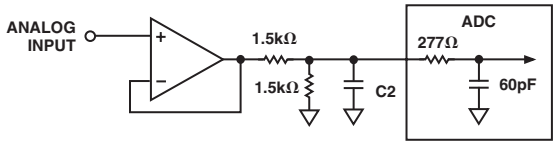


Figure 5a. Analog Input Circuit

The filter is made up of one of the AD15700's internal center-tapped resistors, an external capacitor *C2*, plus the ADC's internal resistance and capacitance. The transfer function of this filter is given by:

$$H(s) = \frac{8.11425\times10^{6}}{1.62285\times10^{7} + 202.288\,sC2 + s + 1.21714\times10^{10}\,sC2}$$

With C2 set to 100 pF, the bandwidth is 1.2 MHz. Without C2, the bandwidth of the filter is 2.6 MHz. To utilize the ADC's maximum 9.6 MHz bandwidth, the components external to the ADC are eliminated. In this case, the ADC is configured for its 0 to 2 REF input range and the resulting equivalent input circuit is shown in Figure 5b.

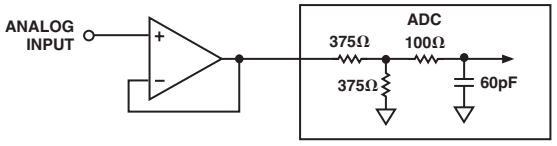


Figure 5b. Analog Input Circuit

Analog Output Section

The output circuitry consists of a DAC, RC filter, and an amplifier. The circuit uses the DAC's output resistance of 6.25 kΩ ± 20% to form a single-pole RC filter with an external capacitor C1. One of the AD15700's internal center-tapped resistors and one of its op amps form an amplifier with a gain of two. The gain is used to bring the DAC's maximum range of REF volts up to 2 REF V.

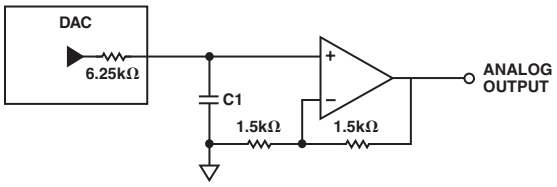


Figure 6. Analog Output Circuit

Voltage Reference Input

The AD15700 uses an external 2.5 V or 3.0 V voltage reference. Because of the dynamic input impedance of the A/D and the code dependent impedance of the D/A, the reference inputs must be driven by a low impedance source. Decoupling consisting of a parallel combination of 47 µF and 0.1 µF capacitors is recommended. Suitable references include the ADR421 for 2.5 V output and the AD780 for selectable 2.5 V or 3.0 V output. Both of these feature low noise and low temperature drift.

Processor Interface

The circuit in Figure 5a uses serial interfacing to minimize the number of signals that connect to the digital circuits. External logic such as a state machine is used to generate clocks and other timing signals for the interface. Ideally, the clocks supplied to the converters are discontinuous and operate at the maximum frequency supported by the converter and the processor. Discontinuous clocks that are quiet during critical times minimize degradation caused by voltage transients on the digital interface. It is best to keep the clocks quiet during ADC conversion and when the DAC output is sampled by the external system. Often, the processor cannot tolerate a discontinuous clock and therefore a separate continuous clock (or clocks) that is synchronous with the converter clocks must be generated. Separate clocks for the DAC and ADC are used to maximize the data transfer rate to each converter. The ADC operates at a maximum rate of 40 MHz while the DAC can operate up to 25 MHz.

ADC CIRCUIT INFORMATION

The ADC is a fast, low power, single-supply precise 16-bit analog-to-digital converter (ADC). It features different modes to optimize performances according to the applications.

In warp mode, it is capable of converting 1,000,000 samples per second (1 MSPS).

The ADC provides the user with an on-chip track/hold, successive approximation ADC that does not exhibit any pipeline or latency, making it ideal for multiple multiplexed channel applications.

It is specified to operate with both bipolar and unipolar input ranges by changing the connection of its input resistive scaler.

The ADC can be operated from a single 5 V supply and be interfaced to either 5 V or 3 V digital logic.

ADC CONVERTER OPERATION

The ADC is a successive approximation analog-to-digital converter based on a charge redistribution DAC. Figure 7 shows the simplified schematic of the ADC. The input analog signal is first scaled down and level-shifted by the internal input resistive scaler, which allows both unipolar ranges (0 V to 2.5 V, 0 V to 5 V, and 0 to 10 V) and bipolar ranges (±2.5 V, ±5 V, and ±10 V). The output voltage range of the resistive scaler is always 0 V to 2.5 V. The capacitive DAC consists of an array of 16 binary weighted capacitors and an additional LSB capacitor. The comparator's negative input is connected to a "dummy" capacitor of the same value as the capacitive DAC array.

During the acquisition phase, the common terminal of the array tied to the comparator's positive input is connected to AGND via SWA. All independent switches are connected to the output of the resistive scaler. Thus, the capacitor array is used as a sampling capacitor and acquires the analog signal. Similarly, the dummy capacitor acquires the analog signal on INGND input.

When the acquisition phase is complete, and the $\overline{\text{CNVST}}$ input goes or is low, a conversion phase is initiated. When the conversion phase begins, SWA and SWB are opened first. The capacitor array and the dummy capacitor are then disconnected from the inputs and connected to the REFGND input. Therefore, the differential voltage between the output of the resistive scaler and INGND captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced.

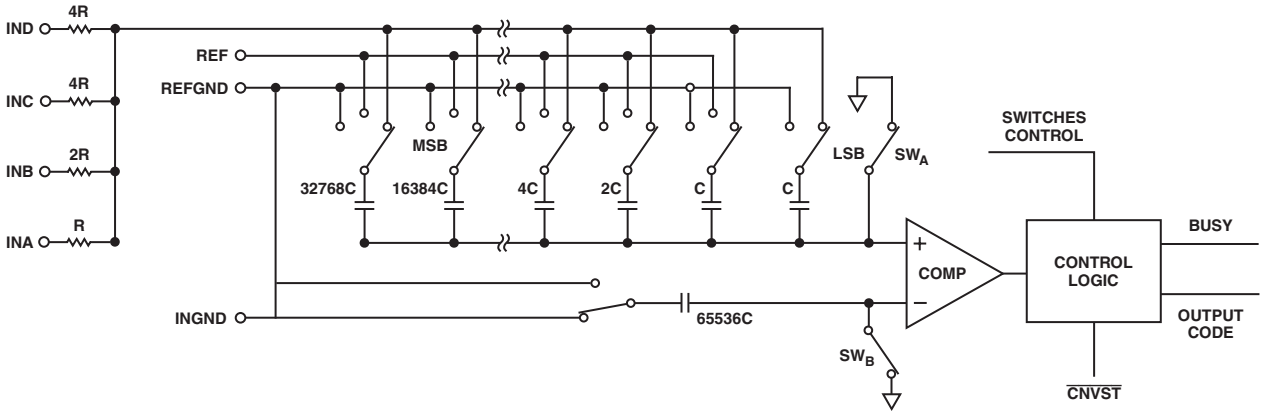


Figure 7. ADC Simplified Schematic

By switching each element of the capacitor array between REFGND or REF, the comparator input varies by binary weighted voltage steps (VREF/2, VREF/4. . .VREF/65536). The control logic toggles these switches, starting with the MSB first, in order to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and brings BUSY output low.

Modes of Operation

The ADC features three modes of operation: warp, normal, and impulse. Each of these modes is more suitable for specific applications.

The warp mode allows the fastest conversion rate up to 1 MSPS. However, in this mode and this mode only, the full specified accuracy is guaranteed only when the time between conversion does not exceed 1 ms. If the time between two consecutive conversions is longer than 1 ms, for instance, after power-up, the first conversion result should be ignored. This mode makes the ADC ideal for applications where both high accuracy and fast sample rate are required.

The normal mode is the fastest mode (800 kSPS) without any limitation about the time between conversions. This mode makes the ADC ideal for asynchronous applications such as data acquisition systems, where both high accuracy and fast sample rate are required.

The impulse mode, the lowest power dissipation mode, allows power saving between conversions. The maximum throughput in this mode is 666 kSPS. When operating at 100 SPS, for example, it typically consumes only 15 µW. This feature makes the ADC ideal for battery-powered applications.

Transfer Functions

Using the OB/2C digital input, the ADC offers two output codings: straight binary and twos complement. The ideal transfer characteristic for the ADC is shown in Figure 8 and Table III.

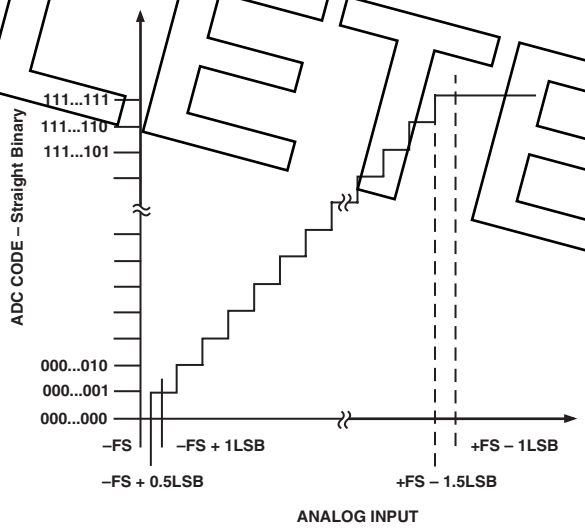


Figure 8. ADC Ideal Transfer Function

Table III. Output Codes and Ideal Input Voltages

Description	Analog Input						Digital Output Code (Hexadecimal)	
							Straight Binary	Twos Complement
Full-Scale Range	±10 V	±5 V	±2.5 V	0 V to 10 V	0 V to 5 V	0 V to 2.5 V		
Least Significant Bit	305.2 µV	152.6 µV	76.3 µV	152.6 µV	76.3 µV	38.15 µV		
FSR –1 LSB	9.999695 V	4.999847 V	2.499924 V	9.999847 V	4.999924 V	2.499962 V	FFFF[1]	7FFF[1]
Midscale +1 LSB	305.2 µV	152.6 µV	76.3 µV	5.000153 V	2.570076 V	1.257038 V	8001	0001
Midscale	0 V	0 V	0 V	5 V	2.5 V	1.25 V	8000	0000
Midscale –1 LSB	–305.2 µV	–152.6 µV	–76.3 µV	4.999847 V	2.499924 V	1.249962 V	7FFF	FFFF
–FSR +1 LSB	–9.999695 V	–4.999847 V	–2.499924 V	152.6 µV	76.3 µV	38.15 µV	0001	8001
–FSR	–10 V	–5 V	–2.5 V	0 V	0 V	0 V	0000[2]	8000[2]

NOTES
[1]This is also the code for an overrange analog input.
[2]This is also the code for an underrange analog input.

Analog Inputs

The ADC is specified to operate with six full-scale analog input ranges. Connections required for each of the four analog inputs, IND, INC, INB, INA, and the resulting full-scale ranges are shown in Table I. The typical input impedance for each analog input range is also shown.

Figure 9 shows a simplified analog input section of the ADC.

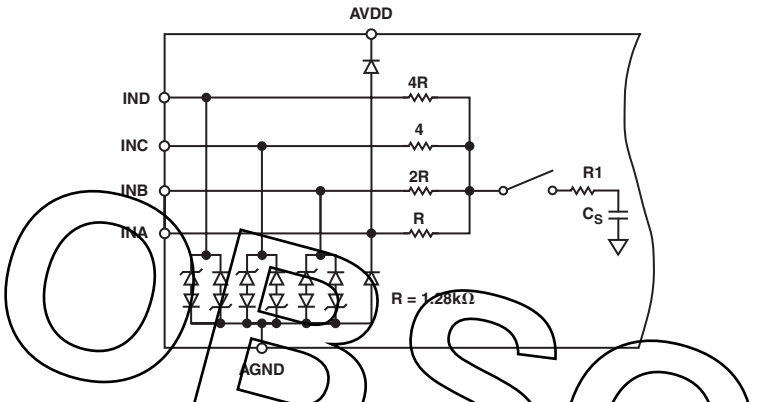


Figure 9. Simplified Analog Input

The four resistors connected to the four analog inputs form a resistive scaler that scales down and shifts the analog input range to a common input range of 0 V to 2.5 V at the input of the switched capacitive ADC.

By connecting the four inputs INA, INB, INC, and IND to the input signal itself, the ground, or a 2.5 V reference, other analog input ranges can be obtained.

The diodes shown in Figure 9 provide ESD protection for the four analog inputs. The inputs INB, INC, and IND, have a high voltage protection (–11 V to +30 V) to allow wide input voltage range. Care must be taken to ensure that the analog input signal never exceeds the absolute ratings on these inputs including INA (0 V to 5 V). This will cause these diodes to become forward-biased and start conducting current. These diodes can handle a forward-biased current of 120 mA maximum. For instance, when using the 0 V to 2.5 V input range, these conditions could eventually occur on the input INA when the input buffer's (U1) supplies are different from AVDD. In such case, an input buffer with a short circuit current limitation can be used to protect the part.

This analog input structure allows the sampling of the differential signal between the output of the resistive scaler and INGND. Unlike other converters, the INGND input is sampled at the same time as the inputs. By using this differential input, small signals common to both inputs are rejected as shown in Figure 10, which represents the typical CMRR over frequency. For instance, by using INGND to sense a remote signal ground, differences of ground potentials between the sensor and the local ADC ground are eliminated. During the acquisition phase for ac signals, the ADC behaves like a one-pole RC filter consisting of the equivalent resistance of the resistive scaler R/2 in series with R1 and C_S. The resistor R1 is typically 100 Ω and is a lumped component made up of some serial resistor and the on resistance of the switches.

The capacitor C_S is typically 60 pF and is mainly the ADC sampling capacitor. This one-pole filter with a typical –3 dB cutoff frequency of 9.6 MHz reduces undesirable aliasing effects and limits the noise coming from the inputs.

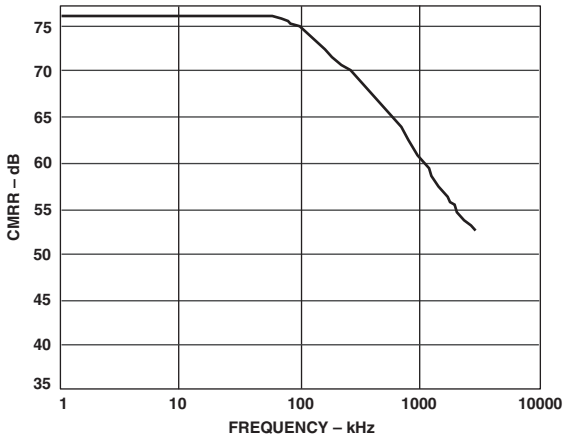


Figure 10. Analog Input CMRR vs. Frequency

Except when using the 0 V to 2.5 V analog input voltage range, the ADC has to be driven by a very low impedance source to avoid gain errors. That can be done by using the driver amplifier.

When using the 0 V to 2.5 V analog input voltage range, the input impedance of the ADC is very high so the ADC can be driven directly by a low impedance source without gain error. That allows putting an external one-pole RC filter between the output of the amplifier output and the ADC analog inputs to even further improve the noise filtering done by the ADC analog input circuit. However, the source impedance has to be kept low because it affects the ac performances, especially the total harmonic distortion (THD). The maximum source impedance depends on the amount of total THD that can be tolerated. The THD degradation is a function of the source impedance and the maximum input frequency, as shown in Figure 11.

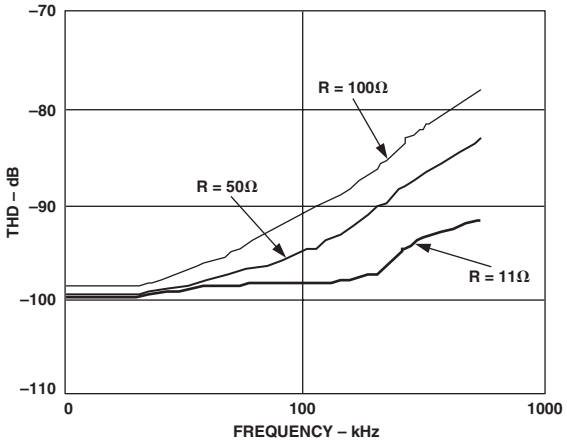


Figure 11. THD vs. Analog Input Frequency and Input Resistance (0 V to 2.5 V Only)

Driver Amplifier Choice

Although the ADC is easy to drive, the driver amplifier needs to meet at least the following requirements:

- The driver amplifier and the ADC analog input circuit must be able, together, to settle for a full-scale step of the capacitor array at a 16-bit level (0.0015%).
- The noise generated by the driver amplifier needs to be kept as low as possible in order to preserve the SNR and transition noise performance of the ADC. The noise coming from the driver is first scaled down by the resistive scaler according to the analog input voltage range used, and is then filtered by the ADC analog input circuit one-pole, low-pass filter made by (R/2 + R1) and CS. The SNR degradation due to the amplifier is:

$$SNR_{LOSS} = \log\left(\frac{28}{\sqrt{784 + \frac{\pi}{2} f_{-3\,dB}\left(\frac{2.5\,N\,e_N}{FSR}\right)^2}}\right)$$

where:

$f_{-3\,dB}$ is the –3 dB input bandwidth in MHz of the ADC (9.6 MHz) or the cutoff frequency of the input filter if any is used (0 V to 2.5 V range).

N is the noise factor of the amplifier (1 if in buffer configuration).

e_N is the equivalent input noise voltage of the op amp in nV/√Hz.

FSR is the full-scale span (i.e., 5 V for ±2.5 V range).

For instance, when using the 0 V to 5 V range, a driver like the AD15700's internal op amp, with an equivalent input noise of 15 nV/√Hz and configured as a buffer, followed by a 3.2 MHz RC filter, the SNR degrades by about 1.3 dB.

- The driver needs to have a THD performance suitable to that of the ADC. Figure 11 gives the THD versus frequency that the driver should preferably exceed.

Voltage Reference Input

The ADC uses an external 2.5 V voltage reference. The voltage reference input REF of the ADC has a dynamic input impedance. Therefore, it should be driven by a low impedance source with an efficient decoupling between REF and REFGND inputs. This decoupling depends on the choice of the voltage reference, but usually consists of a low ESR tantalum capacitor connected to the REF and REFGND inputs with minimum parasitic inductance. 47 µF is an appropriate value for the tantalum capacitor when used with one of the recommended reference voltages:

- The low noise, low temperature drift ADR421 or AD780 voltage references
- The low power ADR291 voltage reference
- The low cost AD1582 voltage reference

Care should also be taken with the reference temperature coefficient of the voltage reference, which directly affects the full-scale accuracy if this parameter matters. For instance, a ±15 ppm/°C tempco of the reference changes the full scale by ±1 LSB/°C.

Scaler Reference Input (Bipolar Input Ranges)

When using the ADC with bipolar input ranges, a buffer amplifier is required to isolate the REFIN pin from the signal dependent current in the AIN pin. A high speed op amp can be used with a single 5 V power supply without degrading the performance of the ADC. The buffer must have good settling characteristics and provide low total noise within the input bandwidth of the ADC.

Power Supply

The ADC uses three sets of power supply pins: an analog 5 V supply AVDD, a digital 5 V core supply DVDD, and a digital input/output interface supply OVDD. The OVDD supply allows direct interface with any logic working between 2.7 V and 5.25 V. To reduce the number of supplies needed, the digital core (DVDD) can be supplied through a simple RC filter from the analog supply. The ADC is independent of power supply sequencing and thus free from supply voltage induced latchup. Additionally, it is very insensitive to power supply variations over a wide frequency range, as shown in Figure 12.

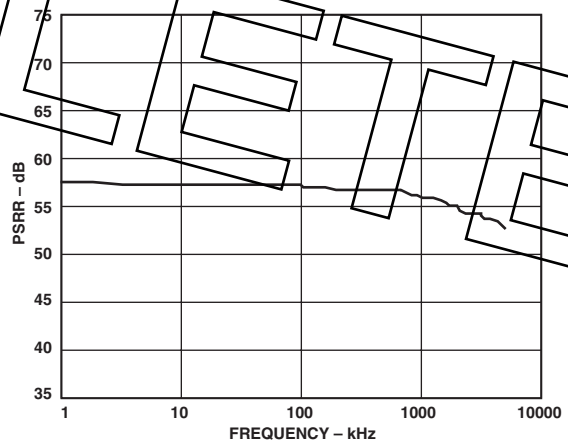


Figure 12. PSRR vs. Frequency

POWER DISSIPATION

In impulse mode, the ADC automatically reduces its power consumption at the end of each conversion phase. During the acquisition phase, the operating currents are very low, which allows a significant power savings when the conversion rate is reduced, as shown in Figure 13. This feature makes the ADC ideal for very low power battery applications.

This does not take into account the power, if any, dissipated by the input resistive scaler, which depends on the input voltage range used and the analog input voltage even in power-down mode. There is no power dissipated when the 0 V to 2.5 V is used or when both the analog input voltage is 0 V and a unipolar range, 0 V to 5 V or 0 V to 10 V, is used.

It should be noted that the digital interface remains active even during the acquisition phase. To reduce the operating digital supply currents even further, the digital inputs need to be driven close to the power rails (i.e., DVDD and DGND) and OVDD should not exceed DVDD by more than 0.3 V.

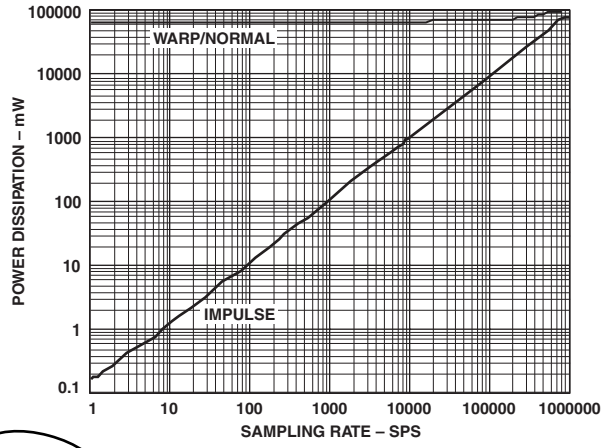


Figure 13. Power Dissipation vs. Sample Rate

CONVERSION CONTROL

Figure 14 shows the detailed timing diagrams of the conversion process. The ADC is controlled by the signal $\overline{\text{CNVST}}$, which initiates conversion. Once initiated, it cannot be restarted or aborted, even by the power-down input PD, until the conversion is complete. The $\overline{\text{CNVST}}$ signal operates independently of $\overline{\text{CS\_ADC}}$ and $\overline{\text{RD}}$ signals.

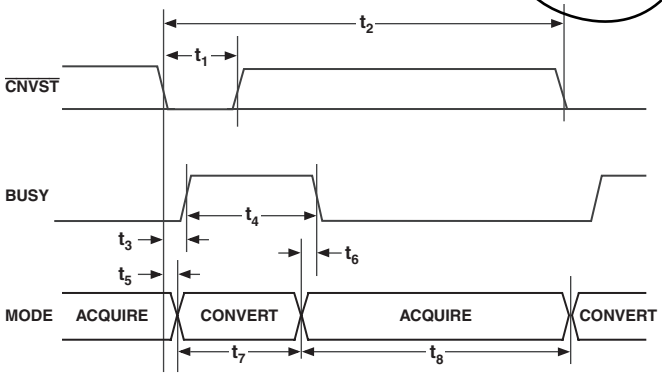


Figure 14. Basic Conversion Timing

In impulse mode, conversions can be automatically initiated. If CNVST is held low when BUSY is low, the ADC controls the acquisition phase and then automatically initiates a new conversion. By keeping CNVST low, the ADC keeps the conversion process running by itself. It should be noted that the analog input has to be settled when BUSY goes low. Also, at power-up, CNVST should be brought low once to initiate the conversion process. In this mode, the ADC could sometimes run slightly faster than the guaranteed limits in the impulse mode of 666 kSPS. This feature does not exist in warp or normal modes.

Although $\overline{\text{CNVST}}$ is a digital signal, it should be designed with special care with fast, clean edges, and levels with minimum overshoot and undershoot or ringing. It is a good thing to shield the $\overline{\text{CNVST}}$ trace with ground and also to add a low value serial resistor (i.e., 50 Ω) termination close to the output of the component that drives this line.

For applications where the SNR is critical, $\overline{\text{CNVST}}$ signal should have a very low jitter. One way to achieve that is to use a dedicated oscillator for $\overline{\text{CNVST}}$ generation, or at least to clock it with a high frequency low jitter clock.

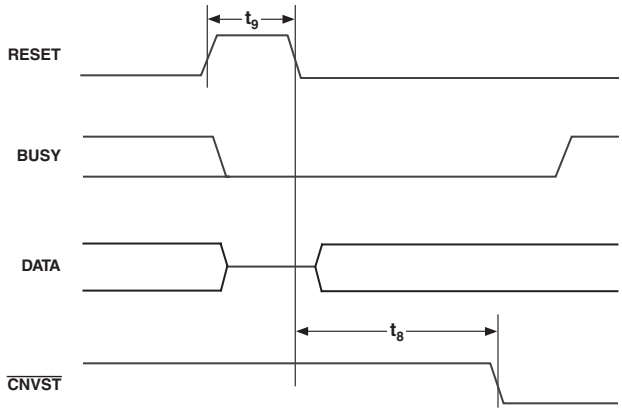


Figure 15. RESET Timing

DIGITAL INTERFACE

The ADC has a versatile digital interface; it can be interfaced with the host system by using either a serial or parallel interface. The serial interface is multiplexed on the parallel data bus. The ADC digital interface also accommodates both 3 V or 5 V logic by simply connecting the OVDD supply pin of the ADC to the host system interface digital supply. Finally, by using the OB/$\overline{\text{2C}}$ input pin, both straight binary or twos complement coding can be used.

The two signals, $\overline{\text{CS\_ADC}}$ and $\overline{\text{RD}}$, control the interface. When at least one of these signals is high, the interface outputs are in high impedance. Usually, $\overline{\text{CS\_ADC}}$ allows the selection of each ADC in multicircuit applications and is held low in a single ADC design. $\overline{\text{RD}}$ is generally used to enable the conversion result on the data bus.

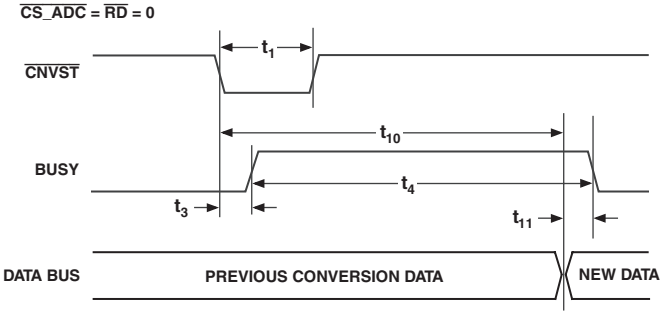


Figure 16. Master Parallel Data Timing for Reading (Continuous Read)

PARALLEL INTERFACE

The ADC is configured to use the parallel interface when the SER/$\overline{PAR}$ is held low. The data can be read either after each conversion, which is during the next acquisition phase, or during the following conversion as shown, respectively, in Figures 18 and 19. When the data is read during the conversion, however, it is recommended that it be read only during the first half of the conversion phase. That avoids any potential feedthrough between voltage transients on the digital interface and the most critical analog conversion circuitry.

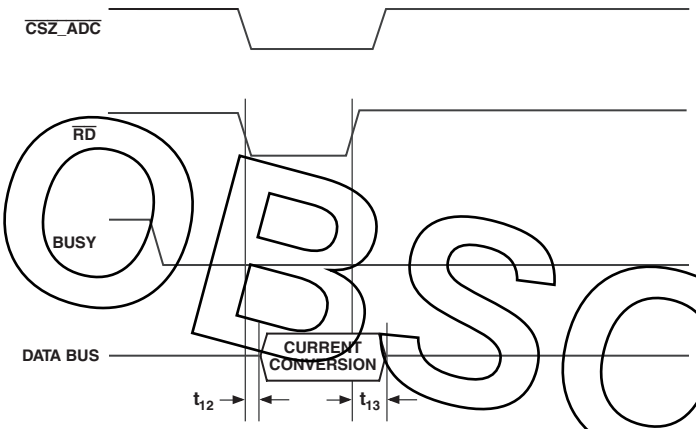


Figure 17. Slave Parallel Data Timing for Reading (Read after Convert)

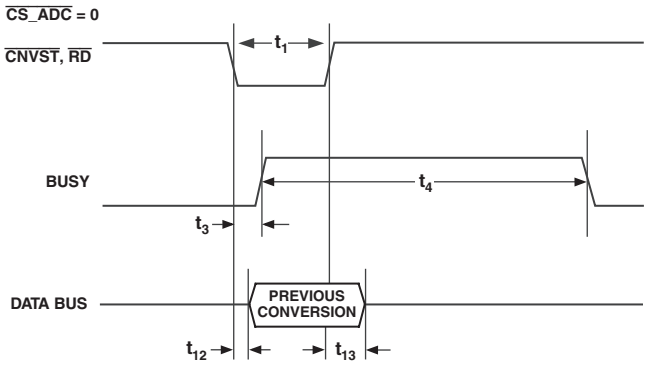


Figure 18. Slave Parallel Data Timing for Reading (Read during Convert)

The BYTESWAP pin allows a glueless interface to an 8-bit bus. As shown in Figure 19, the LSB byte is output on D[7:0] and the MSB is output on D[15:8] when BYTESWAP is low. When BYTESWAP is high, the LSB and MSB are swapped and the LSB is output on D[15:8] and the MSB is output on D[7:0]. By connecting BYTESWAP to an address line, the 16 data bits can be read in two bytes on either D[15:8] or D[7:0].

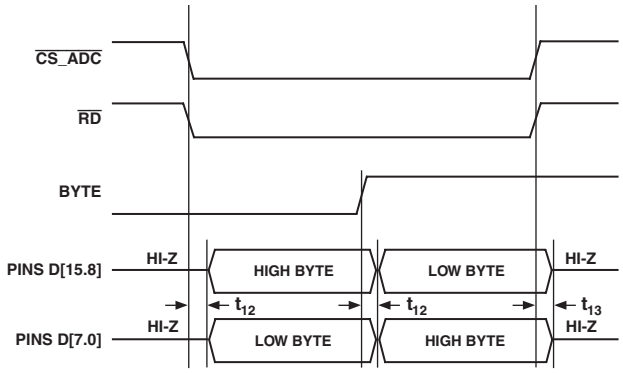


Figure 19. 8-Bit Parallel Interface

SERIAL INTERFACE

The ADC is configured to use the serial interface when the SER/$\overline{PAR}$ is held high. The ADC outputs 16 bits of data, MSB first, on the SDOUT pin. This data is synchronized with the 16 clock pulses provided on the SCLK pin. The output data is valid on both the rising and falling edge of the data clock.

MASTER SERIAL INTERFACE

Internal Clock

The ADC is configured to generate and provide the serial data clock SCLK when the EXT/$\overline{INT}$ pin is held low. It also generates a SYNC signal to indicate to the host when the serial data is valid. The serial clock SCLK and the SYNC signal can be inverted if desired. Depending on RDC/SDIN input, the data can be read after each conversion or during conversion. Figures 20 and 21 show the detailed timing diagrams of these two modes.

Usually, because the ADC is used with a fast throughput, the mode master read during conversion is the most recommended serial mode when it can be used.

In read during conversion mode, the serial clock and data toggle at appropriate instants, which minimizes potential feedthrough between digital activity and the critical conversion decisions.

In read after conversion mode, it should be noted that unlike in other modes, the signal BUSY returns low after the 16 data bits are pulsed out and not at the end of the conversion phase, which results in a longer BUSY width.

SLAVE SERIAL INTERFACE

External Clock

The ADC is configured to accept an externally supplied serial data clock on the $\overline{SCLK}$ pin when the EXT/$\overline{INT}$ pin is held high. In this mode, several methods can be used to read the data. The external serial clock is gated by $\overline{CS\_ADC}$ and the data are output when both $\overline{CS\_ADC}$ and $\overline{RD}$ are low. Thus, depending on $\overline{CS\_ADC}$, the data can be read after each conversion or during the following conversion. The external clock can be either a continuous or discontinuous clock. A discontinuous clock can be either normally high or normally low when inactive. Figure 22 and Figure 24 show the detailed timing diagrams of these methods.

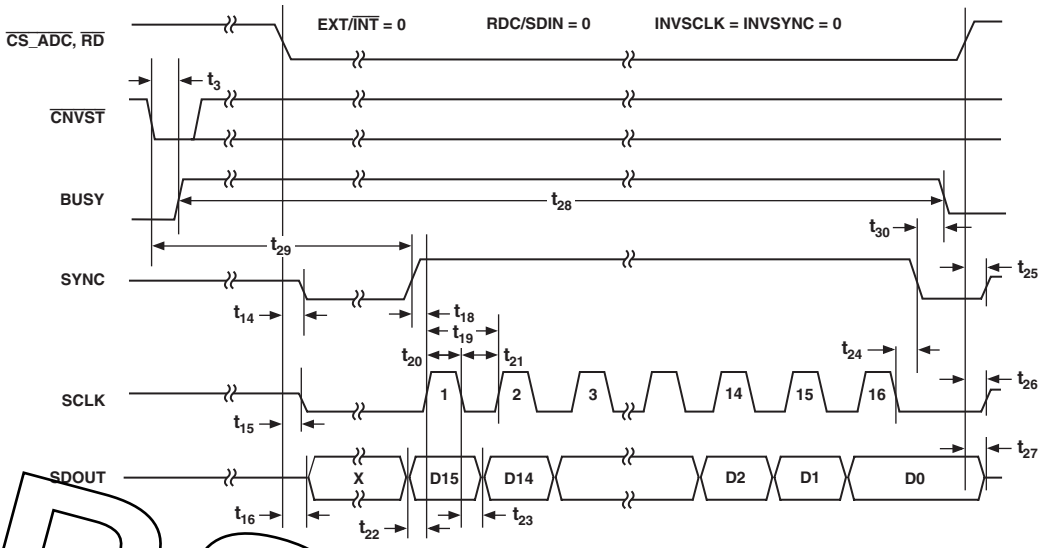


Figure 20. Master Serial Data Timing for Reading (Read after Convert)

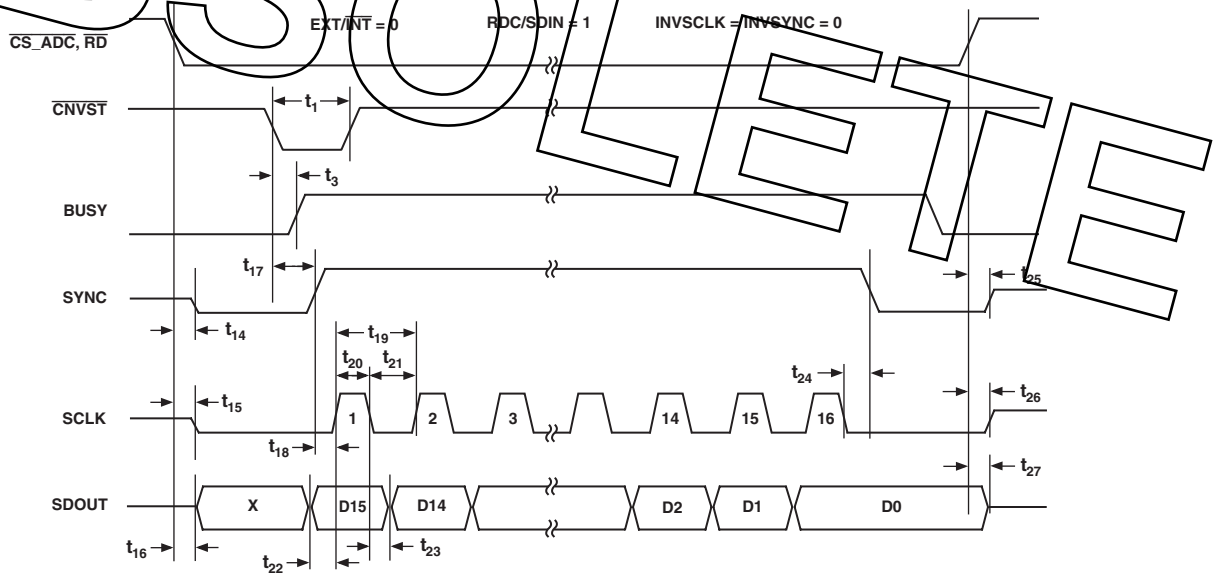


Figure 21. Master Serial Data Timing for Reading (Read Previous Conversion during Convert)

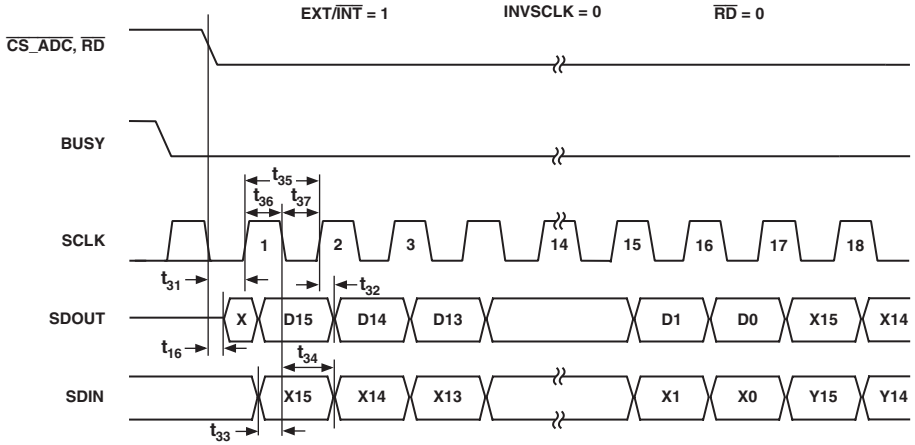


Figure 22. Slave Serial Data Timing for Reading (Read after Convert)

While the ADC is performing a bit decision, it is important that voltage transients not occur on digital input/output pins or degradation of the conversion result could occur. This is particularly important during the second half of the conversion phase because the ADC provides error correction circuitry that can correct for an improper bit decision made during the first half of the conversion phase. For this reason, it is recommended that when an external clock is being provided, it is a discontinuous clock that is toggling only when BUSY is low or, more importantly, that it does not transition during the latter half of BUSY high.

External Discontinuous Clock Data Read after Conversion

Though the maximum throughput cannot be achieved using this mode, it is the most recommended of the serial slave modes. Figure 22 shows the detailed timing diagrams of this method. After a conversion is complete, indicated by BUSY returning low, the result of this conversion can be read while both $\overline{CS\_ADC}$ and $\overline{RD}$ are low. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock. Among the advantages of this method is that the conversion performance is not degraded because there are no voltage transients on the digital interface during the conversion process. Another advantage is to be able to read the data at any speed up to 40 MHz, which accommodates both slow digital host interface and the fastest serial reading.

Finally, in this mode only, the ADC provides a daisy-chain feature using the RDC/SDIN input pin for cascading multiple converters together. This feature is useful for reducing component count and wiring connections when desired as, for instance, in isolated multiconverter applications.

An example of the concatenation of two devices is shown in Figure 23. Simultaneous sampling is possible by using a common $\overline{CNVST}$ signal. It should be noted that the RDC/SDIN input is latched on the opposite edge of SCLK of the one used to shift out the data on SDOUT. Therefore, the MSB of the "upstream" converter just follows the LSB of the "downstream" converter on the next SCLK cycle.

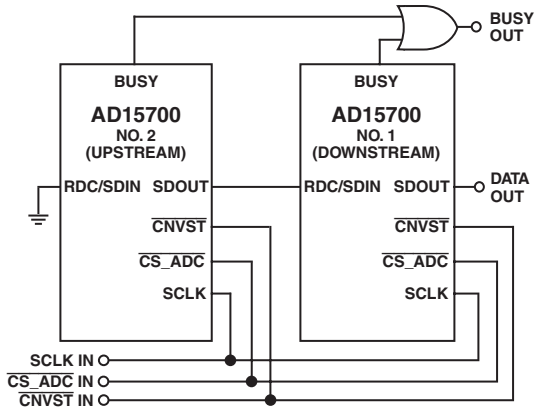


Figure 23. Two AD15700s in a Daisy-Chain Configuration

External Clock Data Read during Conversion

Figure 24 shows the detailed timing diagrams of this method. During a conversion, while both $\overline{CS\_ADC}$ and $\overline{RD}$ are low, the result of the previous conversion can be read. The data is shifted out, MSB first, with 16 clock pulses and is valid on both the rising and falling edge of the clock. The 16 bits have to be read before the current conversion is complete. If that is not done, RDERROR is pulsed high and can be used to interrupt the host interface to prevent incomplete data reading. There is no daisy-chain feature in this mode and RDC/SDIN input should always be tied either high or low.

To reduce performance degradation due to digital activity, a fast discontinuous clock of at least 25 MHz when impulse mode is used, and 32 MHz when normal or 40 MHz when warp mode is used, is recommended to ensure that all the bits are read during the first half of the conversion phase. It is also possible to begin to read the data after conversion and continue to read the last bits even after a new conversion has been initiated. That allows the use of a slower clock speed like 18 MHz in impulse mode, 21 MHz in normal mode, and 26 MHz in warp mode.

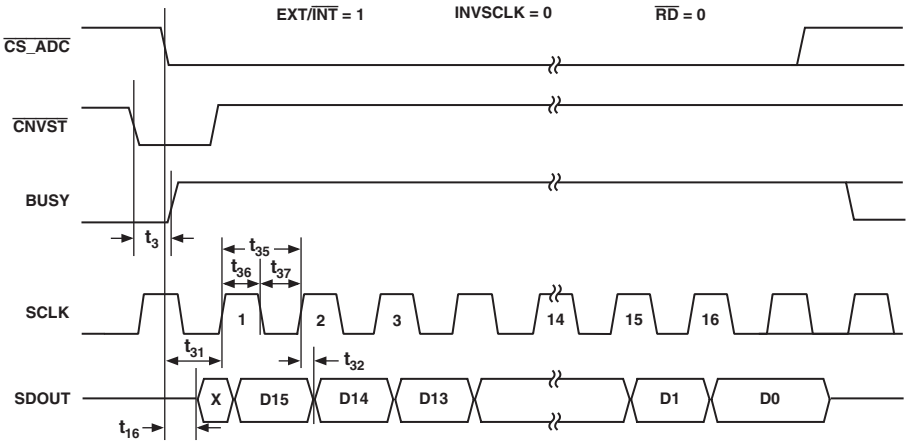


Figure 24. Slave Serial Data Timing for Reading (Read Previous Conversion during Convert)

MICROPROCESSOR INTERFACING

The ADC is ideally suited for traditional dc measurement applications supporting a microprocessor, and ac signal processing applications interfacing to a digital signal processor. The ADC is designed to interface either with a parallel 8-bit or 16-bit wide interface or with a general-purpose serial port or I/O ports on a microcontroller. A variety of external buffers can be used with the ADC to prevent digital noise from coupling into the ADC. The following sections illustrate the use of the ADC with an SPI equipped microcontroller, the ADSP-21065L and ADSP-218x signal processors.

SPI Interface (MC68HC11)

Figure 25 shows an interface diagram between the ADC and an SPI equipped microcontroller like the MC68HC11. To accommodate the slower speed of the microcontroller, the ADC acts as a slave device and data must be read after conversion. This mode also allows the daisy-chain feature. The convert command could be initiated in response to an internal timer interrupt. The reading of output data, one byte at a time, if necessary, could be initiated in response to the end-of-conversion signal (BUSY going low) using an interrupt line of the microcontroller. The serial peripheral interface (SPI) on the MC68HC11 is configured for master mode (MSTR) = 1, Clock Polarity Bit (CPOL) = 0, Clock Phase Bit (CPHA) = 1, and SPI Interrupt Enable (SPIE) = 1 by writing to the SPI Control Register (SPCR). The IRQ is configured for edge-sensitive-only operation (IRQE = 1 in OPTION register).

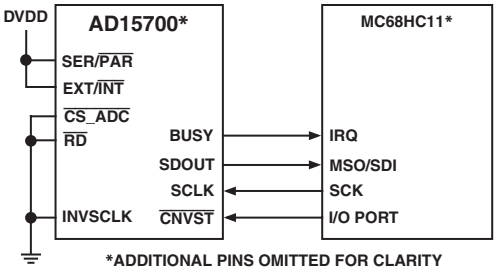


Figure 25. Interfacing the AD15700 to SPI Interface

ADSP-21065L in Master Serial Interface

As shown in Figure 26, AD15700s can be interfaced to the ADSP-21065L using the serial interface in master mode without any glue logic required. This mode combines the advantages of reducing the wire connections and the ability to read the data during or after conversion at maximum speed transfer (DIVSCLK[0:1] both low).

The ADC is configured for the internal clock mode (EXT/$\overline{\text{INT}}$ low) and acts, therefore, as the master device. The convert command can be generated by either an external low jitter oscillator or, as shown, by a FLAG output of the ADSP-21065L or by a frame output TFS of one serial port of the ADSP-21065L, which can be used like a timer. The serial port on the ADSP-21065L is configured for external clock (IRFS = 0), rising edge active (CKRE = 1), external late framed sync signals (IRFS = 0, LAFS = 1, RFSR = 1), and active high (LRFS = 0). The serial port of the ADSP-21065L is configured by writing to its receive control register (SRCTL)—see the *ADSP-2106x SHARC User's Manual.* Because the serial port within the ADSP-21065L will be seeing a discontinuous clock, an initial word reading has to be done after the ADSP-21065L has been reset to ensure that the serial port is properly synchronized to this clock during each following data read operation.

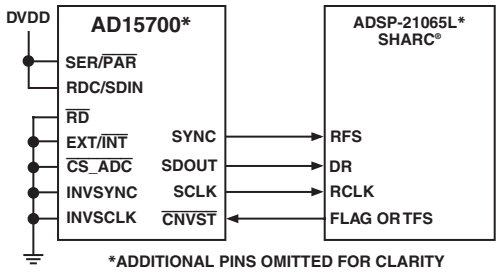


Figure 26. Interfacing to the ADSP-21065L Using the Serial Master Mode

APPLICATION HINTS

Layout

The AD15700's ADC has very good immunity to noise on the power supplies as can be seen in Figure 12. However, care should still be taken with regard to grounding layout.

The printed circuit board that houses the AD15700 should be designed so the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be easily separated. Digital and analog ground planes should be joined in only one place, preferably underneath the AD15700, or at least as close as possible to the AD15700. If the AD15700 is in a system where multiple devices require analog-to-digital ground connections, the connection should still be made at one point only, a star ground point, which should be established as close as possible to the AD15700. It is recommended to avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the switching signals like $\overline{\text{CNVST}}$ or clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and should never run near analog signal paths. Crossover of digital and analog signals should be avoided. Traces on different but close layers of the board should run at right angles to each other. This will reduce the effect of feedthrough through the board.

The power supply lines to the AD15700 should use as large a trace as possible to provide low impedance paths and reduce the effect of glitches on the power supply lines. Good decoupling is also important to lower the supply impedance presented to the AD15700 and reduce the magnitude of the supply spikes. Decoupling ceramic capacitors, typically 100 nF, should be placed on each power supply pin, AVDD, DVDD, and OVDD, close to and ideally right up against these pins and their corresponding ground pins. Additionally, low ESR 10 nF capacitors should be located in the vicinity of the ADC to further reduce low frequency ripple.

The DVDD supply of the AD15700 can be either a separate supply or come from the analog supply, AVDD, or from the digital interface supply, OVDD. When the system digital supply is noisy, or fast switching digital signals are present, it is recommended if no separate supply is available to connect the DVDD digital supply to the analog supply AVDD through an RC filter, and connect the system supply to the interface digital supply OVDD and the remaining digital circuitry. When DVDD is powered from the system supply, it is useful to insert a bead to further reduce high frequency spikes.

The AD15700's ADC has five different ground pins: INGND, REFGND, AGND, DGND, and OGND. INGND is used to sense the analog input signal. REFGND senses the reference voltage and should be a low impedance return to the reference because it carries pulsed currents. AGND is the ground to which most internal ADC analog signals are referenced. This ground must be connected with the least resistance to the analog ground plane. DGND must be tied to the analog or digital ground plane depending on the configuration. OGND is connected to the digital system ground.

The layout of the decoupling of the reference voltage is important. The decoupling capacitor should be close to the ADC and connected with short and large traces to minimize parasitic inductances.

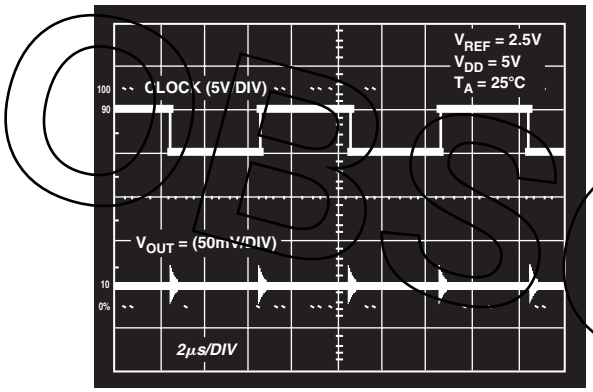


Figure 27. Digital Feedthrough

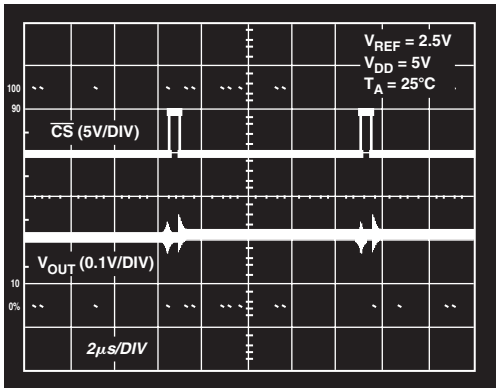


Figure 28. Digital-to-Analog Glitch Impulse

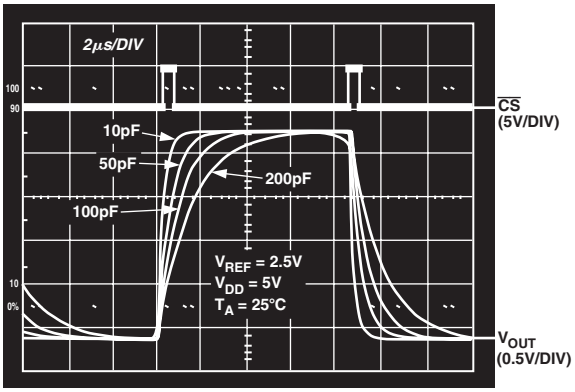


Figure 29. Large Signal Settling Time

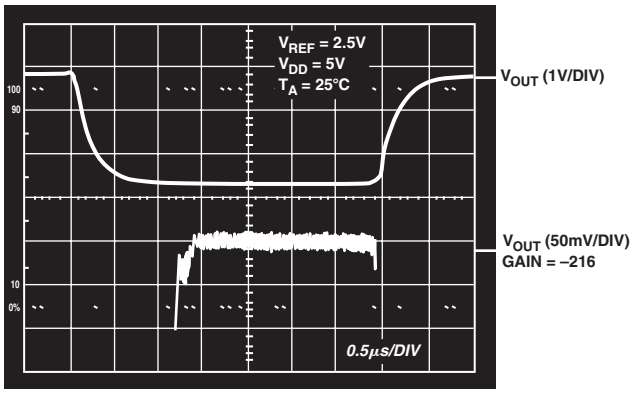


Figure 30. Small Signal Settling Time

DAC Circuit Information

The DAC is a single 14-bit, serial input voltage output. It operates from a single supply ranging from 2.7 V to 5 V and consumes typically 300 mA with a supply of 5 V. Data is written to the devices in a 14-bit word format, via a 3- or 4-wire serial interface. To ensure a known power-up state, the parts were designed with a power-on reset function. In unipolar mode, the output is reset to 0 V.

Digital-to-Analog Section

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 31. The four MSBs of the 14-bit data-word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either AGND or VREF. The remaining 10 bits of the data-word drive switches S0 to S9 of a 10-bit voltage mode R-2R ladder network.

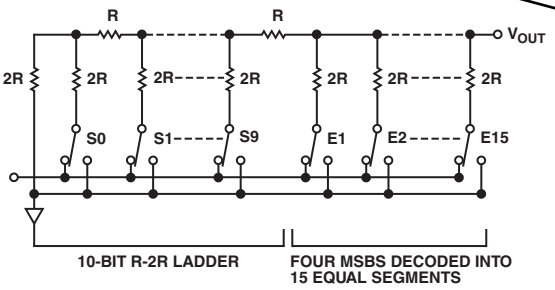


Figure 31. DAC Architecture

With this type of DAC configuration, the output impedance is independent of code, while the input impedance seen by the reference is heavily code dependent. The output voltage is dependent on the reference voltage as shown in the following equation.

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where D is the decimal data-word loaded to the DAC register and N is the resolution of the DAC. For a reference of 2.5 V, the equation simplifies to the following.

$$V_{OUT} = \frac{2.5 \times D}{16,384}$$

giving a V_{OUT} of 1.25 V with midscale loaded, and 2.5 V with full scale loaded to the DAC.

The LSB size is $V_{REF}/16,384$.

Serial Interface

The DAC is controlled by a versatile 3-wire serial interface that operates at clock rates up to 25 MHz and is compatible with SPI, QSPI, MICROWIRE, and DSP interface standards. The timing diagram can be seen in Figure 3. Input data is framed by the chip select input, $\overline{CS\_DAC}$. After a high to low transition on $\overline{CS\_DAC}$, data is shifted synchronously and latched into the input register on the rising edge of the serial clock, SCLK. Data is loaded MSB first in 14-bit words. After 14 data bits have been loaded into the serial input register, a low to high transition on $\overline{CS\_DAC}$ transfers the contents of the shift register to the DAC. Data can only be loaded to the part while $\overline{CS\_DAC}$ is low.

Unipolar Output Operation

The DAC is capable of driving unbuffered loads of 60 kΩ. Unbuffered operation results in low supply current, typically 300 mA, and a low offset error. The DAC provides a unipolar output swing ranging from 0 V to VREF. Figure 32 shows a typical unipolar output voltage circuit. The code table for this mode of operation is shown in Table IV.

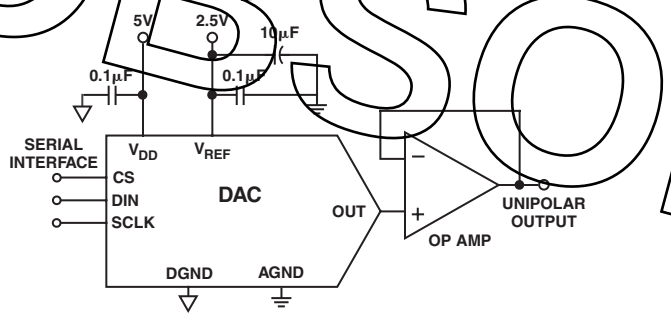


Figure 32. Unipolar Output

Table IV. Unipolar Code Table

DAC Latch Contents	
MSB LSB	**Analog Output**
11 1111 1111 1111	VREF X (16383/16384)
10 0000 0000 0000	VREF X (8192/16384) = 1/2 VREF
00 0000 0000 0001	VREF X (1/16384)
00 0000 0000 0000	0 V

Assuming a perfect reference, the worst-case output voltage may be calculated from the following equation.

$$V_{OUT-UNI} = \frac{D}{2^{14}} \times \left(V_{REF} + V_{GE}\right) + V_{ZSE} + INL$$

where:

$V_{OUT-UNI}$ = Unipolar Mode Worst-Case Output

D = Decimal Code Loaded to DAC

V_{REF} = Reference Voltage Applied to Part

V_{GE} = Gain Error in Volts

V_{ZSE} = Zero Scale Error in Volts

INL = Integral Nonlinearity in Volts

Output Amplifier Selection

In a single-supply application, selection of a suitable op amp may be more difficult as the output swing of the amplifier does not usually include the negative rail, in this case AGND. This can result in some degradation of the specified performance unless the application does not use codes near zero.

The selected op amp needs to have very low offset voltage (the DAC LSB is 152 µV with a 2.5 V reference) to eliminate the need for output offset trims. Input bias current should also be very low as the bias current multiplied by the DAC output impedance (approximately 6 kΩ) will add to the zero code error. Rail-to-rail input and output performance is required. For fast settling, the slew rate of the op amp should not impede the settling time of the DAC. Output impedance of the DAC is constant and code independent, but in order to minimize gain errors, the input impedance of the output amplifier should be as high as possible. The amplifier should also have a 3 dB bandwidth of 1 MHz or greater. The amplifier adds another time constant to the system, thus increasing the settling time of the output. A higher 3 dB amplifier bandwidth results in a faster effective settling time of the combined DAC and amplifier.

Force Sense Buffer Amplifier Selection

These amplifiers can be single-supply or dual-supply, low noise amplifiers. A low output impedance at high frequencies is preferred to be able to handle dynamic currents of up to ±20 mA.

Reference and Ground

As the input impedance is code dependent, the reference pin should be driven from a low impedance source. The DAC operates with a voltage reference ranging from 2 V to V_{DD}. Although DAC's full-scale output voltage is determined by the reference, references below 2 V will result in reduced accuracy. Table IV outlines the analog output voltage for particular digital codes.

Power-On Reset

The DAC has a power-on reset function to ensure the output is at a known state upon power-up. On power-up, the DAC register contains all zeros, until data is loaded from the serial register. However, the serial register is not cleared on power-up, so its contents are undefined. When loading data initially to the DAC, 14 bits or more should be loaded to prevent erroneous data appearing on the output. If more than 14 bits are loaded, only the last 14 are kept, and if fewer than 14 are loaded, bits will remain from the previous word. If the DAC needs to be interfaced with data shorter than 14 bits, the data should be padded with zeros at the LSBs.

Power Supply and Reference Bypassing

For accurate high resolution performance, it is recommended that the reference and supply pins be bypassed with a 10 nF tantalum capacitor in parallel with a 0.1 nF ceramic capacitor.

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the DAC is via a serial bus that uses standard protocol compatible with DSP processors and microcontrollers. The communications channel requires a 3-wire interface consisting of a clock signal, a data signal, and a synchronization signal. The DAC requires a 14-bit data-word with data valid on the rising edge of SCLK. The DAC update may be done automatically when all the data is clocked in.

ADSP-2101/ADSP-2103 to DAC Interface

Figure 33 shows a serial interface between the DAC and the ADSP-2101/ADSP-2103. The ADSP-2101/ADSP-2103 should be set to operate in the SPORT (Serial Port) Transmit Alternate Framing Mode. The ADSP-2101/ADSP-2103 is programmed through the SPORT Control Register and should be configured as follows: internal clock operation, active low framing, 16-bit word length. The first two bits are DON'T CARE as the DAC will keep the last 14 bits. Transmission is initiated by writing a word to the Tx Register after the SPORT has been enabled. Because of the edge-triggered difference, an inverter is required at the SCLKs between the DSP and the DAC.

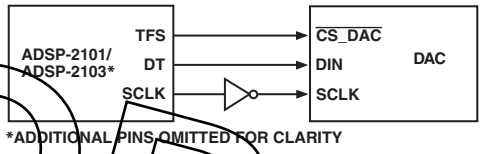


Figure 33. ADSP-2101/ADSP-2103 to DAC Interface

68HC11/68L11 to DAC Interface

Figure 34 shows a serial interface between the DAC and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the DAC, while the MOSI output drives the serial data lines SDIN. CS signal is driven from one of the port lines. The 68HC11/68L11 is configured for master mode; MSTR = 1, CPOL = 0, and CPHA = 0. Data appearing on the MOSI output is valid on the rising edge of SCK.

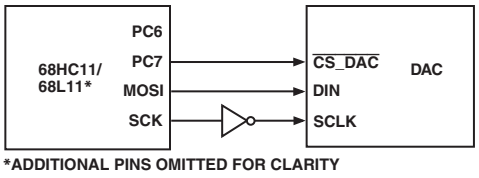


Figure 34. 68HC11/68L11 to DAC Interface

MICROWIRE to DAC Interface

Figure 35 shows an interface between the DAC and any MICROWIRE compatible device. Serial data is shifted out on the falling edge of the serial clock and into the DAC on the rising edge of the serial clock. No glue logic is required as the DAC clocks data into the input shift register on the rising edge.

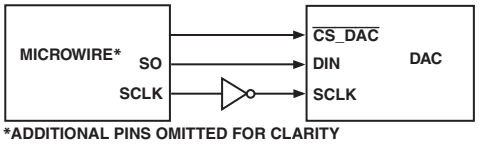


Figure 35. MICROWIRE to DAC Interface

80C51/80L51 to DAC Interface

A serial interface between the DAC and the 80C51/80L51 microcontroller is shown in Figure 36. TxD of the microcontroller drives the SCLK of the DAC, while RxD drives the serial data line of the DAC. P3.3 is a bit programmable pin on the serial port that is used to drive $\overline{\text{CS\_DAC}}$.

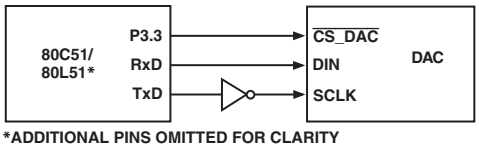


Figure 36. 80C51/80L51 to DAC Interface

The 80C51/80L51 provides the LSB first, while the DAC expects the MSB of the 14-bit word first. Care should be taken to ensure the transmit routine takes this into account. Usually it can be done through software by shifting out and accumulating the bits in the correct order before inputting to the DAC. Also, 80C51 outputs 2-byte word/16-bit data. Thus the first two bits, after rearrangement, should be DON'T CARE as they will be dropped from the DAC's 14-bit word.

When data is to be transmitted to the DAC, P3.3 is taken low. Data on RxD is valid on the falling edge of TxD, so the clock must be inverted as the DAC clocks data into the input shift register on the rising edge of the serial clock. The 80C51/80L51 transmits its data in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. As the DAC requires a 14-bit word, P3.3 (or any one of the other programmable bits) is the $\overline{\text{CS\_DAC}}$ input signal to the DAC, so P3.3 should be brought low at the beginning of the 16-bit write cycle 2 × 8-bit words and held low until the 16-bit 2 × 8 cycle is completed. After that, P3.3 is brought high again and the new data loads to the DAC. Again, the first two bits, after rearranging, should be DON'T CARE.

APPLICATIONS

Optocoupler Interface

The digital inputs of the DAC are Schmitt-triggered, so they can accept slow transitions on the digital input lines. This makes these parts ideal for industrial applications where it may be necessary for the DAC to be isolated from the controller via optocouplers. Figure 37 illustrates such an interface.

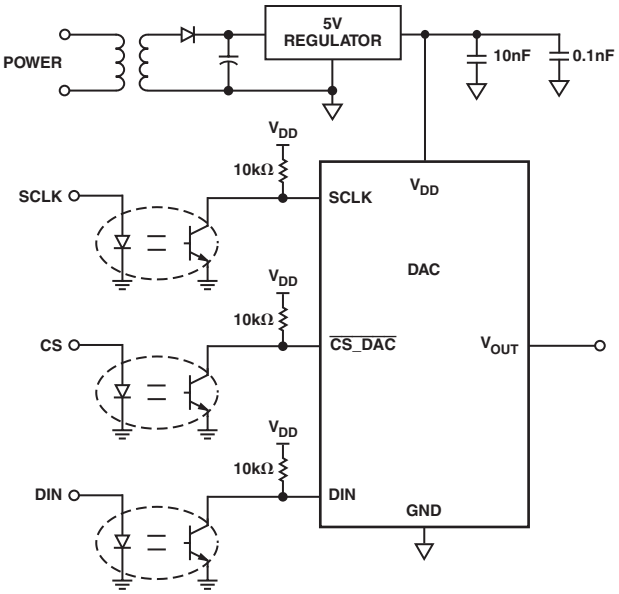


Figure 37. DAC in an Optocoupler Interface

Decoding Multiple DACs

The $\overline{\text{CS\_DAC}}$ pin of the DAC can be used to select one of a number of DACs. All devices receive the same serial clock and serial data, but only one device will receive the $\overline{\text{CS\_DAC}}$ signal at any one time. The DAC addressed will be determined by the decoder. There will be some digital feedthrough from the digital input lines. Using a burst clock will minimize the effects of digital feedthrough on the analog signal channels. Figure 38 shows a typical circuit.

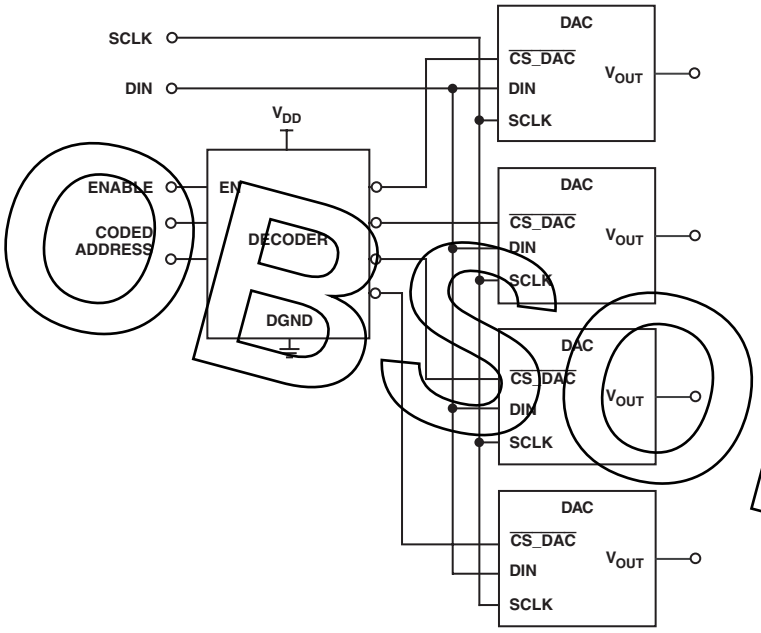


Figure 38. Addressing Multiple DACs

AMPLIFIER THEORY OF OPERATION

The amplifiers are single and dual versions of high speed, low power voltage feedback amplifiers featuring an innovative architecture that maximizes the dynamic range capability on the inputs and outputs. Linear input common-mode range exceeds either supply voltage by 200 mV, and the amplifiers show no phase reversal up to 500 mV beyond supply. The output swings to within 20 mV of either supply when driving a light load; 300 mV when driving up to 5 mA.

The amplifier provides an impressive 80 MHz bandwidth when used as a follower and 30 V/ms slew rate at only 800 mA supply current. Careful design allows the amplifier to operate with a supply voltage as low as 2.7 V.

Input Stage Operation

A simplified schematic of the input stage appears in Figure 39. For common-mode voltages up to 1.1 V within the positive supply, (0 V to 3.9 V on a single 5 V supply) tail current I2 flows through the PNP differential pair, Q13 and Q17. Q5 is cut off; no bias current is routed to the parallel NPN differential pair Q2 and Q3. As the common-mode voltage is driven within 1.1 V of the positive supply, Q5 turns on and routes the tail current away from the PNP pair and to the NPN pair. During this transition region, the amplifier's input current will change magnitude and direction. Reusing the same tail current ensures that the input stage has the same transconductance (which determines the amplifier's gain and bandwidth) in both regions of operation.

Switching to the NPN pair as the common-mode voltage is driven beyond 1 V within the positive supply allows the amplifier to provide useful operation for signals at either end of the supply voltage range and eliminates the possibility of phase reversal for input signals up to 500 mV beyond either power supply. Offset voltage will also change to reflect the offset of the input pair in control. The transition region is small, on the order of 180 mV. These sudden changes in the dc parameters of the input stage can produce glitches that will adversely affect distortion.

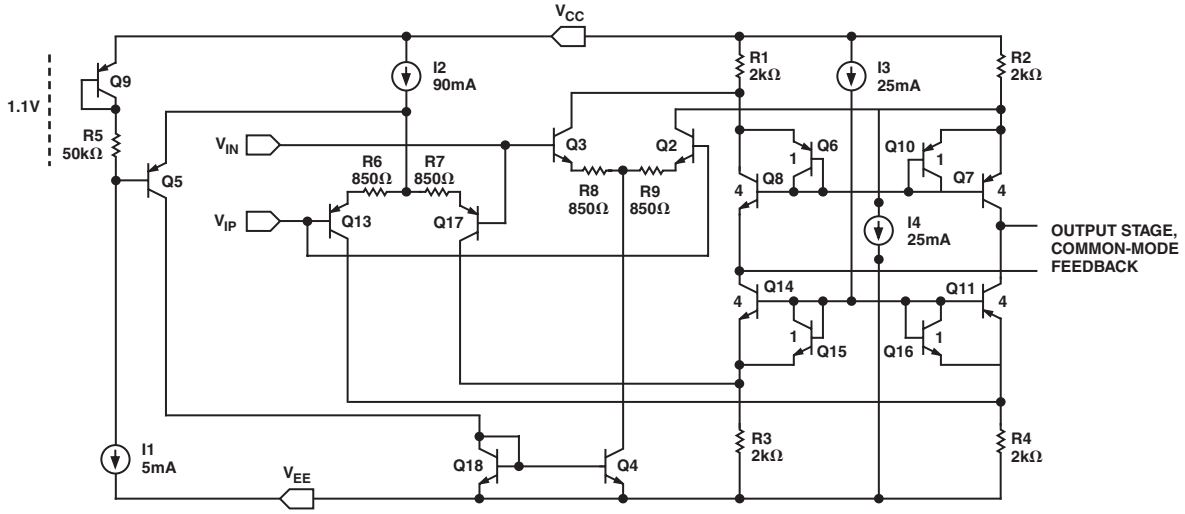


Figure 39. Simplified Schematic of Input Stage

Overdriving the Input Stage

Sustained input differential voltages greater than 3.4 V should be avoided as the input transistors may be damaged. Input clamp diodes are recommended if the possibility of this condition exists.

The voltages at the collectors of the input pairs are set to 200 mV from the power supply rails. This allows the amplifier to remain in linear operation for input voltages up to 500 mV beyond the supply voltages. Driving the input common-mode voltage beyond that point will forward bias the collector junction of the input transistor, resulting in phase reversal. Sustaining this condition for any length of time should be avoided as it is easy to exceed the maximum allowed input differential voltage when the amplifier is in phase reversal.

Output Stage, Open-Loop Gain, and Distortion Versus Clearance from Power Supply

The amplifier features a rail-to-rail output stage. The output transistors operate as common emitter amplifiers, providing the output drive current as well as a large portion of the amplifier's open-loop gain.

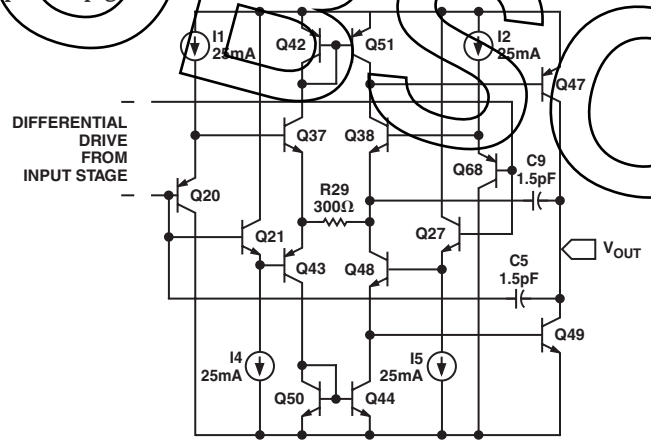


Figure 40. Output Stage Simplified Schematic

The output voltage limit depends on how much current the output transistors are required to source or sink. For applications with very low drive requirements (a unity gain follower driving another amplifier input, for instance), the amplifier typically swings within 20 mV of either voltage supply. As the required current load increases, the saturation output voltage will increase linearly as $I_{LOAD} \times R_C$, where I_{LOAD} is the required load current and R_C is the output transistor collector resistance. For the amplifier, the collector resistances for both output transistors are typically 25 Ω. As the current load exceeds the rated output current of 15 mA, the amount of base drive current required to drive the output transistor into saturation will reach its limit, and the amplifier's output swing will rapidly decrease.

The open-loop gain of the amplifier decreases approximately linearly with load resistance and also depends on the output voltage. Open-loop gain stays constant to within 250 mV of the positive power supply, 150 mV of the negative power supply and then decreases as the output transistors are driven further into saturation.

The distortion performance of the amplifiers differs from conventional amplifiers. Typically an amplifier's distortion performance degrades as the output voltage amplitude increases. Used as a unity gain follower, the amplifier output will exhibit more distortion in the peak output voltage region around V_{CC} –0.7 V. This unusual distortion characteristic is caused by the input stage architecture and is discussed in detail in the section covering Input Stage Operation.

Output Overdrive Recovery

Output overdrive of an amplifier occurs when the amplifier attempts to drive the output voltage to a level outside its normal range. After the overdrive condition is removed, the amplifier must recover to normal operation in a reasonable amount of time. As shown in Figure 41, the amplifier recovers within 100 ns from negative overdrive and within 80 ns from positive overdrive.

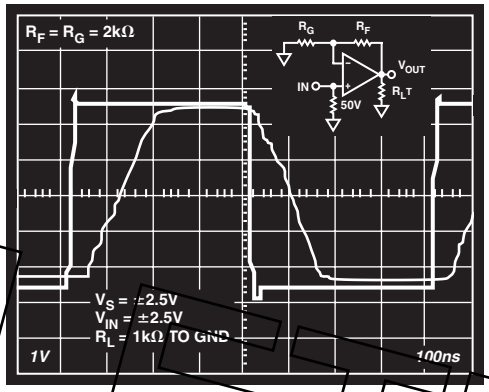


Figure 41. Overdrive Recovery

Driving Capacitive Loads

Capacitive loads interact with an amplifier's output impedance to create an extra delay in the feedback path. This reduces circuit stability and can cause unwanted ringing and oscillation. A given value of capacitance causes much less ringing when the amplifier is used with a higher noise gain.

The capacitive load drive of the amplifier can be increased by adding a low valued resistor in series with the capacitive load. Introducing a series resistor tends to isolate the capacitive load from the feedback loop, thereby diminishing its influence. Figure 42 shows the effect of a series resistor on capacitive drive for varying voltage gains. As the closed-loop gain is increased, the larger phase margin allows for larger capacitive loads with less overshoot. Adding a series resistor at lower closed-loop gains accomplishes the same effect. For large capacitive loads, the frequency response of the amplifier will be dominated by the roll-off of the series resistor and capacitive load.

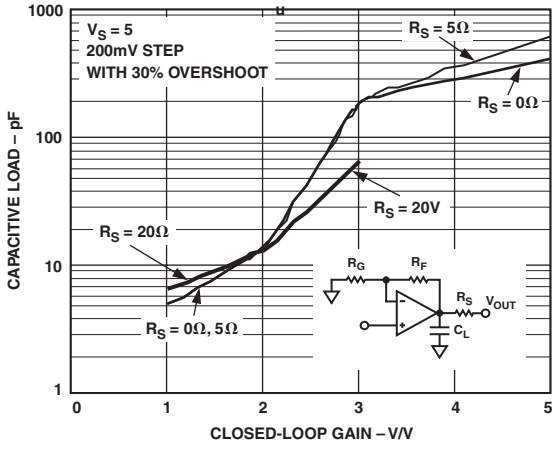


Figure 42. Capacitive Load Drive vs. Closed-Loop Gain

High Performance Single-Supply Line Driver

Even though the amplifier swings close to both rails, the amplifier has optimum distortion performance when the signal has a common-mode level halfway between the supplies and when there is about 500 mV of headroom to each rail. If low distortion is required in single-supply applications for signals that swing close to ground, an emitter follower circuit can be used at the amplifier output.

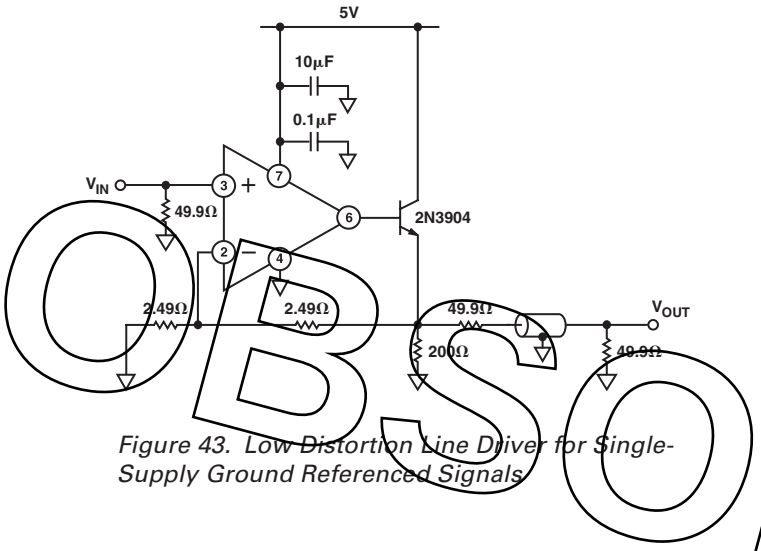


Figure 43. Low Distortion Line Driver for Single-Supply Ground Referenced Signals

Figure 43 shows the amplifier configured as a single-supply gain-of-two line driver. With the output driving a back terminated 50 Ω line, the overall gain from V_{IN} to V_{OUT} is unity. In addition to minimizing reflections, the 50 Ω back termination resistor protects the transistor from damage if the cable is short circuited. The emitter follower, which is inside the feedback loop, ensures that the output voltage from the amplifier stays about 700 mV above ground. Using this circuit, very low distortion is attainable even when the output signal swings to within 50 mV of ground. The circuit was tested at 500 kHz and 2 MHz. Figures 44 and 45 show the output signal swing and frequency spectrum at 500 kHz. At this frequency, the output signal (at V_{OUT}), which has a peak-to-peak swing of 1.95 V (50 mV to 2 V), has a THD of –68 dB (SFDR = –77 dB).

Figures 46 and 47 show the output signal swing and frequency spectrum at 2 MHz. As expected, there is some degradation in signal quality at the higher frequency. When the output signal has a peak-to-peak swing of 1.45 V (swinging from 50 mV to 1.5 V), the THD is –55 dB (SFDR = –60 dB). This circuit could also be used to drive the analog input of a single-supply high speed ADC whose input voltage range is referenced to ground (e.g., 0 V to 2 V or 0 V to 4 V). In this case, a back termination resistor is not necessary (assuming a short physical distance from transistor to ADC), so the emitter of the external transistor would be connected directly to the ADC input. The available output voltage swing of the circuit would, therefore, be doubled.

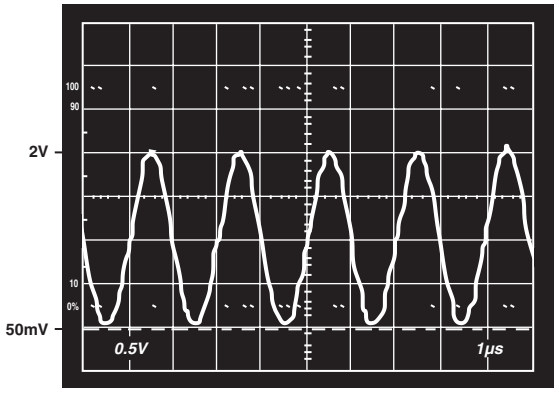


Figure 44. Output Signal Swing of Low Distortion Line Driver at 500 kHz

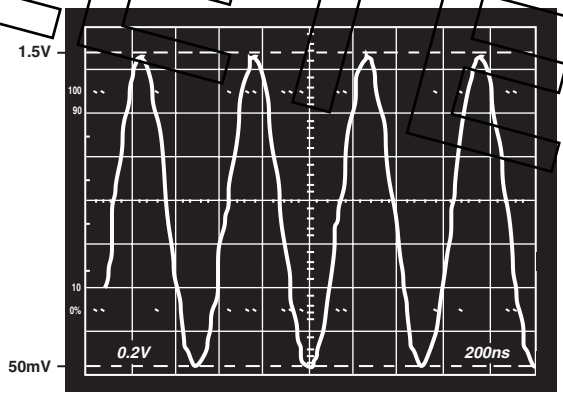


Figure 46. Output Signal Swing of Low Distortion Line Driver at 2 MHz

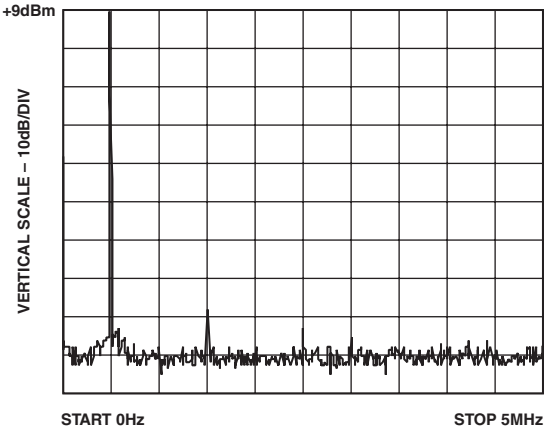


Figure 45. THD of Low Distortion Line Driver at 500 kHz

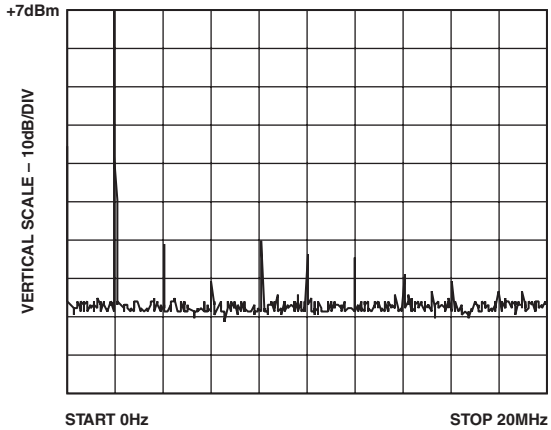


Figure 47. THD of Low Distortion Line Driver at 2 MHz

AD15700 PINOUT

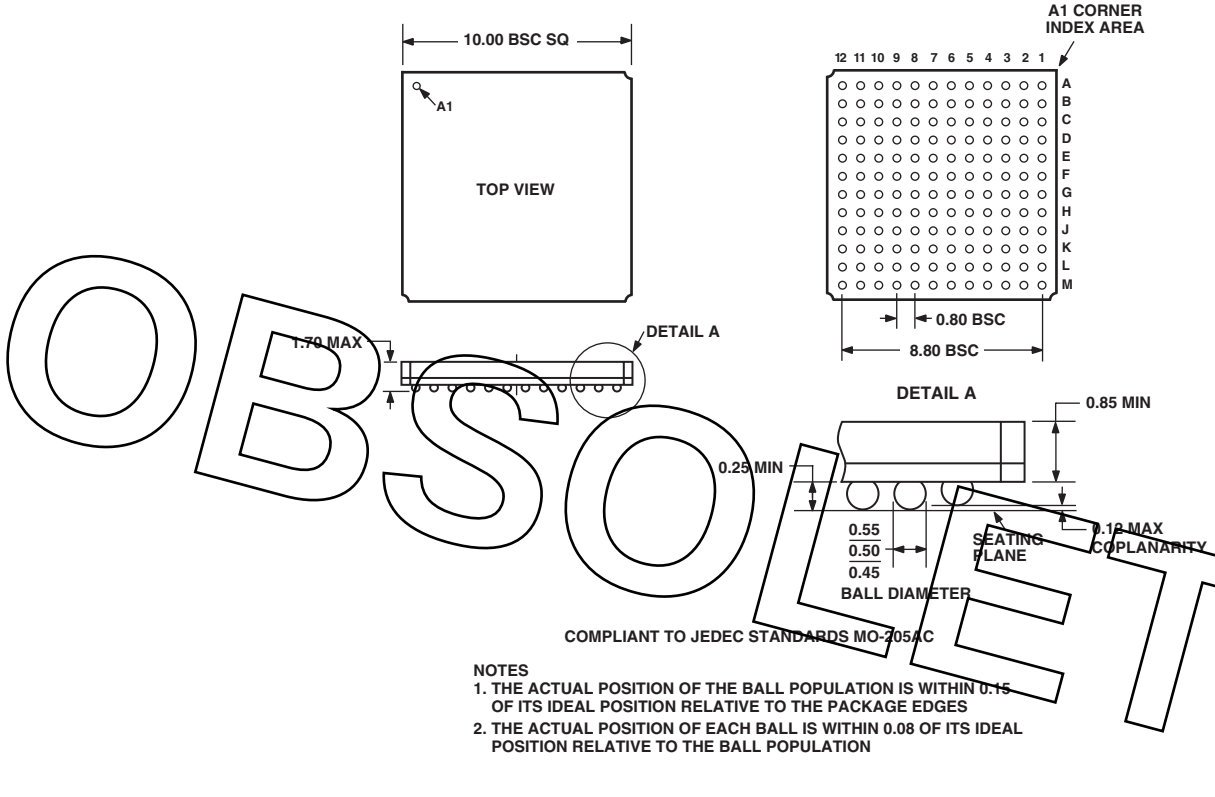
(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11	12	
A	COMMON	VREF	AGND DAC	COMMON	COMMON	VOUT	RPAD1	RB1	–IN1	COMMON	+VS1	COMMON	A
B	$\overline{\text{CS\_DAC}}$	COMMON	COMMON	COMMON	COMMON	COMMON	COMMON	COMMON	RA1	–VS1	–VS1	VOUT1	B
C	COMMON	COMMON	AGND DAC	AGND DAC	COMMON	VDD DAC	COMMON	COMMON	+IN1	COMMON	COMMON	COMMON	C
D	COMMON	COMMON	COMMON	COMMON	COMMON	COMMON	COMMON	COMMON	RC1	COMMON	COMMON	RESET	D
E	SCLK	DIN	DGND DAC	COMMON	COMMON	COMMON	$\overline{\text{CNVST}}$	COMMON	COMMON	$\overline{\text{RD}}$	D15	D14	E
F	COMMON	COMMON	+VS2	COMMON	COMMON	COMMON	COMMON	COMMON	COMMON	COMMON	D13	D12	F
G	–IN2	COMMON	–VS2	COMMON	REF	COMMON	COMMON	COMMON	TEST1	BUSY	D11 RDERROR	D10 SYNC	G
H	COMMON	COMMON	–VS2	COMMON	REFGND	COMMON	COMMON	TEST0	AGND ADC	DGND ADC	D9 SCLK	D8 SDOUT	H
J	+IN2	COMMON	COMMON	COMMON	INA	COMMON	INGND	AGND ADC	AGND ADC	OGND	OVDD	DVDD	J
K	COMMON	COMMON	COMMON	VOUT2	INB	COMMON	COMMON	COMMON	PD	$\overline{\text{CS\_ADC}}$	D6 INVSCLK	D7 RDC/SDN	K
L	RC2	COMMON	COMMON	RA2	INC	COMMON	BYTE SWAP	OB/$\overline{\text{2C}}$	IMPULSE	D1	D3 DIVSCLK1	D5 INVSYNC	L
M	COMMON	COMMON	RPAD2	RB2	IND	AVDD	WARP	SER/$\overline{\text{PAR}}$	D0	D2 DIVSCLK0	D4 EXT/$\overline{\text{INT}}$	AGND ADC	M
	1	2	3	4	5	6	7	8	9	10	11	12	

OUTLINE DIMENSIONS

144-Lead Chip Scale Ball Grid Array [CSPBGA]
(BC-144)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-205AC

NOTES
1. THE ACTUAL POSITION OF THE BALL POPULATION IS WITHIN 0.15 OF ITS IDEAL POSITION RELATIVE TO THE PACKAGE EDGES
2. THE ACTUAL POSITION OF EACH BALL IS WITHIN 0.08 OF ITS IDEAL POSITION RELATIVE TO THE BALL POPULATION

Revision History

Location	Page
2/03—Data Sheet changed from REV. 0 to REV. A.	
Edit to FUNCTIONAL BLOCK DIAGRAM	1
Edits to AMPLIFIER ELECTRICAL CHARACTERISTICS	9
Edit to ADC PIN FUNCTION DESCRIPTIONS	11
Edit to Figure 32	37
Changes to OUTLINE DIMENSIONS	43

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