Si5325

PRELIMINARY DATA SHEET

µP-PROGRAMMABLE PRECISION CLOCK MULTIPLIER

Description

The Si5325 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5325 accepts dual clock inputs ranging from 10 to 710 MHz and generates two clock outputs ranging from 10 to 945 MHz and select frequencies to 1.4 GHz. The two outputs are divided down separately from a common source. The device provides frequency translation combinations across this operating range. The Si5325 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. The Si5325 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5325 is ideal for providing clock multiplication in high performance timing applications.

Applications

- SONET/SDH OC-48/STM-16 and OC-192/STM-64 line cards
- GbE/10GbE, 1/2/4/8/10GFC line cards
- ITU G.709 and custom FEC line cards
- Optical modules
- Wireless basestations
- Data converter clocking
- xDSL
- SONET/SDH + PDH clock synthesis
- Test and measurement

Features

- Generates frequencies from 10 to 945 MHz and select frequencies to 1.4 GHz from an input frequency of 10 to 710 MHz
- Low jitter clock outputs with jitter generation as low as 0.5 ps rms (12 kHz–20 MHz)
- Integrated loop filter with selectable loop bandwidth (150 kHz to 2 MHz)
- Dual clock inputs w/manual or automatically controlled switching
- Dual clock outputs with selectable signal format (LVPECL, LVDS, CML, CMOS)
- Support for ITU G.709 and custom FEC ratios (255/238, 255/237, 255/236)
- LOS, FOS alarm outputs
- Digitally-controlled output phase adjust
- I^2C or SPI programmable
- On-chip voltage regulator for 1.8 ±5%, 2.5 or 3.3 V ±10% operation
- Small size: 6 x 6 mm 36-lead QFN
- Pb-free, ROHS compliant

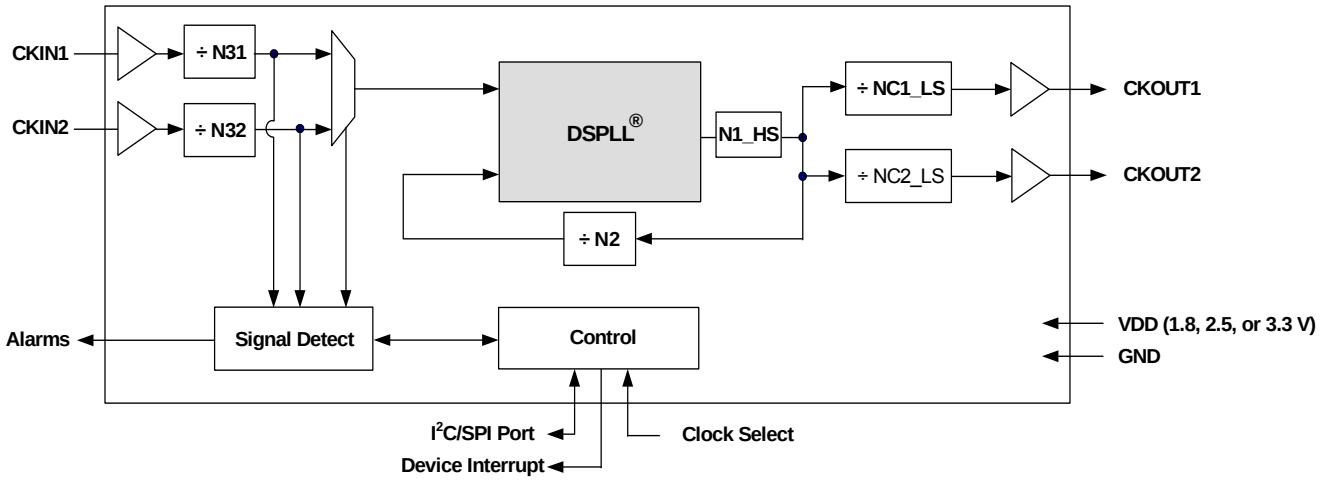

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Table 1. Performance Specifications

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.71	1.8	1.89	V
Supply Current	I_{DD}	f_{OUT} = 622.08 MHz Both CKOUTs enabled LVPECL format output	—	251	279	mA
		CKOUT2 disabled	—	217	243	mA
		f_{OUT} = 19.44 MHz Both CKOUTs enabled CMOS format output	—	204	234	mA
		CKOUT2 disabled	—	194	220	mA
		Disable Mode	—	165	—	mA
Input Clock Frequency (CKIN1, CKIN2)	CK_F	Input frequency and clock multiplication ratio determined by programming device PLL dividers. Consult Silicon Laboratories configuration software DSPLL-*sim* at www.silabs.com/timing (click on Documentation) to determine PLL divider settings for a given input frequency/clock multiplication ratio combination.	10	—	710	MHz
Output Clock Frequency (CKOUT1, CKOUT2)	CK_{OF}		.002 970 1213	— — —	945 1134 1400	MHz
Input Clocks (CKIN1, CKIN2)						
Input Voltage Level Limits	CKN_{VIN}		0	—	V_{DD}	V
Differential Voltage Swing	CKN_{DPP}		0.25	—	—	V_{PP}
Common Mode Voltage	CKN_{VCM}	1.8 V ±5%	0.9	—	1.4	V
		2.5 V ±10%	1.0	—	1.7	V
		3.3 V ±10%	1.1	—	1.95	V
Rise/Fall Time	CKN_{TRF}	20–80%		—	11	ns
Duty Cycle (Minimum Pulse Width)	CKN_{DC}	Whichever is smaller	40	—	60	%
			2	—	—	ns
Output Clocks (CKOUT1, CKOUT2)						
Common Mode	V_{OCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	V_{OD}		1.1	—	1.9	V
Single Ended Output Swing	V_{SE}		0.5	—	0.93	V
Rise/Fall Time	CKO_{TRF}	20–80%	—	230	350	ps
Duty Cycle Uncertainty	CKO_{DC}	LVPECL Differential 100 Ω Line-to-Line Measured at 50% point	–40	—	40	ps

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing (click on Documentation).

Table 1. Performance Specifications (Continued)

(V_{DD} = 1.8 ±5%, 2.5 ±10%, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PLL Performance						
Jitter Generation	J_{GEN}	f_{IN} = f_{OUT} = 622.08 MHz, LVPECL output format 50 kHz–80 MHz	—	0.47	—	ps rms
		12 kHz–20 MHz	—	0.48	—	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB
Phase Noise	CKO_{PN}	f_{IN} = f_{OUT} = 622.08 MHz 100 Hz offset	—	–85	—	dBc/Hz
		1 kHz offset	—	–90	—	dBc/Hz
		10 kHz offset	—	–113	—	dBc/Hz
		100 kHz offset	—	–118	—	dBc/Hz
		1 MHz offset	—	–132	—	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	–88	—	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	–93	—	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	38	—	ºC/W

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing (click on Documentation).

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.8	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
CKINn Voltage Level Limits	CKN_{VIN}	0 to V_{DD}	V
Operating Junction Temperature	T_{JCT}	–55 to 150	C
Storage Temperature Range	T_{STG}	–55 to 150	C
ESD HBM Tolerance (100 pF, 1.5 kΩ); All pins except CKIN+/CKIN–		2	kV
ESD MM Tolerance; All pins except CKIN+/CKIN–		150	V
ESD HBM Tolerance (100 pF, 1.5 kΩ); CKIN+/CKIN–		750	V
ESD MM Tolerance; CKIN+/CKIN–		100	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

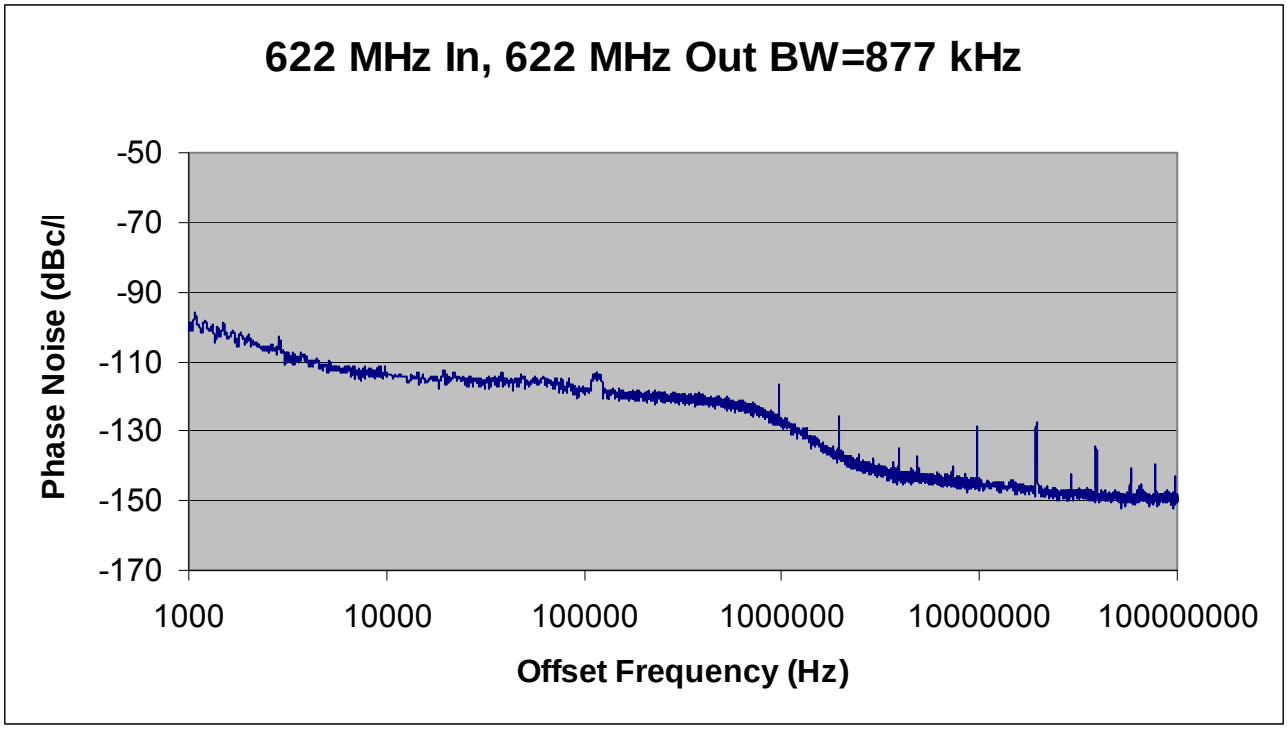
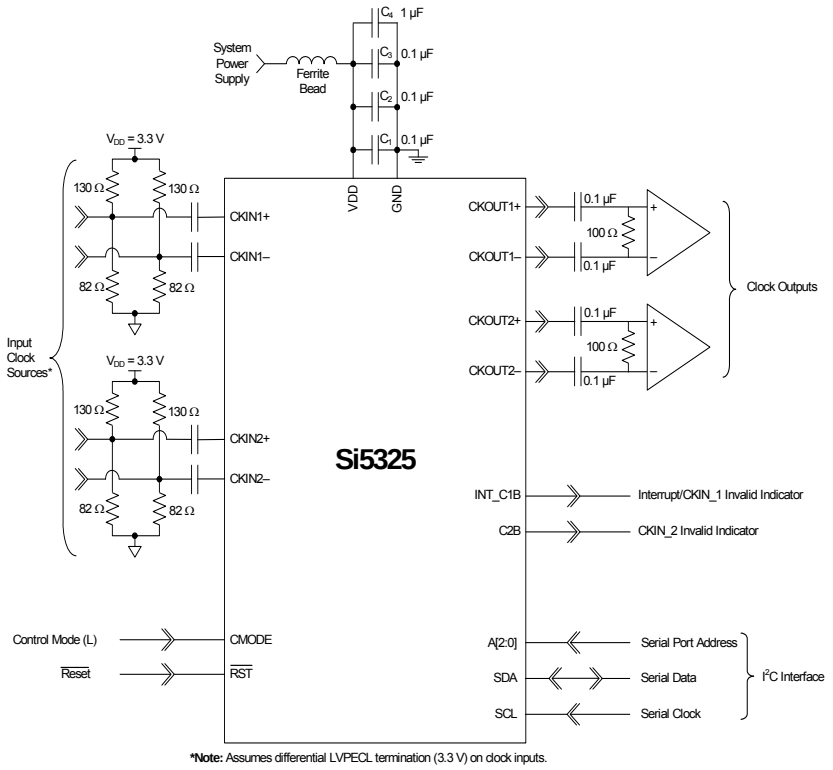


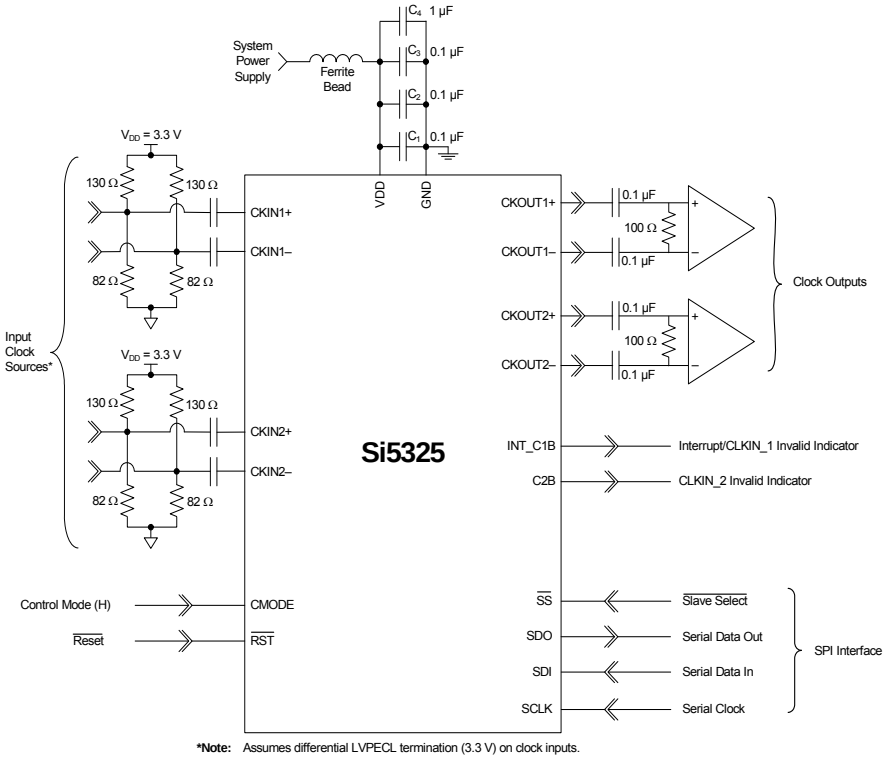
Figure 1. Typical Phase Noise Plot

Jitter Bandwidth	RMS Jitter (fs)
OC-48, 12 kHz to 20 MHz	374
OC-192, 20 kHz to 80 MHz	388
OC-192, 4 MHz to 80 MHz	181
OC-192, 50 kHz to 80 MHz	377
Broadband, 800 Hz to 80 MHz	420



***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

Figure 2. Si5325 Typical Application Circuit (I^2C Control Mode)



***Note:** Assumes differential LVPECL termination (3.3 V) on clock inputs.

Figure 3. Si5325 Typical Application Circuit (SPI Control Mode)

1. Functional Description

The Si5325 is a low jitter, precision clock multiplier for applications requiring clock multiplication without jitter attenuation. The Si5325 accepts dual clock inputs ranging from 10 to 710 MHz and generates two synchronous clock outputs ranging from 10 to 945 MHz and select frequencies to 1.4 GHz. The device provides frequency translation across this operating range. Independent dividers are available for each input clock and output clock, so the Si5325 can accept input clocks at different frequencies and it can generate output clocks at different frequencies. The Si5325 input clock frequency and clock multiplication ratio are programmable through an I^2C or SPI interface. Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that can be used to determine the optimum PLL divider settings for a given input frequency/clock multiplication ratio combination that minimizes phase noise and power consumption. This utility can be downloaded from http://www.silabs.com/timing (click on Documentation).

The Si5325 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides frequency synthesis in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The Si5325 PLL loop bandwidth is digitally programmable and supports a range from 30 kHz to 1.3 MHz. The DSPLL*sim* software utility can be used to calculate valid loop bandwidth settings for a given input clock frequency/clock multiplication ratio.

In the case when the input clocks enter alarm conditions, the PLL will freeze the DCO output frequency near its last value to maintain operation with an internal state close to the last valid operating state.

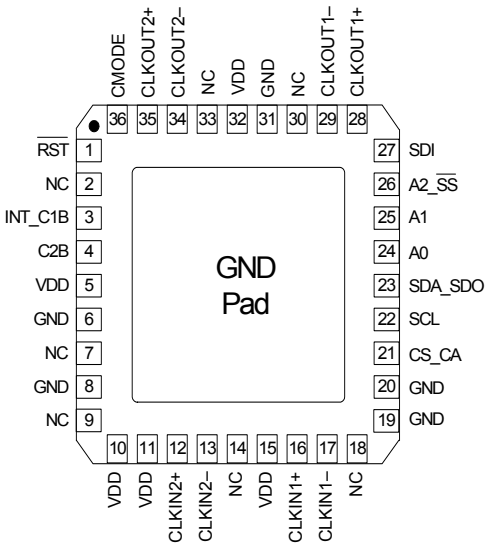
The Si5325 has two differential clock outputs. The electrical format of each clock output is independently programmable to support LVPECL, LVDS, CML, or CMOS loads. If not required, the second clock output can be powered down to minimize power consumption. In addition, the phase of one output clock may be adjusted in relation to the phase of the other output clock. The resolution varies from 800 ps to 2.2 ns depending on the PLL divider settings. Consult the DSPLL*sim* configuration software to determine the phase offset resolution for a given input clock/clock multiplication ratio combination. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

1.1. Further Documentation

Consult the Silicon Laboratories Any-Frequency Precision Clock Family Reference Manual (FRM) for detailed information about the Si5325. Additional design support is available from Silicon Laboratories through your distributor.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. The FRM and this utility can be downloaded from http://www.silabs.com/timing; click on Documentation.

2. Pin Descriptions: Si5325



Pin numbers are preliminary and subject to change.

Table 3. Si5325 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state and forces the device registers to their default value. Clock outputs are tristated during reset. The part must be programmed after a reset or power-on to get a clock output. See Family Reference Manual for details. This pin has a weak pull-up.
2, 7, 9, 14, 18, 30, 33	NC			**No Connect.** This pin must be left unconnected for normal operation.
3	INT_C1B	O	LVCMOS	**Interrupt/CKIN1 Invalid Indicator.** This pin functions as a device interrupt output or an alarm output for CKIN1. If used as an interrupt output, *INT_PIN* must be set to 1. The pin functions as a maskable interrupt output with active polarity controlled by the *INT_POL* register bit. If used as an alarm output, the pin functions as a LOS (and optionally FOS) alarm indicator for CKIN1. Set *CK1_BAD_PIN* = 1 and *INT_PIN* = 0. 0 = CKIN1 present. 1 = LOS (FOS) on CKIN1. The active polarity is controlled by *CK_BAD_POL*. If no function is selected, the pin tristates.
Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Si5325 Register Map.				

Table 3. Si5325 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
4	C2B	O	LVCMOS	**CKIN2 Invalid Indicator.** This pin functions as a LOS (and optionally FOS) alarm indicator for CKIN2 if *CK2_BAD_PIN* = 1. 0 = CKIN2 present. 1 = LOS (FOS) on CKIN2. The active polarity can be changed by *CK_BAD_POL*. If *CK2_BAD_PIN* = 0, the pin tristates.
5, 10, 11, 15, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following VDD pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should also be placed as close to device as is practical.
6, 8, 19, 20 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
12 13	CKIN2+ CKIN2–	I	Multi	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 10 to 710 MHz.
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal. Input frequency range is 10 to 710 MHz.
21	CS_CA	I/O	LVCMOS	**Input Clock Select/Active Clock Indicator.** **Input**: In manual clock selection mode, this pin functions as the manual input clock selector if the *CKSEL_PIN* is set to 1. 0 = Select CKIN1. 1 = Select CKIN2. If *CKSEL_PIN* = 0, the *CKSEL_REG* register bit controls this function. If configured as input, must be set high or low. **Output**: In automatic clock selection mode, this pin indicates which of the two input clocks is currently the active clock. If alarms exist on both clocks, CA will indicate the last active clock that was used before entering the VCO freeze state. The *CK_ACTV_PIN* register bit must be set to 1 to reflect the active clock status to the CA output pin. 0 = CKIN1 active input clock. 1 = CKIN2 active input clock. If *CK_ACTV_PIN* = 0, this pin will tristate. The CA status will always be reflected in the *CK_ACTV_REG* read only register bit.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Si5325 Register Map.

Table 3. Si5325 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
22	SCL	I	LVCMOS	**Serial Clock/Serial Clock.** This pin functions as the serial clock input for both SPI and I^2C modes. This pin has a weak pulldown.
23	SDA_SDO	I/O	LVCMOS	**Serial Data.** In I^2C control mode (CMODE = 0), this pin functions as the bidirectional serial data port. In SPI control mode (CMODE = 1), this pin functions as the serial data output.
25 24	A1 A0	I	LVCMOS	**Serial Port Address.** In I^2C control mode (CMODE = 0), these pins function as hardware controlled address bits. The I^2C address is 1101 [A2] [A1] [A0]. In SPI control mode (CMODE = 1), these pins are ignored. This pin has a weak pulldown.
26	A2_$\overline{SS}$	I	LVCMOS	**Serial Port Address/Slave Select.** In I^2C control mode (CMODE = 0), this pin functions as a hardware controlled address bit [A2]. In SPI control mode (CMODE = 1), this pin functions as the slave select input. This pin has a weak pulldown.
27	SDI	I	LVCMOS	**Serial Data In.** In I^2C control mode (CMODE = 0), this pin is ignored. In SPI control mode (CMODE = 1), this pin functions as the serial data input. This pin has a weak pulldown.
29 28	CKOUT1– CKOUT1+	O	Multi	**Output Clock 1.** Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by *SFOUT1_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
34 35	CKOUT2– CKOUT2+	O	Multi	**Output Clock 2.** Differential output clock with a frequency range of 10 MHz to 1.4175 GHz. Output signal format is selected by *SFOUT2_REG* register bits. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.
36	CMODE	I	LVCMOS	**Control Mode.** Selects I^2C or SPI control mode for the Si5325. 0 = I^2C Control Mode. 1 = SPI Control Mode. Must not float.
GND PAD	GND	GND	Supply	**Ground Pad.** The ground pad must provide a low thermal and electrical impedance to a ground plane.

Note: Internal register names are indicated by underlined italics, e.g., *INT_PIN*. See Si5325 Register Map.

3. Register Map

All register bits that are not defined in this map should always be written with the specified Reset Values. The writing to these bits of values other than the specified Reset Values may result in undefined device behavior. Registers not listed, such as Register 64, should never be written to.

Register	D7	D6	D5	D4	D3	D2	D1	D0
0			CKOUT_ ALWAYS_ ON				BYPASS_ REG	
1					CK_PRIOR2[1:0]		CK_PRIOR[1:0]	
2	BWSEL_REG[3:0]							
3	CKSEL_REG[1:0]			SQ_ICAL				
4	AUTOSEL_REG[1:0]							
5	ICMOS[1:0]							
6		SLEEP	SFOUT2_REG[2:0}			SFOUT1_REG[2:0]		
7						FOSREFSEL[2:0]		
8	HLOG_2[1:0]		HLOG_1[1:0]					
10					DSBL2_ REG	DSBL1_ REG		
11							PD_CK2	PD_CK1
19	FOS_EN	FOS_THR[1:0]		VALTIME[1:0]				
20					CK2_ BAD_ PIN	CK1_ BAD_ PIN		INT_PIN
21							CK1_ACTV_ PIN	CKSEL_PIN
22					CK_ACTV_ POL	CK_BAD_ POL		INT_POL
23						LOS2_MSK	LOS1_MSK	
24						FOS2_MSK	FOS1_MSK	
25	N1_HS[2:0]							
31					NC1_LS[19:16]			
32	NC1_LS[15:8]							
33	NC1_LS[7:0]							
34					NC2_LS[19:16]			
35	NC2_LS[15:8]							
36	NC2_LS[7:0]							

Register	D7	D6	D5	D4	D3	D2	D1	D0
40					N2_LS[19:16]			
41	N2_LS[15:8]							
42	N2_LS[7:0]							
43						N31[18:16]		
44	N31[15:8]							
45	N31[7:0]							
46						N32[18:16]		
47	N32[15:8]							
48	N32[7:0]							
55			CLKIN2RATE[2:0]			CLKIN1RATE[2:0]		
128							CK2_ACTV_REG	CK1_ACTV_REG
129						LOS2_INT	LOS1_INT	
130	CLAT-PROGRESS	DIGHOLD-VALID				FOS2_INT	FOS1_INT	
131						LOS2_FLG	LOS1_FLG	
132					FOS2_FLG	FOS1_FLG		
134	PARTNUM_RO[11:4]							
135	PARTNUM_RO[3:0]				REVID_RO[3:0]			
136	RST_REG	ICAL					GRADE_RO[1:0]	
138							LOS2_EN [1:1]	LOS1_EN [1:1]
139			LOS2_EN [0:0]	LOS1_EN [0:0]			FOS2_EN	FOS1_EN
142	INDEPENDENTSKEW1[7:0]							
143	INDEPENDENTSKEW2[7:0]							
185	NVM_REVID[7:0]							

4. Register Descriptions

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved	CKOUT_ ALWAYS_ ON	Reserved	Reserved	Reserved	BYPASS_ REG	Reserved
Type	R	R	R/W	R	R	R	R/W	R

Reset value = 0001 0100

Bit	Name	Function
7:6	Reserved	**Reserved.**
5	CKOUT_ ALWAYS_ON	**CKOUT Always On.** This will bypass the SQ_ICAL function. Output will be available even if SQ_ICAL is on and ICAL is not complete or successful. See Table 4 on page 46. 0: Squelch output until part is calibrated (ICAL). 1: Provide an output. Note: The frequency may be significantly off until the part is calibrated.
4:2	Reserved	**Reserved.**
1	BYPASS_ REG	**Bypass Register.** This bit enables or disables the PLL bypass mode. Use only when the device is in VCO freeze or before the first ICAL. Bypass mode is not supported for CMOS output clocks. 0: Normal operation 1: Bypass mode. Selected input clock is connected to CKOUT buffers, bypassing PLL.
0	Reserved	**Reserved.**

Register 1.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				CK_PRIOR2 [1:0]		CK_PRIOR1 [1:0]	
Type	R				R/W		R/W	

Reset value = 1110 0100

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:2	CK_PRIOR2 [1:0]	**CK_PRIOR 2.** Selects which of the input clocks will be 2nd priority in the autoselection state machine. 00: CKIN1 is 2nd priority. 01: CKIN2 is 2nd priority. 10: Reserved 11: Reserved
1:0	CK_PRIOR1 [1:0]	**CK_PRIOR 1.** Selects which of the input clocks will be 1st priority in the autoselection state machine. 00: CKIN1 is 1st priority. 01: CKIN2 is 1st priority. 10: Reserved 11: Reserved

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BWSEL_REG [3:0]				Reserved			
Type	R/W				R			

Reset value = 0100 0010

Bit	Name	Function
7:4	BWSEL_REG [3:0]	**BWSEL_REG.** Selects nominal f3dB bandwidth for PLL. See the DSPLLsim for settings. After BWSEL_REG is written with a new value, an ICAL is required for the change to take effect.
3:0	Reserved	**Reserved.**

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CKSEL_REG [1:0]		Reserved	SQ_ICAL	Reserved			
Type	R/W		R	R/W	R			

Reset value = 0000 0101

Bit	Name	Function
7:6	CKSEL_REG [1:0]	**CKSEL_REG.** If the device is operating in register-based manual clock selection mode (AUTOSEL_REG = 00), and CKSEL_PIN = 0, then these bits select which input clock will be the active input clock. If CKSEL_PIN = 1 and AUTOSEL_REG = 00, the CS_CA input pin continues to control clock selection and CKSEL_REG is of no consequence. 00: CKIN_1 selected. 01: CKIN_2 selected. 10: Reserved 11: Reserved
5	Reserved	**Reserved.**
4	SQ_ICAL	**SQ_ICAL.** This bit determines if the output clocks will remain enabled or be squelched (disabled) during an internal calibration. See Table 4 on page 46. 0: Output clocks enabled during ICAL. 1: Output clocks disabled during ICAL.
3:0	Reserved	**Reserved.**

Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	AUTOSEL_REG [1:0]		Reserved	Reserved				
Type	R/W		R	R				

Reset value = 0001 0010

Bit	Name	Function
7:6	AUTOSEL_ REG [1:0]	**AUTOSEL_REG [1:0].** Selects method of input clock selection to be used. 00: Manual (either register or pin controlled, see CKSEL_PIN) 01: Automatic Non-Revertive 10: Automatic Revertive 11: Reserved
5:0	Reserved	**Reserved.**

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ICMOS [1:0]		Reserved					
Type	R/W		R					

Reset value = 1110 1101

Bit	Name	Function
7:6	ICMOS [1:0]	**ICMOS [1:0].** When the output buffer is set to CMOS mode, these bits determine the output buffer drive strength. The first number below refers to 3.3 V operation; the second to 1.8 V operation. These values assume CKOUT+ is tied to CKOUT-. 00: 8mA/2mA. 01: 16mA/4mA 10: 24mA/6mA 11: 32mA/8mA
5:0	Reserved	**Reserved.**

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	SLEEP	SFOUT2_REG [2:0]			SFOUT1_REG [2:0]		
Type	R	R/W	R/W			R/W		

Reset value = 0010 1101

Bit	Name	Function
7	Reserved	**Reserved.**
6	SLEEP	**SLEEP.** In sleep mode, all clock outputs are disabled and the maximum amount of internal circuitry is powered down to reduce power dissipation and noise generation. This bit overrides the SFOUTn_REG[2:0] output signal format settings. 0: Normal operation 1: Sleep mode
5:3	SFOUT2_ REG [2:0]	**SFOUT2_REG [2:0].** Controls output signal format and disable for CKOUT2 output buffer. Bypass mode is not supported for CMOS output clocks. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS
2:0	SFOUT1_ REG [2:0]	**SFOUT1_REG [2:0].** Controls output signal format and disable for CKOUT1 output buffer. Bypass mode is not supported for CMOS output clocks. 000: Reserved 001: Disable 010: CMOS 011: Low swing LVDS 100: Reserved 101: LVPECL 110: CML 111: LVDS

Register 7.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					FOSREFSEL [2:0]		
Type	R					R/W		

Reset value = 0010 1010

Bit	Name	Function
7:3	Reserved.	**Reserved.**
2:0	FOSREFSEL [2:0]	**FOSREFSEL [2:0].** Selects which input clock is used as the reference frequency for Frequency Off-Set (FOS) alarms. 000: XA/XB (External reference) 001: CKIN1 010: CKIN2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved

Register 8.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	HLOG_2[1:0]		HLOG_1[1:0]		Reserved			
Type	R/W		R/W		R			

Reset value = 0000 0000

Bit	Name	Function
7:6	HLOG_2 [1:0]	**HLOG_2 [1:0].** 00: Normal operation 01: Holds CKOUT2 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10:Holds CKOUT2 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
5:4		**HLOG_1 [1:0].** 00: Normal operation 01: Holds CKOUT1 output at static logic 0. Entrance and exit from this state will occur without glitches or runt pulses. 10: Holds CKOUT1 output at static logic 1. Entrance and exit from this state will occur without glitches or runt pulses. 11: Reserved
3:0	Reserved	**Reserved.**

Register 10.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				DSBL2_ REG	DSBL1_ REG	Reserved	Reserved
Type	R				R/W	R/W	R	R

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3	DSBL2_REG	**DSBL2_REG.** This bit controls the powerdown of the CKOUT2 output buffer. If disable mode is selected, the NC2 output divider is also powered down. 0: CKOUT2 enabled 1: CKOUT2 disabled
2	DSBL1_REG	**DSBL1_REG.** This bit controls the powerdown of the CKOUT1 output buffer. If disable mode is selected, the NC1 output divider is also powered down. 0: CKOUT1 enabled 1: CKOUT1 disabled
1:0	Reserved	**Reserved.**

Register 11.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						PD_CK2	PD_CK1
Type	R						R/W	R/W

Reset value = 0100 0000

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	PD_CK2	**PD_CK2.** This bit controls the powerdown of the CKIN2 input buffer. 0: CKIN2 enabled 1: CKIN2 disabled
0	PD_CK1	**PD_CK1.** This bit controls the powerdown of the CKIN1 input buffer. 0: CKIN1 enabled 1: CKIN1 disabled

Register 19.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FOS_EN	FOS_THR [1:0]		VALTIME [1:0]		Reserved		
Type	R/W	R/W		R/W		R		

Reset value = 0010 1100

Bit	Name	Function
7:5	FOS_EN	**FOS_EN.** Frequency Offset Enable globally disables FOS. See the individual FOS enables (FOSX_EN, register 139). 0: FOS disable 1: FOS enabled by FOSx_EN
6:5	FOS_THR [1:0]	**FOS_THR [1:0].** Frequency Offset at which FOS is declared: 00: ± 11 to 12 ppm (Stratum 3/3E compliant, with a Stratum 3/3E used for REFCLK 01: ± 48 to 49 ppm (SMC) 10: ± 30 ppm (SONET Minimum Clock (SMC), with a Stratum 3/3E used for REFCLK. 11: ± 200 ppm
4:3	VALTIME [1:0]	**VALTIME [1:0].** Sets amount of time for input clock to be valid before the associated alarm is removed. 00: 2 ms 01: 100 ms 10: 200 ms 11: 13 seconds
2:0	Reserved	**Reserved.**

Register 20.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				CK2_BAD_PIN	CK1_BAD_PIN	Reserved	INT_PIN
Type	R				R/W	R/W	R	R/W

Reset value = 0011 1110

Bit	Name	Function
7:4	Reserved	**Reserved.**
3	CK2_BAD_PIN	**CK2_BAD_PIN.** The CK2_BAD status can be reflected on the C2B output pin. 0: C2B output pin tristated 1: C2B status reflected to output pin
2	CK1_BAD_PIN	**CK1_BAD_PIN.** The CK1_BAD status can be reflected on the C1B output pin. 0: C1B output pin tristated 1: C1B status reflected to output pin
1	Reserved	**Reserved.**
0	INT_PIN	**INT_PIN.** Reflects the interrupt status on the INT_C1B output pin. 0: Interrupt status not displayed on INT_C1B output pin. If CK1_BAD_PIN = 0, INT_C1B output pin is tristated. 1: Interrupt status reflected to output pin. Instead, the INT_C1B pin indicates when CKIN1 is bad.

Register 21.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved	Reserved					CK1_ACTV_PIN	CKSEL_ PIN
Type	R	Force 1	R	R	R	R	R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	CK1_ACTV_PIN	**CK1_ACTV_PIN.** The CK1_ACTV_REG status bit can be reflected to the CS_CA output pin using the CK1_ACTV_PIN enable function. CK1_ACTV_PIN is of consequence only when pin controlled clock selection is being used. 0: CS_CA output pin tristated. 1: Clock Active status reflected to output pin.
0	CKSEL_PIN	**CKSEL_PIN.** If manual clock selection is being used, clock selection can be controlled via the CKSEL_REG[1:0] register bits or the CS_CA input pin. This bit is only active when AUTOSEL_REG = Manual. 0: CS_CA pin is ignored. CKSEL_REG[1:0] register bits control clock selection. 1: CS_CA input pin controls clock selection.

Register 22.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				CK_ACTV_POL	CK_BAD_ POL	Reserved	INT_POL
Type	R				R/W	R/W	R	R/W

Reset value = 1101 1111

Bit	Name	Function
7:4	Reserved	**Reserved.**
3	CK_ACTV_ POL	**CK_ACTV_POL.** Sets the active polarity for the CS_CA signals when reflected on an output pin. 0: Active low 1: Active high
2	CK_BAD_ POL	**CK_BAD_POL.** Sets the active polarity for the INT_C1B and C2B signals when reflected on output pins. 0: Active low 1: Active high
1	Reserved	**Reserved.**
0	INT_POL	**INT_POL.** Sets the active polarity for the interrupt status when reflected on the INT_C1B output pin. 0: Active low 1: Active high

Register 23.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					LOS2_ MSK	LOS1_ MSK	Reserved
Type	R					R/W	R/W	R

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	**Reserved.**
2	LOS2_MSK	**LOS2_MSK.** Determines if a LOS on CKIN2 (LOS2_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS2_FLG register. 0: LOS2 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: LOS2_FLG ignored in generating interrupt output.
1	LOS1_MSK	**LOS1_MSK.** Determines if a LOS on CKIN1 (LOS1_FLG) is used in the generation of an interrupt. Writes to this register do not change the value held in the LOS1_FLG register. 0: LOS1 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: LOS1_FLG ignored in generating interrupt output.
0	Reserved	**Reserved.**

Register 24.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					FOS2_MSK	FOS1_MSK	Reserved
Type	R					R/W	R/W	R

Reset value = 0011 1111

Bit	Name	Function
7:3	Reserved	**Reserved.**
2	FOS2_MSK	**FOS2_MSK.** Determines if the FOS2_FLG is used to in the generation of an interrupt. Writes to this register do not change the value held in the FOS2_FLG register. 0: FOS2 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: FOS2_FLG ignored in generating interrupt output.
1	FOS1_MSK	**FOS1_MSK.** Determines if the FOS1_FLG is used in the generation of an interrupt. Writes to this register do not change the value held in the FOS1_FLG register. 0: FOS1 alarm triggers active interrupt on INT_C1B output (if INT_PIN=1). 1: FOS1_FLG ignored in generating interrupt output.
0	Reserved	**Reserved.**

Register 25.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N1_HS [2:0]			Reserved				
Type	R/W			R				

Reset value = 0010 0000

Bit	Name	Function
7:5	N1_HS [2:0]	**N1_HS [2:0].** Sets value for N1 high speed divider which drives NCn_LS (n = 1 to 2) low-speed divider. 000: N1= 4 Note: Changing the coarse skew via the INC pin is disabled for this value. 001: N1= 5 010: N1=6 011: N1= 7 100: N1= 8 101: N1= 9 110: N1= 10 111: N1= 11
4:0	Reserved	**Reserved.**

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				NC1_LS [19:16]			
Type	R				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	NC1_LS [19:16]	**NC1_LS [19:16].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC1_LS [15:8]	**NC1_LS [15:8].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC1_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC1_LS [19:0]	**NC1_LS [7:0].** Sets value for NC1 low-speed divider, which drives CKOUT1 output. Must be 0 or odd. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000011 = 4 0000000000000000101 = 6 ... 1111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				NC2_LS [19:16]			
Type	R				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	NC2_LS [19:16]	**NC2_LS [19:16].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000=1 00000000000000000001=2 00000000000000000011=4 00000000000000000101=6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	NC2_LS [15:8]	**NC2_LS [15:8].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 36.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NC2_LS [7:0]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	NC2_LS [7:0]	**NC2_LS [7:0].** Sets value for NC2 low-speed divider, which drives CKOUT2 output. Must be 0 or odd. 00000000000000000000 = 1 00000000000000000001 = 2 00000000000000000011 = 4 00000000000000000101 = 6 ... 11111111111111111111=2^20 Valid divider values=[1, 2, 4, 6, ..., 2^20]

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				N2_LS [19:16]			
Type	R				R/W			

Reset value = 1100 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	N2_LS [19:16]	**N2_LS [19:16].** Sets the value for the N2 low-speed divider, which drives the phase detector. Must be an even number ranging from 32 to 512 (inclusive). 00000000000000100000 = 32 00000000000000100010 = 34 00000000000000100100 = 36 ... 00000000001000000000 = 512 Valid divider values = [32, 34, 36...512]

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N2_LS [15:8]	**N2_LS [15:8].** Sets the value for the N2 low-speed divider, which drives the phase detector. Must be an even number ranging from 32 to 512 (inclusive). 0000000000000100000 = 32 0000000000000100010 = 34 0000000000000100100 = 36 ... 0000000001000000000 = 512 Valid divider values = [32, 34, 36...512]

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N2_LS [7:0]							
Type	R/W							

Reset value = 1111 1001

Bit	Name	Function
7:0	N2_LS [7:0]	**N2_LS [7:0].** Sets the value for the N2 low-speed divider, which drives the phase detector. Must be an even number ranging from 32 to 512 (inclusive). 0000000000000100000 = 32 0000000000000100010 = 34 0000000000000100100 = 36 ... 0000000001000000000 = 512 Valid divider values = [32, 34, 36...512]

Register 43.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					N31 [18:16]		
Type	R					R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	N31 [18:16]	**N31 [18:16].** Sets value for input divider for CKIN1. 000000000000000000 = 1 000000000000000001 = 2 000000000000000010 = 3 ... 111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 44.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N31_[15:8]	**N31_[15:8].** Sets value for input divider for CKIN1. 000000000000000000 = 1 000000000000000001 = 2 000000000000000010 = 3 ... 111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 45.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N31_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N31_[7:0	**N31_[7:0].** Sets value for input divider for CKIN1. 00000000000000000 = 1 00000000000000001 = 2 00000000000000010 = 3 ... 11111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 46.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					N32_[18:16]		
Type	R					R/W		

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	N32_[18:16]	**N32_[18:16].** Sets value for input divider for CKIN2. 00000000000000000 = 1 00000000000000001 = 2 00000000000000010 = 3 ... 11111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[15:8]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	N32_[15:8]	N32_[15:8]. Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	N32_[7:0]							
Type	R/W							

Reset value = 0000 1001

Bit	Name	Function
7:0	N32_[7:0]	**N32_[7:0].** Sets value for input divider for CKIN2. 0000000000000000000 = 1 0000000000000000001 = 2 0000000000000000010 = 3 ... 1111111111111111111 = 2^19 Valid divider values=[1, 2, 3, ..., 2^19]

Register 55h.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		CLKIN2RATE_[2:0]			CLKIN1RATE[2:0]		
Type	R		R/W			R/W		

Reset value = 0000 0000

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:3	CLKIN2RATE[2:0]	**CLKIN2RATE[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10 - 27 MHz 001: 25 - 54 MHz 002: 50 - 105 MHz 003: 95 - 215 MHz 004: 190 - 435 MHz 005: 375 - 710 MHz 006: Reserved 007: Reserved
2:0	CLKIN1RATE [2:0]	**CLKIN1RATE[2:0].** CKINn frequency selection for FOS alarm monitoring. 000: 10 - 27 MHz 001: 25 - 54 MHz 002: 50 - 105 MHz 003: 95 - 215 MHz 004: 190 - 435 MHz 005: 375 - 710 MHz 006: Reserved 007: Reserved

Register 128.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						CK2_ACTV_REG	CK1_ACTV_REG
Type	R						R	R

Reset value = 0010 0000

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	CK2_ACTV_REG	**CK2_ACTV_REG.** Indicates if CKIN2 is currently the active clock for the PLL input. 0: CKIN2 is not the active input clock. Either it is not selected or LOS2_INT is 1. 1: CKIN2 is the active input clock.
0	CK1_ACTV_REG	**CK1_ACTV_REG.** Indicates if CKIN1 is currently the active clock for the PLL input. 0: CKIN1 is not the active input clock. Either it is not selected or LOS1_INT is 1. 1: CKIN1 is the active input clock.

Register 129.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					LOS2_INT	LOS1_INT	Reserved
Type	R					R	R	R

Reset value = 0000 0110

Bit	Name	Function
7:3	Reserved	**Reserved.**
2	LOS2_INT	**LOS2_INT.** Indicates the LOS status on CKIN2. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN2 input.
1	LOS1_INT	**LOS1_INT.** Indicates the LOS status on CKIN1. 0: Normal operation. 1: Internal loss-of-signal alarm on CKIN1 input.
0	Reserved	**Reserved.**

Register 130.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CLATPROGRESS	Reserved				FOS2_INT	FOS1_INT	Reserved
Type	R	R				R	R	R

Reset value = 0000 0001

Bit	Name	Function
7	CLAT-PROGRESS	**CLAT Progress.** Indicates if the last change in the CLAT register has been processed. 0: Coarse skew adjustment not in progress. 1: Coarse skew adjustment in progress.
6:3	Reserved	**Reserved.**
2	FOS2_INT	**CKIN2 Frequency Offset Status.** 0: Normal operation. 1: Internal frequency offset alarm on CKIN2 input.
1	FOS1_INT	**CKIN1 Frequency Offset Status.** 0: Normal operation. 1: Internal frequency offset alarm on CKIN1 input.
0	Reserved	**Reserved.**

Register 131.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved					LOS2_FLG	LOS1_FLG	Reserved
Type	R					R/W	R/W	R

Reset value = 0001 1111

Bit	Name	Function
7:3	Reserved	**Reserved.**
2	LOS2_FLG	**CKIN2 Loss-of-Signal Flag.** 0: Normal operation. 1: Held version of LOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS2_MSK bit. Flag cleared by writing 0 to this bit.
1	LOS1_FLG	**CKIN1 Loss-of-Signal Flag.** 0: Normal operation 1: Held version of LOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by LOS1_MSK bit. Flag cleared by writing 0 to this bit.
0	Reserved	**Reserved.**

Register 132.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved				FOS2_FLG	FOS1_FLG	Reserved	Reserved
Type	R				R/W	R/W	R	R

Reset value = 0000 0010

Bit	Name	Function
7:4, 0	Reserved	**Reserved.**
3	FOS2_FLG	**CLKIN_2 Frequency Offset Flag.** 0: Normal operation. 1: Held version of FOS2_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS2_MSK bit. Flag cleared by writing 0 to this bit.
2	FOS1_FLG	**CLKIN_1 Frequency Offset Flag.** 0: Normal operation 1: Held version of FOS1_INT. Generates active output interrupt if output interrupt pin is enabled (INT_PIN = 1) and if not masked by FOS1_MSK bit. Flag cleared by writing 0 to this bit.
1	Reserved	**Reserved.**

Register 134.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [11:4]							
Type	R							

Reset value = 0000 0001

Bit	Name	Function
7:0	PARTNUM_ RO [11:0]	**Device ID (1 of 2).** 0000 0001 1001: Si5325

Register 135.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PARTNUM_RO [3:0]				REVID_RO [3:0]			
Type	R				R			

Reset value = 1010 0010

Bit	Name	Function
7:4	PARTNUM_ RO [11:0]	**Device ID (2 of 2).** 0000 0001 1001: Si5325
3:0	REVID_RO [3:0]	**Indicates Revision Number of Device.** 0000: Revision A 0001: Revision B 0010: Revision C Others: Reserved

Register 136.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RST_REG	ICAL	Reserved				GRADE_RO [1:0]	
Type	R/W	R/W	R				R	

Reset value = 0000 0000

Bit	Name	Function
7	RST_REG	**Internal Reset (Same as Pin Reset).** **Note:** The I2C (or SPI) port may not be accessed until 10 ms after RST_REG is asserted. 0: Normal operation. 1: Reset of all internal logic. Outputs disabled or tristated during reset.
6	ICAL	**Start an Internal Calibration Sequence.** For proper operation, the device must go through an internal calibration sequence. ICAL is a self-clearing bit. Writing a one to this location initiates an ICAL. The calibration is complete once the LOL alarm goes low. A valid stable clock (within 100 ppm) must be present to begin ICAL. Note: Any divider, CLKINn_RATE or BWSEL_REG changes require an ICAL to take effect. 0: Normal operation. 1: Writing a "1" initiates internal self-calibration. Upon completion of internal self-calibration, LOL will go low.
5:2	Reserved	**Reserved.**
1:0	GRADE_RO [1:0]	**Indicates Maximum Clock Output Frequency of this Device.** Limits the range of the N1_HS divider. 00: N1_HS x NCn_LS > 4. Maximum clock output frequency = 1.4175 GHz. 01: N1_HS x NCn_LS > 6. Maximum clock output frequency = 808 MHz. 10: N1_HS x NCn_LS > 14. Maximum clock output frequency = 346 MHz. 11: N1_HS x NCn_LS > 20. Maximum clock output frequency = 243 MHz.

Register 138.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						LOS2_EN [1:4]	LOS1_EN [1:1]
Type	R						R/W	R/W

Reset value = 0000 1111

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	LOS2_EN [1:0]	**Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).** **Note:** LOS2_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. SEe the Family Reference Manual for details.
0	LOS1_EN [1:0]	**Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the Family Reference Manual for details.

Register 139.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved		LOS2_EN [0:0]	LOS1_EN [0:0]	Reserved		FOS2_EN	FOS1_EN
Type	R		R/W	R/W	R		R/W	R/W

Reset value = 1111 1111

Bit	Name	Function
7:6, 3:2	Reserved	**Reserved.**
5	LOS2_EN [1:0]	**Enable CKIN2 LOS Monitoring on the Specified Input (2 of 2).** **Note:** LOS2_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details
4	LOS1_EN [1:0]	**Enable CKIN1 LOS Monitoring on the Specified Input (1 of 2).** **Note:** LOS1_EN is split between two registers. 00: Disable LOS monitoring. 01: Reserved. 10: Enable LOSA monitoring. 11: Enable LOS monitoring. LOSA is a slower and less sensitive version of LOS. See the family reference manual for details.
1	FOS2_EN	**Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.
0	FOS1_EN	**Enables FOS on a Per Channel Basis.** 0: Disable FOS monitoring. 1: Enable FOS monitoring.

Register 142.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW1 [7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPENDENTSKEW1 [7:0]	**INDEPENDENTSKEW1.** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. Default = 0.

Register 143.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INDEPENDENTSKEW2 [7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	INDEPEND-ENTSKEW2 [7:0]	**INDEPENDENTSKEW2.** 8 bit field that represents a twos complement of the phase offset in terms of clocks from the high speed output divider. Default = 0.

Register 185.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NVM_REVID [7:0]							
Type	R							

Reset value = 0001 0011

Bit	Name	Function
7:0	NVM_REVID [7:0]	**NVM_REVID.**

Table 4. CKOUT_ALWAYS_ON and SQICAL Truth Table

CKOUT_ALWAYS_ON	SQICAL	Results	Output to Output Skew Preserved?
0	0	CKOUT OFF until after the first ICAL	N
0	1	CKOUT OFF until after the first successful ICAL (i.e., when LOL is low)	Y
1	0	CKOUT always ON, including during an ICAL	N
1	1	CKOUT always ON, including during an ICAL	Y

Table 5 lists all of the register locations that should be followed by an ICAL after their contents are changed.

Table 5. Register Locations Requiring ICAL

Addr	Register
0	BYPASS_REG
0	CKOUT_ALWAYS_ON
1	CK_PRIOR2
1	CK_PRIOR1
2	BWSEL_REG
4	HIST_DEL
5	ICMOS
7	FOSREFSEL
9	HIST_AVG
10	DSBL2_REG
10	DSBL1_REG
11	PD_CK2
11	PD_CK1
19	FOS_EN
19	FOS_THR
19	VALTIME
19	LOCKT
21	INCDEC_PIN
25	N1_HS
31	NC1_LS
34	NC2_LS
40	N2_HS
40	N2_LS
43	N31
46	N32
55	CLKIN2RATE
55	CLKIN1RATE

5. Ordering Guide

Ordering Part Number	Output Clock Frequency Range	Package	ROHS6, Pb-Free	Temperature Range
Si5325A-C-GM	10–945 MHz 970–1134 MHz 1.213–1.417 GHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5325B-C-GM	10–808 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C
Si5325C-C-GM	10–346 MHz	36-Lead 6 x 6 mm QFN	Yes	–40 to 85 °C

6. Package Outline: 36-Pin QFN

Figure 4 illustrates the package details for the Si5325. Table 6 lists the values for the dimensions shown in the illustration.

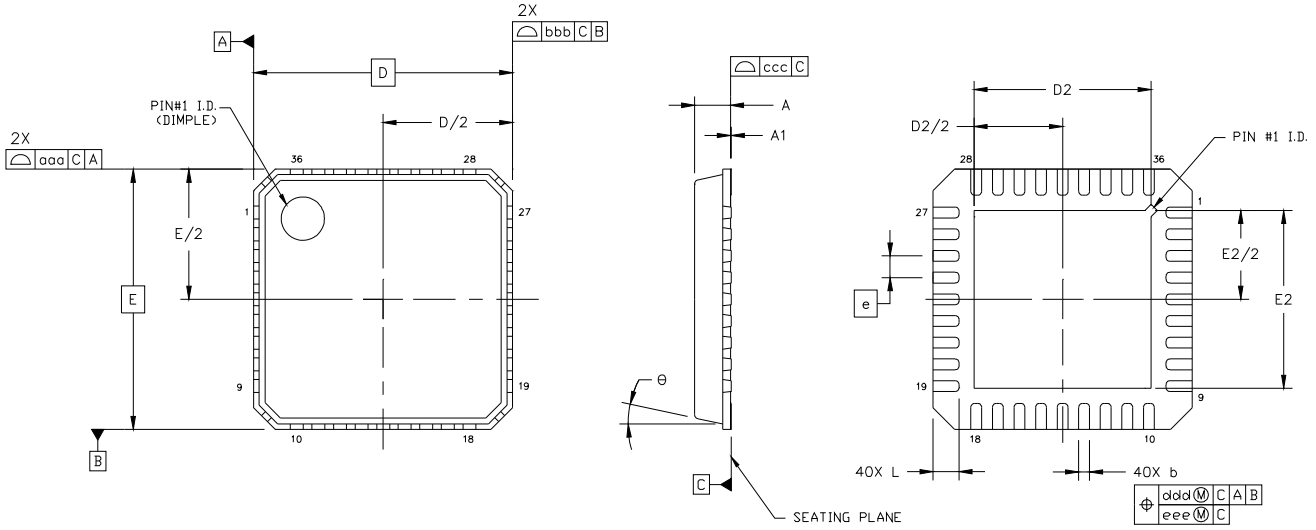


Figure 4. 36-Pin Quad Flat No-lead (QFN)

Table 6. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		6.00 BSC	
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.70
θ	—	—	12º
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Recommended PCB Layout

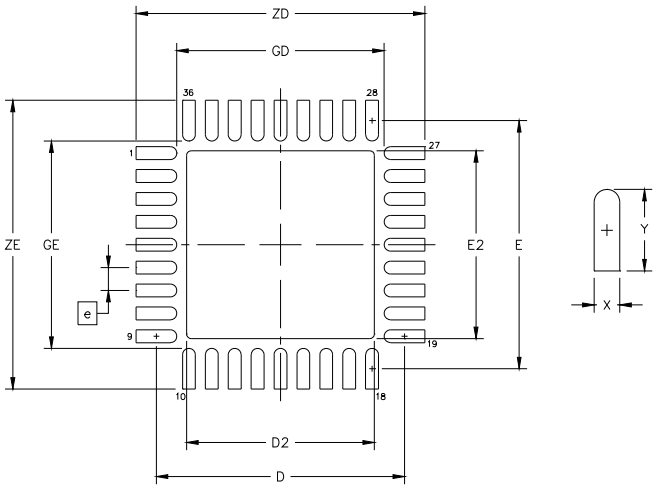


Figure 5. PCB Land Pattern Diagram

Table 7. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

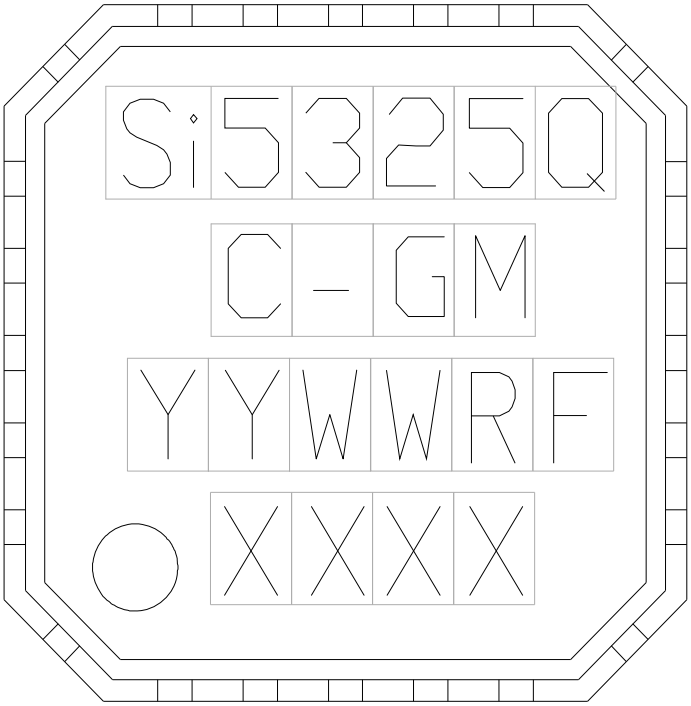
Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Mark



Mark Method:	Laser	
Font Size:	0.80 mm Right-Justified	
Line 1 Marking:	Si5325Q	Customer Part Number Q = Speed Code: A, B, C, D See Ordering Guide for options.
Line 2 Marking:	C-GM	C = Product Revision G = Temperature Range –40 to 85 °C (RoHS6) M = QFN Package
Line 3 Marking:	YYWWRF	YY = Year WW = Work Week R = Die Revision F = Internal code Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 4 Marking:	Pin 1 Identifier	Circle = 0.75 mm Diameter Lower-Left Justified
	XXXX	Internal Code

DOCUMENT CHANGE LIST

Revision 0.23 to Revision 0.24

- Clarified that the two outputs have a common, higher frequency source on page 1.
- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 5.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Updated “2. Pin Descriptions: Si5325”.
  - Removed references to latency control, INC, and DEC.
  - Changed font for register names to underlined italics.
- Updated "5. Ordering Guide" on page 47.
- Added “7. Recommended PCB Layout”.

Revision 0.24 to Revision 0.25

- Updated Section "2. Pin Descriptions: Si5325" on page 9.

Revision 0.25 to Revision 0.26

- Removed Figure 1. “Typical Phase Noise Plot.”
- Changed pins 11 and 15 from NC to VDD in “2. Pin Descriptions: Si5325”.

Revision 0.26 to Revision 0.3

- Changed 1.8 V operating range to ±5%.
- Updated Table 1 on page 4.
- Updated Table 2 on page 5.
- Added page 6.
- Updated "1. Functional Description" on page 8.
- Clarified "2. Pin Descriptions: Si5325" on page 9 including pull-up/pull-down.

Revision 0.3 to Revision 0.4

- Added register map
- Lowered minimum CKOUT frequency
- Updated spec tables
  - ESD tolerance, Table 2 on page 5
  - Minimum input and output clock frequencies, Table 1 on page 4
  - Absolute maximum VDD voltage, Table 2 on page 5
- Added to spec table
  - CKIN voltage limits, Table 2 on page 5
  - Typical jitter and phase noise values, Table 1 on page 4
- No bypass mode with CMOS outputs

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