FEMTOCLOCK™ JITTER ATTENUATOR & FREQUENCY TRANSLATOR W/LVPECL OUTPUTS

ICS813253

General Description

The ICS813253 is a member of the HiperClockS™ family of high performance clock solutions from IDT. The ICS813253 is a PLL based synchronous clock generator that is optimized for Gigabit Ethernet and PCI-Express clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock frequency multiplier that provides the low jitter, high frequency Gigabit Ethernet or PCI-Express output clock.

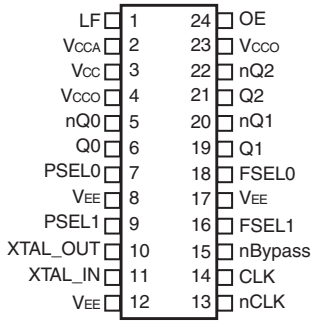
Predivider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in Gigabit Ethernet and PCI-Express applications. The VCXO requires the use of an external, inexpensive pullable crystal. The VCXO uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics.

Features

- Three differential LVPECL outputs
- One differential input supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Accepts input frequencies from 19.6MHz to 136MHz, including: 25MHz, 62.5MHz, 100MHz and 125MHz input clocks
- Attenuates the phase jitter of the input clock by using a low-cost pullable funamental mode VCXO crystal
- Outputs common Gigabit Ethernet or PCI-Express clock rates
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- Absolute pull range: 110ppm
- FemtoClock frequency multiplier provides low jitter, high frequency output
- FemtoClock range: 490MHz - 680MHz
- RMS phase jitter @ 156.25MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.37ps (typical)
- Full 3.3Vsupply, or 3.3V Core/2.5V output supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment

ICS813253
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View



Block Diagram

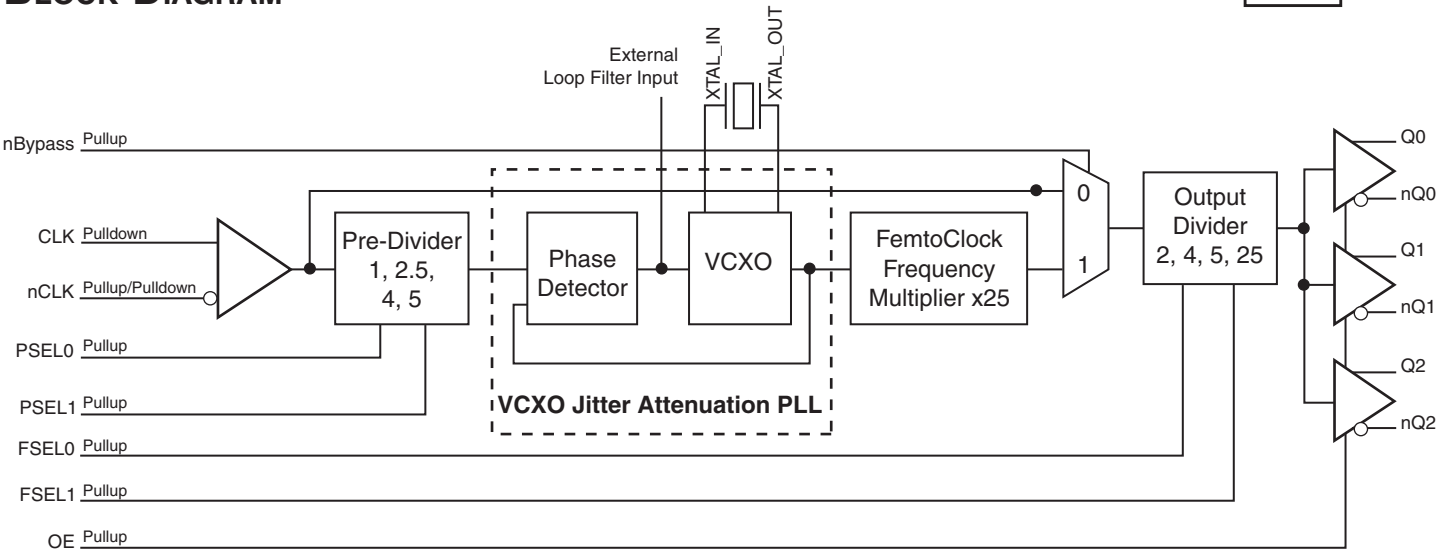


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	LF	Analog Input/Output		Loop filter connection node pin.
2	V_{CCA}	Power		Analog supply pin.
3	V_{CC}	Power		Core power supply pin.
4, 23	V_{CCO}	Power		Output power supply pins.
5, 6	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.
7, 9	PSEL0, PSEL1	Input	Pullup	Pre-divider select pins. See Table 3A.
8, 12, 17	V_{EE}	Power		Negative supply pins.
10, 11	XTAL_OUT, XTAL_IN	Input		VCXO crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
13	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{CC}/2 bias voltage when left floating.
14	CLK	Input	Pulldown	Non-inverting differential clock input.
15	nBypass	Input	Pullup	PLL Bypass control pin. See Table 3D.
16, 18	FSEL1, FSEL0	Input	Pullup	Select pins. See Table 3B.
19, 20	Q1, nQ1	Output		Differential clock outputs. LVPECL interface levels.
21, 22	Q2, nQ2	Output		Differential clock outputs. LVPECL interface levels.
24	OE	Input	Pullup	Output enable. When logic LOW, the clock outputs are HiZ. When logic HIGH, the clock outputs are enabled. LVCMOS/LVTTL interface levels. See Table 3C.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3A. PRE-DIVIDER FUNCTION TABLE

Inputs		Pre-divider Function
PSEL1	PSEL0	
0	0	÷1
0	1	÷2.5
1	0	÷4
1	1	÷5

TABLE 3B. FSEL FUNCTION TABLE

Inputs		Output Divider Function
FSEL1	FSEL0	
0	0	÷2
0	1	÷4
1	0	÷5
1	1	÷25

TABLE 3C. OE FUNCTION TABLE

Input	Clock Outputs	
OE	Q0:Q2	nQ0:nQ2
0	LOW	HIGH
1	Enabled	Enabled

TABLE 3D. BYPASS FUNCTION TABLE

nBypass Input	Operation
0	VCXO jitter attenuation PLL and FemtoClock multiplier bypassed. Input passed directly to N divider.
1 (default)	Normal operation mode.

TABLE 3E. FREQUENCY FUNCTION TABLE

Input Frequency (MHz)	PSEL1:0	Input Divider	VCXO Frequency (MHz)	FemtoClock Frequency (MHz)	FSEL1:0	Output Divider	Output Frequency (MHz)
25	00	1	25	625	00	2	312.5
25	00	1	25	625	01	4	156.25
25	00	1	25	625	10	5	125
25	00	1	25	625	11	25	25
62.5	01	2.5	25	625	00	2	312.5
62.5	01	2.5	25	625	01	4	156.25
62.5	01	2.5	25	625	10	5	125
62.5	01	2.5	25	625	11	25	25
100	10	4	25	625	00	2	312.5
100	10	4	25	625	01	4	156.25
100	10	4	25	625	10	5	125
100	10	4	25	625	11	25	25
100	11	5	20	500	00	2	250
100	11	5	20	500	01	4	125
100	11	5	20	500	10	5	100
100	11	5	20	500	11	25	20
125	11	5	25	625	00	2	312.5
125	11	5	25	625	01	4	156.25
125	11	5	25	625	10	5	125
125	11	5	25	625	11	25	25

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A=0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.12	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				132	mA
I_{CCA}	Analog Supply Current				12	mA
I_{CCO}	Output Supply Current				19	mA

Table 4B. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 2.5V±5\%$, T_A=0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.12	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{EE}	Power Supply Current				132	mA
I_{CCA}	Analog Supply Current				12	mA
I_{CCO}	Output Supply Current				19	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{CC} = 3.3V±5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	$V_{CC} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	$V_{CC} = 3.465V$, $V_{IN} = 0V$	-150			µA

TABLE 4D. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, T_A=0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK, CLK	$V_{IN} = V_{CC} = 3.465V$			150	µA
I_{IL}	Input Low Current	nCLK	V_{IN} = 0V, V_{CC} = 3.465V	-150			µA
		CLK	V_{IN} = 0V, V_{CC} = 3.465V	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{CC} + 0.3V.

TABLE 4E. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 3.3V±5\%$ OR $2.5V±5\%$, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 5A. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A=0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	PSEL = ÷1	19.6		27.2	MHz
		PSEL = ÷2.5	49		68	MHz
		PSEL = ÷4	78.4		108.8	MHz
		PSEL = ÷5	98		136	MHz
f_{OUT}	Output Frequency	FSEL = ÷2	245		340	MHz
		FSEL = ÷4	122.5		170	MHz
		FSEL = ÷5	98		136	MHz
		FSEL = ÷25	19.6		27.2	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	156.25MHz, 25MHz crystal Integration Range: 1.875MHz - 20MHz		0.37		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	400		800	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2, 3		8		40	ps
*t*jit(per)	Period Jitter; NOTE 4		1		3	ps
*t*sk(o)	Output Skew; NOTE 3, 5				60	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	PLL Lock Time					ms

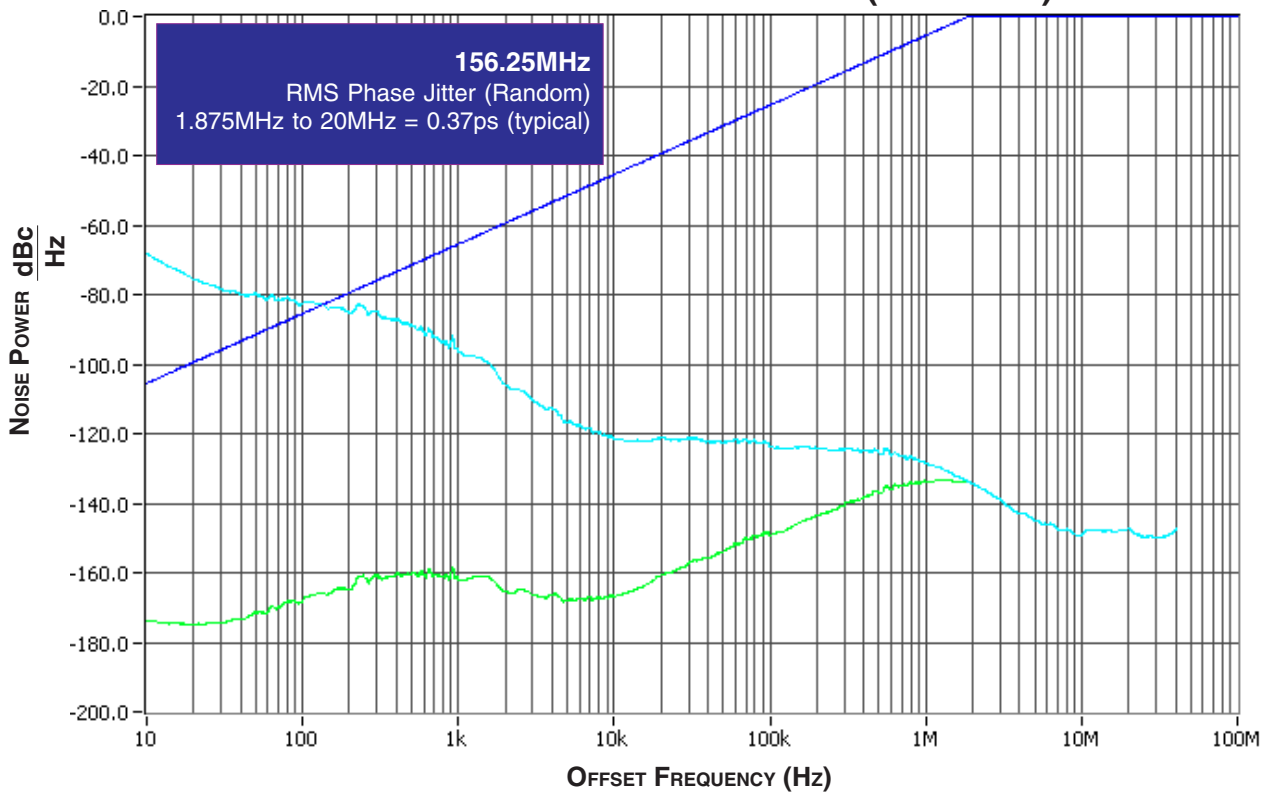
NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Jitter performance using crystal inputs.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load condtions.
Measured at the output differential cross points.

TABLE 5B. AC CHARACTERISTICS, $V_{CC} = V_{CCA} = 3.3V±5\%$, $V_{CCO} = 2.5V±5\%$, T_A=0°C TO 70°C

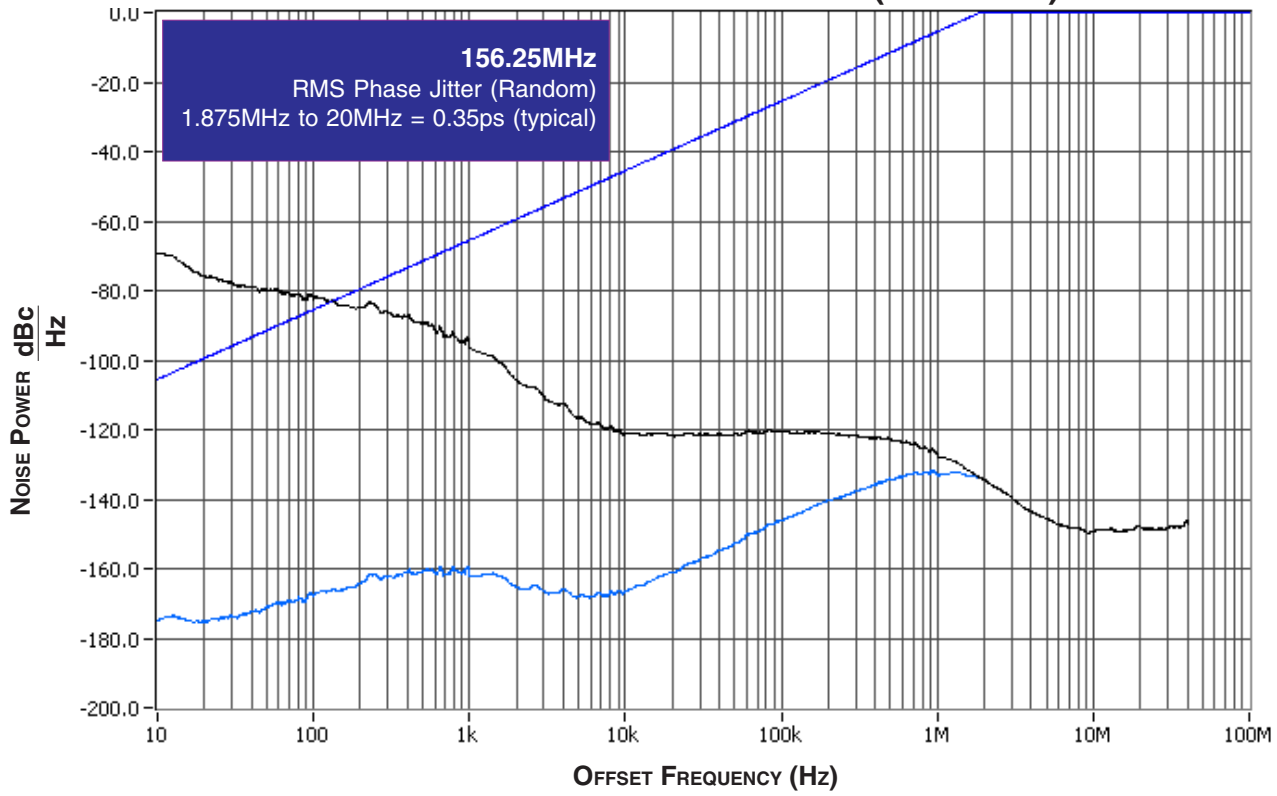
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency	PSEL = ÷1	19.6		27.2	MHz
		PSEL = ÷2.5	49		68	MHz
		PSEL = ÷4	78.4		108.8	MHz
		PSEL = ÷5	98		136	MHz
f_{OUT}	Output Frequency	FSEL = ÷2	245		340	MHz
		FSEL = ÷4	122.5		170	MHz
		FSEL = ÷5	98		136	MHz
		FSEL = ÷25	19.6		27.2	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	156.25MHz, 25MHz crystal Integration Range: 1.875MHz - 20MHz		0.35		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		700	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2, 3		7.5		40	ps
*t*jit(per)	Period Jitter; NOTE 4		0.5		2.5	ps
*t*sk(o)	Output Skew; NOTE 3, 5				60	ps
odc	Output Duty Cycle		48		52	%
t_{LOCK}	PLL Lock Time					ms

NOTE 1: Please refer to the Phase Noise Plot.
NOTE 2: Outputs terminated with 50Ω to V_{CCO} - 2V.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Jitter performance using crystal inputs.
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load condtions. Measured at the output differential cross points.

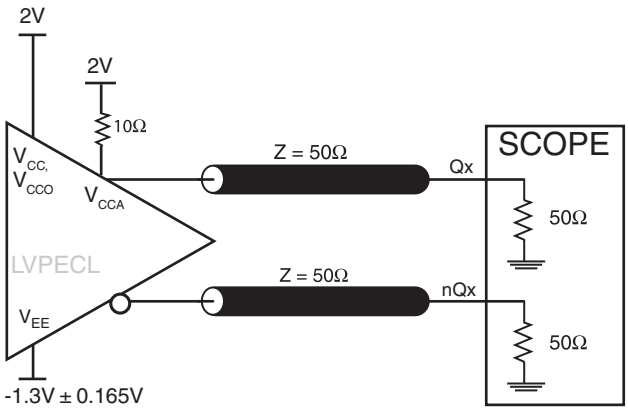
TYPICAL PHASE NOISE AT 156.25MHZ (3.3V/3.3V)



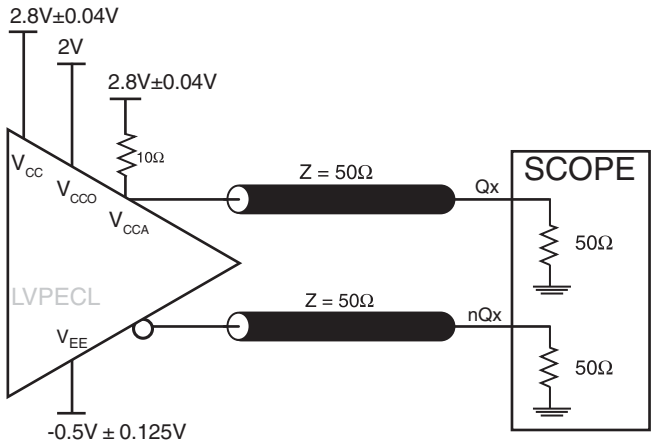
TYPICAL PHASE NOISE AT 156.25MHZ (3.3V/2.5V)



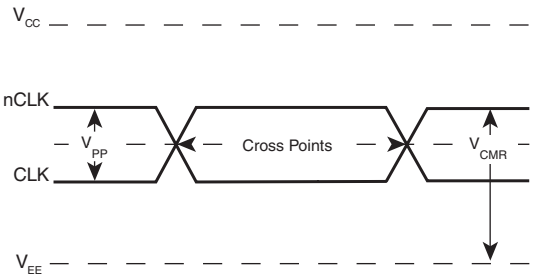
PARAMETER MEASUREMENT INFORMATION



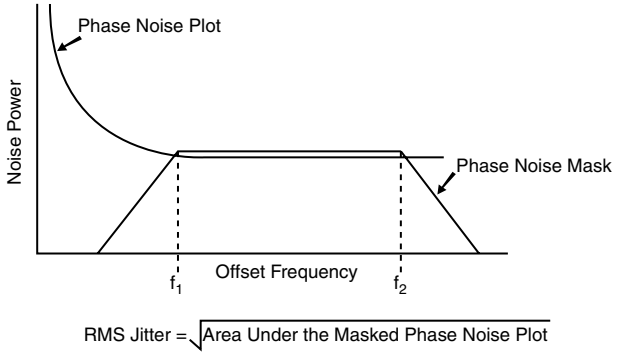
3.3V OUTPUT LOAD AC TEST CIRCUIT



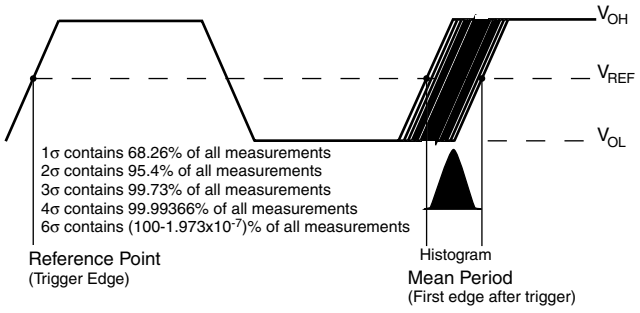
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



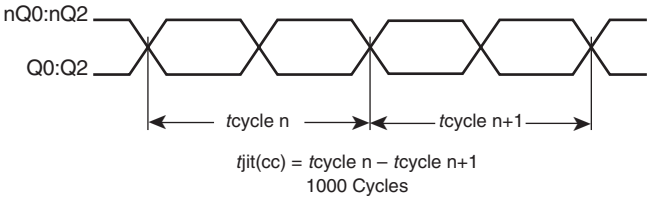
DIFFERENTIAL INPUT LEVEL



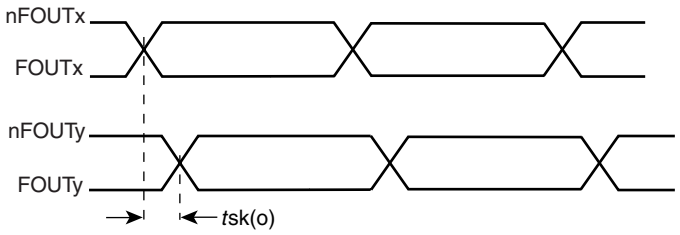
RMS PHASE JITTER



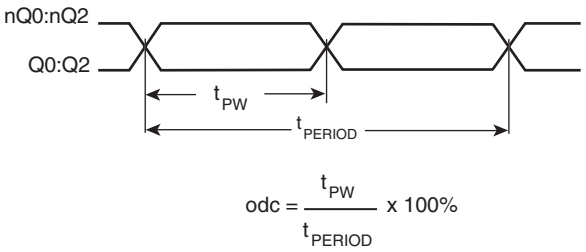
PERIOD JITTER



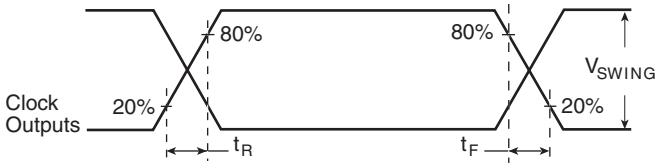
CYCLE-TO-CYCLE JITTER



OUTPUT SKEW



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS813253 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a 10mF and a .01mF bypass capacitor should be connected to each V_{CCA} pin.

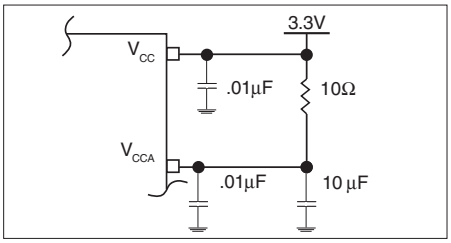


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ~ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

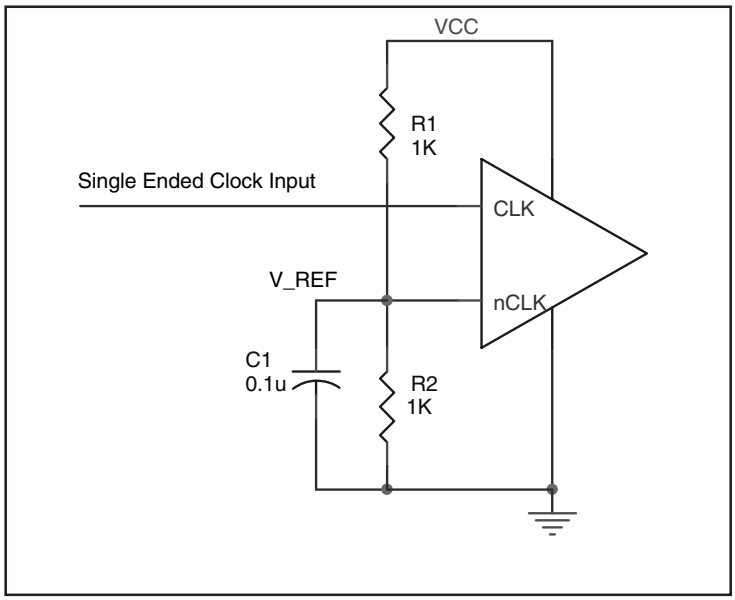


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK/nCLK Input:
For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Output
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

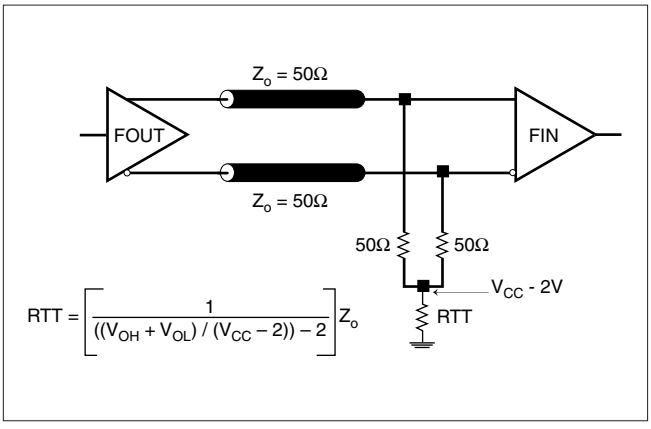


Figure 3A. LVPECL Output Termination

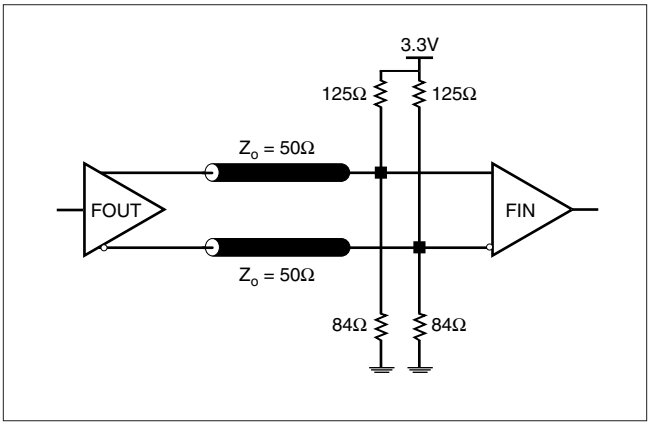


Figure 3B. LVPECL Output Termination

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

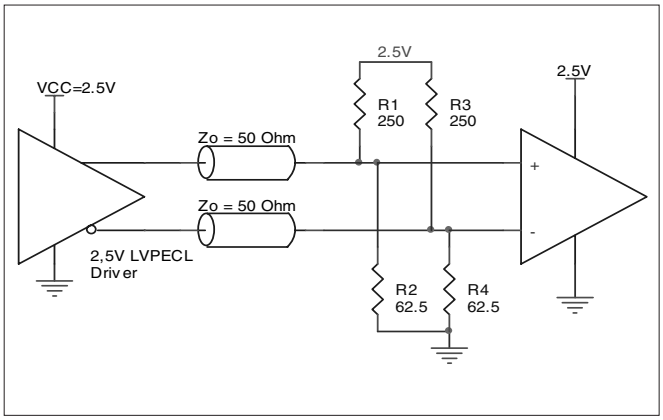


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

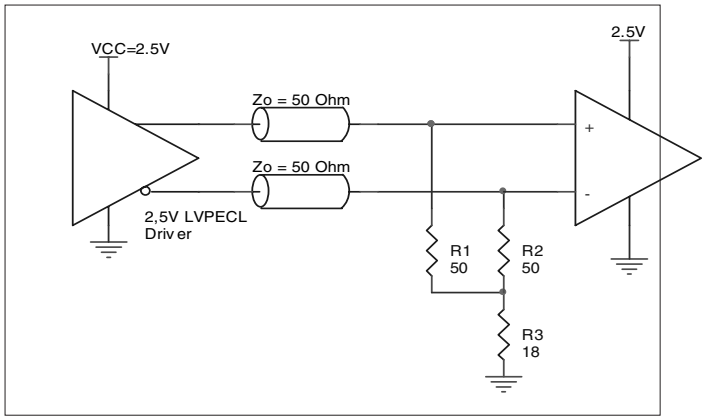


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

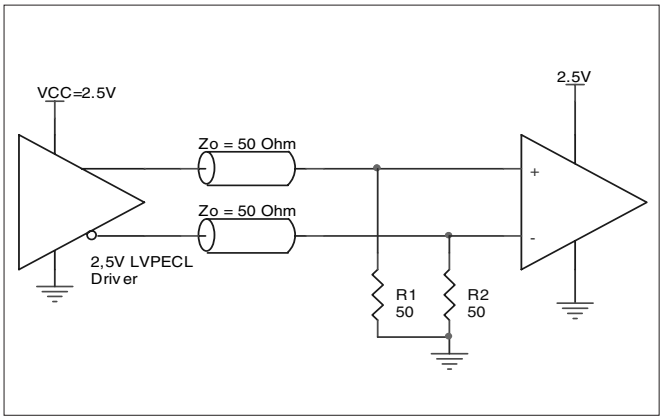


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

Description of the PLL Stages

The ICS813253 is a two stage device, a VCXO PLL followed by a low phase noise FemtoClock frequency multiplier. The VCXO uses an external pullable crystal which can be pulled ±110ppm by the VCXO PLL circuitry to phase lock it to the input reference frequency.

VCXO PLL Loop Response Considerations

Loop response characteristics of the VCXO PLL is affected by the VCXO feedback divider value (bandwidth and damping factor), and by the external loop filter components (bandwidth, damping factor, and 2nd frequency response). A practical range of VCXO PLL bandwidth is from about 1Hz to about 1kHz. The setting of VCXO PLL bandwidth and damping factor is covered later in this document. A PC based PLL bandwidth calculator is also under development. For assistance with loop bandwidth suggestions or value calculation, please contact Idt applications.

Table 3E shows frequency translation configuration examples.

Capacitors with low microphonic sensitivity should be used. PPS film type capacitors are one type that perform well in this environment. Below 5Hz, shielding should be considered to prevent excessive phase wander (low frequency phase jitter or clock phase deviation).

Setting the VCXO PLL Loop Response

The VCXO PLL loop response is determined both by fixed device characteristics and by other characterizes set by the user. This includes the values of R_S, C_S, C_P and R_{SET} as shown in the External VCXO PLL Components figure on this page.

The VCXO PLL loop bandwidth is approximated by:

$$\text{NBW (VCXO PLL)} = \frac{R_S \times I_{CP} \times K_O}{2\pi \times \text{Feedback Divider}}$$

Where:

R_S = Value of resistor R_S in loop filter in Ohms

I_{CP} = Charge pump current in amps (see table on page 12)

K_O = VCXO Gain in Hz/V

The above equation calculates the “normalized” loop bandwidth (denoted as “NBW”) which is approximately equal to the - 3dB bandwidth. NBW does not take into account the effects of damping factor or the second pole imposed by C_P. It does, however, provide a useful approximation of filter performance.

To prevent jitter on the clock output due to modulation of the VCXO PLL by the phase detector frequency, the following general rule should be observed:

$$\text{NBW (VCXO PLL)} \leq \frac{f\ \text{(Phase Detector)}}{20}$$

f (Phase Detector) = Input Frequency ÷ Pre-Divider)

The PLL loop damping factor is determined by:

$$\text{DF} = \frac{R_S}{2} \sqrt{\frac{I_{CP} \times C_S \times K_O}{\text{Feedback Divider}}}$$

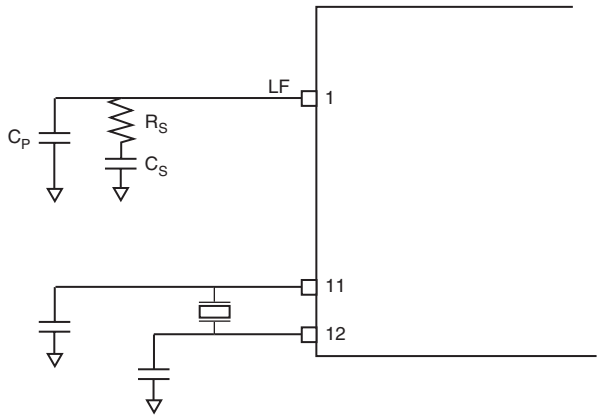
Where:

C_S = Value of capacitor C_S in loop filter in Farads

External VCXO PLL Components

In general, the loop damping factor should be 0.7 or greater to ensure output stability. A higher damping factor will create less peaking in the passband. A higher damping factor may also increase lock time and output clock jitter when there is excess digital noise in the system application, due to the reduced ability of the PLL to respond to and therefore compensate for phase noise ingress.

The external crystal devices and loop filter components should be kept close to the device. Loop filter and crystal PCB connection traces should be kept short and well separated from each other and from other signal traces. Other signal traces shouldnot run underneath the device, the loop filter or crystal components.



NOTES ON SETTING THE VALUE OF C_P

As another general rule, the following relationship should be maintained between components C_S and C_P in the loop filter:

$$C_P = \frac{C_S}{20}$$

C_P establishes a second pole in the VCXO PLL loop filter. For higher damping factors (> 1), calculate the value of C_P based on a C_S value that would be used for a damping factor of 1. This will minimize baseband peaking and loop instability that can lead to output jitter.

C_P also dampens VCXO PLL input voltage modulation by the charge pump correction pulses. A C_P value that is too low will result in increased output phase noise at the phase detector frequency due to this. In extreme cases where input jitter is high, charge pump current is high, and C_P is too small, the VCXO PLL input voltage can hit the supply or ground rail resulting in non-linear loop response.

C_P should be increased in value until it just starts affecting the passband peak.

NOTES ON EXTERNAL CRYSTAL LOAD CAPACITORS

In the loop filter schematic diagram, capacitors are shown between pin 10 to ground and between pin 11 to ground. These are optional crystal load capacitors which can be used to center tune the external pullable crystal (the crystal frequency can only be lowered by adding capacitance, it cannot be raised). Note that the addition of external load capacitors will decrease the crystal pull range and the Kvco value.

EXAMPLE LOOP FILTER COMPONENT VALUES FOR VARIOUS VCXO DIVIDER SELECTIONS

Input Frequency	Bandwidth	Dampening	RS (K)	CS (µF)	CS (µF)
25MHz	1000	2.4	5	1.0	0.01
25MHz	400	3.0	5	10.0	0.1

VCXO Crystal Selection

Choosing a crystal with the correct characteristics is one of the most critical steps in using a Voltage Controlled Crystal Oscillator (VCXO). The crystal parameters affect the tuning range and accuracy of a VCXO. Below are the key variables and an example of using the crystal parameters to calculate the tuning range of the VCXO.

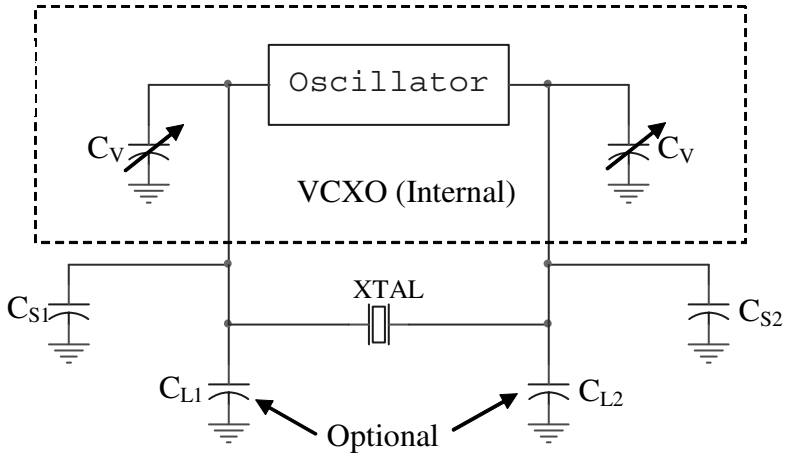


Figure 5: VCXO Oscillator Circuit Example

C_V Varactor capacitance, varies due to the change in control voltage

C_{L1}, C_{L2} Load tuning capacitance used for fine tuning or centering nominal frequency

C_{S1}, C_{S2} Stray Capacitance caused by pads, vias, and other board parasitics

Crystal Parameter Examples

Symbol	Parameter	Minimum	Typical	Maximum	Units
f_N	Nominal Frequency	19.6		27.2	MHz
f_T	Frequency Tolerance			15	ppm
f_S	Frequency Stability			15	ppm
	Operating Temperature Range	0		70	°C
C_L	Load Capacitance			8	pF
C_O	Shunt Capacitance			7	pF
C_0/C_1	Pullability Ratio			250	
ESR	Equivalent Series Resistance			20	
	Drive Level			1	mW
	Aging @ 25°C	±3 per year			ppm
	Mode of Operation	Fundemental			

Varactor Parameters

Symbol	Parameter	Test Condition	Typical	Unit
$C_{V\ LOW}$	Low Varactor Capacitance	V_C = 0V	52	pF
$C_{V\ HIGH}$	High Varactor Capacitance	V_C = 3.3V	5.2	pF

FORMULAS

$$C_{LOW} = \frac{(C_{L1} + C_{S1} + C_{V\_LOW}) \cdot (C_{L2} + C_{S2} + C_{V\_LOW})}{(C_{L1} + C_{S1} + C_{V\_LOW}) + (C_{L2} + C_{S2} + C_{V\_LOW})}$$

C_{Low} is the effective capacitance due to the low varactor capacitance, load capacitance and stray capacitance.

C_{Low} determines the high frequency component on the TPR (Total Pull Range).

$$C_{HIGH} = \frac{(C_{L1} + C_{S1} + C_{V\_HIGH} \cdot (C_{L2} + C_{S2} + C_{V\_HIGH})}{(C_{L1} + C_{S1} + C_{V\_HIGH}) + (C_{L2} + C_{S2} + C_{V\_HIGH})}$$

C_{High} is the effective capacitance due to the high varactor capacitance, load capacitance and stray capacitance.

C_{High} determines the low frequency component on the TPR (Total Pull Range).

$$TPR = \left(\frac{1}{2 \cdot C_0/C_1 \cdot (1+C_{LOW}/C_0)} - \frac{1}{2 \cdot C_0/C_1 \cdot (1+C_{HIGH}/C_0)} \cdot 10^6 \right)$$

AbsolutePullRange (APR) = TotalPullRange – (FrequencyTolerance + FrequencyStability + Aging)

EXAMPLE CALCULATIONS - TBD

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS813253.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS813253 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 132mA = **457.38mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 3 * 30mW = **90mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 457.28mW + 90mW = **547.38mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 1 meter per second and a multi-layer board, the appropriate value is 65°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.547W * 65°C/W = 105.6°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 24 LEAD TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

3. Calculations and Equations.
The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 6.*

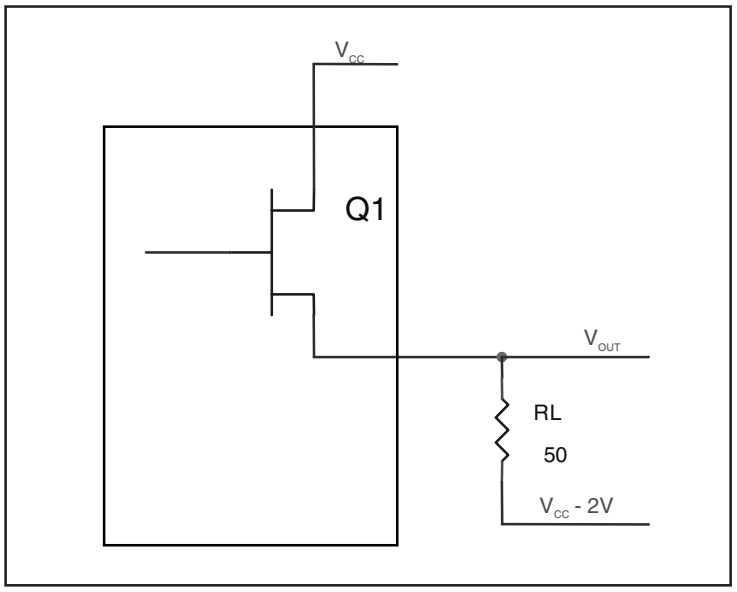


FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS813253 is: 2915

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

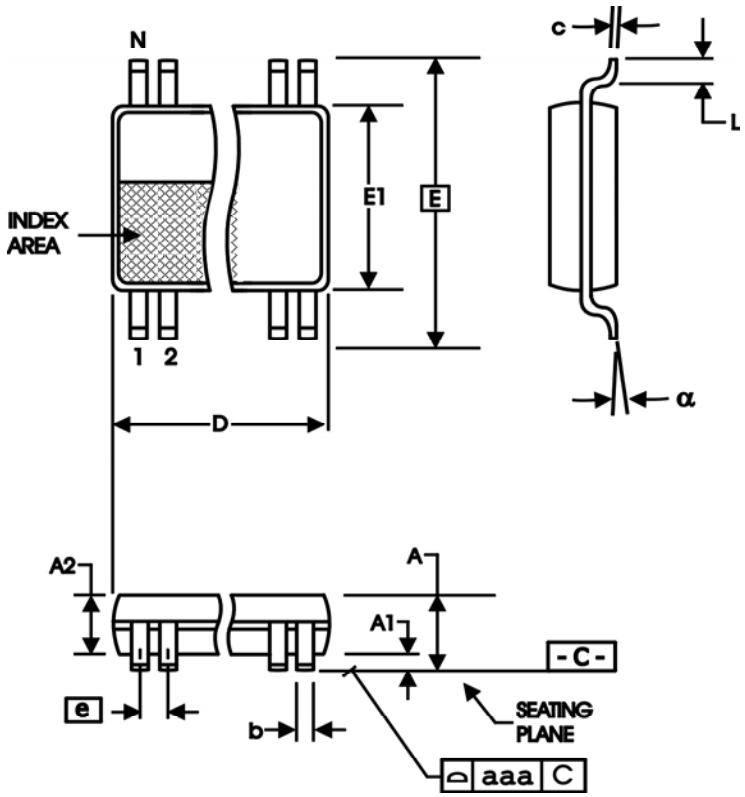


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS813253AG	ICS813253AG	24 Lead TSSOP	tube	0°C to 70°C
ICS813253AGT	ICS813253AG	24 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS813253AGLF	ICS813253AGLF	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS813253AGLFT	ICS813253AGLF	24 Lead "Lead-Free" TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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