SY89538L

3.3V, Precision LVPECL and LVDS Programmable Multiple Output Bank Clock Synthesizer and Fanout Buffer with Zero Delay

General Description

The SY89538L integrated programmable clock synthesizer and fanout is part of a precision PLL-based clock generation family optimized for enterprise switch, router, and multiprocessor server applications. This family is ideal for generating internal system timing requirements up to 750MHz for multiple ASICs, FPGAs, and NPUs. These devices integrate the following blocks into a single monolithic IC:

- PLL (Phase-Lock-Loop) based synthesizer
- Zero-delay MUX and feedback capability
- 1:4 LVPECL fanout
- 1:3 LVDS fanout
- Clock generator (dividers)
- Logic translation (LVPECL, LVDS)
- Five-independently programmable output banks

This level of integration minimizes additive jitter and part-to-part skew associated with discrete alternatives, resulting in superior system-level timing with reduced board space and power. For applications that do not require a zero-delay function, see the SY89537L.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Applications

- Enterprise routers, switches, servers and workstations
- Parallel processor-based systems
- Internal system clock generation for ASICs, NPUs and FPGAs

Markets

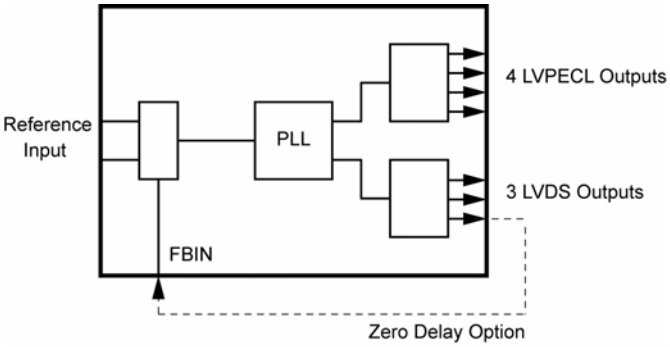
- LAN/WAN
- Enterprise servers
- Test and measurement

Precision Edge®

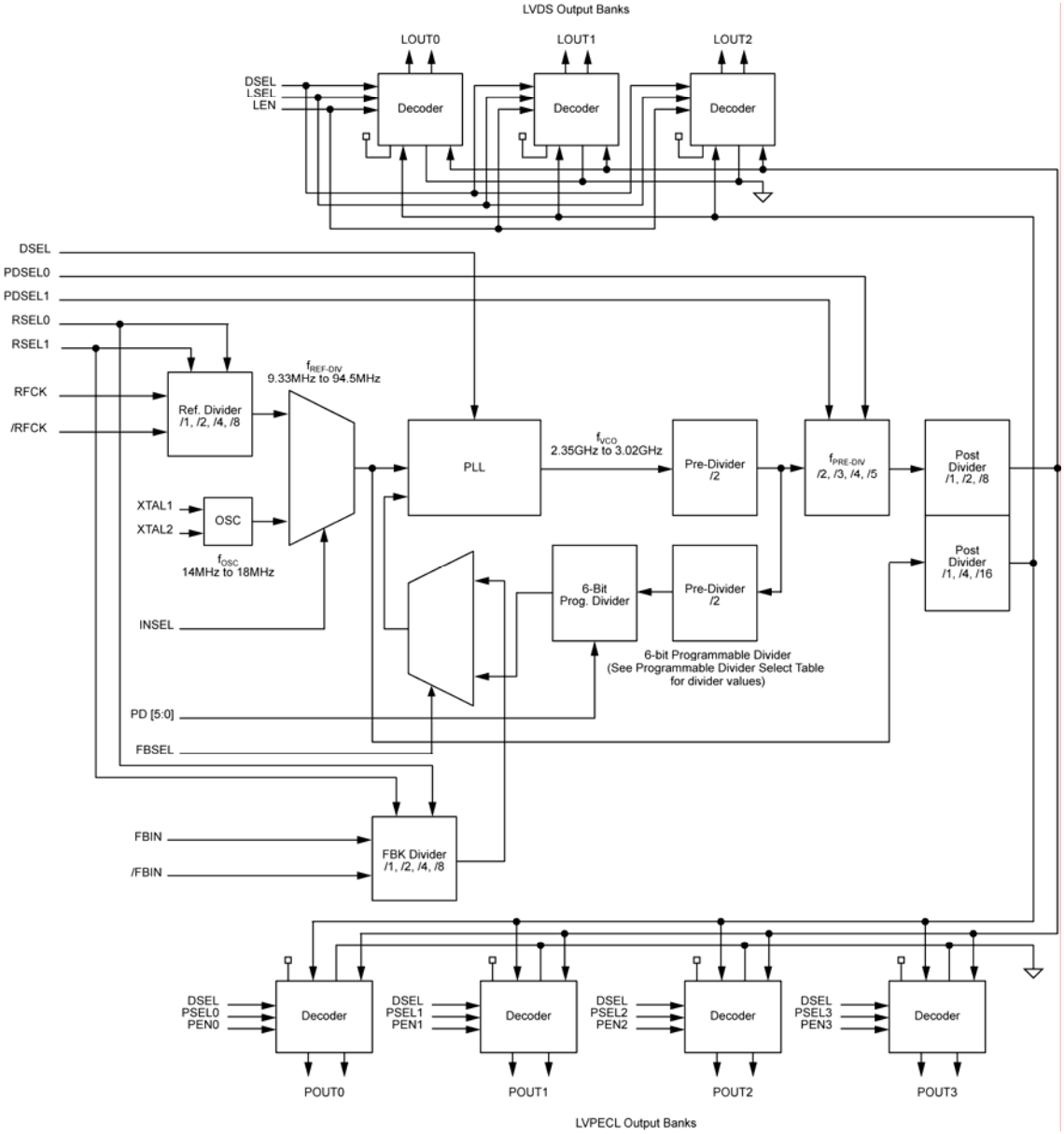
Features

- Integrated programmable synthesizer with multiple output dividers, fanout buffers, and clock drivers
- Zero-delay capability: 29.375MHz to 756MHz
- Reference clock input: 9.325MHz to 756MHz
- Input MUX accepts a reference and a crystal (XTAL) source
  - Ideal for reference backup clock source or system test frequency source
  - Patent-pending unique input MUX isolates XTAL and reference inputs which minimizes crosstalk
- Guaranteed AC performance:
  - Output frequency range: 29.375MHz to 756MHz
  - <150ps$_{PP}$ total jitter
  - <6ps$_{RMS}$ cycle-to-cycle jitter (XTAL Input)
  - <8ps$_{PP}$ deterministic jitter
  - <0.7ps$_{RMS}$ crosstalk induced jitter
  - <75ps output-to-output skew
- TTL/CMOS-compatible control logic
- Five-independently programmable output frequency banks:
  - Four differential LVPECL output banks
  - One differential LVDS output bank with three output pairs
- Output bank synchronization control pin
- Output enable
- 3.3V ±10% power supply (2.5V output capable)
- Guaranteed over the industrial temperature range (-40°C to +85°C)
- Available in a 64-pin EPAD-TQFP

Typical Application



Functional Block Diagram



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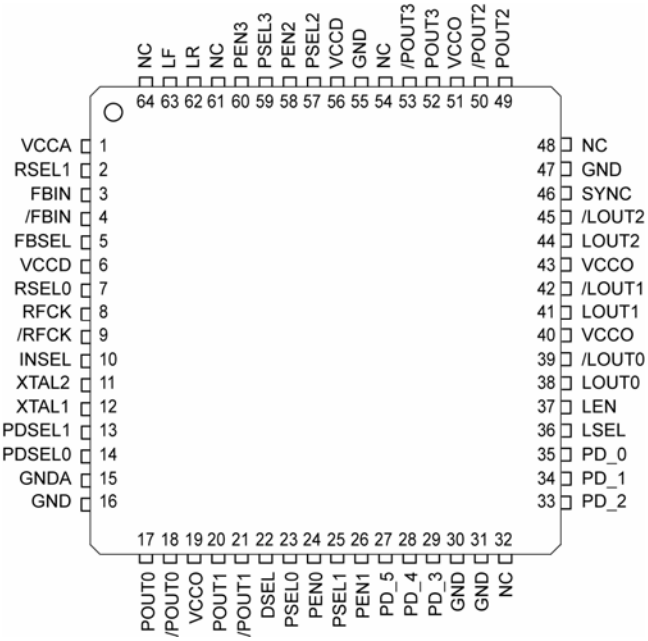
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89538LHG	H64-1	Industrial	SY89538LHG with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89538LHGTR[2]	H64-1	Industrial	SY89538LHG with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



64-Pin EPAD TQFP (H64-1)

Pin Description

Power

Pin Number	Pin Name	Pin Function
1	VCCA	Analog PLL Power Pin. Connects to “quiet” 3.3V supply. 3.3V power pins must be connected together on the PCB. Bypass with 0.1µF//0.01µF low ESR capacitors and place them as close to the VCCA pin as possible.
6, 56	VCCD	Digital Logic Core Power Pin. VCCD connects to a 3.3V supply. All power pins must be connected together on the PCB. Bypass with 0.1µF//0.01µF low ESR capacitors and place them as close to the VCCD pin as possible.
19, 40, 43, 51	VCCO	LVDS and LVPECL Output Driver Power Pins. These outputs can be powered from a 2.5V or 3.3V supply. Connect all VCCO pins to the same power supply: 3.3V ±10% or 2.5V ±5%. All power pins must be connected together on the PCB. Bypass with 0.1µF//0.01µF low ESR capacitor and place them as close to the VCCO pin as possible.
15	GNDA	Analog PLL Ground. Connect to “quiet” ground. GNDA and GND must be connected together on the PCB.
16, 30, 31, 47, 55	GND, Exposed Pad	Ground: GND pins and exposed pad must both be connected to the same ground plane.

Control and Configuration

Pin Number	Pin Name	Pin Function
62	LR	Analog Input/Output. Provides the reference voltage for the PLL loop filter and is used with the LF pin. See “External Loop Filter Considerations” for recommended loop filter values.
63	LF	Analog Input/Output. Provides the loop filter node for the PLL. See “External Loop Filter Considerations” for recommended loop filter values.
2, 7	RSEL1, RSEL0	TTL/CMOS Reference input pre-scalar and Zero Delay MUX divider select inputs. The two-bit input pre-scalar divides the input reference frequency by /1, /2, /4, or /8. RSEL0 is the LSB bit. See “Reference Input Divider and Zero Delay MUX Divider Select Table” for proper decoding. The threshold voltage $V_{TH} = V_{CC}/2$. Internal 25kΩ pull-up. The default logic is HIGH.
10	INSEL	TTL/CMOS Input Select Control. Selects either XTAL or Reference (RFCK) input. Internal 25kΩ pull-up. The default is logic HIGH, and selects the XTAL input. The threshold voltage $V_{TH} = V_{CC}/2$. Logic HIGH: XTAL Select Logic LOW: Reference Input Select
36	LSEL	TTL/CMOS input select control signal for the LVDS LOUT0-LOUT2 outputs. LSEL, DSEL, and LEN are used together to decode the selection and post divider of the LVDS outputs. Internal 25kΩ pull-up. See “LVDS Output Post-Divider and Frequency Select Table” for proper decoding. The threshold voltage $V_{TH} = V_{CC}/2$. The default logic is HIGH.
37	LEN	TTL/CMOS input enable pin. Used to control the LOUT0-LOUT2 outputs and acts as a frequency select pin. LEN, DSEL, and LSEL are used together to decode the selection and post divide of the LVDS output bank, see the “LVDS Output Post-Divider and Frequency Select Table” for proper decoding. Internal 25kΩ pull-up. When disabled, LOUT0-LOUT2 outputs are LOW, and the complimentary outputs are HIGH. The threshold voltage $V_{TH} = V_{CC}/2$. The default logic is HIGH.
23 25 57 59	PSEL0 PSEL1 PSEL2 PSEL3	TTL/CMOS input select control signals for the PECL POUT0-POUT3 outputs. PSELx, DSEL and PENx are used together to decode the selection and post divider of the PECL outputs. PSELx pins include an internal 25kΩ pull-up. The threshold voltage $V_{TH} = V_{CC}/2$. See "LVPECL Output Post-Divider and Frequency Select Table” for proper decoding.

Pin Description

Control and Configuration (continued)

Pin Number	Pin Name	Pin Function
24 26 58 60	PEN0 PEN1 PEN2 PEN3	TTL/CMOS input enable pin. Used to control the PECL POUT0-POUT3 outputs and as a frequency select pins. PENx, PSELx, and DSEL are used together; see the "LVPECL Output Post-Divider and Frequency Select Table" for proper decoding. PENx contains internal 25kΩ pull-up. When disabled, PECL0-PECL3 outputs are a logic LOW. The threshold voltage $V_{TH} = V_{CC}/2$.
46	SYNC	TTL/CMOS Output Bank Synchronization Control. Internal 25kΩ pull-up. The default state is HIGH. After any bank has been programmed, all PECL and LVDS outputs are synchronized when the SYNC control pin is toggled with a HIGH-LOW-HIGH transition. See "Synchronization" section for details. The threshold voltage $V_{TH} = V_{CC}/2$.
5	FBSEL	TTL/CMOS Input Select Control. Selects either internal or external feedback (zero-delay function). Internal 25kΩ pull-up. The threshold voltage $V_{TH} = V_{CC}/2$. Default is logic HIGH, and selects internal feedback. Logic HIGH: Internal feedback (from the Programmable Divider) Logic Low: External feedback (from the FBIN inputs)
28 33 35	PD_4 PD_2 PD_0	TTL/CMOS Programmable Divider-Select Control. Internal 25kΩ pull-down. Default is logic LOW. The threshold voltage $V_{TH} = V_{CC}/2$. See "Programmable-Divider Select Table" for proper decoding.
27 29 34	PD_5 PD_3 PD_1	TTL/CMOS Programmable Divider-Select Control. Internal 25kΩ pull-up. Default is logic HIGH. The threshold voltage $V_{TH} = V_{CC}/2$. See "Programmable-Divider Select Table" for proper decoding.
13, 14	PDSEL1, PDSEL0	TTL/CMOS Pre-Divider Select Input. Internal 25kΩ pull-up. This two-bit input divider scales the VCO/2 frequency. See "Pre-Divider Frequency Select Table" for proper decoding. The threshold voltage $V_{TH} = V_{CC}/2$.
22	DSEL	TTL/CMOS Post-Divider Option Control. Internal 25kΩ pull-up. Default is logic HIGH. The threshold voltage $V_{TH} = V_{CC}/2$. Logic HIGH: All LVPECL and LVDS outputs operate with their respective output frequency control (PSELx, PENx, LSEL, LEN). Logic LOW: Internal PLL is disabled, reference and XTAL signals by-passes the PLL through a /1, /4, and /16 Post-Divider. See "LVPECL and LVDS Output Post-Divider and Frequency Select Table" for proper decoding.

Pin Description

Input/Output

Pin Number	Pin Name	Pin Function
3, 4	FBIN, /FBIN	External Feedback Input used as the zero delay input. Output feeds into the inputs to configure the device in zero-delay mode, which forces the output frequency to the same frequency of the RFCK frequency. Requires external termination. See "Zero Delay FBIN Input" section for more details.
8, 9	RFCK, /RFCK	Reference Clock Differential Input. Input accepts any input, single-ended or differential: TTL/CMOS, LVPECL, LVDS, HSTL, and SSTL. RFCK requires an external termination. See "Input Interface" and "Input Termination" sections for more details.
11, 12	XTAL2, XTAL1	Crystal Input. Directly connect a series resonant crystal across inputs. See "Quartz Crystal Oscillator Specification" table. Place crystal as close to the input as possible, keep XTAL and traces away from adjacent noisy traces to minimize noise coupling, and place the XTAL on the same side as the SY89538L (component side).
17, 18 20, 21 49, 50 52, 53	POUT0, /POUT0 POUT1, /POUT1 POUT2, /POUT2 POUT3, /POUT3	100K LVPECL Output Drivers. Terminate all LVPECL outputs with 50Ω to V_{CCO}–2V. Each output pair has a respective output frequency control (PSELx, PENx, DSEL). See "LVPECL Output Post-Divider and Frequency Select Table" for proper decoding. For low-jitter applications, unused LVPECL output pairs should be terminated with pull-down resistors. See "Output Termination Recommendations" section for termination detail.
38, 39 41, 42 44, 45	LOUT0, /LOUT0 LOUT1, /LOUT1 LOUT2, /LOUT2	Differential LVDS-Compatible Output Drivers. Output termination is 100Ω across the pair. For low-jitter applications, unused LVDS output pairs should be terminated with 100Ω across the pair. See "Output Termination Recommendations" section for details.
32, 48, 54, 61, 64	NC	No connect.

Input Driver Select Table

RSEL1	RSEL0	Internal Reference Clock	Zero-Delay MUX Divider
0	0	RFCK / 8	FBIN / 8
0	1	RFCK / 4	FBIN / 4
1	0	RFCK / 2	FBIN / 2
1	1	RFCK / 1	FBIN / 1

Table 1. Reference Input Divider and Zero-Delay MUX Divider Select Table

Pre-Divider Frequency Select Table

PDSEL1	PDSEL0	Pre-Div-Out Frequency
0	0	(VCO/2) / 5
0	1	(VCO/2) / 4
1	0	(VCO/2) / 3
1	1	(VCO/2) / 2

Table 2. Pre-Divider Select Table

Output and Frequency Select Tables

PSELx	PENx	DSEL	POUTx
0	0	0	Disable Output (HIGH)
0	1	0	$f_{REF-DIV}$ / 4
1	0	0	$f_{REF-DIV}$ / 16
1	1	0	$f_{REF-DIV}$ / 1
0	0	1	Disable Output (LOW)
0	1	1	$f_{PRE-DIV}$ / 2
1	0	1	$f_{PRE-DIV}$ / 8
1	1	1	$f_{PRE-DIV}$ / 1

Table 3. LVPECL Output Post-Divider and Frequency Select Table

LSEL	LEN	DSEL	LOUTx
0	0	0	Disable Output (HIGH)
0	1	0	$f_{REF-DIV}$ / 4
1	0	0	$f_{REF-DIV}$ / 16
1	1	0	$f_{REF-DIV}$ / 1
0	0	1	Disable Output (LOW)
0	1	1	$f_{PRE-DIV}$ / 2
1	0	1	$f_{PRE-DIV}$ / 8
1	1	1	$f_{PRE-DIV}$ / 1

Table 4. LVDS Output Post-Divider and Frequency Select Table

Programmable-Divider Select Table

PD_5	PD_4	PD_3	PD_2	PD_1	PD_0	6-Bit Prog. Divider	f_{VCO}
0	0	1	0	0	0	8	f_{Ref} x 32
0	0	1	0	0	1	9	f_{Ref} x 36
0	0	1	0	1	0	10	f_{Ref} x 40
0	0	1	0	1	1	11	f_{Ref} x 44
0	0	1	1	0	0	12	f_{Ref} x 48
…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…
1	0	1	0	0	0	40	f_{Ref} x 160
1	0	1	0	0	1	41	f_{Ref} x 164
1	0	1	0	1	0	42	f_{Ref} x 168
1	0	1	0	1	1	43	f_{Ref} x 172
1	0	1	1	0	0	44	f_{Ref} x 176
…	…	…	…	…	…	…	…
…	…	…	…	…	…	…	…
1	1	1	0	1	1	59	f_{Ref} x 236
1	1	1	1	0	0	60	f_{Ref} x 240
1	1	1	1	0	1	61	f_{Ref} x 244
1	1	1	1	1	0	62	f_{Ref} x 248
1	1	1	1	1	1	63	f_{Ref} x 252

Table 5. Programmable-Divider Select Table

Note:

See “Reference Input Frequency and Valid Programmable Divider Range” section for more details.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CCD}, V_{CCA}, V_{CCO}) ..... –0.5V to +4.0V
Input Voltage (RFCK, FBIN) ..... –0.5V to V_{CC}
XTAL Input Voltage ($V_{XTAL1, 2}$) ..... V_{CC} –1.9V to V_{CC}
Output Current (I_{OUT})
- LVPECL Outputs (Surge) 100mA
- LVPECL Outputs (Continuous) 50mA
- LVDS Outputs ..... ±10mA

Lead Temperature (soldering, 20 sec.) ..... +260°C
Storage Temperature (T_s) ..... –65°C to 150°C

Operating Ratings[2]

Supply Voltage
- V_{CCO}A and V_{CCO}C ..... +3.0V to +3.6V
- V_{CCO}B ..... +2.375V to +3.6V

Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance (Junction-to-Ambient)
With Die attach soldered to GND:
- TQFP (θ_{JA}) Still-Air ..... 23°C/W
- TQFP (θ_{JA}) 200lfpm ..... 18°C/W
- TQFP (θ_{JA}) 500lfpm ..... 15°C/W

With Die attach NOT soldered to GND[3]:
- TQFP (θ_{JA}) Still-Air ..... 44°C/W
- TQFP (θ_{JA}) 200lfpm ..... 36°C/W
- TQFP (θ_{JA}) 500lfpm ..... 30°C/W

Package Thermal Resistance (Junction-to-Board)
- TQFP (θ_{JC}) ..... 7°C/W

DC Electrical Characteristics[4]

Power Supply

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CCA}	PLL Power Supply	Note 5	3.0	3.3	3.6	V
V_{CCD}	Control Logic Supply Voltage	Note 5	3.0	3.3	3.6	V
V_{CCO}	Output Supply Voltage		2.375	2.5	2.625	V
			3.0	3.3	3.6	V
I_{CC}	Power Supply Current	No load, max. V_{CC}, Note 6		240	300	mA
I_{CCA}	Analog Supply Current	Max. V_{CC}		10		mA
I_{CCO}	Output Supply Current	No load, max. V_{CC}		55		mA
I_{CCD}	Digital Supply Current	Max. V_{CC}		175		mA

LVCMOS/LVTTL Input Control Logic

V_{CCA} = V_{CCD} = +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC}	–125		150	µA
I_{IL}	Input Low Current	V_{IN} = 0.5V	–300			µA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. It is recommended that the user always solder the exposed die pad to a ground plane for enhanced heat dissipation.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{CCA} and V_{CCD} are not internally connected. They must be connected together on the PCB.
6. I_{CC} = I_{CCA} + I_{CCO} + I_{CCD}.

Reference Clock Inputs/External Feedback Inputs

V_{CCA} = V_{CCD} = +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	RFCK, /RFCK FBIN, /FBIN			V_{CCD} + 0.3	V
V_{IL}	Input LOW Voltage	RFCK, /RFCK FBIN, /FBIN	–0.3			V
V_{IN}	Input Voltage Swing	RFCK, /RFCK, FBIN, /FBIN See Figure 1a.	100			mV
V_{DIFF_IN}	Differential Input Voltage Swing	RFCK, /RFCK, FBIN, /FBIN See Figure 1b.	200			mV

100K LVPECL Output DC Electrical Characteristics

V_{CCA} = V_{CCD} = +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%, R_L = 50Ω into V_{CCO}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage		V_{CCO}–1.075		V_{CCO}–0.830	V
V_{OL}	Output LOW Voltage		V_{CCO}–1.860		V_{CCO}–1.570	V
V_{OUT}	Output Voltage Swing	See Figure 1a.	550	800		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 1b.	1100	1600		mV

LVDS Output DC Electrical Characteristics

V_{CCA} = V_{CCD} = +3.3V ±10%, V_{CCO} = +2.5V ±5% or +3.3V ±10%, R_L = 100Ω across the pair; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT}	Output Voltage Swing	See Figure 1a.	250	325		mV
$V_{DIFF-OUT}$	Differential Output Voltage Swing	See Figure 1b.	500	650		mV
V_{OCM}	Output Common Mode Voltage		1.125		1.275	V
ΔV_{OCM}	Change in Common Mode Voltage				25	mV

AC Electrical Characteristics

V_{CCA} = V_{CCD} = +3.3V ±10%; V_{CCO} = +2.5V ±5% or +3.3V ±10%, R_L (LVDS) = 100Ω across the output pairs, R_L (LVPECL) = 50Ω into V_{CCO}–2V; T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{IN}	XTAL Input Frequency Range	Note 7	14		18	MHz
	Reference Input Frequency Range	See Table 8	9.325		756	MHz
	Zero Delay Input Frequency Range	See Table 9	29.375		756	MHz
f_{REF}	Phase Detector Operating Frequency Range	INSEL = LOW	9.325		94.5	MHz
		INSEL = HIGH	14		18	MHz
f_{OUT}	Output Frequency Range		29.375		756	MHz
f_{VCO}	Internal VCO Frequency Range		2352		3024	MHz
t_{SKEW}	Output-to-Output	Note 8		15	75	ps
t_{LOCK}	Minimum PLL Lock Time				10	ms
t_{JITTER}	Loop Filter Optimized for Cycle-to-Cycle Jitter • R = 50Ω • C1 = 0.47µF • C2 = 1000pF					
	1-Sigma Cycle-to-Cycle Jitter (XTAL Input)	Note 9		4	6	ps_{RMS}
	1-Sigma Cycle-to-Cycle Jitter (RFCK Reference)	Note 9		5	14	ps_{RMS}
	Total Jitter	Note 10		80	150	ps_{PP}
	Spur			-35		dBc@ fphase
	XTAL/RFCK Crosstalk-Induced Jitter	Note 11			0.7	ps_{RMS}
BW	PLL Bandwidth	See Table 10 $14 \le f_{REF} \le 18$	11.1		38.4	kHz
t_{DC}	F_{OUT} Duty Cycle		43	50	57	%
t_r, t_f	Output Rise/Fall Time (20% to 80%)	LVPECL	100	250	400	ps
	Output Rise/Fall Time (20% to 80%)	LVDS	80	150	300	ps
$t_{PW\_SYNC\_MIN}$	Minimum SYNC Pulse Width	See “Synchronization” section	8			Internal clock cycle
t_{PD_SYNC}	Synchronization Delay	See “Synchronization” section		8		Internal clock cycle

Notes:

7. Fundamental mode, series resonant crystal.
8. The output-to-output skew is defined as the worst-case difference between any outputs within a single device operating at the same voltage and temperature.
9. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles, $T_n - T_{n-1}$ where T is the time between rising edges of the output signal.
10. Total jitter definition: with an ideal clock input of frequency <f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.
11. Crosstalk is measured at the output while applying two similar differential clock frequencies that are asynchronous with respect to each other at the inputs.

Single-Ended and Differential Swings

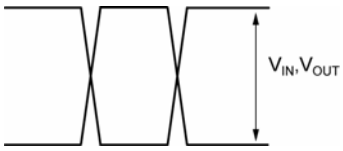


Figure 1a. Single-Ended Voltage Swing

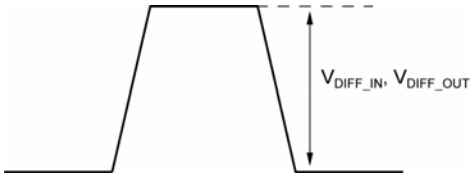


Figure 1b. Differential Voltage Swing

Functional Description

Overall Function

The SY89538L integrated programmable clock synthesizer and fanout buffer with zero delay is part of a precision PLL-based clock generation family optimized for internal system clock generation (FPGAs, ASICs, NPU).

Inputs

XTAL

The SY89538L features a fully integrated on-board oscillator, which minimizes system implementation cost. The oscillator is a series resonant, multi-vibrator type crystal driver designed to drive a 14MHz to 18MHz series resonant crystal, see Table 6 and 7 for more details on the crystal frequency range and specifications.

XTAL (MHz)			f_{VCO} (GHz)	
Min.	Max.	X R_{REF}	Min.	Max.
14	18	168	2.352	3.024

Table 6. XTAL Frequency Range and Valid Programmable Range Table

	Min.	Typ.	Max.	Units
Frequency Range (Fundamental Mode-Series Resonant)	14		18	MHz
Frequency Tolerance @ 25°C		±30	±50	PPM
Frequency Stability over 0°C to 70°C		±50	±100	PPM
Operating Temperature Range	-40		+85	°C
Storage Temperature Range	-55		+125	°C
Aging (per yr/1st 3yrs)			±5	PPM
Equivalent Series Resistance (ESR)			50	Ω
Drive Level		100		µW

Table 7. Quartz Crystal Oscillator Specifications

Oscillator Tips

1. Mount the crystal as close to the SY89538L as possible to minimize parasitic effects.
2. Mount the crystal on the same plane as the SY89538L to minimize on via hole inductance.
3. To minimize noise pick up on the loop filter pins, cut the ground plane directly underneath the loop filter component pads and traces.
4. Keep the crystal and its traces away from adjacent noisy traces to minimize noise coupling.

Figure 2 below illustrates how to interface the crystal with the SY89538L.

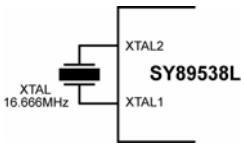


Figure 2. Crystal Interface

Quartz Crystal Selection:

Note: Raltron Series Resonant: AS-16.666-S-SMD-T-MI (2) Raltron

RFCK

The input MUX drives the PLLs phase detector, which expects a frequency between 9.325MHz and 94.5MHz. Therefore, reference clock maximum input frequency is 756MHz when the reference divider is set to a divide-by-8 and the reference clock minimum frequency is 9.325MHz when the reference divider is set to a divide-by-1. Given that the VCO frequency range is from 2.352GHz to 3.024GHz, the minimum and maximum frequency range of RFCK can be calculated as follows:

Minimum Output Frequency (9.33MHz Input):

$$f_{OUT} = \frac{f_{PHASE} \times \Pr eDivider \times FeedbackDivider}{\Pr eDivider \times PostDivider \times (Div-by-2)}$$

$$f_{OUT} = \frac{(9.33MHz) \times (63 \times 2) \times (2)}{(5) \times (8) \times (2)}$$

$$f_{OUT} = 29.4MHz$$

Maximum Output Frequency (756MHz Input):

$$f_{OUT} = \frac{\left(\frac{756MHz}{8}\right) \times (8 \times 2) \times (2)}{(2) \times (1) \times (2)}$$

$$f_{OUT} = 756MHz$$

Table 8 summarizes the input reference frequency and associated divider values:

f_{RFCK} (MHz)			f_{REF} (MHz)		f_{VCO} (GHz)	
Ref-Div = 1	**Ref-Div = 8**	**X f_{REF}**	**Min.**	**Max.**	**Min.**	**Max.**
73.5	756	32	73.5	94.5	2.352	3.024
65.3	672	36	65.3	84.0	2.352	3.024
58.8	605	40	58.8	75.6	2.352	3.024
53.5	550	44	53.5	68.7	2.352	3.024
49.0	504	48	49.0	63.0	2.352	3.024
…	…	…	…	…	…	…
14.7	151	160	14.7	18.9	2.352	3.024
14.3	148	164	14.3	18.4	2.352	3.024
14.0	144	168	14.0	18.0	2.352	3.024
13.7	141	172	13.7	17.6	2.352	3.024
13.4	137	176	13.4	17.2	2.352	3.024
…	…	…	…	…	…	…
9.97	103	236	9.97	12.8	2.352	3.024
9.80	101	240	9.80	12.6	2.352	3.024
9.64	99.1	244	9.64	12.4	2.352	3.024
9.48	97.5	248	9.48	12.2	2.352	3.024
9.33	96.0	252	9.33	12.0	2.352	3.024

Table 8. Reference Input Frequency and Valid Programmable Divider Range Table

Zero Delay FBIN Input

The SY89538L features a zero delay MUX that forces the output to be at the same phase relationship as the reference. This effectively configures the SY89538L as a zero delay buffer when FBSEL is logic HIGH and the output is fed into the feedback input FBIN as shown in Figures 3a and 3b.

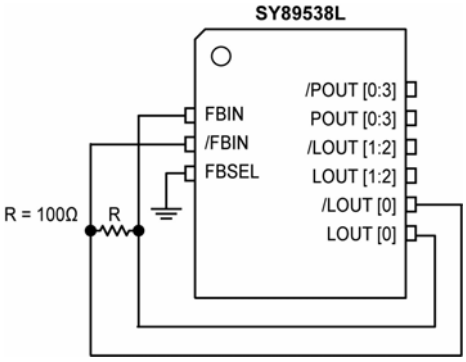


Figure 3a. Zero Delay Mode (LVDS Output)

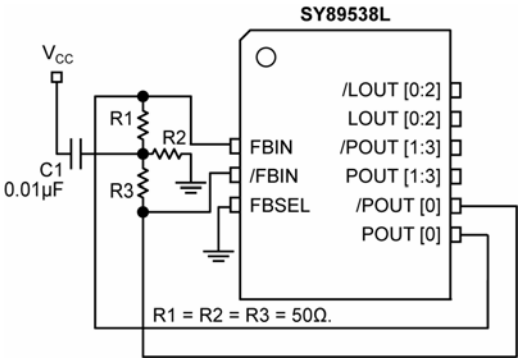


Figure 3b. Zero Delay Mode (LVPECL Output)

How Does Zero Delay Work?

From the block diagram,

$$f_{REF} = \frac{f_{RFCK}}{\text{Ref. Divider}} \text{ and } f_{FBK} = \frac{f_{FBIN}}{\text{FBK Divider}}$$

When the PLL is locked, $f_{REF} = f_{FBK}$ and since Ref. Divider = FBK Divider, f_{RFCK} is forced to equal $\mathbf{f_{FBIN}}$.

In zero delay mode, f_{OUT} is fed into FBIN, therefore, f_{RFCK} is forced to equal f_{OUT}.

						Ref-Divider = 1		Ref-Divider = 2		Ref-Divider = 4		Ref-Divider = 8	
f_{VCO} (MHz)		Post-Divider	Pre-Divider	f_{OUT} (MHz)		f_{REF} (MHz)		f_{REF} (MHz)		f_{REF} (MHz)		f_{REF} (MHz)	
Min.	Max.			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
2.35	3.02	1	2	588.0	755.0	588.0	755.0	294.0	377.5	147.0	188.8	73.5	94.4
2.35	3.02	1	3	392.0	503.0	392.0	503.0	196.0	251.5	98.0	125.8	49.0	62.9
2.35	3.02	1	4	294.0	378.0	294.0	378.0	147.0	189.0	73.5	94.5	36.8	47.3
2.35	3.02	1	5	235.0	302.0	235.0	302.0	117.5	151.0	58.8	75.5	29.4	37.8
2.35	3.02	2	2	294.0	378.0	294.0	378.0	147.0	189.0	73.5	94.5	36.8	47.3
2.35	3.02	2	3	196.0	252.0	196.0	252.0	98.0	126.0	49.0	63.0	24.5	31.5
2.35	3.02	2	4	147.0	189.0	147.0	189.0	73.5	94.5	36.8	47.3	18.4	23.6
2.35	3.02	2	5	118.0	151.0	118.0	151.0	59.0	75.5	29.5	37.8	14.8	18.9
2.35	3.02	8	2	73.4	94.4	73.4	94.4	36.7	47.2	18.4	23.6	**Not Valid**	11.8
2.35	3.02	8	3	49.0	62.9	49.0	62.9	24.5	31.5	12.3	15.7	**Not Valid**	**Not Valid**
2.35	3.02	8	4	36.7	47.2	36.7	47.2	18.4	23.6	**Not Valid**	11.8	**Not Valid**	**Not Valid**
2.35	3.02	8	5	29.4	37.8	29.4	37.8	14.7	18.9	**Not Valid**	**Not Valid**	**Not Valid**	**Not Valid**

Table 9. Zero Delay Divider Cases

Considerations when in zero delay mode:

- The input and output frequency range is 29.375MHz to 756MHz
- The phase detector frequency range is 9.325MHz to 94.5MHz
- There are cases in which certain divider combinations at certain frequencies are not valid, see Table 9 for more details
- Systematic phase offset is caused by added and parasitic capacitance
- Phase offset is introduced by increased trace length
- Phase offset second order effects can be introduced with high ε_R die-electric constants since the velocity of electromagnetic waves slows down as the die-electric constant increases

External Loop Filter Considerations

The SY89538L features an external PLL loop filter that allows the users to tailor the PLL's behavior. It is recommended that ceramic capacitors with NPO or X7R dielectric be used, since they have very low effective series resistance. For applications that require ultra-low cycle-to-cycle jitter, use the components shown in Figure 4. Larger values of the zero capacitor (capacitor shown in parallel) results in less cycle-to- cycle jitter, however the total jitter increases as the value of the zero capacitor increases. In addition, as the zero capacitor increases, loop stability decreases as the zero capacitor begins to dominate over the pole capacitor (capacitor in series with the damping resistor). The external loop filter allows the user to change the loop filter values for specific jitter requirements. Using a smaller resistor in the loop filter decreases the PLL's loop bandwidth. This results in less noise from the PLL input, but potentially more noise from the VCO. Take care to keep the loop filter components on the same side of the board and as close as possible to the SY89538L's LR and LF pins. To minimize noise pick up on the loop filter pins, cut the ground plane directly underneath the loop filter component pads and traces. However, the benefit may not be significant in all applications.

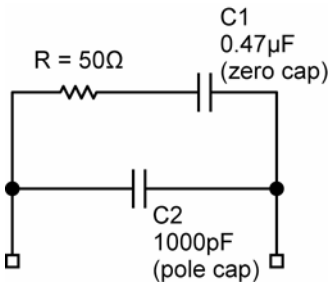


Figure 4. Loop Filter

Power Supply Filtering Techniques

As with any high-speed integrated circuit, power supply filtering is very important. At a minimum, VCCA, VCCD, and all VCCO pins should be individually connected using a via to the power supply plane, and separate bypass capacitors should be used for each pin. To achieve optimal jitter performance, each power supply pin should use separate instances of the circuit shown in Figure 5.

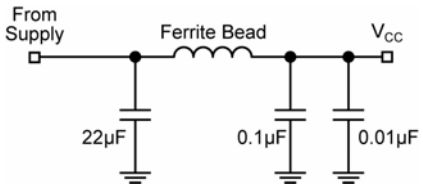


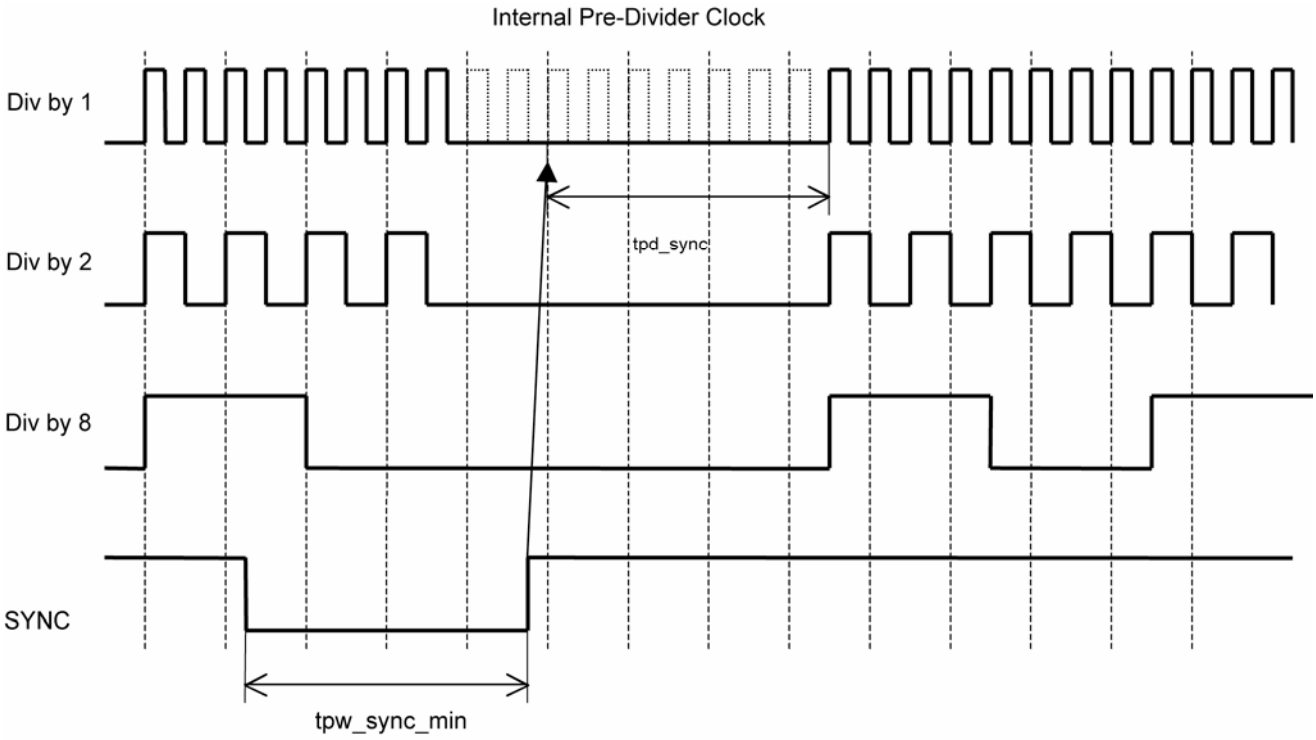
Figure 5. Recommended Power Supply Filter

Note:

For V_{CCA} and V_{CCD} use ferrite bead, 200mA, Murata P/N BLM21A1025.

For V_{CCO} use ferrite bead3A, 0.025Ω DC, Murata, P/N BLM31P005.

Synchronization



Output Synchronization Controlled by SYNC Timing Diagram

The SYNC control input is used to synchronize all divider outputs of the post divider. When a HIGH-LOW transition is applied to the SYNC control input the outputs are disabled when all post-divider outputs are LOW, see “Output Synchronization Controlled by SYNC Timing Diagram” for details. Once SYNC is asserted with a rising edge, the outputs are enabled when all internal divider stages are reaching their LOW state. This ensures a simultaneous switching of all outputs with the next LOW-HIGH transition of the pre-divider clock.

PLL Loop Stability

For the loop filter configurations shown in Figure 4, Table 10 below summarizes the PLL's loop stability in terms of damping factor, natural frequency, and bandwidth, and illustrates the pole and zero cutoff frequencies determined by the loop filter when the SY89538L is driven by a 14MHz to 18MHz crystal when the feedback divider is effectively 168.

Parameter										Units
Vcc	3	3	3	3.3	3.3	3.3	3.6	3.6	3.6	V
RM Temperature	-40	-40	-40	25	25	25	85	85	85	C
Die Temperature	-18	-18	-18	55	55	55	125	125	125	C
VCO Frequency	2352	2800	3024	2352	2800	3024	2352	2800	3024	MHz
Charge Pump Current	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	1.80E-04	A
Loop Filter Resistor	50	50	50	50	50	50	50	50	50	Ohms
Zero Capacitor	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	4.70E-07	F
Pole Capacitor	1.00E-10	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	1.00E-09	F
VCO Gain (KVCO)	3.20E+09	4.50E+09	4.50E+09	2.80E+09	3.30E+09	3.10E+09	2.30E+09	1.70E+09	1.30E+09	Hz/V
Feedback Divider	168	168	168	168	168	168	168	168	168	Integer
Phase Detector Frequency	14	16	18	14	16	18	14	16	18	MHz
Damping Factor	1.0	1.2	1.2	0.9	1.0	1.0	0.9	0.7	0.6	
Natural Frequency	13600.29	16127.95	16127.95	12721.90	13811.16	13386.09	11530.20	9912.83	8668.52	Hz
Ratio=Phase Detector Freq / Fc	513	417	469	586	568	681	714	1103	1623	

Table 10. PLL Loop Stability[1]

Note:

1. Feedback divider = 168 = 42 (6-bit programmable divider) x divide-by-2 x divide-by-2. Reference Frequency = 14, 16, and 18MHz.

Figure 6 shows the open and closed loop gain of the SY89538L. The closed loop-gain plot shows that the SY89538L when configured with the recommended loop filter values has essentially no jitter peaking near the -3dB point. In addition, the open loop curve shows the frequency at which unity gain occurs for a typical case of the SY89538L with V_{CC} = 3.3V at T_A = 25°C. At unity gain, Figure 7 can be used to determine the phase margin or stability of the SY89538L.

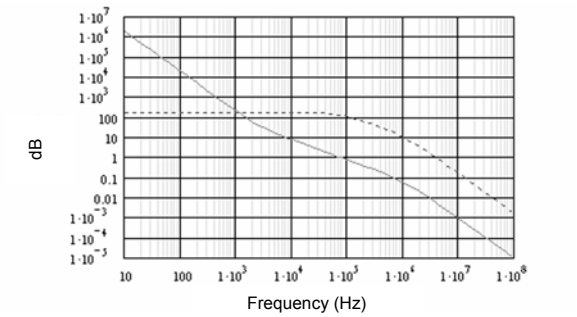


Figure 6. Open and Closed Loop Gain at V_{CC} = 3.3V, T_A = 25°C

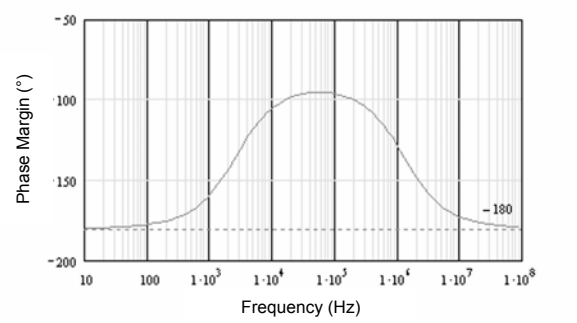


Figure 7. Phase Margin Plot at V_{CC} = 3.3V, T_A = 25°C

Figure 8 illustrates the VCO frequency versus the loop filter control voltage at 3.3V, T_A = 25°C. The normal loop filter control voltage is -300mV to +300mV. Figure 9 illustrates the VCO gain curve at V_{CC} = 3.3V, T_A = 25°C. With this set of information, determining the loop stability with other sets of loop filter configurations is possible.

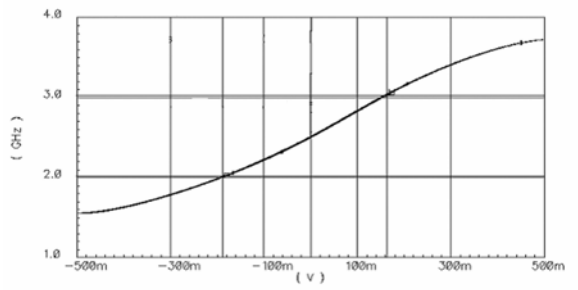


Figure 8. Loop Filter Control Voltage vs. Frequency at 3.3V, T_A = 25°C

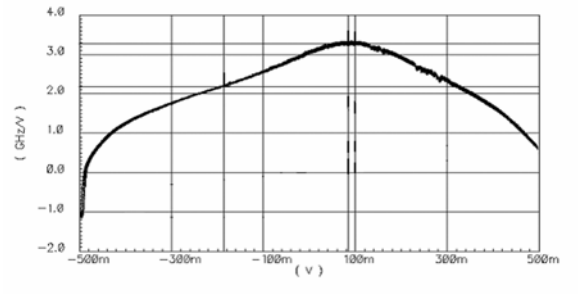


Figure 9. Frequency vs. Loop Filter Control Voltage at 3.3V, T_A = 25°C

Input Interface

RFCK and FBIN are designed to accept any differential or single-ended input signal 300mV above V_{CC} or 300mV below GND. RFCK and FBIN should not be left floating. Tie either the true or complement input to GND, but not both. A logic zero is achieved by connecting the complement input to GND with the true input floating. For TTL input, tie a 2.5kΩ resistor between the complement input and GND. LVDS, CML and HSTL differential signals may be connected directly to the reference inputs.

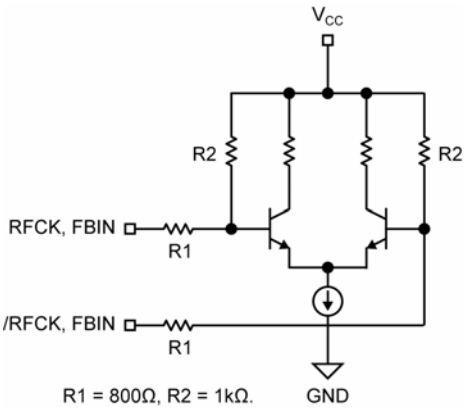


Figure 10. Simplified Input Structure

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Input Termination (RFCK and FBIN)

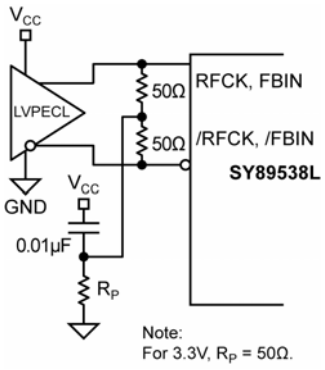

Figure 11a. LVPECL Interface (DC-Coupled)

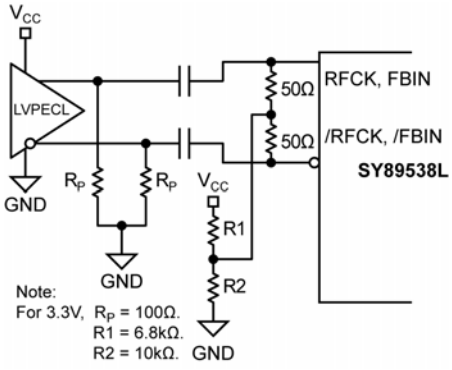

Figure 11b. LVPECL Interface (AC-Coupled)

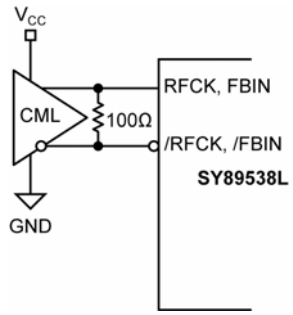

Figure 11c. CML Interface (DC-Coupled)

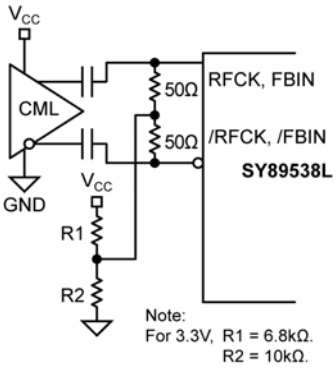

Figure 11d. CML Interface (AC-Coupled)

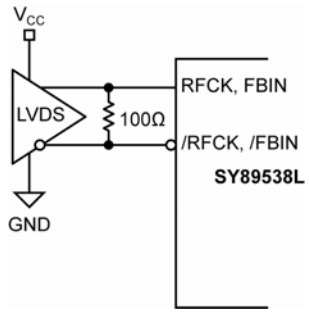

Figure 11e. LVDS (DC-Coupled)

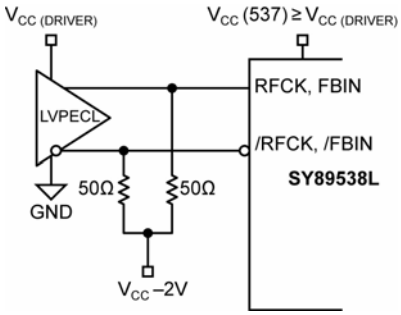

Figure 11f. 2.5V LVPECL (DC-Coupled)

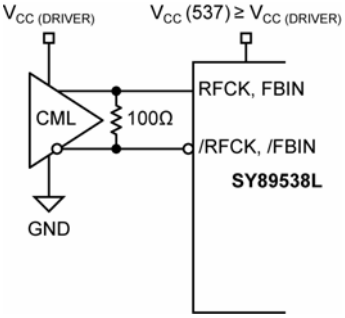

Figure 11g. 2.5V CML (DC-Coupled)

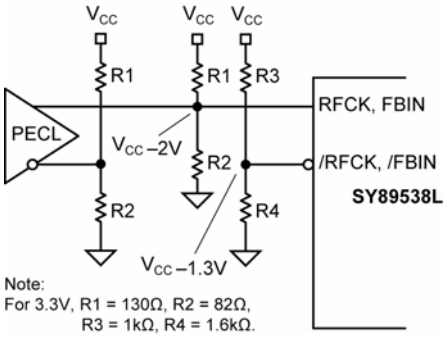

Figure 11h. Single-Ended Input Interface

Output Bank and Frequency Control

There are five independently programmable output frequency banks, four differential LVPECL output banks and one differential LVDS output bank with three output pairs. Each bank has frequency control DSEL, SELx and Enx to generate different divider ratios (see "LVPECL and LVDS Output Post-Divider Frequency Select" Tables). It can be programmed for pass-through, internal divided VCO clock divide-by-/2, /8 or disable state. When disabled, the non-inverted output goes to static LOW and the inverted output goes to static HIGH.

Output Logic Characteristics

See "Output Termination Recommendations" for proper termination. When LVPECL single-ended output is desired, the unused complimentary output should be terminated. Unused LVPECL output pairs can be left floating. LVDS output pairs should be terminated with 100Ω across the pair. In order to minimize jitter and skew, unused LVDS output banks and unused LVDS output pairs should be terminated with 100Ω across each pair.

LVPECL Outputs:

- Typical voltage swing is 800mV into 50Ω.
- Common mode voltage is V_{CCO}–1.3V.

LVDS Outputs:

- Typical voltage swing is 325mV into 100Ω.
- Common mode voltage is 1.2V.

Output Termination Recommendations

LVPECL

LVPECL has high input impedance, very low output (open emitter) impedance, and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω-and-100Ω-controlled impedance transmission lines. There are several techniques for terminating the LVPECL output: Single-ended termination, Parallel Termination Thevenin-Equivalent, 3-Resistor Y-Termination, and AC-coupled termination.

Single-Ended LVPECL Termination

Unused output pairs may be left floating. Terminating single-ended and unused outputs will enhance the performance. Terminate LVPECL outputs by 50Ω to V_{CC}–2V. The unused input terminal must be biased to V_{CC}–1.3V using a resistor network. See Figure 11h for more details.

DC-Coupled LVPECL Parallel Termination

Terminate LVPECL by an output impedance of 50Ω to V_{CC}–2V. Termination resistor values are a function of V_{CC}. For a 3.3V supply, the optimal parallel combination is 130Ω||82Ω. See Figure 12a for details.

The LVPECL output can also be terminated with three 50Ω resistors as shown in Figure 12b. A 0.1µF low ESR decoupling capacitor from V_{CC} to Y-Junction is recommended in order to reduce noise in the signal.

AC-Coupled LVPECL Termination

While terminating an AC-coupled LVPECL signal, pull-down resistor is used to create a DC current path to GND to produce an output swing. For 3.3V supply, 100Ω provides the necessary pull-down. At the final destination, proper termination to create a V_{CC}–1.3V termination bias is required 82Ω||130Ω. Please refer to Figure 12c.

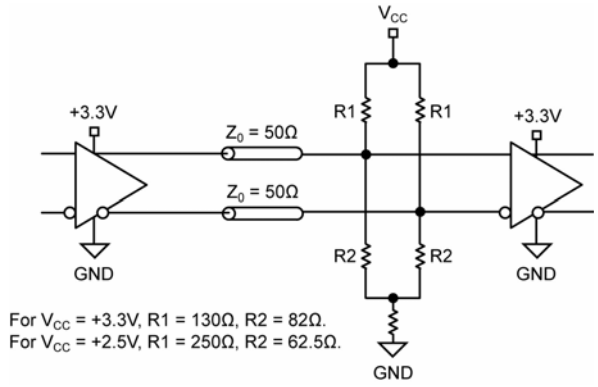

Figure 12a. LVPECL Parallel Thevenin-Equivalent

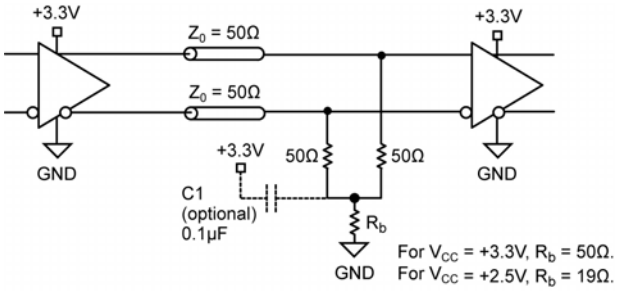

Figure 12b. LVPECL Parallel Termination

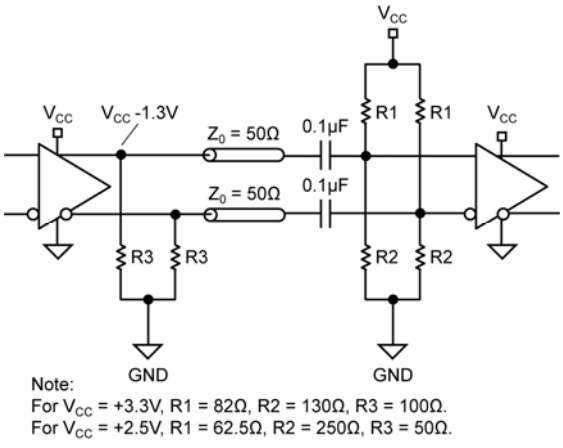

Figure 12c. LVPECL AC-Coupled Parallel Thevenin-Equivalent

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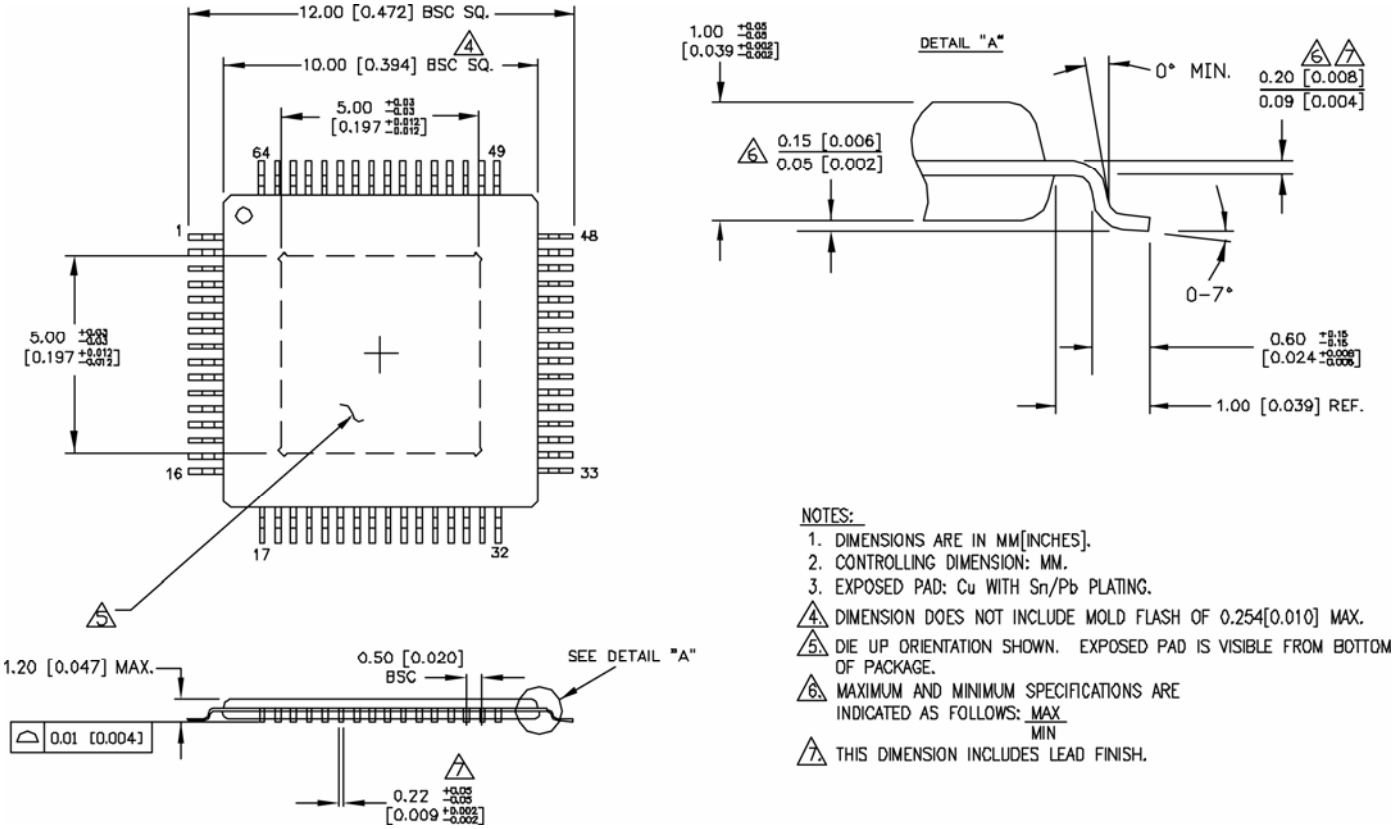
LVDS

LVDS specifies a small swing of 325mV typical, on a nominal 1.2V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of LVDS input, is kept to a minimum, to keep EMI low conveniently to ASKs and FPGAs. Each LVDS output pair requires 100Ω across the differential pair at the end destination (often intended integrated into the ASIC).

Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY89537L	3.3V, Precision LVPECL and LVDS Programmable, Multiple Output Bank Clock Synthesizer and Fanout Buffer with Zero Delay	http://www.micrel.com/product-info/products/sy89537l.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml
	MLF™ Application Note	www.amkor.com/products/notes_papers/MLFAppNote.pdf

Package Information



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