DIFFERENTIAL-TO-0.7V DIFFERENTIAL PCI EXPRESS™ JITTER ATTENUATOR

ICS871004I-04

General Description

The ICS871004I-04 is a high performance Differential-to-0.7V Differential Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, highphase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS871004I-04 has 3 PLL bandwidth modes: 200kHz, 400kHz and 800kHz. The 200kHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 400kHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. The 800kHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. The ICS871004I-04 can be set for different modes using the F_SEL pins as shown in Table 3C.

The ICS871004I-04 uses IDT's 3rd Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 24 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

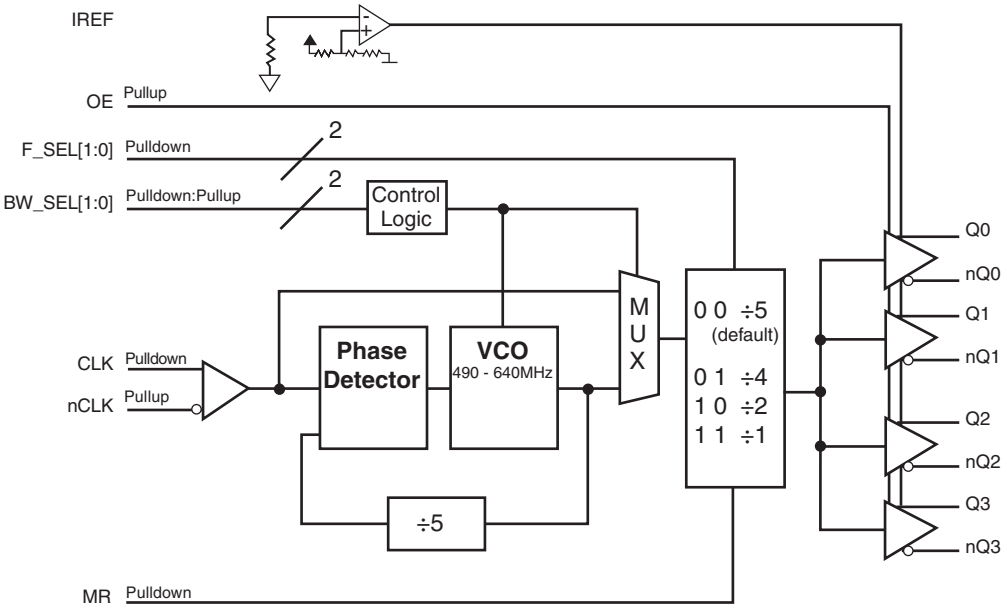
Features

- Four 0.7V differential output pairs
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 640MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 19ps (typical)
- Additive phase jitter, RMS: 0.23ps (typical)
- 3.3V operating supply
- Three bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

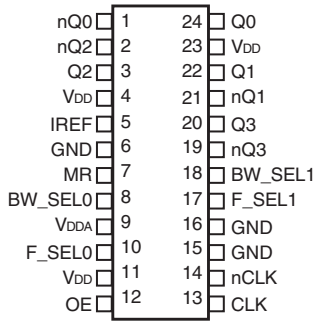
PLL Bandwidth

BW_SEL[1:0]
0 0 = PLL Bandwidth: ~200kHz
0 1 = PLL Bandwidth: ~400kHz (default)
1 0 = PLL Bandwidth: ~800kHz
1 1 = PLL BYPASS

Block Diagram



Pin Assignment



ICS871004I-04
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm package body
G Package
Top View

The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 24	nQ0, Q0	Output		Differential output pair. PCI Express interface levels.
2, 3	nQ2, Q2	Output		Differential output pair. PCI Express interface levels.
4, 11, 23	V_{DD}	Power		Core supply pin.
5	IREF	Input		A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode QAx/nQAx and QBx/nQBx clock outputs.
6, 15, 16	GND	Power		Power supply ground.
7	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (nQx) to go low and the inverted outputs (Qx) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
8	BW_SEL0	Input	Pullup	Selects PLL Bandwidth input. LVCMOS/LVTTL interface levels. See Table 3B.
9	V_{DDA}	Power		Analog supply pin.
10, 17	F_SEL0, F_SEL1	Input	Pulldown	Frequency select pins. LVCMOS/LVTTL interface levels. See Table 3C.
12	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
13	CLK	Input	Pulldown	Non-inverting differential clock input.
14	nCLK	Input	Pullup	Inverting differential clock input.
18	BW_SEL1	Input	Pulldown	Selects PLL Bandwidth input. LVCMOS/LVTTL interface levels. See Table 3B.
19, 20	nQ3, Q3	Output		Differential output pair. PCI Express interface levels.
21, 22	nQ1, Q1	Output		Differential output pair. PCI Express interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3A. OUTPUT ENABLE FUNCTION TABLE

Inputs	Outputs	
OE	**Q0:Q3**	**nQ0:nQ3**
0	HiZ	HiZ
1	Enabled	Enabled

TABLE 3B. PLL BANDWIDTH/PLL BYPASS CONTROL

Inputs		PLL Bandwidth
BW_SEL1	**BW_SEL0**	
0	0	~200kHz
0	1	~400kHz (default)
1	0	~800kHz
1	1	PLL BYPASS

TABLE 3C. FREQUENCY SELECT FUNCTION TABLE

Inputs				Output Frequency Range (MHz)
Input Frequency	**F_SEL1**	**F_SEL0**	**Divider Value**	
100	0	0	5	100 (default)
100	0	1	4	125
100	1	0	2	250
100	1	1	1	500

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	82.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} – I_{DDA}$*10Ω	3.3	V_{DD}	V
I_{DD}	Power Supply Current			TBD		mA
I_{DDA}	Analog Supply Current			TBD		mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	MR, OE, F_SEL0. F_SEL1,		2		V_{DD} + 0.3	V
		BW_SEL0, BW_SEL1		V_{DD} - 0.3		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	MR, OE, F_SEL0. F_SEL1,		-0.3		0.8	V
		BW_SEL0, BW_SEL1		-0.3		0.3	V
I_{IH}	Input High Current	BW_SEL0, OE	$V_{DD} = V_{IN}$ = 3.465V			5	µA
		MR, BW_SEL1, F_SEL0. F_SEL1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	BW_SEL0, OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		MR, BW_SEL1, F_SEL0. F_SEL1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, $V_{DD} = V_{DDA} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK,	$V_{DD} = V_{IN}$ = 3.465V	5			µA
I_{IL}	Input Low Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		nCLK	$V_{DD} = V_{IN}$ = 3.465V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK at V_{DD} + 0.3V.

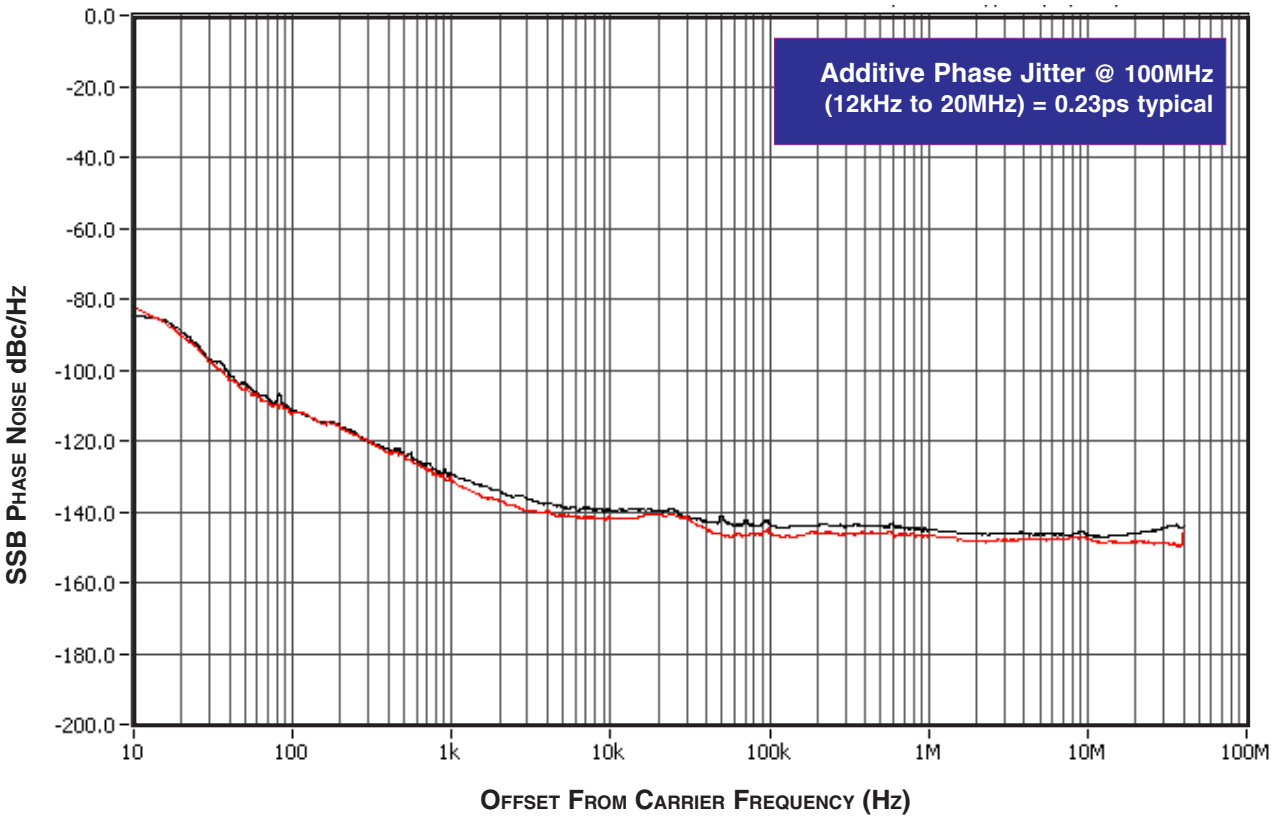
TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 10\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		98		640	MHz
t_{PD}	Propagation Delay; NOTE 1	PLL in BYPASS Mode		3.8		ns
*t*jit	Buffer Additive Phase Jitter, RMS; Refer to Additive Phase Jitter Section	PLL in BYPASS Mode 100MHz, Integration Range: 12kHz - 20MHz		0.23		ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 2	PLL Mode		19		ps
t_L	PLL Lock Time			TBD		ms
V_{HIGH}	Voltage High		660		850	mV
V_{LOW}	Voltage Low		-150			mV
V_{OVS}	Max. Voltage, Overshoot				V_{HIGH} + 0.3	V
V_{UDS}	Min. Voltage, Undershoot		-0.3			V
V_{rb}	Ringback Voltage				0.2	V
V_{CROSS}	Absolute Crossing Voltage		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges				140	mV
t_R / t_F	Output Rise/Fall Time	measured between 0.175 to 0.525		475		ps
$\Delta t_R / \Delta t_F$	Rise/Fall Time Variation				125	ps
t_{RFM}	Rise/Fall Matching				125	ps
odc	Output Duty Cycle			50		%

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

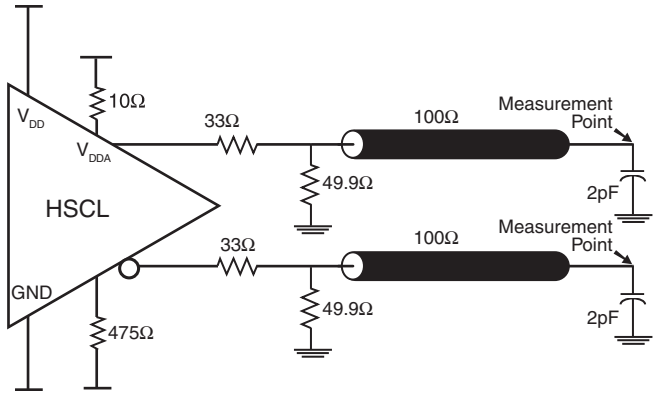
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

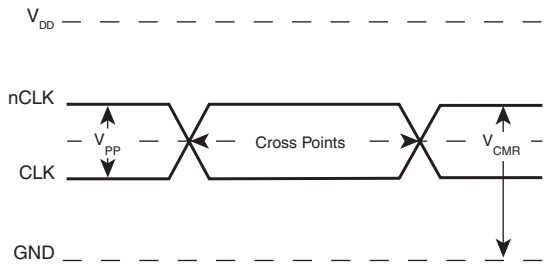


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

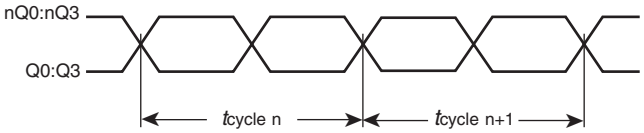
PARAMETER MEASUREMENT INFORMATION



3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT - TBD

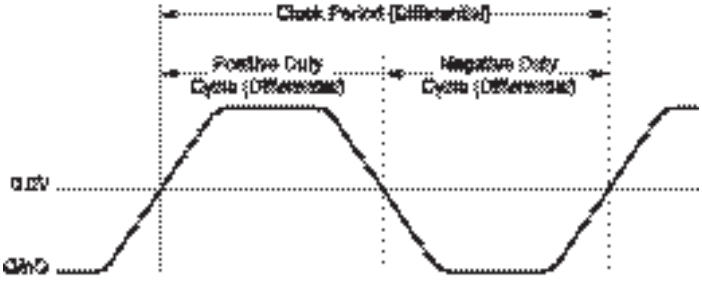


DIFFERENTIAL INPUT LEVEL

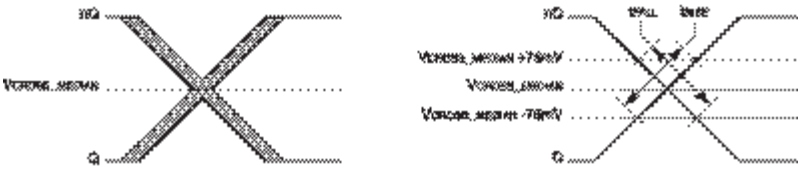


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

CYCLE-TO-CYCLE JITTER

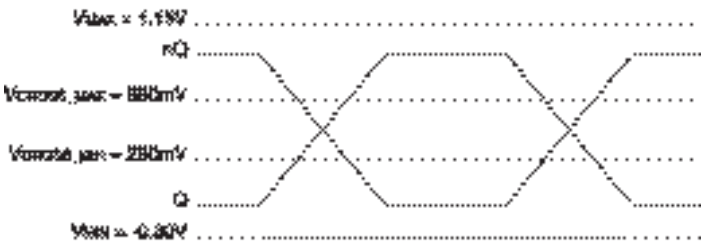


DIFFERENTIAL MEASUREMENT POINTS FOR DUTY CYCLE/PERIOD

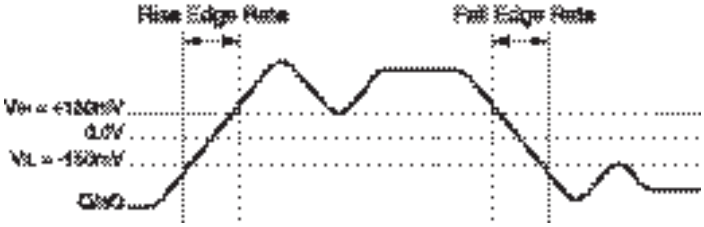


SE MEASUREMENT POINTS FOR RISE/FALL TIME MATCHING

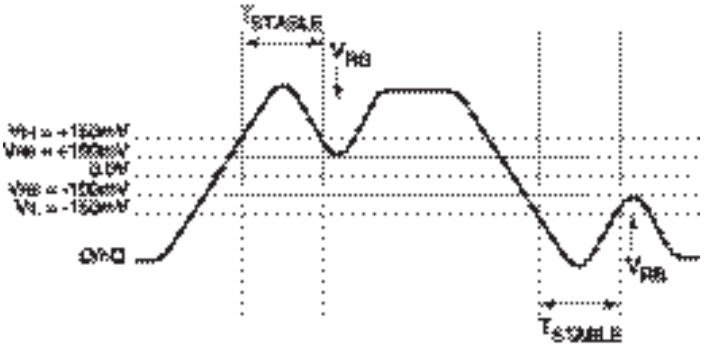
PARAMETER MEASUREMENT INFORMATION, CONTINUED



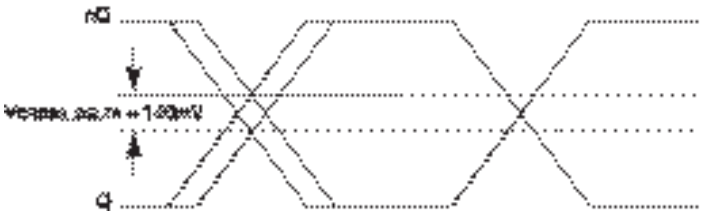
SE MEASUREMENT POINTS FOR ABSOLUTE CROSS POINT/SWING



DIFFERENTIAL MEASUREMENT POINTS FOR RISE/FALL TIME



DIFFERENTIAL MEASUREMENT POINTS FOR RINGBACK



SE MEASUREMENT POINTS FOR DELTA CROSS POINT

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS871004I-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

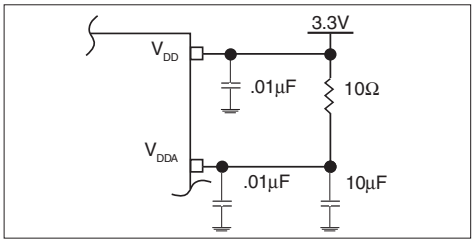


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

DIFFERENTIAL OUTPUTS

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

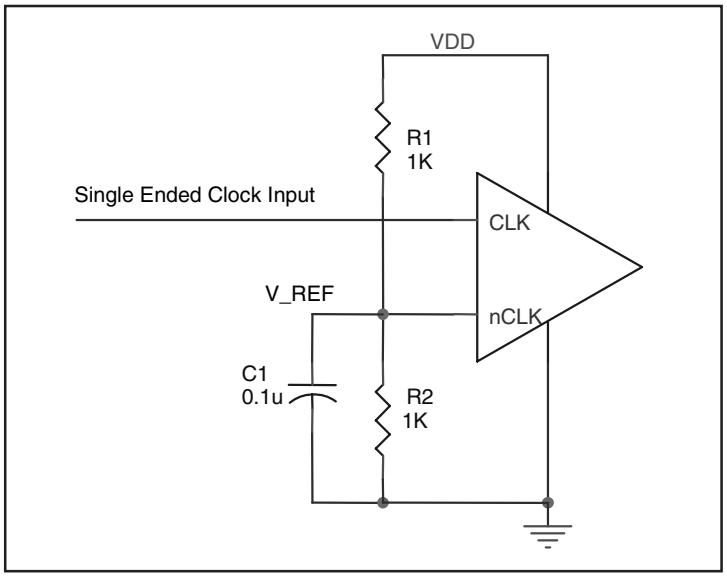


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

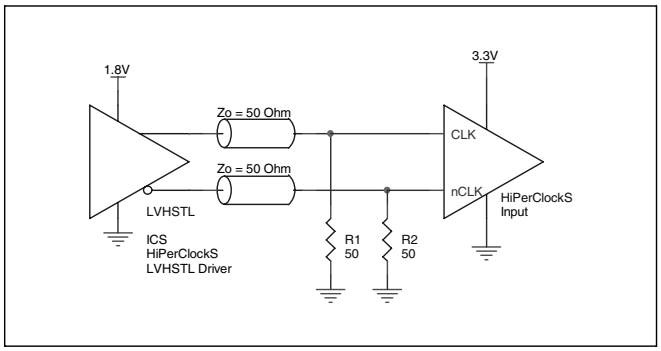


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY AN IDT OPEN EMITTER HIPERCLOCKS LVHSTL DRIVER

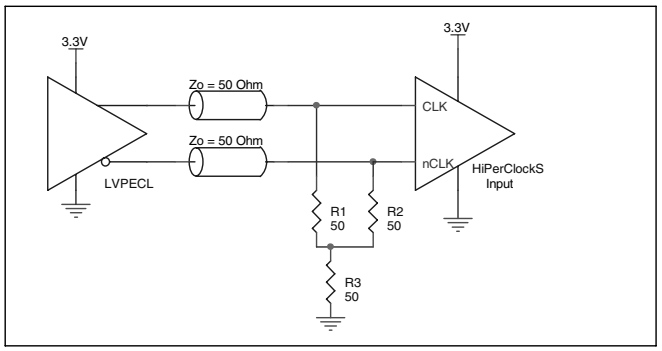


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

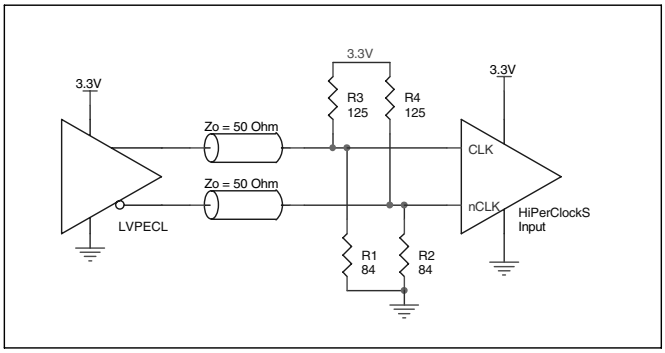


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

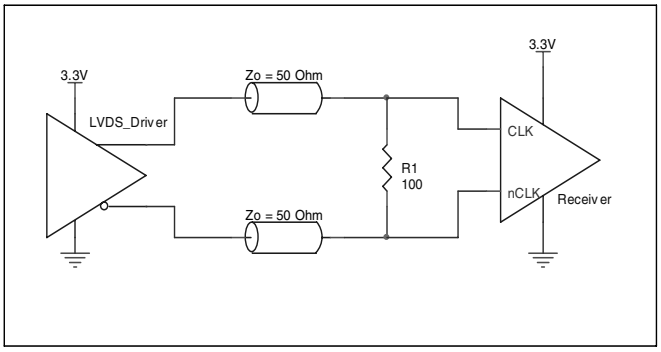


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

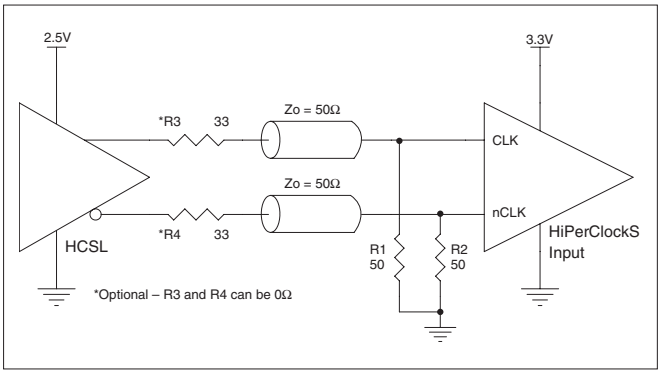


FIGURE 3E. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 3.3V HCSL DRIVER

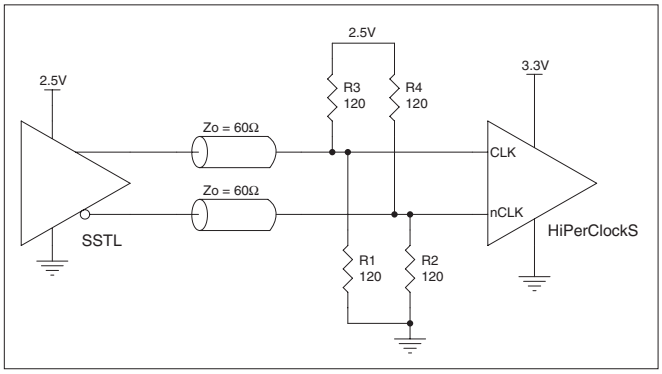


FIGURE 3F. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY A 2.5V SSTL DRIVER

RECOMMENDED TERMINATION

Figure 4A is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ù impedance.

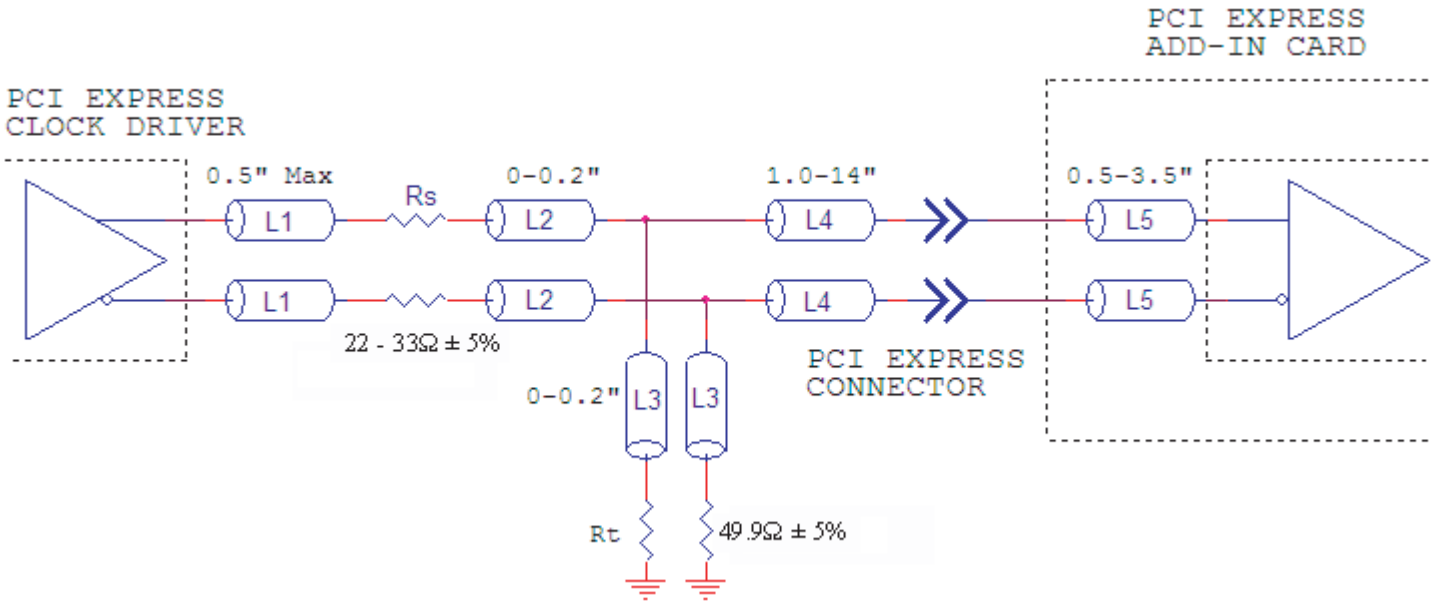


FIGURE 4A. RECOMMENDED TERMINATION

Figure 6B is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ù impedance.

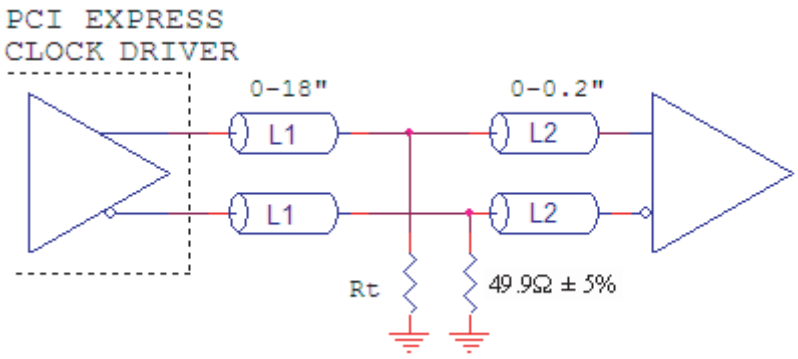


FIGURE 4B. RECOMMENDED TERMINATION

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	82.3°C/W	78°C/W	75.9°C/W

TRANSISTOR COUNT

The transistor count for ICS871004I-04 is: 1395

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

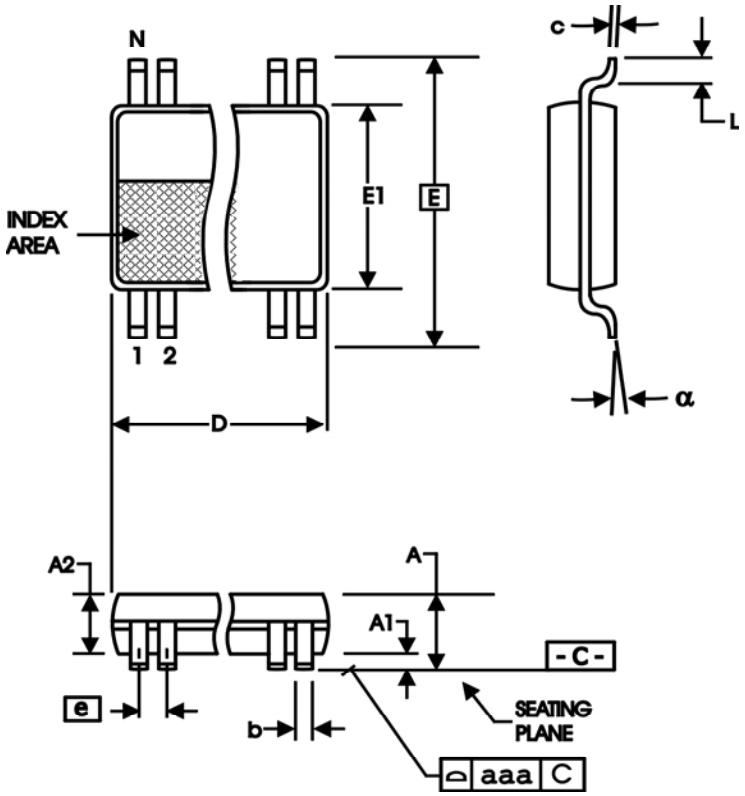


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS871004AGI-04	ICS871004AI04	24 Lead TSSOP	tube	-40°C to 85°C
ICS871004AGI-04T	ICS871004AI04	24 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS871004AGI-04LF	ICS71004AI04L	24 Lead "Lead-Free" TSSOP	Tray	-40°C to 85°C
ICS871004AGI-04LFT	ICS71004AI04L	24 Lead "Lead-Free" TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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