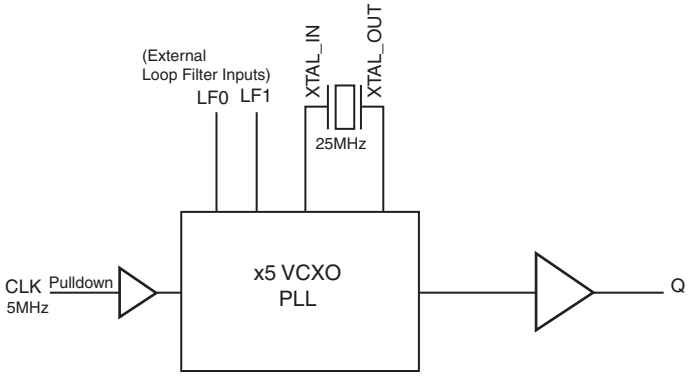
General Description

The ICS810525I is a high performance, low jitter/low phase noise VCXO from IDT. The ICS810525I works in conjunction with a 25MHz pullable crystal to generate an LVCMOS/LVTTL output clock of 25MHz from an input clock of 5MHz. The frequency of the VCXO is adjusted by the VC control voltage input. The output range is ±100ppm around the nominal crystal frequency. The LF1 control voltage range is 0 – V_{DD}. The device is packaged in a small 16 TSSOP package and is ideal for use on space constrained boards.

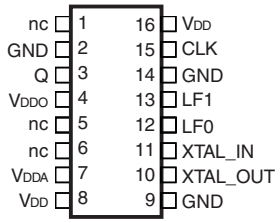
Features

- One single-ended LVCMOS/LVTTL output
- One single-ended clock accepts the following input types: LVCMOS, LVTTL
- Accepts input frequency of 5MHz
- Absolute pull range: 100ppm
- Proprietary multiplier provides low jitter, high frequency output
- RMS phase jitter @ 25MHz, using a 25MHz crystal (1kHz – 1MHz): 0.27ps (typical)
- Full 3.3V supply, or 3.3V core/2.5V output supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



ICS810525I
16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 5, 6	nc	Unused		No connect.
2, 9, 14	GND	Power		Power supply ground.
3	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
4	V_{DDO}	Power		Output power supply pin.
7	V_{DDA}	Power		Analog supply pin.
8, 16	V_{DD}	Power		Core power supply pins.
10, 11	XTAL_OUT, XTAL_IN	Input		VCXO crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
12, 13	LF0, LF1	Analog Input/Output		Loop filter connection node pins.
15	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.

NOTE: *Pulldown* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
C_{PD}	Power Dissipation Capacitance	V_{DDO} = 3.465V		8		pF
		V_{DDO} = 2.625V		5		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{OUT}	Output Impedance	V_{DDO} = 3.3V		15		Ω
		V_{DDO} = 2.5V		20		Ω

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	92.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.05	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				35	mA
I_{DDA}	Analog Supply Current				5	mA

Table 3B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.05	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				35	mA
I_{DDA}	Analog Supply Current				5	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{LF1}	VCXO Control Voltage		0		V_{DD}	V
I_{IH}	Input High Current	$V_{DD} = V_{IN} = 3.465V$ or 2.625V			150	µA
I_{IL}	Input Low Current	$V_{DD} = 3.465V$ or 2.625V, $V_{IN} = 0V$	-5			µA
I_I	Input Current of V_{LF1} pin	$V_{DD} = 3.465V$ or 2.625V	-100		100	µA
V_{OH}	Output High Voltage	$V_{DDO} = 3.3V \pm 5\%$, I_{OH} = -12mA	2.6			V
		$V_{DDO} = 2.5V \pm 5\%$, I_{OH} = -12mA	1.8			V
V_{OL}	Output Low Voltage	$V_{DDO} = 3.3V$ or $2.5V \pm 5\%$ I_{OL} = 12mA			0.5	V

TABLE 4A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V±5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				25	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	Integration Range: 1kHz – 1MHz		0.27		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	500		1200	ps
odc	Output Duty Cycle		48		52	%

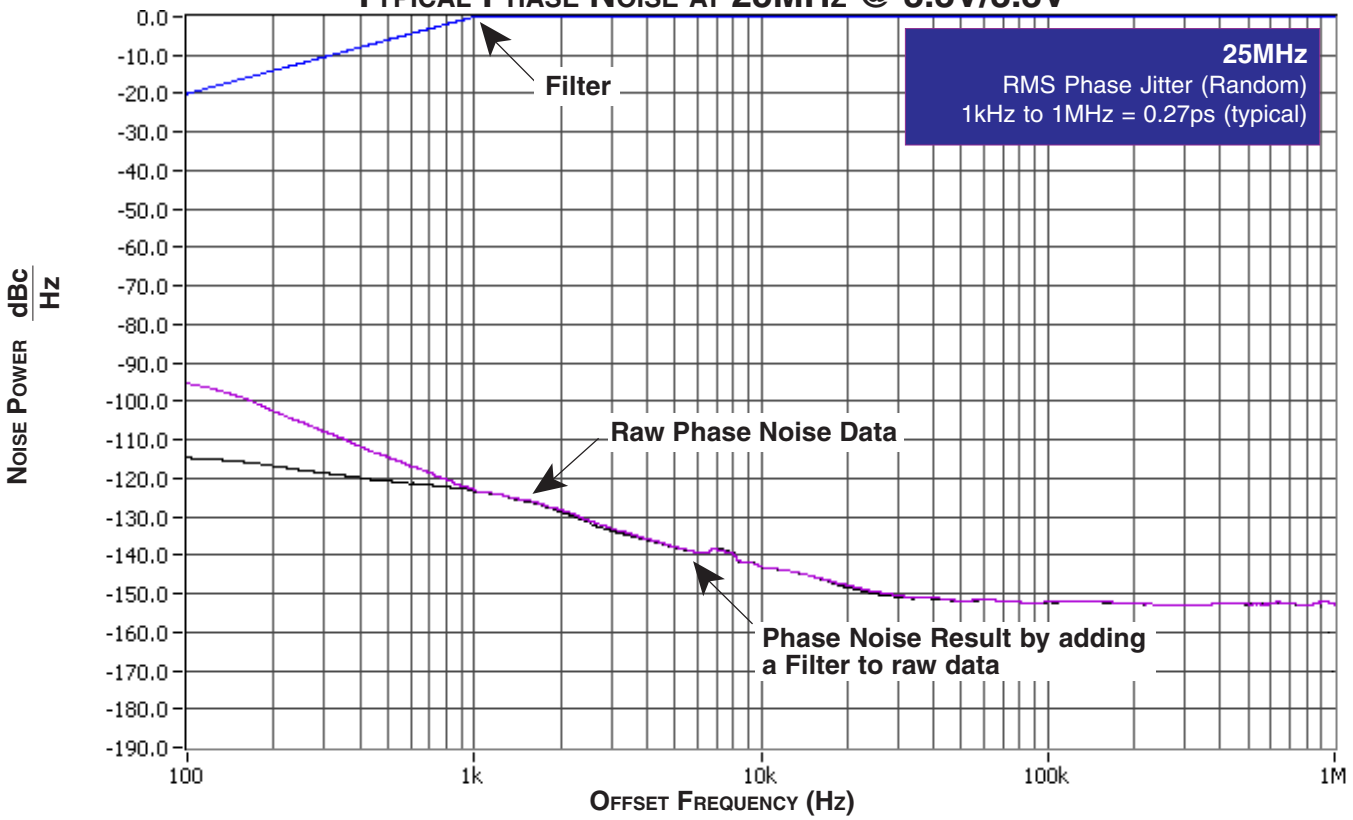
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
Characterized using a 3kHz bandwidth filter.
NOTE 1: Please refer to the Phase Noise Plot.

TABLE 4B. AC CHARACTERISTICS, $V_{DD} = 3.3V±5\%$, $V_{DDO} = 2.5V±5\%$, T_A = -40°C TO 85°C

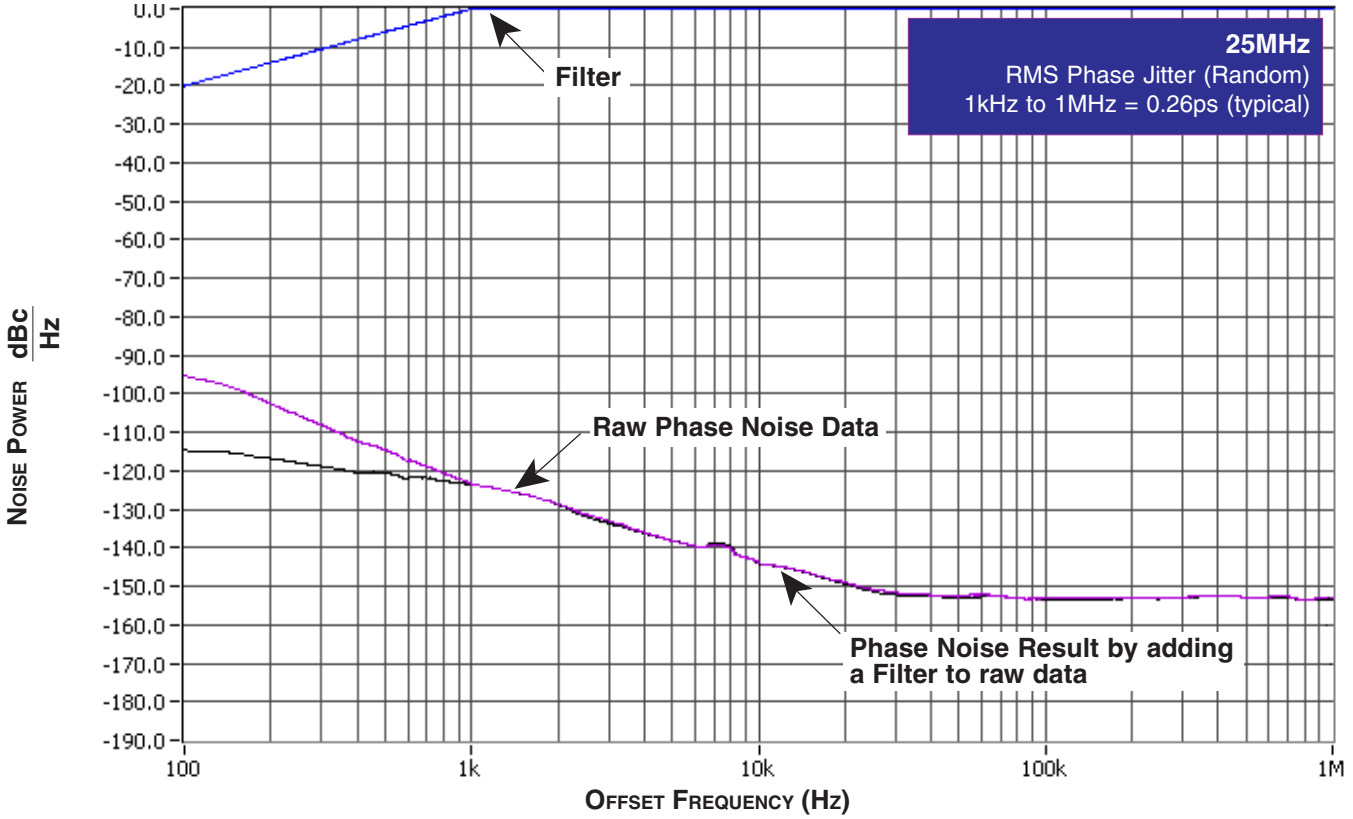
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				25	MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	Integration Range: 1kHz – 1MHz		0.26		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	600		2100	ps
odc	Output Duty Cycle		44		56	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
Characterized using a 3kHz bandwidth filter.
NOTE 1: Please refer to the Phase Noise Plot.

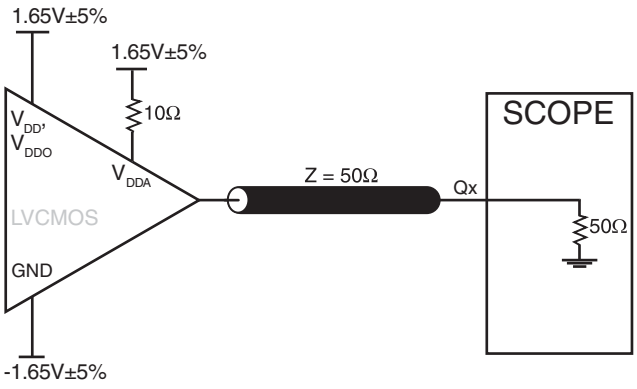
TYPICAL PHASE NOISE AT 25MHZ @ 3.3V/3.3V



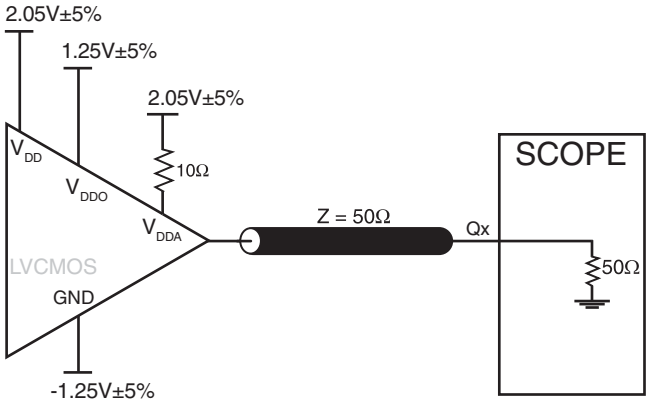
TYPICAL PHASE NOISE AT 25MHZ @ 3.3V/2.5V



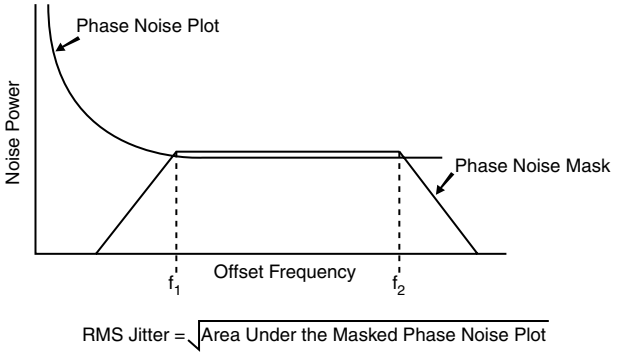
Parameter Measurement Information



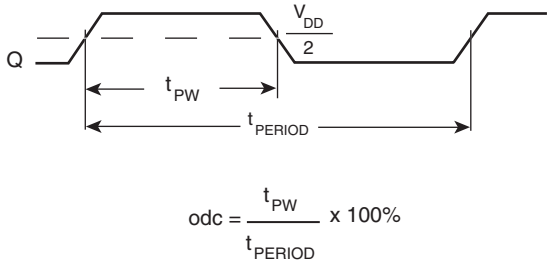
3.3V Core/3.3V Output Load AC Test Circuit



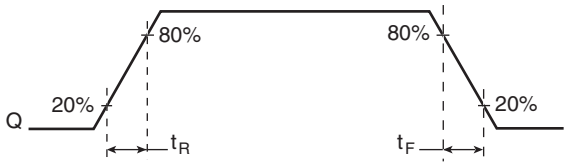
3.3V Core/2.5V Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

APPLICATION INFORMATION

SCHEMATIC EXAMPLE

Figure 1 shows an example of the ICS810525I application schematic. In this example, the device is operated at V_{DD} = 3.3V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVCMOS driver. A 2-pole filter loop filter with Low LBW setting is used in this example. It is recommended to refer to the ICS810525I datasheet for more detail on loop filter values.

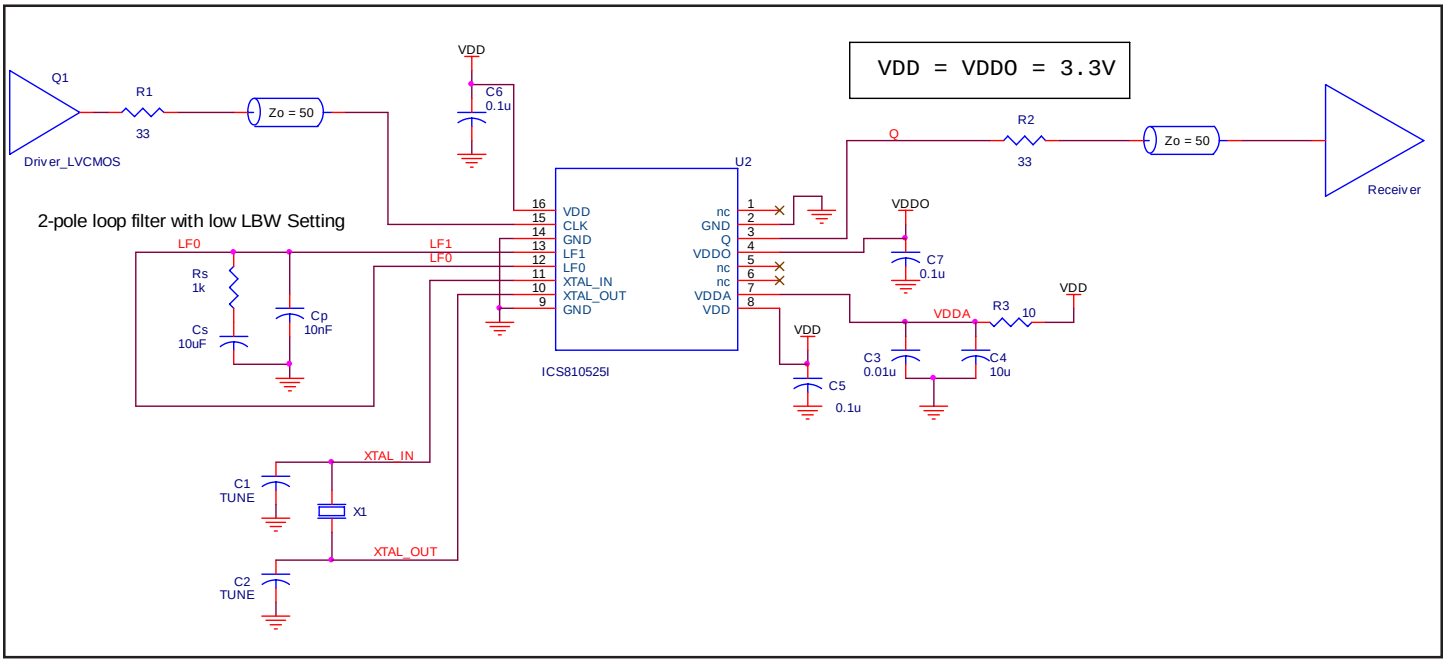


FIGURE 1. ICS810525I SCHEMATIC EXAMPLE

VCXO-PLL External Components

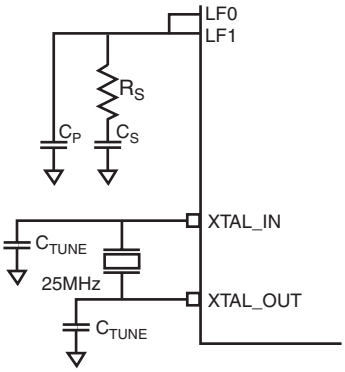
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note.*

The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal's C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal's C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependent on the characteristics of the VCXO. The recommended C_L in the Crystal Parameter Table balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows R_S, C_S and C_P values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note.*

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO Characteristics Table

Symbol	Parameter	Typical	Unit
k_{VCXO}	VCXO Gain	15	kHz/V
C_{V_LOW}	Low Varactor Capacitance	9.8	pF
C_{V_HIGH}	High Varactor Capacitance	22.7	pF

VCXO-PLL Approximate Loop Bandwidth Selection Table

Bandwidth	Crystal Frequency (MHz)	R_S (kΩ)	C_S (µF)	C_P (pF)
125Hz (Low)	25MHz	1	10	10000
1.5kHz (Mid)	25MHz	12	0.1	100
3kHz (High)	25MHz	25	0.1	100

Crystal Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
	Mode of Operation		Fundamental		
f_N	Frequency		25		MHz
f_T	Frequency Tolerance			±20	ppm
f_S	Frequency Stability			±20	ppm
	Operating Temperature Range	-40		85	°C
C_L	Load Capacitance		10		pF
C_O	Shunt Capacitance		4		pF
C_O/C_1	Pullability Ratio		220	240	
ESR	Equivalent Series Resistance			40	Ω
	Drive Level			1	mW
	Aging @ 25°C			±3 per year	ppm

Reliability Information

Table 5. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	92.4°C/W	88.0°C/W	85.9°C/W

Transistor Count

The transistor count for ICS810525I is: 635

Package Outline & Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

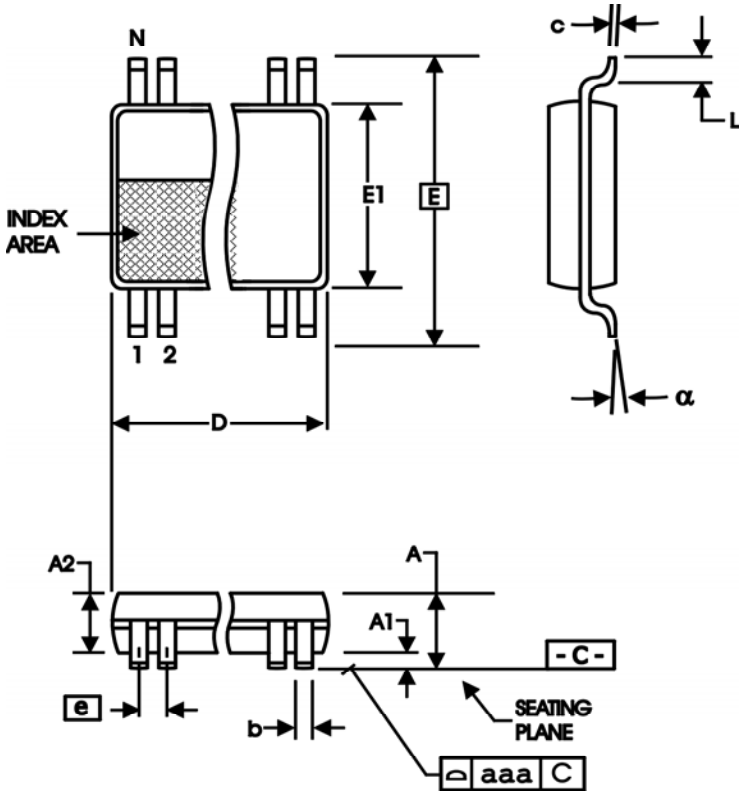


Table 6. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
810525AGILF	10525AIL	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
810525AGILFT	10525AIL	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T3C	3	LVCMOS DC Characteristics - added to V_{OH}/V_{OL} test conditions.	2/24/09

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