

# MPEG Clock Generator with VCXO

## Features

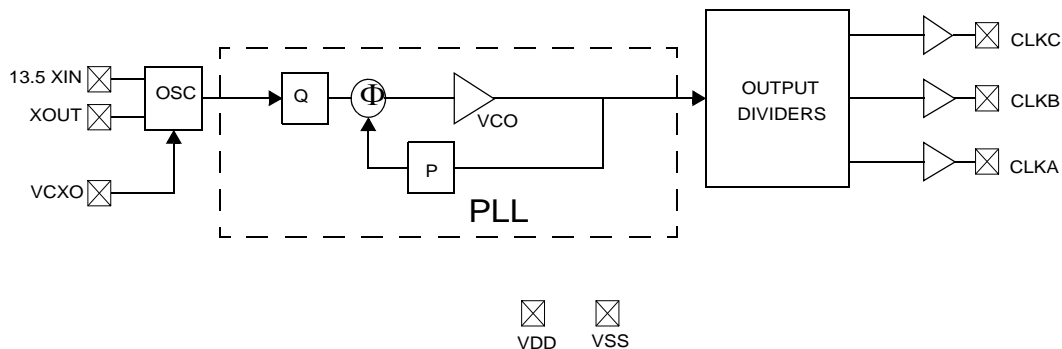
- Integrated phase-locked loop (PLL)
- Low-jitter, high-accuracy outputs
- VCXO with analog adjust
- 3.3V operation
- 8-pin SOIC package

## Benefits

- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
- Large  $\pm 150$ -ppm range, better linearity
- Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Profile
CY2412-1	3	13.5-MHz pullable crystal input per Cypress specification	Two 27 MHz outputs, one 54 MHz (3.3V)	Linear
CY2412-3	3	13.5-MHz pullable crystal input per Cypress specification	27 MHz, 13.5 MHz, 54 MHz (3.3V)	Linear

## Logic Block Diagram



## Pin Configuration

Figure 1. CY2412, 8-Pin SOIC

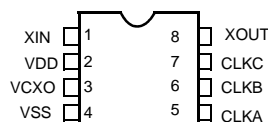


Table 1. Pin Definition - CY2412, 8-Pin SOIC

Pin Name	Pin Number	Pin Description
X <sub>IN</sub>	1	Reference Crystal Input
V <sub>DD</sub>	2	Voltage Supply
VCXO	3	Input Analog Control for VCXO
V <sub>SS</sub>	4	Ground
CLKA	5	54-MHz clock output
CLKB	6	13.5-MHz clock output
CLKC	7	27-MHz clock output
X <sub>OUT</sub> <sup>[2]</sup>	8	Reference Crystal Output

## Pullable Crystal Specifications<sup>[1]</sup>

Parameter	Description	Condition	Min	Typ.	Max	Unit
F <sub>NOM</sub>	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	13.5	–	MHz
C <sub>LNOM</sub>	Nominal load capacitance		–	14	–	pF
R <sub>1</sub>	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R <sub>3</sub> /R <sub>1</sub>	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R <sub>1</sub> values are much less than the maximum spec.	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2.0	mW
F <sub>3SEPHI</sub>	Third overtone separation from 3*F <sub>NOM</sub>	High side	300	–	–	ppm
F <sub>3SEPLO</sub>	Third overtone separation from 3*F <sub>NOM</sub>	Low side	–	–	–150	ppm
C <sub>0</sub>	Crystal shunt capacitance		–	–	7	pF
C <sub>0</sub> /C <sub>1</sub>	Ratio of shunt to motional capacitance		180	–	250	
C <sub>1</sub>	Crystal motional capacitance		14.4	18	21.6	pF

## Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	–0.5	7.0	V
T <sub>S</sub>	Storage Temperature <sup>[3]</sup>	–65	125	°C
T <sub>J</sub>	Junction Temperature	–	125	°C
	Digital Inputs	V <sub>SS</sub> – 0.3	V <sub>DD</sub> + 0.3	V
	Digital Outputs referred to V <sub>DD</sub>	V <sub>SS</sub> – 0.3	V <sub>DD</sub> + 0.3	V
	Electrostatic Discharge	2		kV

## Recommended Operating Conditions

Parameter	Description	Min	Typ.	Max	Unit
V <sub>DD</sub>	Operating Voltage	3.14	3.3	3.47	V
T <sub>A</sub>	Ambient Temperature	0		70	°C
C <sub>LOAD</sub>	Max. Load Capacitance			15	pF
f <sub>REF</sub>	Reference Frequency		13.5		MHz
t <sub>PU</sub>	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

## DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> – 0.5, V <sub>DD</sub> = 3.3V	12	24		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V	12	24		mA
C <sub>IN</sub>	Input Capacitance				7	pF
I <sub>IZ</sub>	Input Leakage Current			5		μA

### Notes

- Crystals that meet this specification includes: Ecliptek ECX-5788-13.500M, Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL, PDI HA13500XFSA14XC.
- Float X<sub>OUT</sub> if X<sub>IN</sub> is externally driven.
- Rated for ten years.

## DC Electrical Characteristics (continued)

Parameter	Description	Test Conditions	Min	Typ.	Max	Unit
$f_{\Delta XO}$	VCXO pullability range		$\pm 150$			ppm
$V_{VCXO}$	VCXO input range		0		$V_{DD}$	V
$f_{VBW}$	VCXO input bandwidth			DC to 200		kHz
$I_{DD}$	Supply Current	Sum of Core and Output Current			35	mA

## AC Electrical Characteristics

Parameter <sup>[4]</sup>	Description	Test Conditions	Min	Typ.	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 2, 50% of $V_{DD}$	45	50	55	%
ER	Rising Edge Rate	Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$ , $C_{LOAD} = 15$ pF. See Figure 3.	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$ , $C_{LOAD} = 15$ pF. See Figure 3.	0.8	1.4		V/ns
$t_j$	Clock Jitter	Peak to Peak period jitter		100	200	ps
$t_{10}$	PLL Lock Time				3	ms

Figure 2. Duty Cycle Definition;  $DC = t_2/t_1$

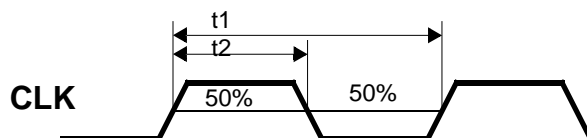


Figure 3. Rise and Fall Time Definitions:  $ER = 0.6 \times V_{DD} / t_3$ ,  $EF = 0.6 \times V_{DD} / t_4$

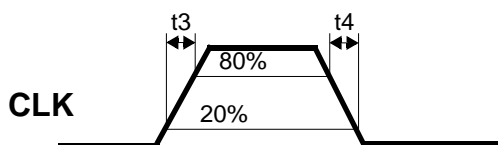
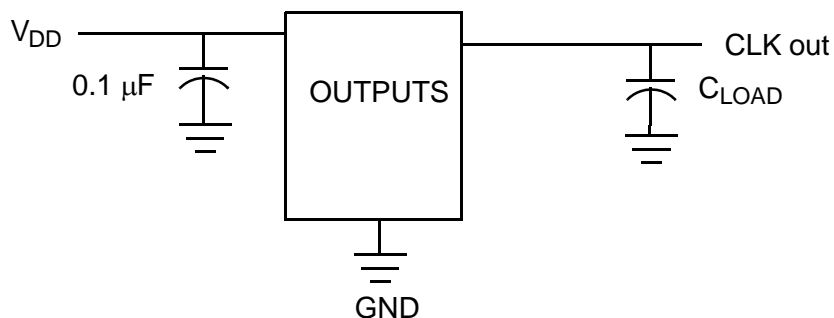


Figure 4. Test Circuit



### Notes

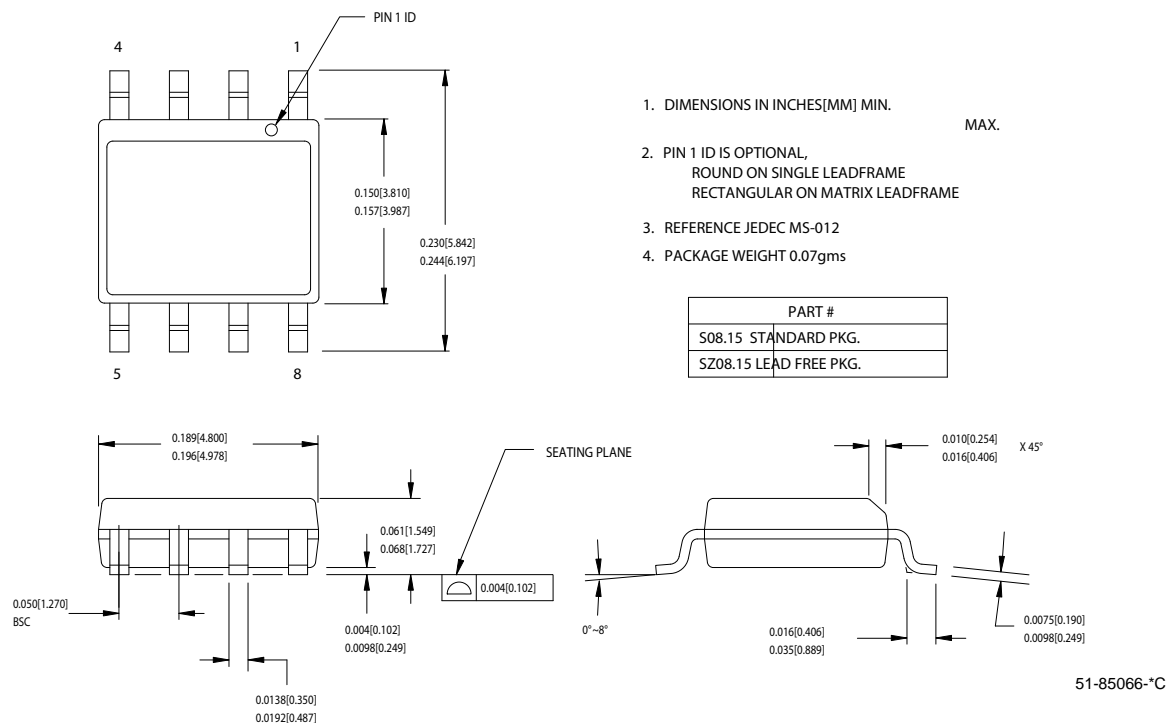
4. Not 100% tested.

## Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage
CY2412SC-1 <sup>[5]</sup>	8-pin SOIC	Commercial	3.3V
CY2412SC-1T <sup>[5]</sup>	8-pin SOIC–Tape and Reel	Commercial	3.3V
CY2412SC-3 <sup>[5]</sup>	8-pin SOIC	Commercial	3.3V
CY2412SC-3T <sup>[5]</sup>	8-pin SOIC–Tape and Reel	Commercial	3.3V
<b>Pb-Free</b>			
CY2412SXC-1 <sup>[5]</sup>	8-pin SOIC	Commercial	3.3V
CY2412SXC-1T <sup>[5]</sup>	8-pin SOIC–Tape and Reel	Commercial	3.3V
CY2412SXC-3 <sup>[5]</sup>	8-pin SOIC	Commercial	3.3V
CY2412SXC-3T <sup>[5]</sup>	8-pin SOIC–Tape and Reel	Commercial	3.3V
CY2412KSXC-1	8-pin SOIC	Commercial	3.3V
CY2412KSXC-1T	8-pin SOIC–Tape and Reel	Commercial	3.3V

## Package Diagram

Figure 5. 8-Lead (150-Mil) SOIC S8



### Note

- Not recommended for new designs.

## Document History Page

Document Title: CY2412 MPEG Clock Generator with VCXO Document Number: 38-07227				
REV.	ECN	Orig. of Change	Submission Date	Description of Change
**	110492	SZV	10/28/01	Change from Spec number: 38-00898 to 38-07227
*A	112457	CKN	03/14/02	Added CY2412-2 to data sheet
*B	116961	CKN	08/06/02	Removed CY2412-2 from the datasheet. Added CY2412-3 to data sheet
*C	121879	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*D	299735	RGL	02/15/05	Added lead-free for CY2412-1 and CY2412-3 devices
*E	2440866	AESA	04/25/08	Updated template. Added Note "Not recommended for new designs." Added part number CY2412KSXC-1, and CY2412KSXC-1T in ordering information table. Replaced Lead-Free with Pb-Free.
*F	2512734	AESA	06/05/08	Added border to Logic Block Diagram. Added Sales, Solutions, and Legal Information.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [cypress.com/sales](http://cypress.com/sales).

### Products

PSoC	<a href="http://psoc.cypress.com">psoc.cypress.com</a>
Clocks & Buffers	<a href="http://clocks.cypress.com">clocks.cypress.com</a>
Wireless	<a href="http://wireless.cypress.com">wireless.cypress.com</a>
Memories	<a href="http://memory.cypress.com">memory.cypress.com</a>
Image Sensors	<a href="http://image.cypress.com">image.cypress.com</a>

### PSoC Solutions

General	<a href="http://psoc.cypress.com/solutions">psoc.cypress.com/solutions</a>
Low Power/Low Voltage	<a href="http://psoc.cypress.com/low-power">psoc.cypress.com/low-power</a>
Precision Analog	<a href="http://psoc.cypress.com/precision-analog">psoc.cypress.com/precision-analog</a>
LCD Drive	<a href="http://psoc.cypress.com/lcd-drive">psoc.cypress.com/lcd-drive</a>
CAN 2.0b	<a href="http://psoc.cypress.com/can">psoc.cypress.com/can</a>
USB	<a href="http://psoc.cypress.com/usb">psoc.cypress.com/usb</a>

© Cypress Semiconductor Corporation, 2001-2008. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.