# SERIAL PROGRAMMABLE PCI SS VERSACLOCK SYNTHESIZER MK1716-01

## Description

The MK1716-01 is a versatile serial programmable clock source which takes up very little board space.

The device can simultaneously generate two groups of 4 output clocks and a reference clock output. Both clock groups (CLKA and CLKB) are derived from a single PLL, and have the ability to incorporate Spread Spectrum frequency modulation for reduced system EMI. Each group has control of independent PLL output divide values. Outputs may be programmed on the fly, and will lock to a new frequency in 10 ms or less.

Each of the two groups are powered by a separate VDDIO voltage. The reference clock uses the fixed VDD voltage. VDDIO may vary from 2.5 V to VDD.

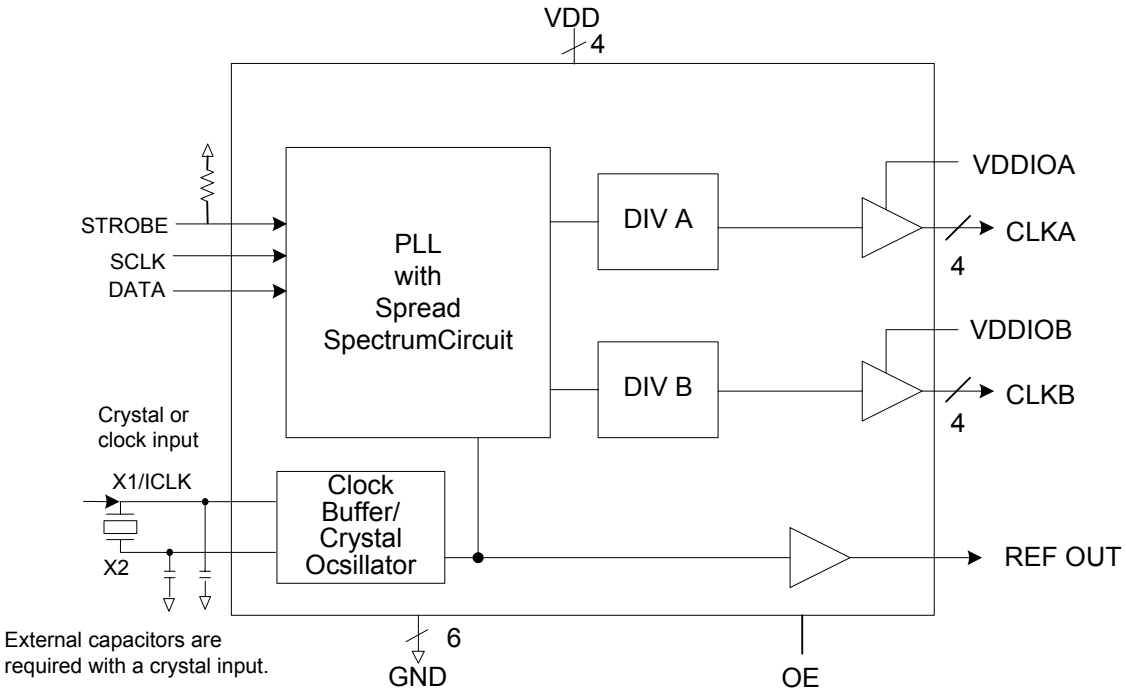
The devices includes a OE pin which tri-states the output clocks and when tied low.

IDT's VersaClock™ software allows the user to generate MK1716-01 device optimizing configuration code for target output frequencies and spread spectrum amounts.

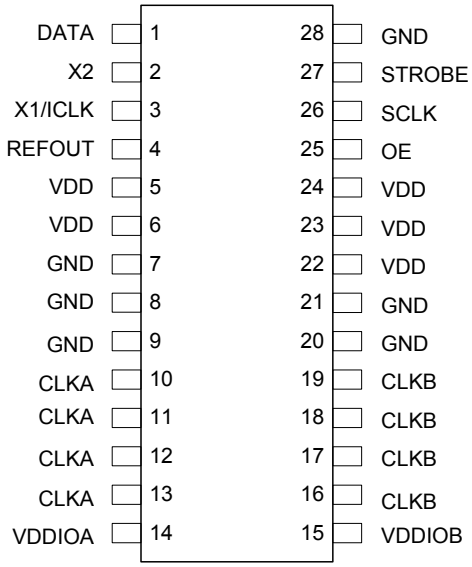
## Features

- Packaged in 28-pin SSOP
- Operating voltage 3.3 V
- Serially programmable: user determines the output frequency via a 3-wire interface
- Highly accurate frequency generation
- M/N Multiplier PLL: M = 1..2048, N = 1..1024
- Eliminates the need for custom Quartz Oscillators
- Input crystal frequency of 5-27 MHz
- Input clock frequency of 3-50 MHz
- Output clock frequencies of 250 kHz to 133.33 MHz
- Spread Spectrum frequency modulation for reduced system EMI
- Center or down spread ±0.5% min to 4% total
- Selectable 32 kHz and 120 kHz modulation rate
- Advanced, low power, sub-micron CMOS process
- Separate VDD 's for each bank of 4 outputs
- Output skew <250 ps within output bank
- OE control on outputs

## Block Diagram



## Pin Assignment




Note:

Clock A and Clock B can be at the same frequency or not, but must be powered by separate VDDs.

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 1 | DATA | Input | Serial shift register data input. |
| 2 | X2 | XO | Connect to crystal. Leave open for clock input. |
| 3 | X1/ICLK | XI | Connect this pin to a crystal or external clock input. |
| 4 | REFOUT | Output | Reference clock output. |
| 5-6 | VDD | P | Connect to +3.3 V. |
| 7-9 | GND | P | Connect to ground. |
| 10-13 | CLKA | Output | Output clock. |
| 14 | VDDIOA | P | Power supply to CLKA. |
| 15 | VDDIOB | P | Power supply to CLKB. |
| 16-19 | CLKB | Output | Output clock. |
| 20-21 | GND | P | Connect to ground. |
| 22-24 | VDD | P | Connect to +3.3 V. |
| 25 | OE | Input | Output enable active high. |
| 26 | SRCLK | Input | Serial shift register clock. |
| 27 | STROBE | Input | Strobe to load data. See timing diagram. Use external 250 kOhm pull-up. |
| 28 | GND | Input | Connect to ground. |

## Configuring the MK1716-01

Initial State: The MK1716-01 may be configured to have up to nine frequency outputs, utilizing a single PLL and on-board spread spectrum circuitry. Unprogrammed, the part has the following outputs, related to the reference input clock:

| Default Outputs | |
|---|---|
| **Output** | **Frequency** |
| Clock 1-9 (Pins 4, 10 - 19) | Reference output |

The STROBE pin must have an external 250 kOhm pull-up resistor to acheive the Initial State.

The input crystal range for the MK1716-01 is 5 MHz to 27 MHz.

The MK1716-01 can be programmed to set the output functions and frequencies. 160 data bits generated by the VersaClock™ software are written in DATA pin in this order: MSB (left most bit) first.

As show in Figure 2, after these 160 bits are clocked into the MK1716-01, taking STROBE high will send this data to the internal latch and the CLK output will lock within 10 ms.

**Note**: STROBE utilizes a transparent latch that is latched when in the high state. If STROBE is in the high state and SCLK is pulsed, DATA is clocked directly to the internal latch and the output conditions will change accordingly. Although this will not damage the MK1716-01, it is recommended that STROBE be kept low while DATA is being clocked into the MK1716-01 in order to avoid unintended changes on the output clocks.

## AC Parameters for Writing to the MK1716-01

| Parameter | Condition | Min. | Max. | Units |
|---|---|---|---|---|
| $t_{SETUP}$ | Setup time | 10 | | ns |
| $t_{HOLD}$ | Hold time after SCLK | 10 | | ns |
| $t_W$ | Data wait time | 10 | | ns |
| $t_S$ | Strobe pulse width | 40 | | ns |
| | SCLK Frequency | | 30 | MHz |

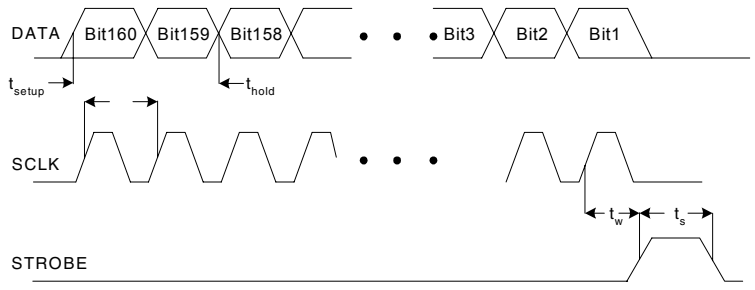



Figure 2. Timing Diagram for Programming the MK1716-01

# External Components

### Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

### STROBE Pull-up Resistor

In order for the device to start up in the default state, a 250 kOhm pull-up resistor is required.

### Decoupling Capacitors

As with any high-performance mixed-signal IC, the MK1716-01 must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01µF must be connected between each VDD and the PCB ground plane.

### Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) been the crystal and device. Crystal capacitors must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal ($C_L$ -6 pF)*2. In this equation, $C_L$= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2] = 20.

## PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) Each 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to each clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers.

## MK1716-01 Configuration Capabilities

The architecture of the MK1716-01 allows the user to easily configure the device to a wide range of output frequencies, for a given input reference frequency.

The frequency multiplier PLL provides a high degree of precision. The M/N values (the multiplier/divide values available to generate the target VCO frequency) can be set within the range of M = 1 to 2048 and N = 1 to 1024.

The MK1716-01 also provides separate output divide values, from 2 through 20, to allow the two output clock banks to support widely differing frequency values from the same PLL.

Each output frequency can be represented as:

Output Freq. = (Ref. Freq)*(M/N)/Output Divide

Each output clock bank has an separate voltage drive control pin (VDDIOA and VDDIOB) that sets the output clock voltage swing.

## IDT VersaClock Software

IDT applies years of PLL optimization experience into a user friendly software that accepts the user's target reference clock and output frequencies and generates the lowest jitter, lowest power configuration, with only a press of a button. The user does not need to have prior PLL experience or determine the optimal VCO frequency to support multiple output frequencies.

VersaClock software quickly evaluates accessible VCO frequencies with available output divide values and provides an easy to understand, bar code rating for the target output

frequencies. The user may evaluate output accuracy, performance trade-off scenarios in seconds.

## Spread Spectrum Modulation

The MK1716-01 utilizes frequency modulation (FM) to distribute energy over a range of frequencies. By modulating the output clock frequencies, the device effectively lowers energy across a broader range of frequencies; thus, lowering a system's electro-magnetic interference (EMI). The modulation rate is the time from transitioning from a minimum frequency to a maximum frequency and then back to the minimum.

Spread Spectrum Modulation can be applied as either "center spread" or "down spread". During center spread modulation, the deviation from the target frequency is equal in the positive and negative directions. The effective average frequency is equal to the target frequency. In applications where the clock is driving a component with a maximum frequency rating, down spread should be applied. In this case, the maximum frequency, including modulation, is the target frequency. The effective average frequency is less than the target frequency.

The MK1716-01 operates in both center spread and down spread modes. For center spread, the frequency can be modulated between ±0.125% to ±2.0%. For down spread, the frequency can be modulated between -0.25% to -4.0%.

Both output frequency banks will utilize identical spread spectrum percentage deviations and modulation rates, if a common VCO frequency can be identified.

### Spread Spectrum Modulation Rate

The spread spectrum modulation frequency applied to the output clock frequency may occur at a variety of rates. For applications requiring the driving of "down-circuit" PLLs, Zero Delay Buffers, or those adhering to PCI standards, the spread spectrum modulation rate should be set to 30-33 kHz. For other applications, a 120 kHz modulation option is available.

# Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1716-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Parameter | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Supply Voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs | Referenced to GND | -0.5 | | VDD + 0.5 | V |
| Clock Outputs | Referenced to GND | -0.5 | | VDD + 0.5 | V |
| Storage Temperature | | -65 | | 150 | °C |
| Soldering Temperature | Max 10 seconds | | | 260 | °C |

## Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Ambient Operating Temperature | 0 | | +70 | °C |
| Power Supply Voltage (measured in respect to GND) | +3.0 | | +3.6 | V |
| Power Supply Ramp Time | | | 4 | ms |

## DC Electrical Characteristics

**VDD=3.3 V ±10%** Ambient temperature 0 to +70° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Operating Voltage | VDD | | 3.00 | | 3.60 | V |
| Operating Supply Current Input High Voltage | IDD | Configuration Dependent See VersaClock™ | | | | mA |
| | | Ex. 14.31818 MHz crystal, VDD=VDDIO=3.3V, | | 55 | | mA |
| | | OE = 0 | | 15 | | mA |
| VDDIO Voltage | | VDDIOA and VDDIOB | 2.25 | | VDD | V |
| Input High Voltage | $V_{IH}$ | ICLK only | (VDD/2)+1 | | | V |
| Input Low Voltage | $V_{IL}$ | ICLK only | | | (VDD/2)-1 | V |
| Input High Voltage | $V_{IH}$ | | VDD-0.5 | | | V |
| Input Low Voltage | $V_{IL}$ | OE, SCLK, DATA, STROBE | | | 0.8 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -8 mA | 2.4 | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8 mA | | | 0.4 | V |
| Output High Voltage, CMOS level | $V_{OH}$ | $I_{OH}$ = -4 mA | VDD-0.4 | | | V |
| Short Circuit Current | | CLK outputs | | ±70 | | mA |
| Nominal Output Impedance | $Z_{OUT}$ | | | 20 | | Ω |
| Input Capacitance | $C_{IN}$ | OE pin | | 4 | | pF |
| Internal Pull-down Resistor | $R_{PD}$ | CLK outputs | | 510 | | kΩ |
| Internal Pull-up Resistor | $R_{PU}$ | OE pin | | 240 | | kΩ |

## AC Electrical Characteristics

**VDD = 3.3 V ±10%**, Ambient Temperature 0 to +70° C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Input Frequency | $F_{IN}$ | Fundamental crystal | 5 | | 27 | MHz |
| | | Input clock | 2 | | 50 | MHz |
| Output Frequency | | VDD=3.3 V | 0.25 | | 133.33 | MHz |
| Output Clock Rise Time | $t_{OR}$ | 20% to 80%, Note 1 | | 0.8 | | ns |
| Output Clock Fall Time | $t_{OF}$ | 80% to 20%, Note 1 | | 0.8 | | ns |
| Output Clock Duty Cycle | | Note 2 | 40 | 49-51 | 60 | % |
| Power-up Time | | STROBE goes high until stable CLK out | | 3 | 10 | ms |
| | | OE goes high until stable CLK out, PLL already running | | | 50 | ns |
| Maximum Output Jitter, short term | $t_j$ | Reference clock, Note 1 | | ±300 | | ps |
| Maximum Output Jitter, short term | $t_j$ | All other clocks, Note 1 configuration dependent | | ±200 | | ps |
| Skew on the same bank | | Same voltage and frequency | | 150 | | ps |
| Skew bank to bank | | Same voltage and frequency | | 150 | | ps |
| Spread Spectrum Modulation Amount | | Center or down spread | 0.5 | | 4.0 | % |

Note 1: Measured with 15 pF load.

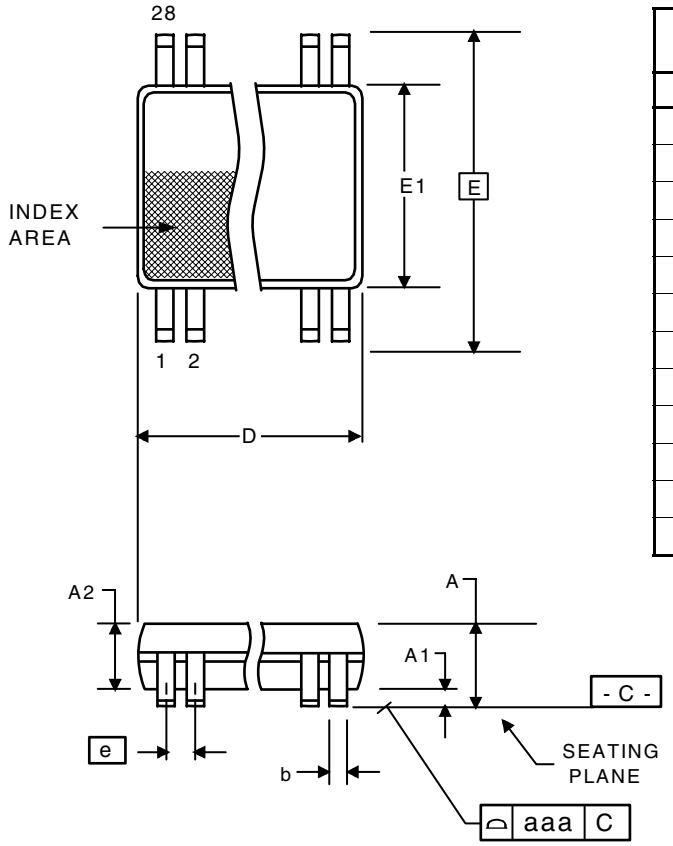
Note 2: Duty Cycle is configuration dependent. Most configurations are min 45% / max 55%

## Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $\theta_{JA}$ | Still air | | 135 | | °C/W |
| | $\theta_{JA}$ | 1 m/s air flow | | 93 | | °C/W |
| | $\theta_{JA}$ | 3 m/s air flow | | 78 | | °C/W |
| Thermal Resistance Junction to Case | $\theta_{JC}$ | | | 60 | | °C/W |

## Package Outline and Package Dimensions (28-pin SSOP, 150 Mil. Wide Body)

Package dimensions are kept current with JEDEC Publication No. 95




| | Millimeters | | Inches | |
|---|---|---|---|---|
| Symbol | Min | Max | Min | Max |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | -- | 1.50 | -- | 0.059 |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| c | 0.18 | 0.25 | 0.007 | 0.010 |
| D | 9.80 | 10.00 | .386 | .394 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | .635 Basic | | .025 Basic | |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| α | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---|---|---|---|---|
| MK1716-01RLF | | Tubes | 28-pin SSOP | 0 to +70° C |
| MK1716-01RLFT | | Tape and Reel | 28-pin SSOP | 0 to +70° C |

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