14-Output Clock Generator

AD9516-5

FEATURES

- Low phase noise, phase-locked loop
  - Supports external VCO/VCXO to 2.4 GHz
  - 1 differential or 2 single-ended reference inputs
  - Accepts CMOS, LVDS, or LVPECL references to 250 MHz
  - Reference monitoring capability
  - Auto and manual reference switchover/holdover modes with selectable revertive/nonrevertive switching
  - Glitch-free (hitless) switchover between references
  - Automatic recovery from holdover
  - Programmable delays in path to PFD
  - Digital or analog lock detect, selectable
- Six 1.6 GHz LVPECL outputs arranged in 3 groups
  - Each group shares 1 to 32 dividers with coarse phase delay
  - Additive output jitter: 225 fs rms
  - Channel-to-channel skew paired outputs: <10 ps
- Four 800 MHz LVDS clock outputs arranged in 2 groups
  - Each group shares 2 cascaded 1-to-32 dividers with coarse phase delay
  - Additive output jitter: 275 fs rms
  - Fine delay adjust (ΔT) on each LVDS output
  - Each LVDS output can be configured as 2 CMOS outputs (for $f_{OUT} \leq 250$ MHz)
- Automatic synchronization of all outputs on power-up
- Manual synchronization of outputs as needed
- SPI-compatible serial control port
- 64-lead LFCSP

APPLICATIONS

- Low jitter, low phase noise clock distribution
- Clock generation and translation for SONET, 10Ge, 10G FC, and other 10 Gbps protocols
- Clocking high speed ADCs, DACs, DDSs, DDCs, DUCs, MxFEs
- High performance wireless transceivers
- High performance instrumentation
- Broadband infrastructure
- ATE and high performance instrumentation

GENERAL DESCRIPTION

The AD9516-5[1] provides a multioutput clock distribution function with subpicosecond jitter performance, along with an on-chip PLL that can be used with an external VCO/VCXO.

FUNCTIONAL BLOCK DIAGRAM

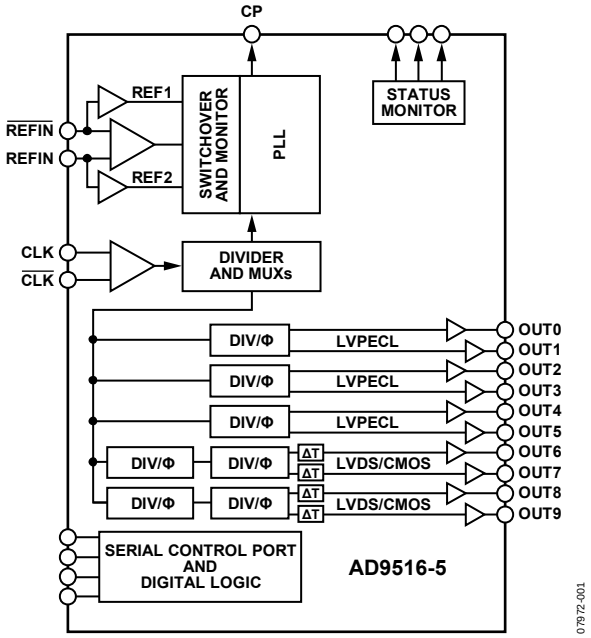

Figure 1.

The AD9516-5 emphasizes low jitter and phase noise to maximize data converter performance and is suitable for other applications with demanding phase noise and jitter requirements.

The AD9516-5 features six LVPECL outputs in three groups, along with four LVDS outputs in two groups. Any LVDS output can be reconfigured as two CMOS outputs. The LVPECL outputs operate to 1.6 GHz, the LVDS outputs operate to 800 MHz, and the CMOS outputs operate to 250 MHz.

Each pair of outputs has dividers that allow both the divide ratio and coarse delay (or phase) to be set. The range of division for the LVPECL outputs is 1 to 32. The LVDS/CMOS outputs allow a range of divisions up to a maximum of 1024.

The AD9516-5 is available in a 64-lead LFCSP and can be operated from a single 3.3 V supply. An external VCO, which requires an extended voltage range, can be accommodated by connecting the charge pump supply (VCP) to 5.5 V. A separate LVPECL power supply can be from 2.375 V to 3.6 V.

The AD9516-5 is specified for operation over the standard industrial range of −40°C to +85°C.

For applications requiring an integrated EEPROM, or needing additional outputs, the AD9520-5 and AD9522-5 are available.

[1] The AD9516 is used throughout to refer to all the members of the AD9516 family. However, when AD9516-5 is used, it refers to that specific member of the AD9516 family.

Rev. 0

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REVISION HISTORY

1/09—Revision 0: Initial Version

SPECIFICATIONS

Typical (typ) is given for VS = VS_LVPECL = 3.3 V ± 5%; VS ≤ VCP ≤ 5.25 V; T_A = 25°C; RSET = 4.12 kΩ; CPRSET = 5.1 kΩ, unless otherwise noted. Minimum (min) and maximum (max) values are given over full V_S and T_A (−40°C to +85°C) variation.

POWER SUPPLY REQUIREMENTS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VS	3.135	3.3	3.465	V	This is 3.3 V ± 5%
VS_LVPECL	2.375		VS	V	This is nominally 2.5 V to 3.3 V ± 5%
VCP	VS		5.25	V	This is nominally 3.3 V to 5.0 V ± 5%
RSET Pin Resistor		4.12		kΩ	Sets internal biasing currents; connect to ground
CPRSET Pin Resistor		5.1		kΩ	Sets internal CP current range, nominally 4.8 mA (CP_Isb = 600 µA); actual current can be calculated by: CP_Isb = 3.06/CPRSET; connect to ground

PLL CHARACTERISTICS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE INPUTS					
Differential Mode (REFIN, $\overline{\text{REFIN}}$)					Differential mode (can accommodate single-ended input by ac grounding undriven input)
Input Frequency	0		250	MHz	Frequencies below about 1 MHz should be dc-coupled; be careful to match V_{CM} (self-bias voltage)
Input Sensitivity		250		mV p-p	PLL figure of merit increases with increasing slew rate; see Figure 13
Self-Bias Voltage, REFIN	1.35	1.60	1.75	V	Self-bias voltage of REFIN[1]
Self-Bias Voltage, $\overline{\text{REFIN}}$	1.30	1.50	1.60	V	Self-bias voltage of $\overline{\text{REFIN}}$[1]
Input Resistance, REFIN	4.0	4.8	5.9	kΩ	Self-biased[1]
Input Resistance, $\overline{\text{REFIN}}$	4.4	5.3	6.4	kΩ	Self-biased[1]
Dual Single-Ended Mode (REF1, REF2)					Two single-ended CMOS-compatible inputs
Input Frequency (AC-Coupled)	20		250	MHz	Slew rate > 50 V/µs
Input Frequency (DC-Coupled)	0		250	MHz	Slew rate > 50 V/µs; CMOS levels
Input Sensitivity (AC-Coupled)		0.8		V p-p	Should not exceed V_S p-p
Input Logic High	2.0			V	
Input Logic Low			0.8	V	
Input Current	−100		+100	µA	
Input Capacitance		2		pF	Each pin, REFIN (REF1)/$\overline{\text{REFIN}}$ (REF2)
PHASE/FREQUENCY DETECTOR (PFD)					
PFD Input Frequency			100	MHz	Antibacklash pulse width = 1.3 ns, 2.9 ns
			45	MHz	Antibacklash pulse width = 6.0 ns
Antibacklash Pulse Width		1.3		ns	0x017[1:0] = 01b
		2.9		ns	0x017[1:0] = 00b; 0x017[1:0] = 11b
		6.0		ns	0x017[1:0] = 10b
CHARGE PUMP (CP)					
I_{CP} Sink/Source					Programmable
High Value		4.8		mA	With CPRSET = 5.1 kΩ
Low Value		0.60		mA	
Absolute Accuracy		2.5		%	V_{CP} = VCP/2
CPRSET Range		2.7/10		kΩ	
I_{CP} High Impedance Mode Leakage		1		nA	
Sink-and-Source Current Matching		2		%	0.5 < V_{CP} < VCP − 0.5 V
I_{CP} vs. V_{CP}		1.5		%	0.5 < V_{CP} < VCP − 0.5 V
I_{CP} vs. Temperature		2		%	V_{CP} = VCP/2 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PRESCALER (PART OF N DIVIDER)					
Prescaler Input Frequency					
P = 1 FD			300	MHz	
P = 2 FD			600	MHz	
P = 3 FD			900	MHz	
P = 2 DM (2/3)			600	MHz	
P = 4 DM (4/5)			1000	MHz	
P = 8 DM (8/9)			2400	MHz	
P = 16 DM (16/17)			3000	MHz	
P = 32 DM (32/33)			3000	MHz	
Prescaler Output Frequency			300	MHz	A, B counter input frequency (prescaler input frequency divided by P)
PLL DIVIDER DELAYS					Register 0x019: R[5:3], N[2:0]; see Table 49
000		Off			
001		330		ps	
010		440		ps	
011		550		ps	
100		660		ps	
101		770		ps	
110		880		ps	
111		990		ps	
NOISE CHARACTERISTICS					
In-Band Phase Noise of the Charge Pump/Phase Frequency Detector (In-Band Means Within the LBW of the PLL)					The PLL in-band phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the value of the N divider)
@ 500 kHz PFD Frequency		−165		dBc/Hz	
@ 1 MHz PFD Frequency		−162		dBc/Hz	
@ 10 MHz PFD Frequency		−151		dBc/Hz	
@ 50 MHz PFD Frequency		−143		dBc/Hz	
PLL Figure of Merit (FOM)		−220		dBc/Hz	Reference slew rate > 0.25 V/ns; FOM +10 log(f_{PFD}) is an approximation of the PFD/CP in-band phase noise (in the flat region) inside the PLL loop bandwidth; when running closed loop, the phase noise, as observed at the VCO output, is increased by 20 log(*N*)
PLL DIGITAL LOCK DETECT WINDOW[2]					Signal available at the LD, STATUS, and REFMON pins when selected by appropriate register settings
Required to Lock (Coincidence of Edges)					Selected by 0x017[1:0] and 0x018[4]
Low Range (ABP 1.3 ns, 2.9 ns)		3.5		ns	0x017[1:0] = 00b, 01b, 11b; 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		7.5		ns	0x017[1:0] = 00b, 01b, 11b; 0x018[4] = 0b
High Range (ABP 6.0 ns)		3.5		ns	0x017[1:0] = 10b; 0x018[4] = 0b
To Unlock After Lock (Hysteresis)[2]					
Low Range (ABP 1.3 ns, 2.9 ns)		7		ns	0x017[1:0] = 00b, 01b, 11b; 0x018[4] = 1b
High Range (ABP 1.3 ns, 2.9 ns)		15		ns	0x017[1:0] = 00b, 01b, 11b; 0x018[4] = 0b
High Range (ABP 6.0 ns)		11		ns	0x017[1:0] = 10b; 0x018[4] = 0b

[1] The REFIN and $\overline{\text{REFIN}}$ self-bias points are offset slightly to avoid chatter on an open input condition.
[2] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the unlock-after-lock time.

CLOCK INPUTS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUTS (CLK, $\overline{CLK}$)					Differential input
Input Frequency	0[1]		2.4	GHz	High frequency distribution (VCO divider enabled)
	0[1]		1.6	GHz	Distribution only (VCO divider bypassed); this is the frequency range supported by the channel divider
Input Sensitivity, Differential		150		mV p-p	Measured at 2.4 GHz; jitter performance is improved with slew rates > 1 V/ns
Input Level, Differential			2	V p-p	Larger voltage swings can turn on the protection diodes and can degrade jitter performance
Input Common-Mode Voltage, V_{CM}	1.3	1.57	1.8	V	Self-biased; enables ac coupling
Input Common-Mode Range, V_{CMR}	1.3		1.8	V	With 200 mV p-p signal applied; dc-coupled
Input Sensitivity, Single-Ended		150		mV p-p	CLK ac-coupled; $\overline{CLK}$ ac-bypassed to RF ground
Input Resistance	3.9	4.7	5.7	kΩ	Self-biased
Input Capacitance		2		pF	

[1] Below about 1 MHz, the input should be dc-coupled. Care should be taken to match V_{CM}.

CLOCK OUTPUTS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL CLOCK OUTPUTS					Termination = 50 Ω to VS_LVPECL − 2 V
OUT0, OUT1, OUT2, OUT3, OUT4, OUT5					Differential (OUT, $\overline{OUT}$)
Output Frequency, Maximum	2400			MHz	Using direct to output; see Figure 20 for amplitude vs. frequency; the maximum output frequency is limited by the maximum frequency at the CLK inputs
Output High Voltage (V_{OH})	VS_LVPECL − 1.12	VS_LVPECL − 0.98	VS_LVPECL − 0.84	V	Measured at dc; see Figure 20 for amplitude vs. frequency
Output Low Voltage (V_{OL})	VS_LVPECL − 2.03	VS_LVPECL − 1.77	VS_LVPECL − 1.49	V	Measured at dc; see Figure 20 for amplitude vs. frequency
Output Differential Voltage (V_{OD})	550	790	980	mV	Measured at dc; see Figure 20 for amplitude vs. frequency
LVDS CLOCK OUTPUTS					Differential termination 100 Ω @ 3.5 mA
OUT6, OUT7, OUT8, OUT9					Differential (OUT, $\overline{OUT}$)
Output Frequency, Maximum	800			MHz	See Figure 21; the LVDS outputs can toggle at higher frequencies, but the output amplitude may not meet the V_{OD} specification
Differential Output Voltage (V_{OD})	247	360	454	mV	$V_{OH} - V_{OL}$ measurement across a differential pair at the default amplitude setting with output driver not toggling; see Figure 21 for variation over frequency
Delta V_{OD}			25	mV	The absolute value of the difference between V_{OD} when the normal output is high vs. when the complementary output is high
Output Offset Voltage (V_{OS})	1.125	1.24	1.375	V	$(V_{OH} + V_{OL})/2$ across a differential pair at the default amplitude setting with output driver not toggling
Delta V_{OS}			25	mV	The absolute value of the difference between V_{OS} when the normal output is high vs. when the complementary output is high
Short-Circuit Current (I_{SA}, I_{SB})		14	24	mA	Output shorted to GND

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS CLOCK OUTPUTS					
OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, OUT9B					Single-ended; termination = 10 pF
Output Frequency			250	MHz	See Figure 22
Output Voltage High (V_{OH})	VS − 0.1			V	1 mA load
Output Voltage Low (V_{OL})			0.1	V	1 mA load

TIMING CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL					Termination = 50 Ω to VS_LVPECL − 2 V; amplitude = 810 mV
Output Rise Time, t_{RP}		70	180	ps	20% to 80%, measured differentially
Output Fall Time, t_{FP}		70	180	ps	80% to 20%, measured differentially
PROPAGATION DELAY, t_{PECL}, CLK-TO-LVPECL OUTPUT					
High Frequency Clock Distribution Configuration	835	995	1180	ps	See Figure 33
Clock Distribution Configuration	773	933	1090	ps	See Figure 32
Variation with Temperature		0.8		ps/°C	
OUTPUT SKEW, LVPECL OUTPUTS[1]					
LVPECL Outputs That Share the Same Divider		5	15	ps	
LVPECL Outputs on Different Dividers		13	40	ps	
All LVPECL Outputs Across Multiple Parts			220	ps	
LVDS					Termination = 100 Ω differential; 3.5 mA
Output Rise Time, t_{RL}		170	350	ps	20% to 80%, measured differentially[2]
Output Fall Time, t_{FL}		160	350	ps	20% to 80%, measured differentially[2]
PROPAGATION DELAY, t_{LVDS}, CLK-TO-LVDS OUTPUT					Delay off on all outputs
OUT6, OUT7, OUT8, OUT9					
For All Divide Values	1.4	1.8	2.1	ns	
Variation with Temperature		1.25		ps/°C	
OUTPUT SKEW, LVDS OUTPUTS[1]					Delay off on all outputs
LVDS Outputs That Share the Same Divider		6	62	ps	
LVDS Outputs on Different Dividers		25	150	ps	
All LVDS Outputs Across Multiple Parts			430	ps	
CMOS					Termination = open
Output Rise Time, t_{RC}		495	1000	ps	20% to 80%; C_{LOAD} = 10 pF
Output Fall Time, t_{FC}		475	985	ps	80% to 20%; C_{LOAD} = 10 pF
PROPAGATION DELAY, t_{CMOS}, CLK-TO-CMOS OUTPUT					Fine delay off
For All Divide Values	1.6	2.1	2.6	ns	
Variation with Temperature		2.6		ps/°C	
OUTPUT SKEW, CMOS OUTPUTS[1]					Fine delay off
CMOS Outputs That Share the Same Divider		4	66	ps	
All CMOS Outputs on Different Dividers		28	180	ps	
All CMOS Outputs Across Multiple Parts			675	ps	
DELAY ADJUST[3]					LVDS and CMOS
Shortest Delay Range[4]					0x0A1 (0x0A4) (0x0A7) (0x0AA) [5:0] 111111b
Zero Scale	50	315	680	ps	0x0A2 (0x0A5) (0x0A8) (0x0AB) [5:0] 000000b
Full Scale	540	880	1180	ps	0x0A2 (0x0A5) (0x0A8) (0x0AB) [5:0] 101111b
Longest Delay Range[4]					0x0A1 (0x0A4) (0x0A7) (0x0AA) [5:0] 000000b
Zero Scale	200	570	950	ps	0x0A2 (0x0A5) (0x0A8) (0x0AB) [5:0] 000000b
Quarter Scale	1.72	2.31	2.89	ns	0x0A2 (0x0A5) (0x0A8) (0x0AB) [5:0] 001100b
Full Scale	5.7	8.0	10.1	ns	0x0A2 (0x0A5) (0x0A8) (0x0AB) [5:0] 101111b

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Delay Variation with Temperature					
Short Delay Range[5]					
Zero Scale		0.23		ps/°C	
Full Scale		−0.02		ps/°C	
Long Delay Range[5]					
Zero Scale		0.3		ps/°C	
Full Scale		0.24		ps/°C	

[1] This is the difference between any two similar delay paths while operating at the same voltage and temperature.
[2] Corresponding CMOS drivers set to OUTxA for noninverting, and OUTxB for inverting, x = 6, 7, 8, or 9.
[3] The maximum delay that can be used is a little less than one-half the period of the clock. A longer delay disables the output.
[4] Incremental delay; does not include propagation delay.
[5] All delays between zero scale and full scale can be estimated by linear interpolation.

Timing Diagrams

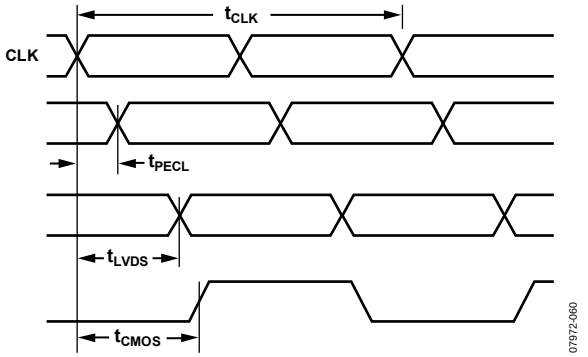

Figure 2. CLK/$\overline{CLK}$ to Clock Output Timing, DIV = 1

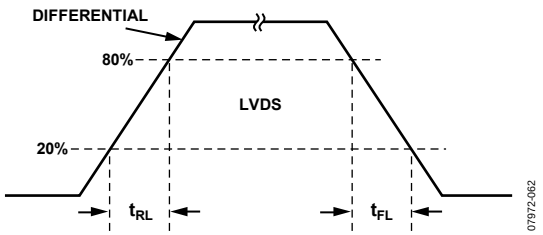

Figure 4. LVDS Timing, Differential

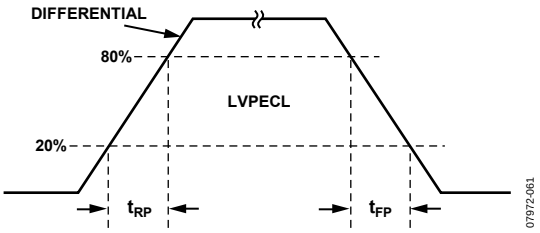

Figure 3. LVPECL Timing, Differential

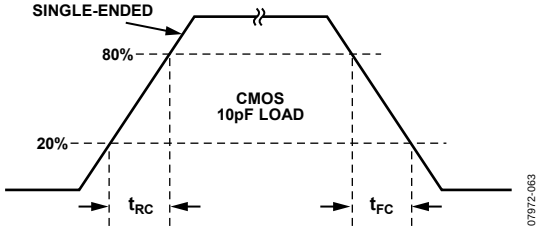

Figure 5. CMOS Timing, Single-Ended, 10 pF Load

CLOCK OUTPUT ADDITIVE PHASE NOISE (DISTRIBUTION ONLY; VCO DIVIDER NOT USED)

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK-TO-LVPECL ADDITIVE PHASE NOISE					Distribution section only; does not include PLL
CLK = 1 GHz, Output = 1 GHz					Input slew rate > 1 V/ns
Divider = 1					
@ 10 Hz Offset		−109		dBc/Hz	
@ 100 Hz Offset		−118		dBc/Hz	
@ 1 kHz Offset		−130		dBc/Hz	
@ 10 kHz Offset		−139		dBc/Hz	
@ 100 kHz Offset		−144		dBc/Hz	
@ 1 MHz Offset		−146		dBc/Hz	
@ 10 MHz Offset		−147		dBc/Hz	
@ 100 MHz Offset		−149		dBc/Hz	
CLK = 1 GHz, Output = 200 MHz					Input slew rate > 1 V/ns
Divider = 5					
@ 10 Hz Offset		−120		dBc/Hz	
@ 100 Hz Offset		−126		dBc/Hz	
@ 1 kHz Offset		−139		dBc/Hz	
@ 10 kHz Offset		−150		dBc/Hz	
@ 100 kHz Offset		−155		dBc/Hz	
@ 1 MHz Offset		−157		dBc/Hz	
>10 MHz Offset		−157		dBc/Hz	
CLK-TO-LVDS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL
CLK = 1.6 GHz, Output = 800 MHz					Input slew rate > 1 V/ns
Divider = 2					
@ 10 Hz Offset		−103		dBc/Hz	
@ 100 Hz Offset		−110		dBc/Hz	
@ 1 kHz Offset		−120		dBc/Hz	
@ 10 kHz Offset		−127		dBc/Hz	
@ 100 kHz Offset		−133		dBc/Hz	
@ 1 MHz Offset		−138		dBc/Hz	
@ 10 MHz Offset		−147		dBc/Hz	
@ 100 MHz Offset		−149		dBc/Hz	
CLK = 1.6 GHz, Output = 400 MHz					Input slew rate > 1 V/ns
Divider = 4					
@ 10 Hz Offset		−114		dBc/Hz	
@ 100 Hz Offset		−122		dBc/Hz	
@ 1 kHz Offset		−132		dBc/Hz	
@ 10 kHz Offset		−140		dBc/Hz	
@ 100 kHz Offset		−146		dBc/Hz	
@ 1 MHz Offset		−150		dBc/Hz	
>10 MHz Offset		−155		dBc/Hz	
CLK-TO-CMOS ADDITIVE PHASE NOISE					Distribution section only; does not include PLL
CLK = 1 GHz, Output = 250 MHz					Input slew rate > 1 V/ns
Divider = 4					
@ 10 Hz Offset		−110		dBc/Hz	
@ 100 Hz Offset		−120		dBc/Hz	
@ 1 kHz Offset		−127		dBc/Hz	
@ 10 kHz Offset		−136		dBc/Hz	
@ 100 kHz Offset		−144		dBc/Hz	
@ 1 MHz Offset		−147		dBc/Hz	
>10 MHz Offset		−154		dBc/Hz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CLK = 1 GHz, Output = 50 MHz					Input slew rate > 1 V/ns
Divider = 20					
@ 10 Hz Offset		−124		dBc/Hz	
@ 100 Hz Offset		−134		dBc/Hz	
@ 1 kHz Offset		−142		dBc/Hz	
@ 10 kHz Offset		−151		dBc/Hz	
@ 100 kHz Offset		−157		dBc/Hz	
@ 1 MHz Offset		−160		dBc/Hz	
>10 MHz Offset		−163		dBc/Hz	

CLOCK OUTPUT ABSOLUTE TIME JITTER (CLOCK GENERATION USING EXTERNAL VCXO)

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ABSOLUTE TIME JITTER					Application example based on a typical setup using an external 245.76 MHz VCXO (Toyocom TCO-2112); reference = 15.36 MHz; R DIV = 1
LVPECL = 245.76 MHz; PLL LBW = 125 Hz		54		fs rms	Integration bandwidth = 200 kHz to 5 MHz
		77		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		109		fs rms	Integration bandwidth = 12 kHz to 20 MHz
LVPECL = 122.88 MHz; PLL LBW = 125 Hz		79		fs rms	Integration bandwidth = 200 kHz to 5 MHz
		114		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		163		fs rms	Integration bandwidth = 12 kHz to 20 MHz
LVPECL = 61.44 MHz; PLL LBW = 125 Hz		124		fs rms	Integration bandwidth = 200 kHz to 5 MHz
		176		fs rms	Integration bandwidth = 200 kHz to 10 MHz
		259		fs rms	Integration bandwidth = 12 kHz to 20 MHz

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER NOT USED)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL; rising edge of clock signal
CLK = 622.08 MHz; LVPECL = 622.08 MHz; Divider = 1		40		fs rms	Bandwidth = 12 kHz to 20 MHz
CLK = 622.08 MHz; LVPECL = 155.52 MHz; Divider = 4		80		fs rms	Bandwidth = 12 kHz to 20 MHz
CLK = 1.6 GHz; LVPECL = 100 MHz; Divider = 16		215		fs rms	Calculated from SNR of ADC method; DCC not used for even divides
CLK = 500 MHz; LVPECL = 100 MHz; Divider = 5		245		fs rms	Calculated from SNR of ADIC method; DCC on
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL; rising edge of clock signal
CLK = 1.6 GHz; LVDS = 800 MHz; Divider = 2; VCO Divider Not Used		85		fs rms	Bandwidth = 12 kHz to 20 MHz
CLK = 1 GHz; LVDS = 200 MHz; Divider = 5		113		fs rms	Bandwidth = 12 kHz to 20 MHz
CLK = 1.6 GHz; LVDS = 100 MHz; Divider = 16		280		fs rms	Calculated from SNR of ADC method; DCC not used for even divides
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL; rising edge of clock signal
CLK = 1.6 GHz; CMOS = 100 MHz; Divider = 16		365		fs rms	Calculated from SNR of ADC method; DCC not used for even divides

CLOCK OUTPUT ADDITIVE TIME JITTER (VCO DIVIDER USED)

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LVPECL OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; LVPECL = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		210		fs rms	Calculated from SNR of ADC method
LVDS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; LVDS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		285		fs rms	Calculated from SNR of ADC method
CMOS OUTPUT ADDITIVE TIME JITTER					Distribution section only; does not include PLL; uses rising edge of clock signal
CLK = 2.4 GHz; VCO DIV = 2; CMOS = 100 MHz; Divider = 12; Duty-Cycle Correction = Off		350		fs rms	Calculated from SNR of ADC method

DELAY BLOCK ADDITIVE TIME JITTER

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DELAY BLOCK ADDITIVE TIME JITTER[1]					Incremental additive jitter
100 MHz Output					
Delay (1600 µA, 1C) Fine Adjust 000000		0.54		ps rms	
Delay (1600 µA, 1C) Fine Adjust 101111		0.60		ps rms	
Delay (800 µA, 1C) Fine Adjust 000000		0.65		ps rms	
Delay (800 µA, 1C) Fine Adjust 101111		0.85		ps rms	
Delay (800 µA, 4C) Fine Adjust 000000		0.79		ps rms	
Delay (800 µA, 4C) Fine Adjust 101111		1.2		ps rms	
Delay (400 µA, 4C) Fine Adjust 000000		1.2		ps rms	
Delay (400 µA, 4C) Fine Adjust 101111		2.0		ps rms	
Delay (200 µA, 1C) Fine Adjust 000000		1.3		ps rms	
Delay (200 µA, 1C) Fine Adjust 101111		2.5		ps rms	
Delay (200 µA, 4C) Fine Adjust 000000		1.9		ps rms	
Delay (200 µA, 4C) Fine Adjust 101111		3.8		ps rms	

[1] This value is incremental; that is, it is in addition to the jitter of the LVDS or CMOS output without the delay. To estimate the total jitter, the LVDS or CMOS output jitter should be added to this value using the root sum of the squares (RSS) method.

SERIAL CONTROL PORT

Table 11.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{CS}$ (INPUT)					$\overline{CS}$ has an internal 30 kΩ pull-up resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current			3	µA	
Input Logic 0 Current		110		µA	
Input Capacitance		2		pF	
SCLK (INPUT)					SCLK has an internal 30 kΩ pull-down resistor
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		110		µA	
Input Logic 0 Current			1	µA	
Input Capacitance		2		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SDIO (WHEN INPUT)					
Input Logic 1 Voltage	2.0			V	
Input Logic 0 Voltage			0.8	V	
Input Logic 1 Current		10		nA	
Input Logic 0 Current		20		nA	
Input Capacitance		2		pF	
SDIO, SDO (OUTPUTS)					
Output Logic 1 Voltage	2.7			V	
Output Logic 0 Voltage			0.4	V	
TIMING					
Clock Rate (SCLK, $1/t_{CLK}$)			25	MHz	
Pulse Width High, t_{HIGH}	16			ns	
Pulse Width Low, t_{LOW}	16			ns	
SDIO to SCLK Setup, t_{DS}	2			ns	
SCLK to SDIO Hold, t_{DH}	1.1			ns	
SCLK to Valid SDIO and SDO, t_{DV}			8	ns	
$\overline{CS}$ to SCLK Setup and Hold, t_S, t_H	2			ns	
$\overline{CS}$ Minimum Pulse Width High, t_{PWH}	3			ns	

$\overline{PD}$, $\overline{SYNC}$, AND $\overline{RESET}$ PINS

Table 12.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT CHARACTERISTICS					Each of these pins has an internal 30 kΩ pull-up resistor
Logic 1 Voltage	2.0			V	
Logic 0 Voltage			0.8	V	
Logic 1 Current		110		µA	
Logic 0 Current			1	µA	
Capacitance		2		pF	
RESET TIMING					
Pulse Width Low	50			ns	
$\overline{SYNC}$ TIMING					
Pulse Width Low	1.5			High speed clock cycles	High speed clock is CLK input signal

LD, STATUS, REFMON PINS

Table 13.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS					When selected as a digital output (CMOS); there are other modes in which these pins are not CMOS digital outputs; see Table 49, 0x017, 0x01A, and 0x01B
Output Voltage High, V_{OH}	2.7			V	
Output Voltage Low, V_{OL}			0.4	V	
MAXIMUM TOGGLE RATE		100		MHz	Applies when mux is set to any divider or counter output, or PFD up/down pulse; also applies in analog lock detect mode; usually debug mode only; beware that spurs may couple to output when any of these pins are toggling
ANALOG LOCK DETECT					
Capacitance		3		pF	On-chip capacitance; used to calculate RC time constant for analog lock detect readback; use a pull-up resistor

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
REF1, REF2, AND CLK FREQUENCY STATUS MONITOR					
Normal Range	1.02			MHz	Frequency above which the monitor indicates the presence of the reference
Extended Range	8			kHz	Frequency above which the monitor indicates the presence of the reference
LD PIN COMPARATOR					
Trip Point		1.6		V	
Hysteresis		260		mV	

POWER DISSIPATION

Table 14.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER DISSIPATION, CHIP					The values in this table include all power supplies, unless otherwise noted; the power deltas for individual drivers are at dc; see Figure 7, Figure 8, and Figure 9 for power dissipation vs. output frequency
Power-On Default		1.0	1.2	W	No clock; no programming; default register values; does not include power dissipated in external resistors; this configuration has the following blocks already powered up: VCO divider, six channel dividers, three LVPECL drivers, and two LVDS drivers
Full Operation; CMOS Outputs at 225 MHz		1.5	2.1	W	f_{CLK} = 2.25 GHz; VCO divider = 2; all channel dividers on; six LVPECL outputs @ 562.5 MHz; eight CMOS outputs (10 pF load) @ 225 MHz; all 4 fine delay blocks on, maximum current; does not include power dissipated in external resistors
Full Operation; LVDS Outputs at 225 MHz		1.5	2.1	W	f_{CLK} = 2.25 GHz; VCO divider = 2; all channel dividers on; six LVPECL outputs @ 562.5 MHz; four LVDS outputs @ 225 MHz; all 4 fine delay blocks on: maximum current; does not include power dissipated in external resistors
$\overline{PD}$ Power-Down		75	185	mW	$\overline{PD}$ pin pulled low; does not include power dissipated in terminations
$\overline{PD}$ Power-Down, Maximum Sleep		31		mW	$\overline{PD}$ pin pulled low; PLL power-down 0x010[1:0] = 01b; SYNC power-down 0x230[2] = 1b; REF for distribution power-down 0x230[1] = 1b
VCP Supply		4	4.8	mW	PLL operating; typical closed-loop configuration (this number is included in all other power measurements)
AD9516 Core		220		mW	AD9516 core only, all drivers off, PLL off, VCO divider off, and delay blocks off; the power consumption of the configuration of the user can be derived from this number and the power deltas that follow
POWER DELTAS, INDIVIDUAL FUNCTIONS					Power delta when a function is enabled/disabled
VCO Divider		30		mW	VCO divider on/off
REFIN (Differential)		20		mW	All references off to differential reference enabled
REF1, REF2 (Single-Ended)		4		mW	All references off to REF1 or REF2 enabled; differential reference not enabled
PLL		75		mW	PLL off to PLL on, normal operation; no reference enabled
Channel Divider		30		mW	Divider bypassed to divide-by-2 to divide-by-32
LVPECL Channel (Divider Plus Output Driver)		120		mW	No LVPECL output on to one LVPECL output on (that is, enabling OUT0 with OUT1 off; Divider 0 enabled)
LVPECL Driver		90		mW	Second LVPECL output turned on, same channel (that is, enabling OUT0 with OUT1 already on)
LVDS Channel (Divider Plus Output Driver)		140		mW	No LVDS output on to one LVDS output on (that is, enabling OUT8 with OUT9 off with Divider 4.1 enabled and Divider 4.2 bypassed)
LVDS Driver		50		mW	Second LVDS output turned on, same channel (that is, enabling OUT8 with OUT9 already on)

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CMOS Channel (Divider Plus Output Driver)		100		mW	Static; no CMOS output on to one CMOS output on (that is, enabling OUT8A starting with OUT8 and OUT9 off)
CMOS Driver (Second in Pair)		0		mW	Static; second CMOS output, same pair, turned on (that is, enabling OUT8A with OUT8B already on)
CMOS Driver (First in Second Pair)		30		mW	Static; first output, second pair, turned on (that is, enabling OUT9A with OUT9B off and OUT8A and OUT8B already on)
Fine Delay Block		50		mW	Delay block off to delay block enabled; maximum current setting

ABSOLUTE MAXIMUM RATINGS

Table 15.

Parameter or Pin	With Respect To	Rating
VS, VS_LVPECL	GND	−0.3 V to +3.6 V
VCP	GND	−0.3 V to +5.8 V
REFIN, $\overline{\text{REFIN}}$	GND	−0.3 V to VS + 0.3 V
REFIN	$\overline{\text{REFIN}}$	−3.3 V to +3.3 V
RSET	GND	−0.3 V to VS + 0.3 V
CPRSET	GND	−0.3 V to VS + 0.3 V
CLK, $\overline{\text{CLK}}$	GND	−0.3 V to VS + 0.3 V
CLK	$\overline{\text{CLK}}$	−1.2 V to +1.2 V
SCLK, SDIO, SDO, $\overline{\text{CS}}$	GND	−0.3 V to VS + 0.3 V
OUT0, $\overline{\text{OUT0}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, OUT5, $\overline{\text{OUT5}}$, OUT6, $\overline{\text{OUT6}}$, OUT7, $\overline{\text{OUT7}}$, OUT8, $\overline{\text{OUT8}}$, OUT9, $\overline{\text{OUT9}}$	GND	−0.3 V to VS + 0.3 V
$\overline{\text{SYNC}}$	GND	−0.3 V to VS + 0.3 V
REFMON, STATUS, LD	GND	−0.3 V to VS + 0.3 V
Junction Temperature[1]		150°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (10 sec)		300°C

[1] See Table 16 for θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal impedance measurements were taken on a 4-layer board in still air in accordance with EIA/JESD51-7.

Table 16.

Package Type	θ_{JA}	Unit
64-Lead LFCSP (CP-64-4)	22	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

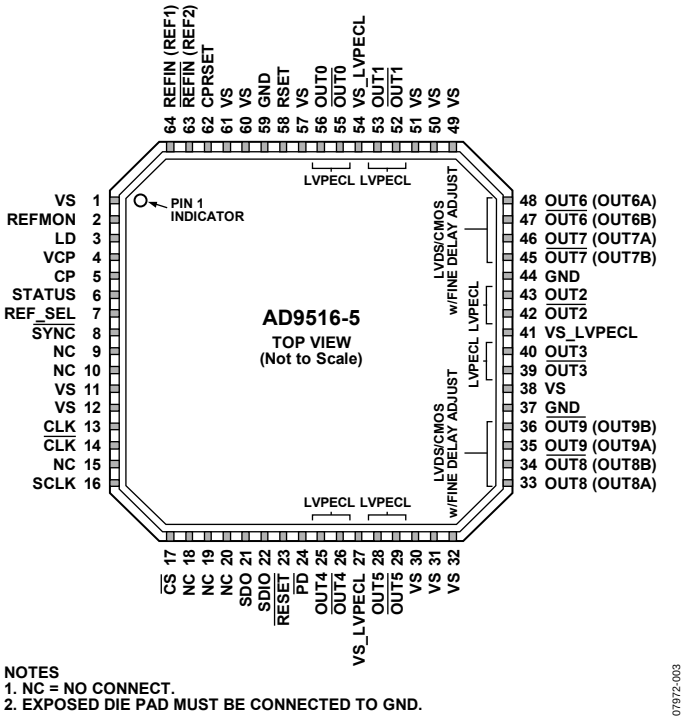

Figure 6. Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
1, 11, 12, 30, 31, 32, 38, 49, 50, 51, 57, 60, 61	I	Power	VS	3.3 V Power Pins.
2	O	3.3 V CMOS	REFMON	Reference Monitor (Output). This pin has multiple selectable outputs; see Table 49 0x01B.
3	O	3.3 V CMOS	LD	Lock Detect (Output). This pin has multiple selectable outputs; see Table 49 0x01A.
4	I	Power	VCP	Power Supply for Charge Pump (CP); VS < VCP < 5.25 V.
5	O	Loop filter	CP	Charge Pump (Output). This pin connects to an external loop filter. This pin can be left unconnected if the PLL is not used.
6	O	3.3 V CMOS	STATUS	Status (Output). This pin has multiple selectable outputs; see Table 49, 0x017.
7	I	3.3 V CMOS	REF_SEL	Reference Select. Selects REF1 (low) or REF2 (high). This pin has an internal 30 kΩ pull-down resistor.
8	I	3.3 V CMOS	$\overline{\text{SYNC}}$	Manual Synchronizations and Manual Holdover. This pin initiates a manual synchronization and is also used for manual holdover. Active low. This pin has an internal 30 kΩ pull-up resistor.
9, 10, 15, 18, 19, 20			NC	No Connection. These pins can be left floating.
13	I	Differential clock input	CLK	Along with $\overline{\text{CLK}}$, this is the differential input for the clock distribution section.
14	I	Differential clock input	$\overline{\text{CLK}}$	Along with CLK, this is the differential input for the clock distribution section. If a single-ended input is connected to the CLK pin, connect a 0.1 µF bypass capacitor from $\overline{\text{CLK}}$ to ground.

Pin No.	Input/ Output	Pin Type	Mnemonic	Description
16	I	3.3 V CMOS	SCLK	Serial Control Port Data Clock Signal.
17	I	3.3 V CMOS	$\overline{CS}$	Serial Control Port Chip Select; Active Low. This pin has an internal 30 kΩ pull-up resistor.
21	O	3.3 V CMOS	SDO	Serial Control Port Unidirectional Serial Data Output.
22	I/O	3.3 V CMOS	SDIO	Serial Control Port Bidirectional Serial Data Input/Output.
23	I	3.3 V CMOS	$\overline{RESET}$	Chip Reset; Active Low. This pin has an internal 30 kΩ pull-up resistor.
24	I	3.3 V CMOS	$\overline{PD}$	Chip Power-Down; Active Low. This pin has an internal 30 kΩ pull-up resistor.
25	O	LVPECL	OUT4	LVPECL Output; One Side of a Differential LVPECL Output.
26	O	LVPECL	$\overline{OUT4}$	LVPECL Output; One Side of a Differential LVPECL Output.
27, 41, 54	I	Power	VS_LVPECL	Extended Voltage 2.5 V to 3.3 V LVPECL Power Pins.
28	O	LVPECL	OUT5	LVPECL Output; One Side of a Differential LVPECL Output.
29	O	LVPECL	$\overline{OUT5}$	LVPECL Output; One Side of a Differential LVPECL Output.
33	O	LVDS or CMOS	OUT8 (OUT8A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
34	O	LVDS or CMOS	$\overline{OUT8}$ (OUT8B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
35	O	LVDS or CMOS	OUT9 (OUT9A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
36	O	LVDS or CMOS	$\overline{OUT9}$ (OUT9B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
37, 44, 59	I	GND	GND	Ground Pins.
39	O	LVPECL	$\overline{OUT3}$	LVPECL Output; One Side of a Differential LVPECL Output.
40	O	LVPECL	OUT3	LVPECL Output; One Side of a Differential LVPECL Output.
42	O	LVPECL	$\overline{OUT2}$	LVPECL Output; One Side of a Differential LVPECL Output.
43	O	LVPECL	OUT2	LVPECL Output; One Side of a Differential LVPECL Output.
45	O	LVDS or CMOS	$\overline{OUT7}$ (OUT7B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
46	O	LVDS or CMOS	OUT7 (OUT7A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
47	O	LVDS or CMOS	$\overline{OUT6}$ (OUT6B)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
48	O	LVDS or CMOS	OUT6 (OUT6A)	LVDS/CMOS Output; One Side of a Differential LVDS Output, or a Single-Ended CMOS Output.
52	O	LVPECL	$\overline{OUT1}$	LVPECL Output; One Side of a Differential LVPECL Output.
53	O	LVPECL	OUT1	LVPECL Output; One Side of a Differential LVPECL Output.
55	O	LVPECL	$\overline{OUT0}$	LVPECL Output; One Side of a Differential LVPECL Output.
56	O	LVPECL	OUT0	LVPECL Output; One Side of a Differential LVPECL Output.
58	O	Current set resistor	RSET	Resistor Connected Here Sets Internal Bias Currents. Nominal Value = 4.12 kΩ.
62	O	Current set resistor	CPRSET	Resistor Connected Here Sets the CP Current Range. Nominal Value = 5.1 kΩ. This resistor can be omitted if the PLL is not used.
63	I	Reference input	$\overline{REFIN}$ (REF2)	Along with REFIN, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF2. This pin can be left unconnected when the PLL is not used.
64	I	Reference input	REFIN (REF1)	Along with $\overline{REFIN}$, this is the differential input for the PLL reference. Alternatively, this pin is a single-ended input for REF1. This pin can be left unconnected when the PLL is not used.
EPAD		GND	GND	The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

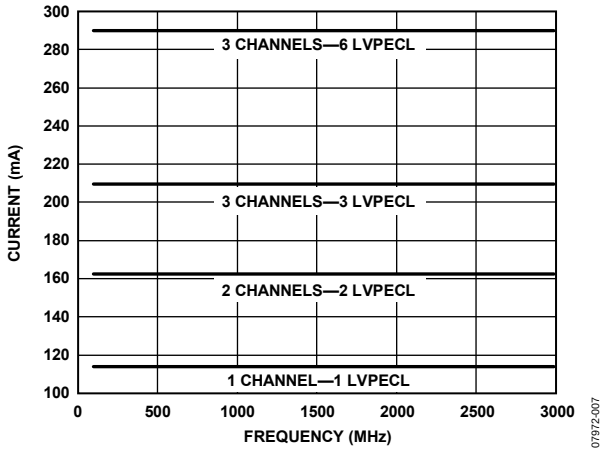

Figure 7. Current vs. Frequency, Direct to Output, LVPECL Outputs

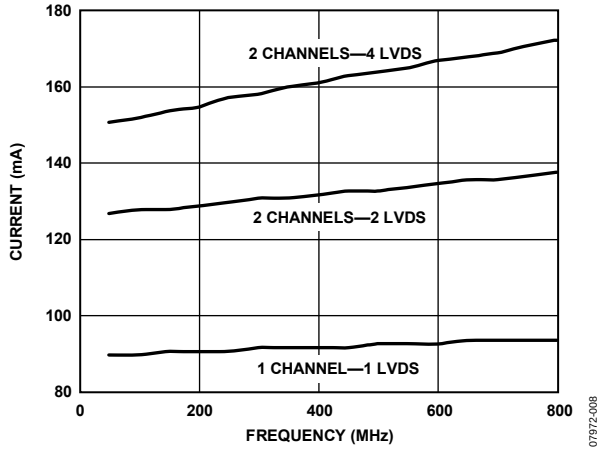

Figure 8. Current vs. Frequency—LVDS Outputs

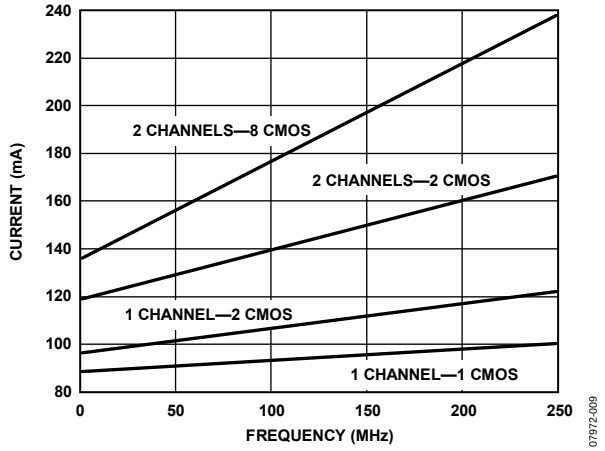

Figure 9. Current vs. Frequency—CMOS Outputs with 10 pF load

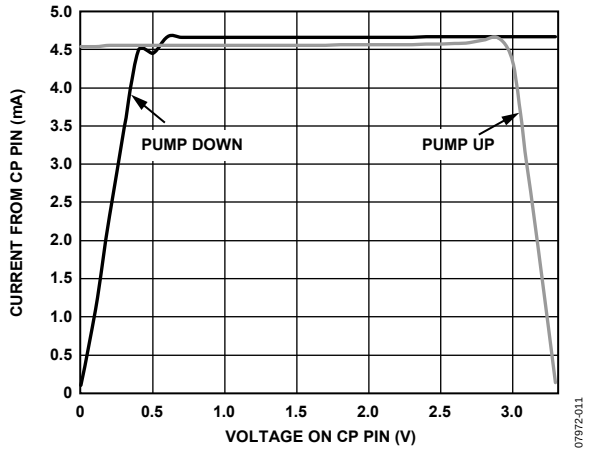

Figure 10. Charge Pump Characteristics @ VCP = 3.3 V

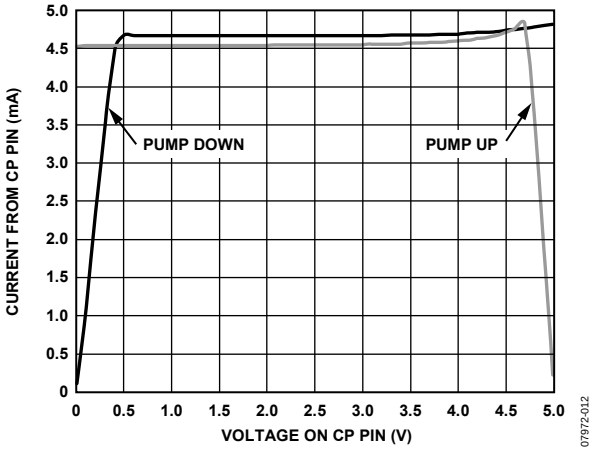

Figure 11. Charge Pump Characteristics @ VCP = 5.0 V

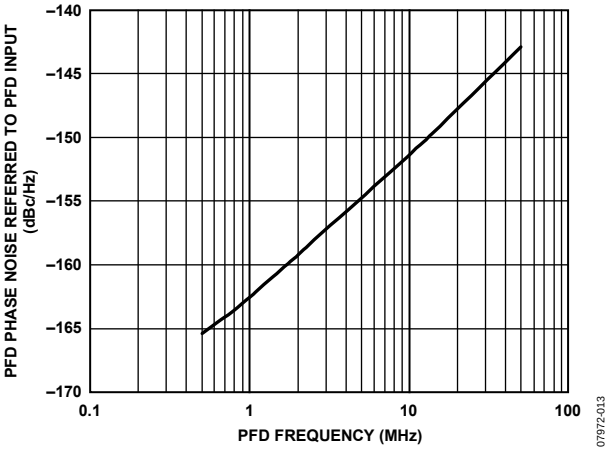

Figure 12. PFD Phase Noise Referred to PFD Input vs. PFD Frequency

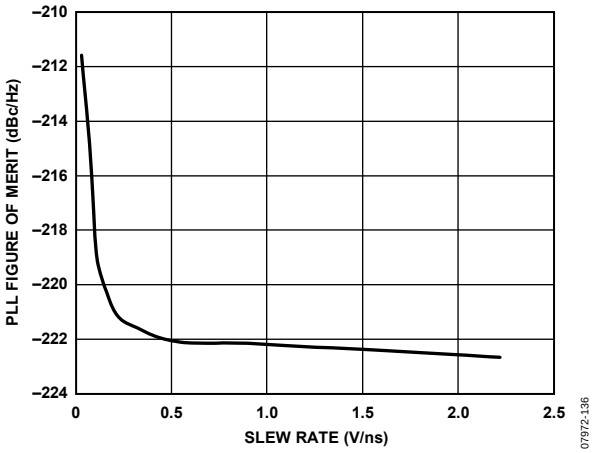

Figure 13. PLL Figure of Merit vs. Slew Rate at REFIN/$\overline{\text{REFIN}}$

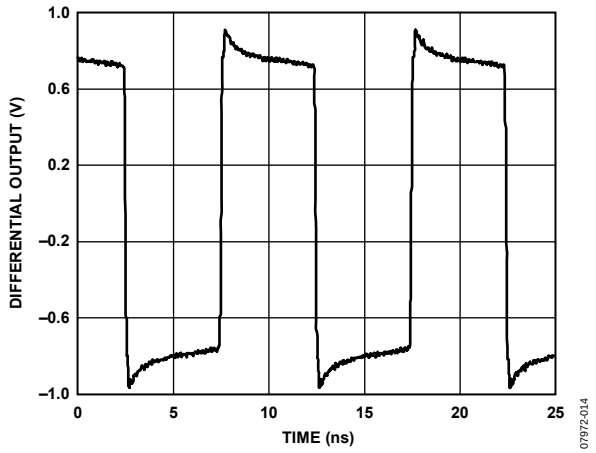

Figure 14. LVPECL Output (Differential) @ 100 MHz

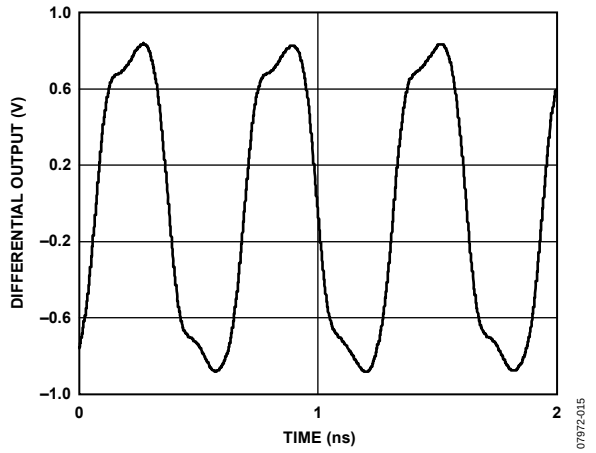

Figure 15. LVPECL Output (Differential) @ 1600 MHz

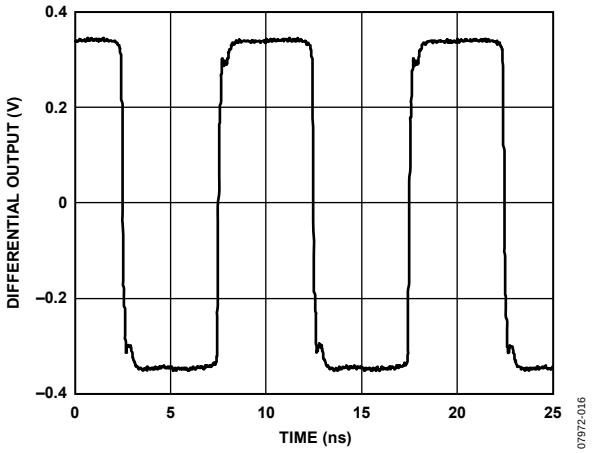

Figure 16. LVDS Output (Differential) @ 100 MHz

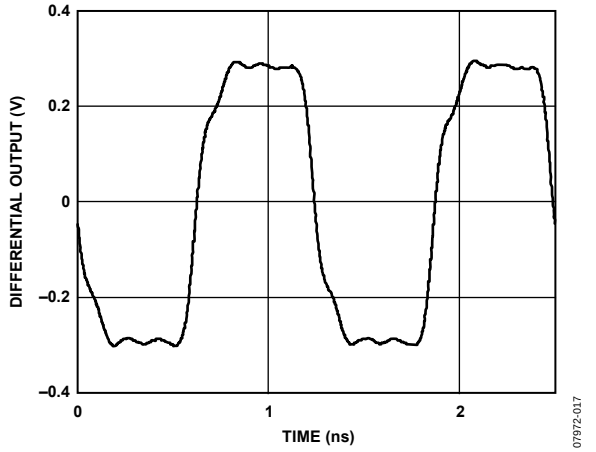

Figure 17. LVDS Output (Differential) @ 800 MHz

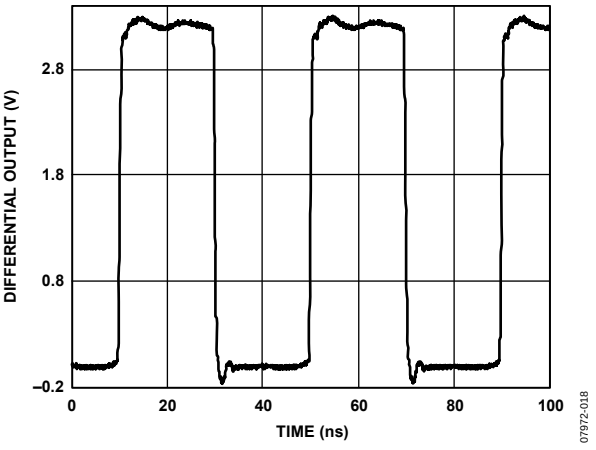

Figure 18. CMOS Output @ 25 MHz

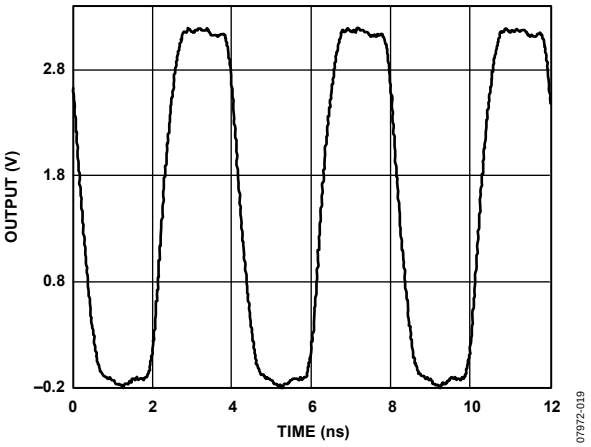

Figure 19. CMOS Output @ 250 MHz

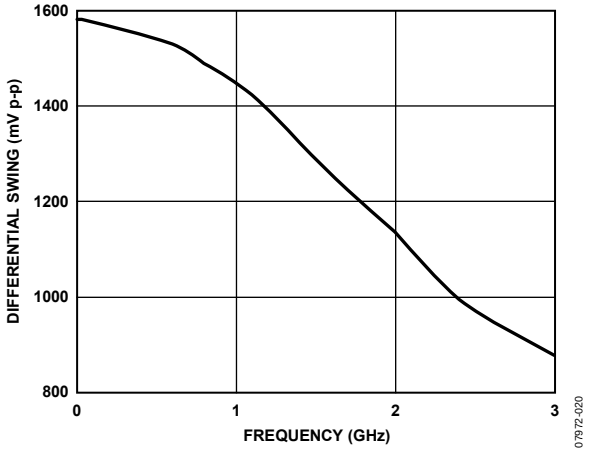

Figure 20. LVPECL Differential Swing vs. Frequency

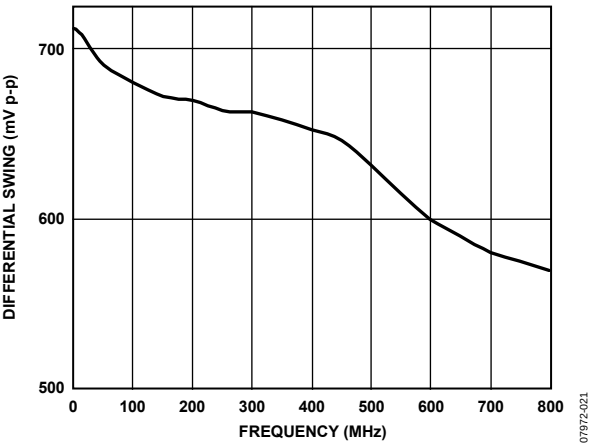

Figure 21. LVDS Differential Swing vs. Frequency

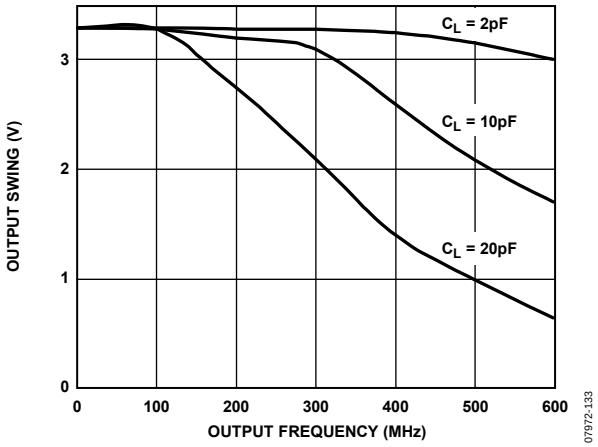

Figure 22. CMOS Output Swing vs. Frequency and Capacitive Load

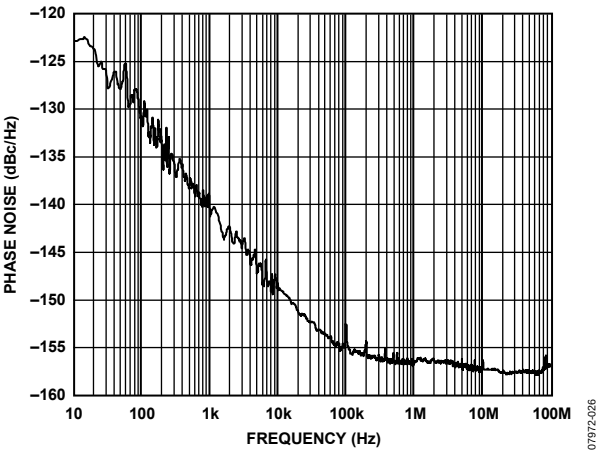

Figure 23. Phase Noise (Additive) LVPECL @ 245.76 MHz, Divide-by-1

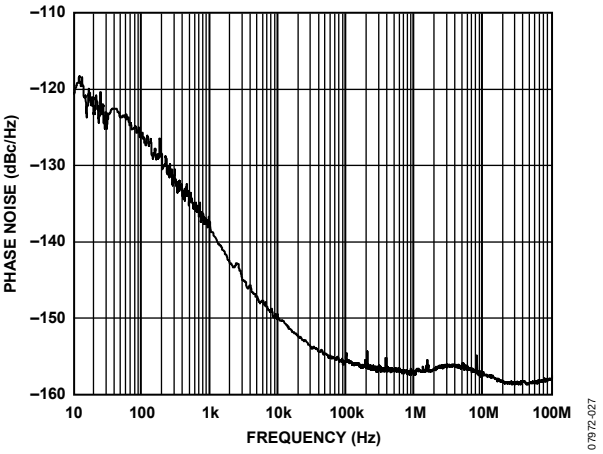

Figure 24. Phase Noise (Additive) LVPECL @ 200 MHz, Divide-by-5

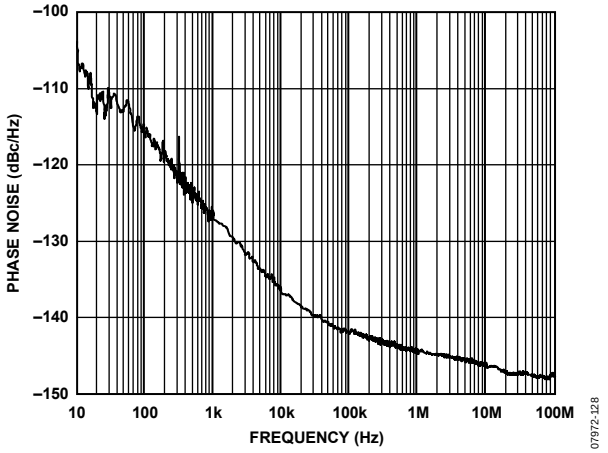

Figure 25. Phase Noise (Additive) LVPECL @ 1600 MHz, Divide-by-1

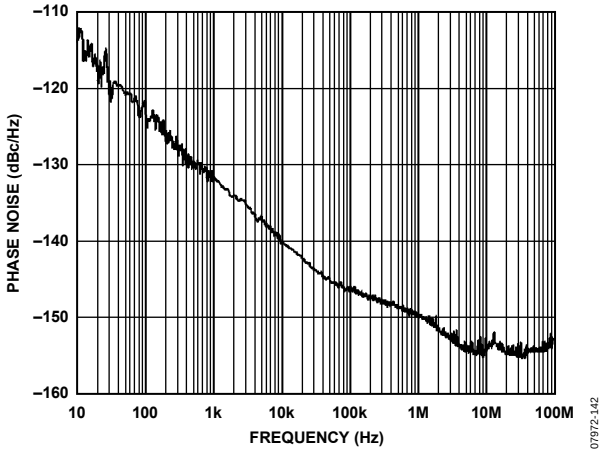

Figure 26. Phase Noise (Additive) LVDS @ 200 MHz, Divide-by-1

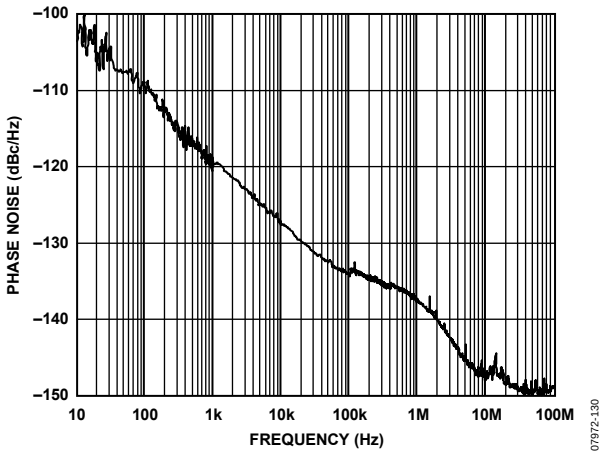

Figure 27. Phase Noise (Additive) LVDS @ 800 MHz, Divide-by-2

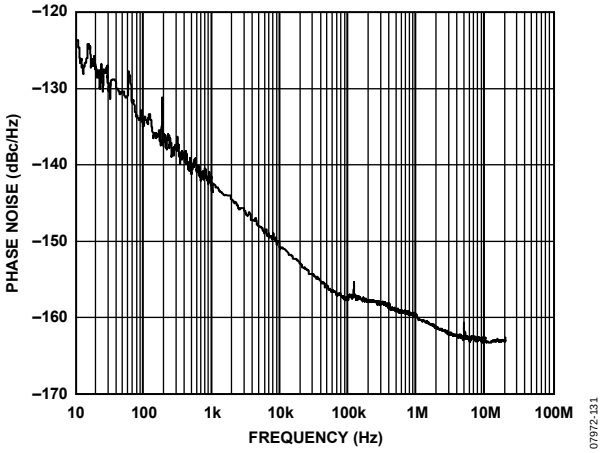

Figure 28. Phase Noise (Additive) CMOS @ 50 MHz, Divide-by-20

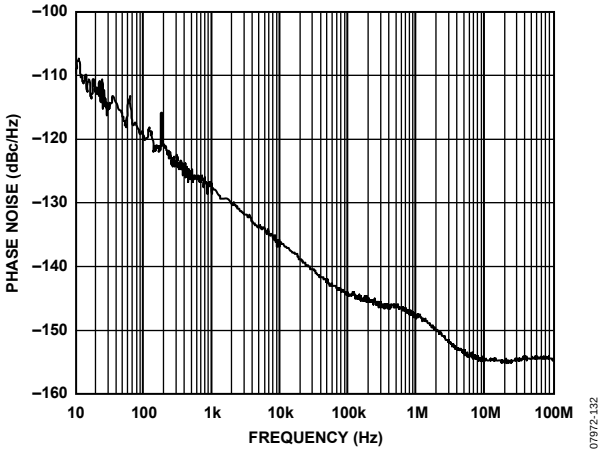

Figure 29. Phase Noise (Additive) CMOS @ 250 MHz, Divide-by-4

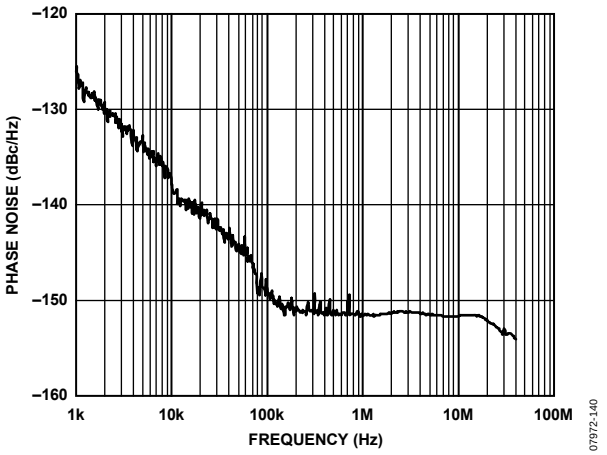

Figure 30. Phase Noise (Absolute), External VCXO (Toyocom TCO-2112) @ 245.76 MHz; PFD = 15.36 MHz; LBW = 250 Hz; LVPECL Output = 245.76 MHz

TERMINOLOGY

Phase Jitter and Phase Noise

An ideal sine wave has a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, have a variation from the ideal phase progression over time. This variation is called phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as Gaussian (normal) in distribution.

This phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

DETAILED BLOCK DIAGRAM

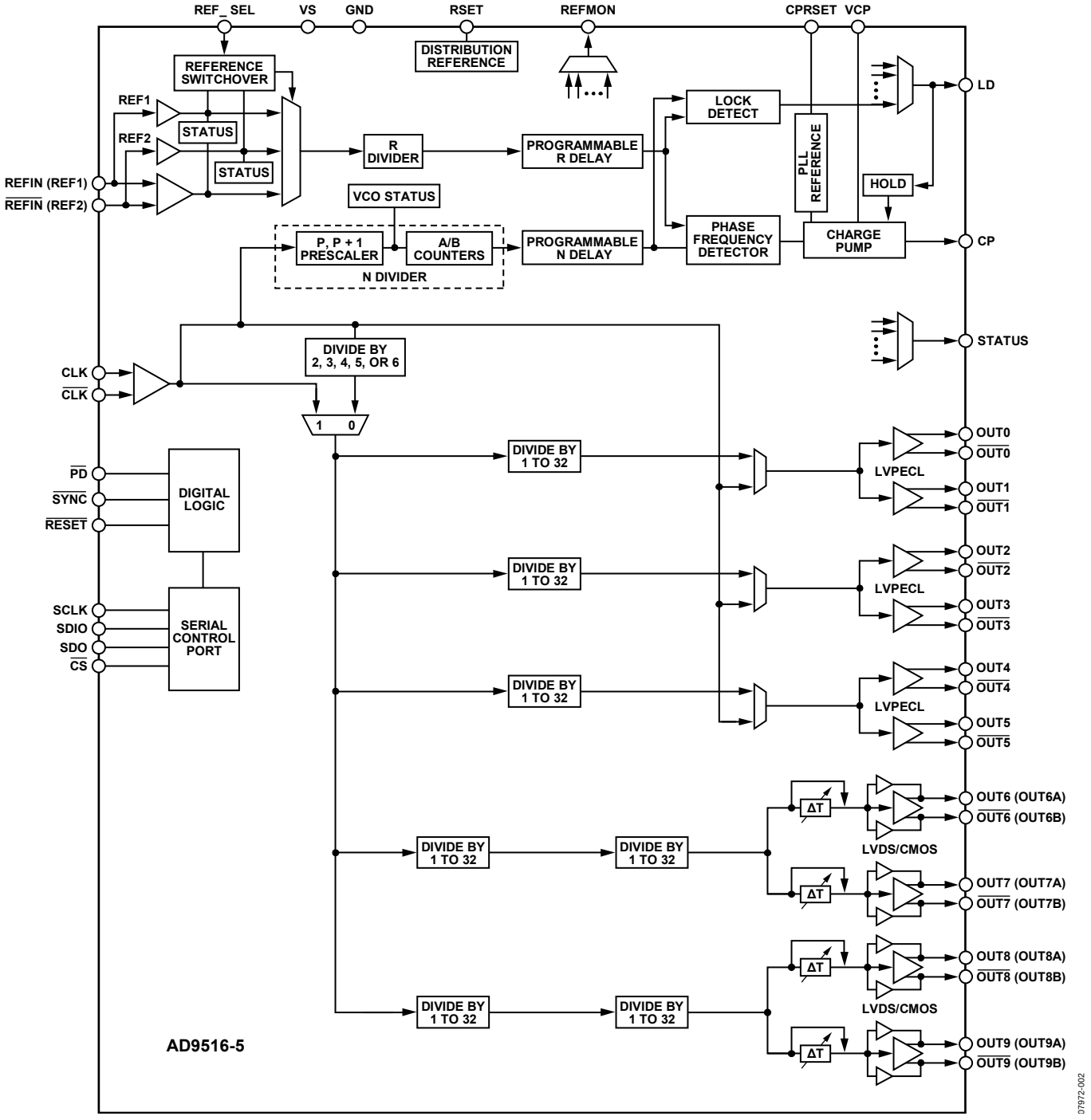

Figure 31. Detailed Block Diagram

THEORY OF OPERATION

OPERATIONAL CONFIGURATIONS

The AD9516 can be configured in several ways. These configurations must be set up by loading the control registers (see Table 47 and Table 48 through Table 57). Each section or function must be individually programmed by setting the appropriate bits in the corresponding control register or registers.

Mode1: Clock Distribution or External VCO < 1600 MHz

Mode 1 bypasses the VCO divider. It can only be used when the external clock source is less than 1600 MHz due to the maximum input frequency allowed at the channel dividers.

For clock distribution applications where the external clock is <1600 MHz, the register settings shown in Table 18 should be used.

Table 18. Settings for Clock Distribution < 1600 MHz

Register	Description
0x010[1:0] = 01b	PLL asynchronous power-down (PLL off)
0x1E1[0] = 1b	Bypass the VCO divider as source for distribution section

When using the internal PLL with an external VCO <1600 MHz, the PLL must be turned on.

Table 19. Settings for Using Internal PLL with External VCO < 1600 MHz

Register	Description
0x1E1[0] = 1b	Bypass the VCO divider as source for distribution section
0x010[1:0] = 00b	PLL normal operation (PLL on) along with other appropriate PLL settings in 0x010 to 0x01E

An external VCO/VCXO requires an external loop filter that must be connected between CP and the tuning pin of the VCO/VCXO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO/VCXO being used.

Table 20. Setting the PFD Polarity

Register	Description
0x010[7] = 0	PFD polarity positive (higher control voltage produces higher frequency)
0x010[7] = 1	PFD polarity negative (higher control voltage produces lower frequency)

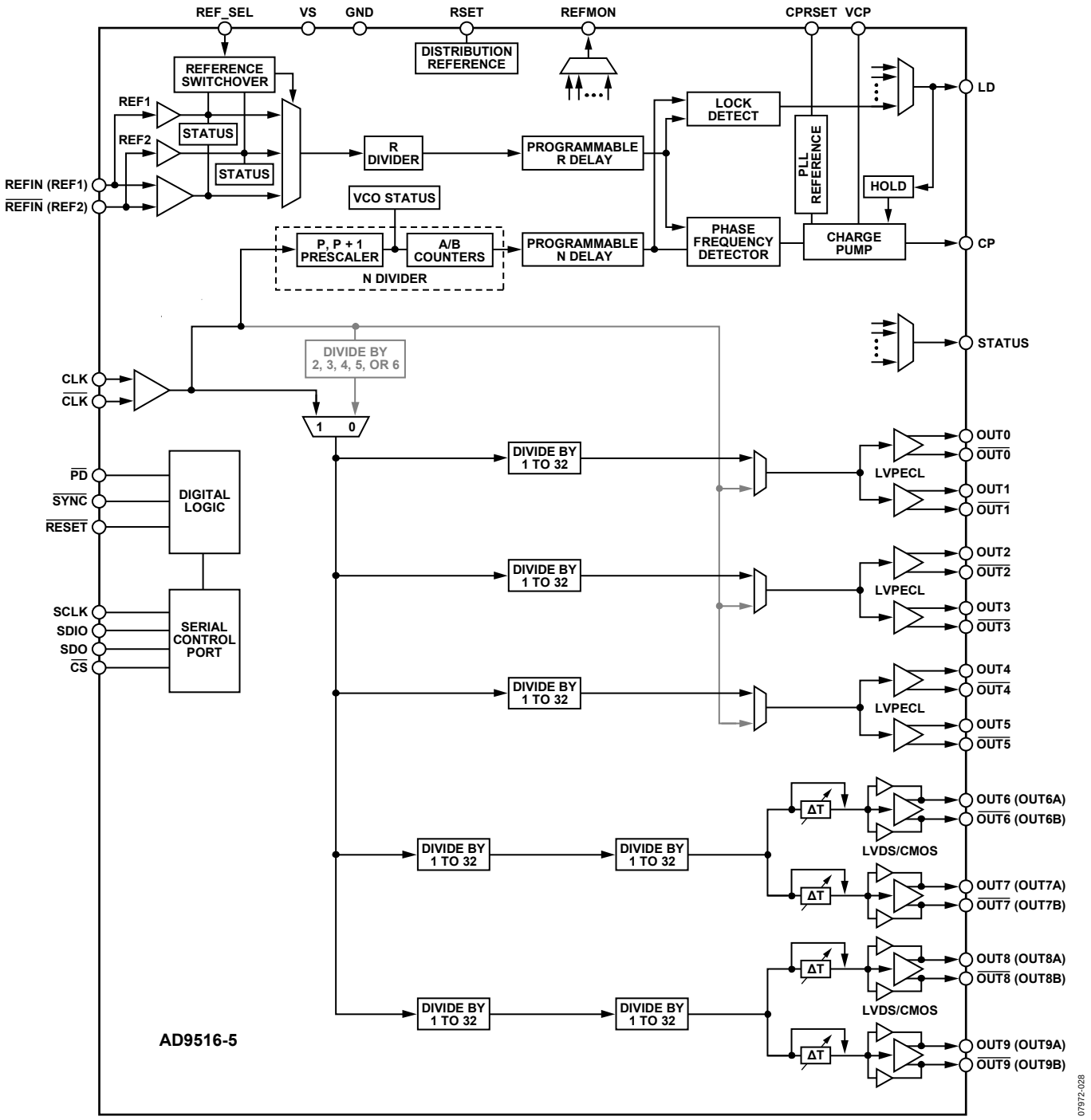

Figure 32. Clock Distribution or External VCO < 1600 MHz (Mode 1)

Mode 2: High Frequency Clock Distribution—CLK or External VCO >1600 MHz

The AD9516 power-up default configuration has the PLL powered off and the routing of the input set so that the CLK/$\overline{\text{CLK}}$ input is connected to the distribution section through the VCO divider (divide-by-2/divide-by-3/divide-by-4/divide-by-5/divide-by-6). This is a distribution-only mode that allows for an external input up to 2400 MHz (see Table 3). The maximum frequency that can be applied to the channel dividers is 1600 MHz; therefore, higher input frequencies must be divided down before reaching the channel dividers. This input routing can also be used for lower input frequencies, but the minimum divide is 2 before the channel dividers.

When the PLL is enabled, this routing also allows the use of the PLL with an external VCO or VCXO with a frequency <2400 MHz. In this configuration, the external VCO/VCXO feeds directly into the prescaler.

The register settings shown in Table 21 are the default values of these registers at power-up or after a reset operation. If the contents of the registers are altered by prior programming after power-up or reset, these registers may also be set intentionally to these values.

Table 21. Default Settings of Some PLL Registers

Register	Description
0x010[1:0] = 01b	PLL asynchronous power-down (PLL off)
0x1E0[2:0] = 010b	Set VCO divider = 4
0x1E1[0] = 0b	Use the VCO divider

When using the internal PLL with an external VCO, the PLL must be turned on.

Table 22. Settings When Using an External VCO

Register	Description
0x010[1:0] = 00b	PLL normal operation (PLL on).
0x010 to 0x01D	PLL settings. Select and enable a reference input; set R, N (P, A, B), PFD polarity, and I_{CP} according to the intended loop configuration.

An external VCO requires an external loop filter that must be connected between CP and the tuning pin of the VCO. This loop filter determines the loop bandwidth and stability of the PLL. Make sure to select the proper PFD polarity for the VCO being used.

Table 23. Setting the PFD Polarity

Register	Description
0x010[7] = 0b	PFD polarity positive (higher control voltage produces higher frequency)
0x010[7] = 1b	PFD polarity negative (higher control voltage produces lower frequency)

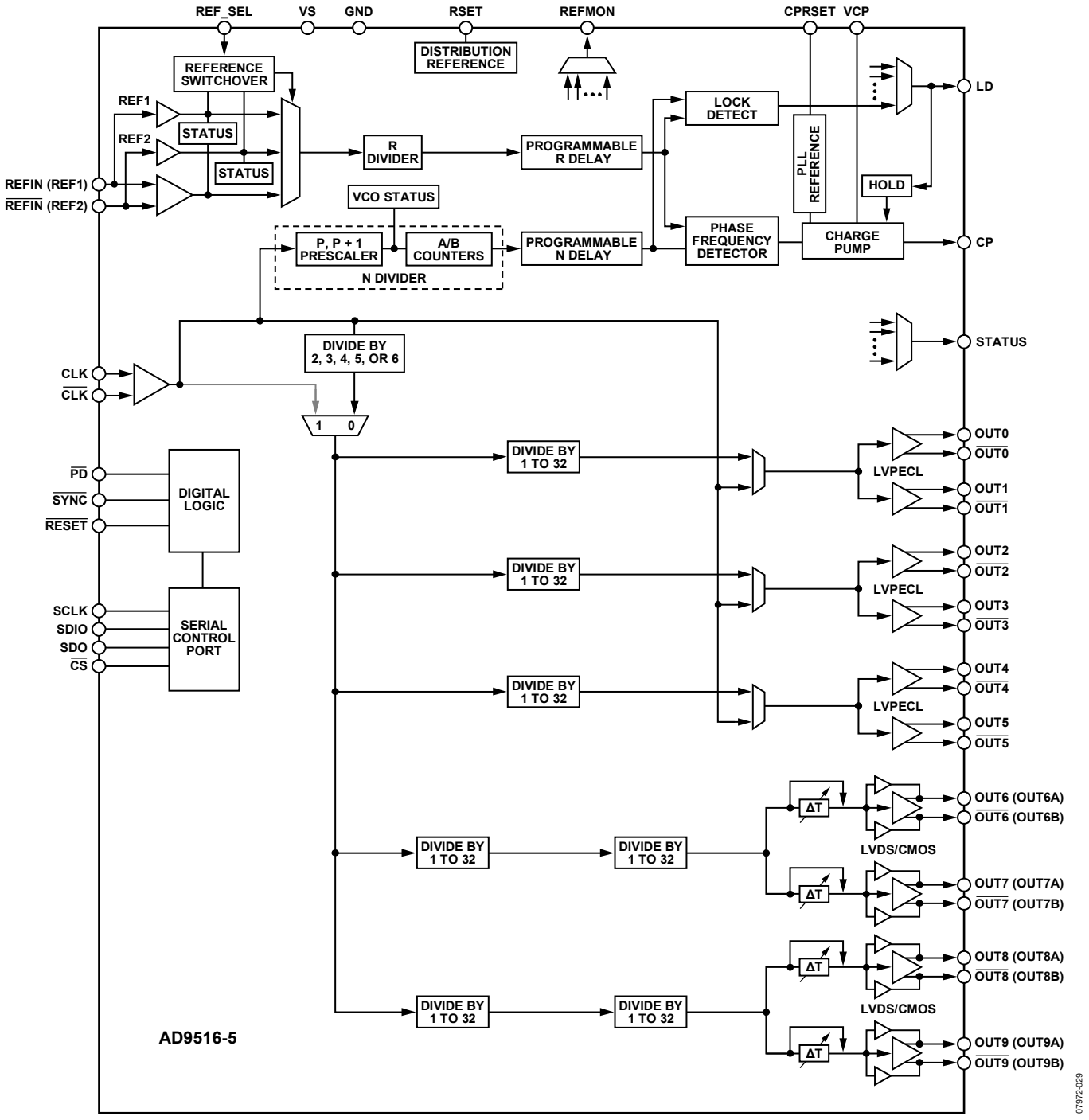

Figure 33. High Frequency Clock Distribution—CLK or External VCO > 1600 MHz (Mode 2)

Phase-Locked Loop (PLL)

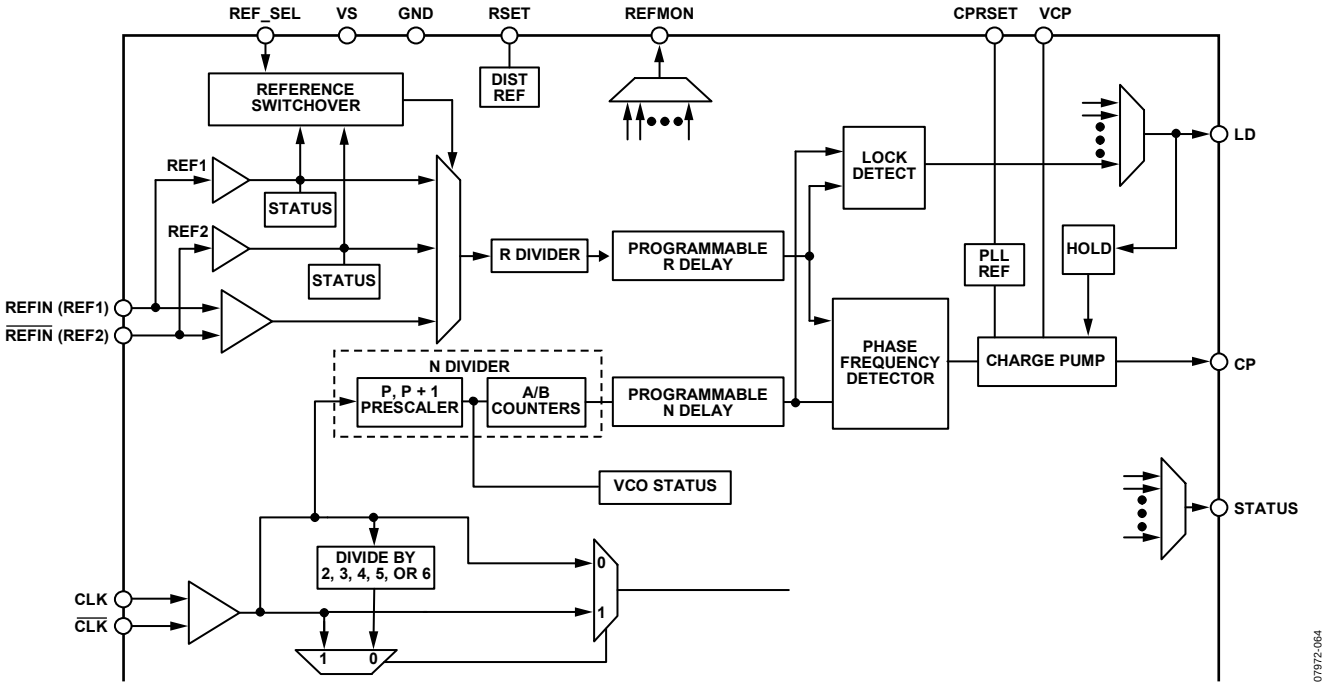

Figure 34. PLL Functional Block Diagram

The AD9516 includes on-chip PLL blocks that can be used with an external VCO or VCXO to create a complete phase-locked loop. The PLL requires an external loop filter, which usually consists of a small number of capacitors and resistors. The configuration and components of the loop filter help to establish the loop bandwidth and stability of the PLL.

The AD9516 PLL is useful for generating clock frequencies from a supplied reference frequency. This includes conversion of reference frequencies to much higher frequencies for subsequent division and distribution. In addition, the PLL can be used to clean up jitter and phase noise on a noisy reference. The exact choice of PLL parameters and loop dynamics is application specific. The flexibility and depth of the AD9516 PLL allow the part to be tailored to function in many different applications and signal environments.

Configuration of the PLL

Configuration of the PLL is accomplished by programming the various settings for the R divider, N divider, PFD polarity, and charge pump current. The combination of these settings determines the PLL loop bandwidth. These are managed through programmable register settings and by the design of the external loop filter.

Successful PLL operation and satisfactory PLL loop performance are highly dependent on proper configuration of the PLL settings, and the design of the external loop filter is crucial to the proper operation of the PLL.

ADIsimCLK™ is a free program that can help with the design and exploration of the capabilities and features of the AD9516, including the design of the PLL loop filter. ADIsimCLK Version 1.2 (or later) can be used for modeling the AD9516 loop filter. It is available at www.analog.com/clocks.

Phase Frequency Detector (PFD)

The PFD takes inputs from the R divider and N divider and produces an output proportional to the phase and frequency difference between them. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. The antibacklash pulse width is set by 0x017[1:0].

An important limit to keep in mind is the maximum frequency allowed into the PFD. The maximum input frequency into the PFD is a function of the antibacklash pulse setting, as specified in Table 2, Phase/Frequency Detector (PFD) parameter.

Charge Pump (CP)

The charge pump is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs, and tells the CP to pump up or pump down to charge or discharge the integrating node (part of the loop filter). The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the external VCO to move the VCO frequency up or down. The CP can be set (0x010[6:4]) for high impedance (allows holdover operation), for normal operation (attempts to lock the PLL loop), for pump-up, or for pump-down (test modes). The CP current is programmable in eight steps from (nominally) 0.6 mA to 4.8 mA. The exact value of the CP current LSB is set by the CPRSET resistor, which is nominally 5.1 kΩ. Doubling the CPRSET resistor allows the charge pump current to be programmed from (nominally) 0.3 mA to 2.4 mA

PLL External Loop Filter

An example of an external loop filter for a PLL is shown in Figure 35. A loop filter must be calculated for each desired PLL configuration. The values of the components depend on the VCO frequency, the K_{VCO}, the PFD frequency, the charge pump current, the desired loop bandwidth, and the desired phase margin. The loop filter affects the phase noise, the loop settling time, and the loop stability. A basic knowledge of PLL theory is necessary for understanding loop filter design. ADIsimCLK can help with the calculation of a loop filter according to the application requirements.

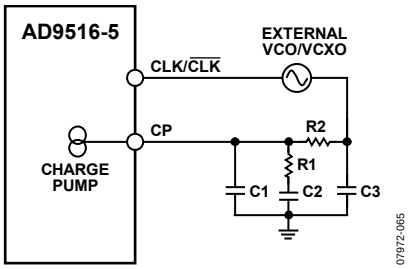

Figure 35. Example of External Loop Filter for PLL

PLL Reference Inputs

The AD9516 features a flexible PLL reference input circuit that allows a fully differential input or two separate single-ended inputs. The input frequency range for the reference inputs is specified in Table 2. Both the differential and the single-ended inputs are self-biased, allowing for easy ac coupling of input signals.

The differential input and the single-ended inputs share two pins, REFIN (REF1) and $\overline{\text{REFIN}}$ (REF2). The desired reference input type is selected and controlled by 0x01C (see Table 47 and Table 49).

When the differential reference input is selected, the self-bias level of the two sides is offset slightly (see Table 2) to prevent chattering of the input buffer when the reference is slow or missing. The specification for this voltage level is found in Table 2. The input hysteresis increases the voltage swing required of the driver to overcome the offset.

The single-ended inputs can be driven by either a dc-coupled CMOS level signal or an ac-coupled sine wave or square wave. Each single-ended input can be independently powered down when not needed to increase isolation and reduce power. Either a differential or a single-ended reference must be specifically enabled. All PLL reference inputs are off by default.

The differential reference input is powered down whenever the PLL is powered down, or when the differential reference input is not selected. The single-ended buffers power down when the PLL is powered down, and when their individual power-down registers are set. When the differential mode is selected, the single-ended inputs are powered down.

In differential mode, the reference input pins are internally self-biased so that they can be ac-coupled via capacitors. It is possible to dc couple to these inputs. If the differential REFIN is driven by a single-ended signal, the unused side ($\overline{\text{REFIN}}$) should be decoupled via a suitable capacitor to a quiet ground. Figure 36 shows the equivalent circuit of REFIN.

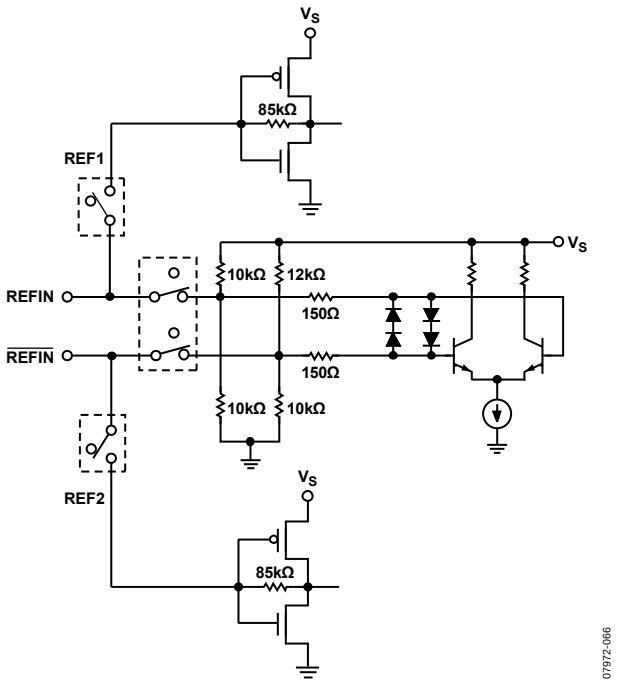

Figure 36. REFIN Equivalent Circuit

Reference Switchover

The AD9516 supports dual single-ended CMOS inputs, as well as a single differential reference input. In the dual single-ended reference mode, the AD9516 supports automatic and manual PLL reference clock switching between REF1 (on Pin REFIN) and REF2 (on Pin $\overline{\text{REFIN}}$). This feature supports networking and other applications that require redundant references. When using reference switchover, the single-ended reference inputs should be dc-coupled CMOS levels and never be allowed to go to high impedance. If these inputs are allowed to go to high impedance, noise may cause the buffer to chatter, causing a false detection of the presence of a reference.

There are several configurable modes of reference switchover. The switchover can be performed manually or automatically.

Manual switchover is performed either through Register 0x01C or by using the REF_SEL pin. The automatic switchover occurs when REF1 disappears. The switchover deglitch feature ensures that the PLL does not receive rising edges that are far out of alignment with the newly selected reference.

There are two automatic reference switchover modes (0x01C):

- Prefer REF1. Switch from REF1 to REF2 when REF1 disappears. Return to REF1 from REF2 when REF1 returns.
- Stay on REF2. Automatically switch to REF2 if REF1 disappears but do not switch back to REF1 if it reappears. The reference can be set back to REF1 manually at an appropriate time.

In automatic mode, REF1 is monitored by REF2. If REF1 disappears (two consecutive falling edges of REF2 without an edge transition on REF1), REF1 is considered missing. On the next subsequent rising edge of REF2, REF2 is used as the reference clock to the PLL. If 0x01C[3] = 0b (default), when REF1 returns (four rising edges of REF1 without two falling edges of REF2 between the REF1 edges), the PLL reference switches back to REF1. If 0x01C[3] = 1b, the user can control when to switch back to REF1. This is done by programming the part to manual reference select mode (0x01C[4] = 0b) and by ensuring that the registers and/or the REF_SEL pin are set to select the desired reference. Automatic mode can be reenabled when REF1 is reselected.

Manual switchover requires a valid clock on the reference input being switched to or that the deglitching feature be disabled (0x01C[7]).

Reference Divider R

The reference inputs are routed to the reference divider, R. R (a 14-bit counter) can be set to any value from 0 to 16,383 by writing to 0x011 and 0x012. (Both R = 0 and R = 1 give divide-by-1.) The output of the R divider goes to one of the PFD inputs to be compared with the VCO frequency divided by the N divider. The frequency applied to the PFD must not exceed the maximum allowable frequency. The antibacklash pulse setting should also be set according to Table 2 for a given PFD frequency.

The R divider has its own reset. R divider can be reset using the shared reset bit of the R, A, and B counters. It can also be reset by a $\overline{\text{SYNC}}$ operation.

VCXO/VCO Feedback Divider N: P, A, B

The N divider is a combination of a prescaler (P) and two counters, A and B. The total divider value is

$$N = (P \times B) + A$$

where *P* can be 2, 4, 8, 16, or 32.

Prescaler

The prescaler of the AD9516 allows for two modes of operation: a fixed divide (FD) mode of 1, 2, or 3, and a dual modulus (DM) mode where the prescaler divides by P and (P + 1) {2 and 3, 4 and 5, 8 and 9, 16 and 17, or 32 and 33}. The prescaler modes of operation are given in Table 49, 0x016[2:0]. Not all modes are available at all frequencies (see Table 2).

When operating the AD9516 in dual modulus mode, P/(P + 1), the equation used to relate the input reference frequency to the VCO output frequency is

$$f_{VCO} = (f_{REF}/R) \times (P \times B + A) = f_{REF} \times N/R$$

However, when operating the prescaler in FD Mode 1, FD Mode 2, or FD Mode 3, the A counter is not used (A = 0) and the equation simplifies to

$$f_{VCO} = (f_{REF}/R) \times (P \times B) = f_{REF} \times N/R$$

When A = 0, the divide is a fixed divide of P = 2, 4, 8, 16, or 32.

By using combinations of DM and FD modes, the AD9516 can achieve values of N all the way down to N = 1. Table 24 shows how a 10 MHz reference input may be locked to any integer multiple of N.

Note that the same value of N can be derived in different ways, as illustrated by the case of N = 12. The user can choose a fixed divide mode P = 2 with B = 6, use the dual modulus mode 2/3 with A = 0, B = 6, or use the dual modulus mode 4/5 with A = 0, B = 3.

A and B Counters

The B counter must be ≥3 or bypassed, and unlike the R counter, A = 0 is actually zero.

The maximum input frequency to the A/B counter is reflected in the maximum prescaler output frequency (~300 MHz) specified in Table 2. This is the prescaler input frequency (external VCO or CLK) divided by P. For example, dual-modulus P = 8/9 mode is not allowed if the external VCO frequency is >2400 MHz because the frequency going to the A counter and B counter is too high.

When the B counter is bypassed (B = 1), the A counter should be set to zero, and the overall resulting divide is equal to the prescaler setting, P. The possible divide ratios in this mode are 1, 2, 3, 4, 8, 16, and 32.

Although manual reset is not normally required, the A/B counters have their own reset bit. Alternatively, the A and B counters can be reset using the shared reset bit of the R, A, and B counters. Note that these reset bits are not self-clearing.

R, A, and B Counters: $\overline{\text{SYNC}}$ Pin Reset

The R, A, and B counters can also be reset simultaneously through the $\overline{\text{SYNC}}$ pin. This function is controlled by 0x019[7:6] (see Table 49). The $\overline{\text{SYNC}}$ pin reset is disabled by default.

R and N Divider Delays

Both the R and N dividers feature a programmable delay cell. These delays can be enabled to allow adjustment of the phase relationship between the PLL reference clock and the VCO or CLK. Each delay is controlled by three bits. The total delay range is about 1 ns. See 0x019 in Table 49.

Table 24. How a 10 MHz Reference Input May Be Locked to Any Integer Multiple of N

f_{REF} (MHz)	R	P	A	B	N	f_{VCO} (MHz)	Mode	Notes
10	1	1	X[1]	1	1	10	FD	P = 1, B = 1 (bypassed)
10	1	2	X[1]	1	2	20	FD	P = 2, B = 1 (bypassed)
10	1	1	X[1]	3	3	30	FD	P = 1, B = 3
10	1	1	X[1]	4	4	40	FD	P = 1, B = 4
10	1	1	X[1]	5	5	50	FD	P = 1, B = 5
10	1	2	X[1]	3	6	60	FD	P = 2, B = 3
10	1	2	0	3	6	60	DM	P = 2 and P + 1 = 3, A = 0, B = 3
10	1	2	1	3	7	70	DM	P = 2 and P + 1 = 3, A = 1, B = 3
10	1	2	2	3	8	80	DM	P = 2 and P + 1 = 3, A = 2, B = 3
10	1	2	1	4	9	90	DM	P = 2 and P + 1 = 3, A = 1, B = 4
10	1	2	X[1]	5	10	100	FD	P = 2, B = 5
10	1	2	0	5	10	100	DM	P = 2 and P + 1 = 3, A = 0, B = 5
10	1	2	1	5	11	110	DM	P = 2 and P + 1 = 3, A = 1, B = 5
10	1	2	X[1]	6	12	120	FD	P = 2, B = 6
10	1	2	0	6	12	120	DM	P = 2 and P + 1 = 3, A = 0, B = 6
10	1	4	0	3	12	120	DM	P = 4 and P + 1 = 5, A = 0, B = 3
10	1	4	1	3	13	130	DM	P = 4 and P + 1 = 5, A = 1, B = 3

[1] X = don't care.

Digital Lock Detect (DLD)

By selecting the proper output through the mux on each pin, the DLD function is available at the LD, STATUS, and REFMON pins. The digital lock detect circuit indicates a lock when the time difference of the rising edges at the PFD inputs is less than a specified value (the lock threshold). The loss of a lock is indicated when the time difference exceeds a specified value (the unlock threshold). Note that the unlock threshold is wider than the lock threshold, which allows some phase error in excess of the lock window to occur without chattering on the lock indicator.

The lock detect window timing depends on the value of the CPRSET resistor, as well as three settings: the digital lock detect window bit (0x018[4]), the antibacklash pulse width bit (0x017[1:0], see Table 2), and the lock detect counter (0x018[6:5]). The lock and unlock detection values in Table 2 are for the nominal value of CPRSET = 5.11 kΩ. Doubling the CPRSET value to 10 kΩ doubles the values in Table 2.

A lock is not indicated until there is a programmable number of consecutive PFD cycles with a time difference less than the lock detect threshold. The lock detect circuit continues to indicate a lock until a time difference greater than the unlock threshold occurs on a single subsequent cycle. For the lock detect to work properly, the period of the PFD frequency must be greater than the unlock threshold. The number of consecutive PFD cycles required for a lock is programmable (0x018[6:5]).

Note that it is possible in certain low (<500 Hz) loop bandwidth, high phase margin cases that the DLD can chatter during acquisition, which can cause the AD9516 to automatically enter and exit holdover. To avoid this problem, it is recommended to make provisions for a capacitor to ground on the LD pin so that current source digital lock detect (CSDLD) mode can be used.

Analog Lock Detect (ALD)

The AD9516 provides an ALD function that can be selected for use at the LD pin. There are two versions of ALD.

- N-channel open-drain lock detect. This signal requires a pull-up resistor to the positive supply, VS. The output is normally high with short, low going pulses. Lock is indicated by the minimum duty cycle of the low going pulses.
- P-channel open-drain lock detect. This signal requires a pull-down resistor to GND. The output is normally low with short, high going pulses. Lock is indicated by the minimum duty cycle of the high going pulses.

The analog lock detect function requires an RC filter to provide a logic level indicating lock vs. unlock.

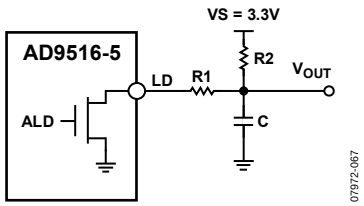

Figure 37. Example of Analog Lock Detect Filter, Using N-Channel Open-Drain Driver

Current Source Digital Lock Detect (CSDLD)

During the PLL locking sequence, it is normal for the DLD signal to toggle a number of times before remaining steady when the PLL is completely locked and stable. There may be applications where it is desirable to have DLD asserted only after the PLL is solidly locked. This is possible by using the current source digital lock detect function.

The current source lock detect provides a current of 110 µA when DLD is true and shorts to ground when DLD is false. If a capacitor is connected to the LD pin, it charges at a rate determined by the current source during the DLD true time but is discharged nearly instantly when DLD is false. By monitoring the voltage at the LD pin (top of the capacitor), LD = high happens only after the DLD is true for a sufficiently long time. Any momentary DLD false resets the charging. By selecting a properly sized capacitor, it is possible to delay a lock detect indication until the PLL is stably locked and the lock detect does not chatter.

To use current source digital lock detect, do the following:

- Place a capacitor to ground on the LD pin
- Set 0x01A[5:0] = 0x04
- Enable the LD pin comparator (0x01D[3] = 1)

The LD pin comparator senses the voltage on the LD pin, and the comparator output can be made available at the REFMON pin control (0x01B[4:0]) or the STATUS pin control (0x017[7:2]). The internal LD pin comparator trip point and hysteresis are given in Table 13. The voltage on the capacitor can also be sensed by an external comparator connected to the LD pin. In this case, enabling the on-board LD pin comparator is not necessary.

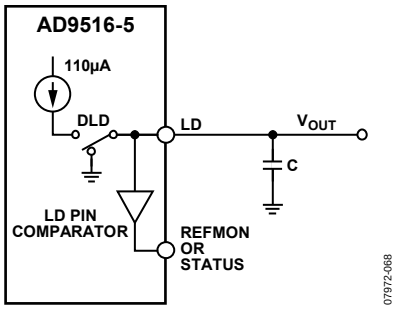

Figure 38. Current Source Lock Detect

External VCXO/VCO Clock Input (CLK/$\overline{\text{CLK}}$)

CLK is a differential input that can be used to drive the AD9516 clock distribution section. This input can receive up to 2.4 GHz. The pins are internally self-biased, and the input signal should be ac-coupled via capacitors.

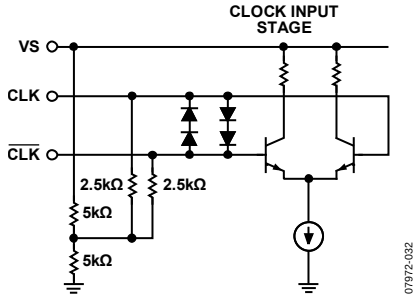

Figure 39. CLK Equivalent Input Circuit

The CLK/$\overline{\text{CLK}}$ input can be used either as a distribution only input (with the PLL off), or as a feedback input for an external VCO/VCXO using the PLL. The CLK/$\overline{\text{CLK}}$ input can be used for frequencies up to 2.4 GHz.

Holdover

The AD9516 PLL has a holdover function. Holdover is implemented by putting the charge pump into a high impedance state. This is useful when the PLL reference clock is lost. Holdover mode allows the VCO to maintain a relatively constant frequency even though there is no reference clock. Without this function, the charge pump is placed into a constant pump-up or pump-down state, resulting in a large VCO frequency shift. Because the charge pump is placed in a high impedance state, any leakage that occurs at the charge pump output or the VCO tuning node causes a drift of the VCO frequency. This can be mitigated by using a loop filter that contains a large capacitive component because this drift is limited by the current leakage induced slew rate (I_{LEAK}/C) of the VCO control voltage.

Both a manual holdover mode, using the $\overline{\text{SYNC}}$ pin, and an automatic holdover mode are provided. To use either function, the holdover function must be enabled (0x01D[0] and 0x01D[2]).

Manual Holdover Mode

A manual holdover mode can be enabled that allows the user to place the charge pump into a high impedance state when the $\overline{\text{SYNC}}$ pin is asserted low. This operation is edge sensitive, not level sensitive. The charge pump enters a high impedance state immediately. To take the charge pump out of a high impedance state, take the $\overline{\text{SYNC}}$ pin high. The charge pump then leaves the high impedance state synchronously with the next PFD rising edge from the reference clock. This prevents extraneous charge pump events from occurring during the time between $\overline{\text{SYNC}}$ going high and the next PFD event. This also means that the charge pump stays in a high impedance state if there is no reference clock present.

The B counter (in the N divider) is reset synchronously with the charge pump leaving the high impedance state on the reference path PFD event. This helps align the edges out of the R and N dividers for faster settling of the PLL. Because the prescaler is not reset, this feature works best when the B and R numbers are close because this results in a smaller phase difference for the loop to settle out.

When using this mode, the channel dividers should be set to ignore the $\overline{\text{SYNC}}$ pin (at least after an initial $\overline{\text{SYNC}}$ event). If the dividers are not set to ignore the $\overline{\text{SYNC}}$ pin, any time $\overline{\text{SYNC}}$ is taken low to put the part into holdover, the distribution outputs turn off.

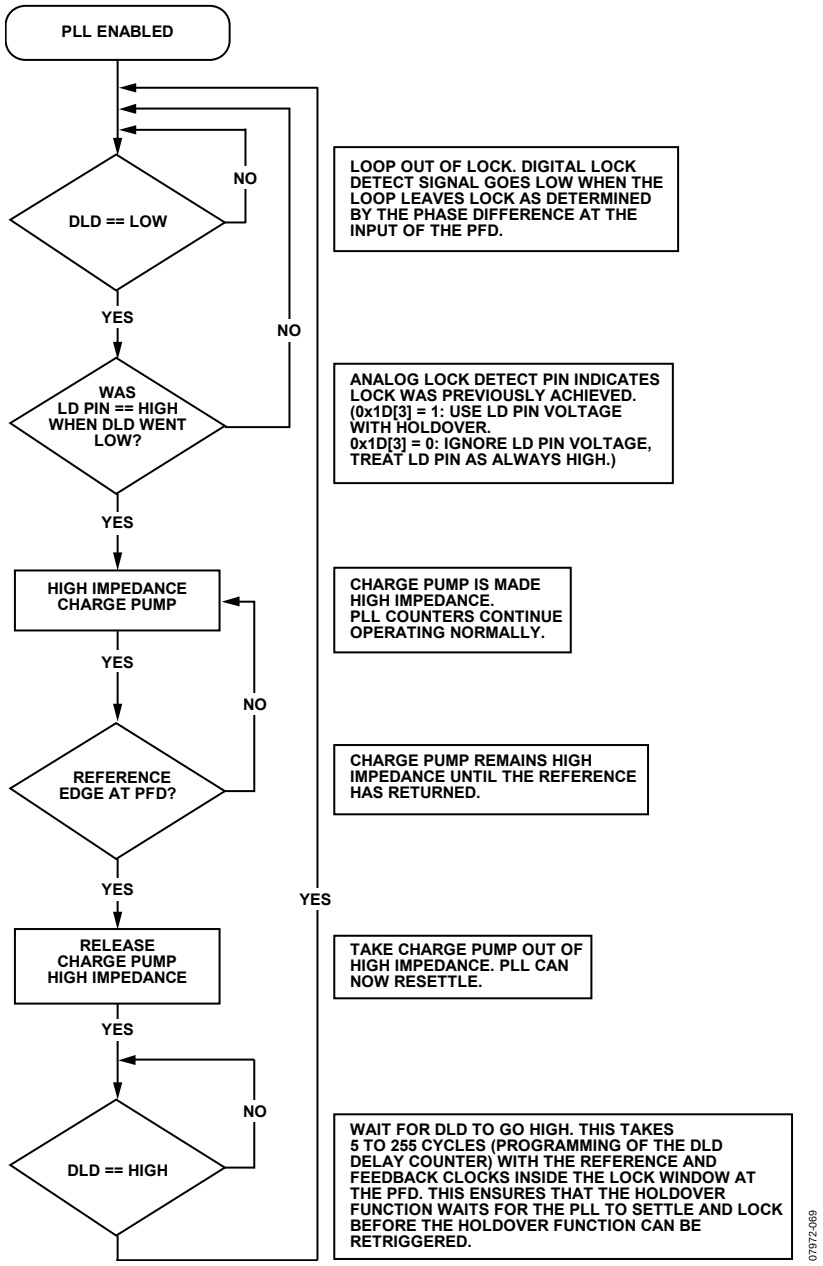

Figure 40. Flowchart of Automatic/Internal Holdover Mode

Automatic/Internal Holdover Mode

When enabled, the automatic/internal holdover mode automatically puts the charge pump into a high impedance state when the loop loses lock. The assumption is that the only reason that the loop loses lock is due to the PLL losing the reference clock; therefore, the holdover function puts the charge pump into a high impedance state to maintain the VCO frequency as close as possible to the original frequency before the reference clock disappeared.

A flowchart of the internal/automatic holdover function operation is shown in Figure 40.

The holdover function senses the logic level of the LD pin as a condition to enter holdover. The signal at LD can be from the DLD, ALD, or current source digital LD (CSDLD) mode. It is possible to disable the LD comparator (0x01D[3]), which causes the holdover function to always sense LD as being high. If DLD is used, it is possible for the DLD signal to chatter while the PLL is reacquiring lock. The holdover function may retrigger, thereby preventing the holdover mode from terminating. Use of the current source lock detect mode is recommended to avoid this situation (see the Current Source Digital Lock Detect section).

When in holdover mode, the charge pump stays in a high impedance state as long as there is no reference clock present.

As in the external holdover mode, the B counter (in the N divider) is reset synchronously with the charge pump leaving the high impedance state on the reference path PFD event. This helps align the edges out of the R and N dividers for faster settling of the PLL and reduces frequency errors during settling. Because the prescaler is not reset, this feature works best when the B and R numbers are close because this results in a smaller phase difference for the loop to settle out.

After leaving holdover, the loop then reacquires lock and the LD pin must go high (if 0x01D[3] = 1) before it can reenter holdover.

The holdover function always responds to the state of the currently selected reference (0x01C). If the loop loses lock during a reference switchover (see the Reference Switchover section), holdover is triggered briefly until the next reference clock edge at the PFD.

The following registers affect the automatic/internal holdover function:

- 0x018[6:5]—lock detect counter. This changes how many consecutive PFD cycles with edges inside the lock detect window are required for the DLD indicator to indicate lock. This impacts the time required before the LD pin can begin to charge, as well as the delay from the end of a holdover event until the holdover function can be reengaged.
- 0x018[3]—disable digital lock detect. This bit must be set to a 0 to enable the DLD circuit. Internal/automatic holdover does not operate correctly without the DLD function enabled.
- 0x01A[5:0]—lock detect pin control. Set this to 000100b to put it in the current source lock detect mode if using the LD pin comparator. Load the LD pin with a capacitor of an appropriate value.
- 0x01D[3]—LD pin comparator enable. 1 = enable; 0 = disable. When disabled, the holdover function always senses the LD pin as high.
- 0x01D[1]— external holdover control.
- 0x01D[0] and 0x01D[2]—holdover enable. If holdover is disabled, both external and automatic/internal holdover are disabled.

In the following example, automatic holdover is configured with:

- Automatic reference switchover, prefer REF1.
- Digital lock detect: five PFD cycles, high range window.
- Automatic holdover using the LD pin comparator.

The following registers are set (in addition to the normal PLL registers):

- 0x018[6:5] = 00b; lock detect counter = five cycles.
- 0x018[4] = 0b; digital lock detect window = high range.
- 0x018[3] = 0b; disable DLD normal operation.
- 0x01A[5:0] = 000100b; program LD pin control to current source lock detect mode.
- 0x01C[4] = 1b; enable automatic reference switchover.
- 0x01C[3] = 0b; prefer REF1.
- 0x01C[2:1] = 11b; enable REF1 and REF2 input buffers.
- 0x01D[3] = 1b; enable LD pin comparator.
- 0x01D[2] = 1b; enable the holdover function.
- 0x01D[1] = 0b; use external holdover mode.
- 0x01D[0] = 1b; holdover enable.

Frequency Status Monitors

The AD9516 contains three frequency status monitors that are used to indicate if the PLL reference (or references in the case of single-ended mode) and the VCO have fallen below a threshold frequency. Figure 41 is a diagram that shows their location in the PLL.

The PLL reference monitors have two threshold frequencies: normal and extended (see Table 13). The reference frequency monitor thresholds are selected in 0x01F.

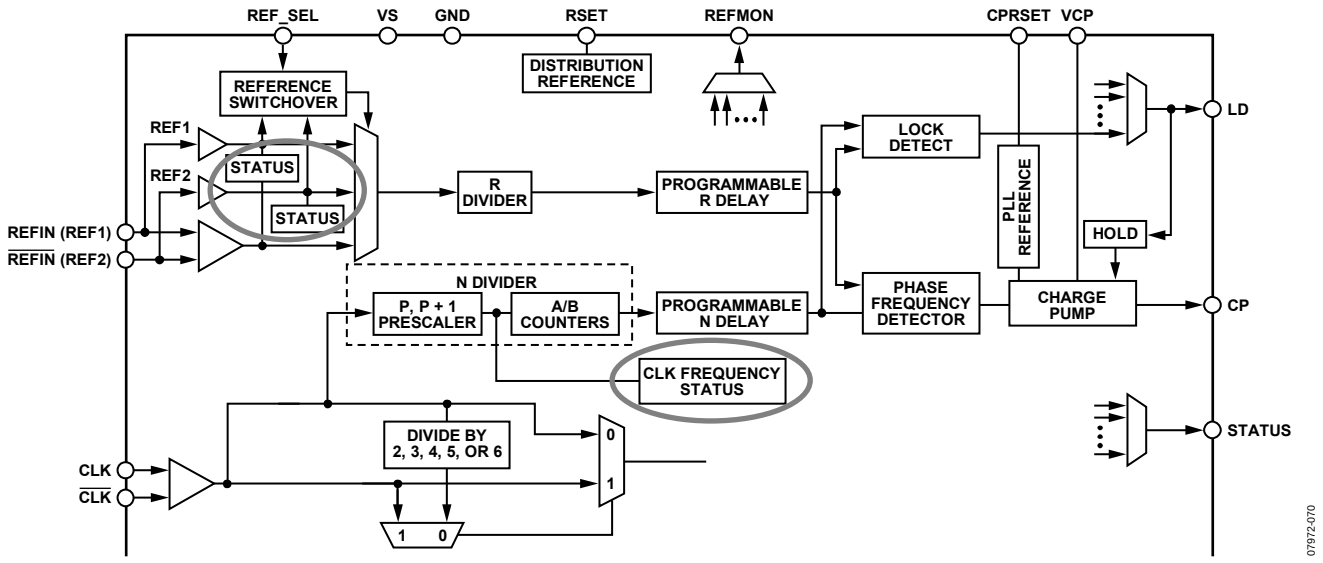

Figure 41. Reference and CLK Status Monitors

CLOCK DISTRIBUTION

A clock channel consists of a pair (or double pair, in the case of CMOS) of outputs that share a common divider. A clock output consists of the drivers that connect to the output pins. The clock outputs have either LVPECL or LVDS/CMOS signal levels at the pins.

The AD9516 has five clock channels: three channels are LVPECL (six outputs); two channels are LVDS/CMOS (up to four LVDS outputs, or up to eight CMOS outputs).

Each channel has its own programmable divider that divides the clock frequency applied to its input. The LVPECL channel dividers contain a divider that can divide by any integer from 1 to 32. Each LVDS/CMOS channel divider contains two cascaded dividers that can be set to divide by any integer from 1 to 32. The total division of the channel is the product of the divide value of the two cascaded dividers. This allows divide values of (1 to 32) × (1 to 32), or up to 1024 (notice that this is not all values from 1 to 1024 but only the set of numbers that are the product of the two dividers).

The VCO divider can be set to divide by 2, 3, 4, 5, or 6 and must be used if the external clock signal connected to the CLK input is greater than 1600 MHz.

The channel dividers allow for a selection of various duty cycles, depending on the currently set division. That is, for any specific division, D, the output of the divider can be set to high for N + 1 input clock cycles and low for M + 1 input clock cycles (where D = N + M + 2). For example, a divide-by-5 can be high for one divider input cycle and low for four cycles, or a divide-by-5 can be high for three divider input cycles and low for two cycles. Other combinations are also possible.

The channel dividers include a duty-cycle correction function that can be disabled. In contrast to the selectable duty cycle just described, this function can correct a non-50% duty cycle caused by an odd division. However, this requires that the division be set by M = N + 1.

In addition, the channel dividers allow a coarse phase offset or delay to be set. Depending on the division selected, the output can be delayed by up to 31 input clock cycles. The divider outputs can also be set to start high or to start low.

Operating Modes

There are two clock distribution operating modes. These operating modes are shown in Table 25.

It is not necessary to use the VCO divider if the CLK frequency is less than the maximum channel divider input frequency (1600 MHz); otherwise, the VCO divider must be used to reduce the frequency going to the channel dividers.

Table 25. Clock Distribution Operating Modes

Mode	0x1E1[0]	VCO Divider
2	0	Used
1	1	Not used

CLK Direct to LVPECL Outputs

It is possible to connect the CLK directly to the LVPECL outputs, OUT0 to OUT5. However, the LVPECL outputs may not be able to provide full a voltage swing at the highest frequencies.

To connect the LVPECL outputs directly to the CLK input, the VCO divider must be selected as the source to the distribution section even if no channel uses it.

Table 26. Settings for Routing VCO Divider Input Directly to LVPECL Outputs

Register Setting	Selection
0x1E1[0] = 0b	VCO divider selected
0x192[1] = 1b	Direct to output OUT0, OUT1
0x195[1] = 1b	Direct to output OUT2, OUT3
0x198[1] = 1b	Direct to output OUT4, OUT5

Clock Frequency Division

The total frequency division is a combination of the VCO divider (when used) and the channel divider. When the VCO divider is used, the total division from the VCO or CLK to the output is the product of the VCO divider (2, 3, 4, 5, and 6) and the division of the channel divider. Table 27 and Table 28 indicate how the frequency division for a channel is set. For the LVPECL outputs, there is only one divider per channel. For the LVDS/CMOS outputs, there are two dividers (X.1, X.2) cascaded per channel.

Table 27. Frequency Division for Divider 0 to Divider 2

VCO Divider Setting	Channel Divider Setting	CLK Direct to Output Setting	Frequency Division
2 to 6	Don't care	Enable	1
2 to 6	Bypass	Disable	(2 to 6) × (1)
2 to 6	2 to 32	Disable	(2 to 6) × (2 to 32)
VCO Divider Bypassed	Bypass	No	1
VCO Divider Bypassed	2 to 32	No	2 to 32

Table 28. Frequency Division for Divider 3 and Divider 4

VCO Divider Setting	Channel Divider Setting		Resulting Frequency Division
	X.1	X.2	
2 to 6	Bypass	Bypass	(2 to 6) × (1) × (1)
2 to 6	2 to 32	Bypass	(2 to 6) × (2 to 32) × (1)
2 to 6	2 to 32	2 to 32	(2 to 6) × (2 to 32) × (2 to 32)
Bypass	1	1	1
Bypass	2 to 32	1	(2 to 32) × (1)
Bypass	2 to 32	2 to 32	2 to 32 × (2 to 32)

The channel dividers feeding the LVPECL output drivers contain one 2-to-32 frequency divider. This divider provides for division by 1 to 32. Division by 1 is accomplished by bypassing the divider. The dividers also provide for a programmable duty cycle, with optional duty-cycle correction when the divide ratio is odd. A phase offset or delay in increments of the input clock cycle is selectable. The channel dividers operate with a signal at their inputs up to 1600 MHz. The features and settings of the dividers are selected by programming the appropriate setup and control registers (see Table 47 through Table 57).

VCO Divider

The VCO divider provides frequency division between the external CLK input and the clock distribution channel dividers. The VCO divider can be set to divide by 2, 3, 4, 5, or 6 (see Table 55, 0x1E0[2:0]).

Channel Dividers—LVPECL Outputs

Each pair of LVPECL outputs is driven by a channel divider. There are three channel dividers (0, 1, and 2) driving six LVPECL outputs (OUT0 to OUT5). Table 29 gives the register locations used for setting the division and other functions of these dividers. The division is set by the values of M and N. The divider can be bypassed (equivalent to divide-by-1, divider circuit is powered down) by setting the bypass bit. The duty-cycle correction can be enabled or disabled according to the setting of the DCCOFF bits.

Table 29. Setting D_X for Divider 0, Divider 1, and Divider 2

Divider	Low Cycles M	High Cycles N	Bypass	DCCOFF
0	0x190[7:4]	0x190[3:0]	0x191[7]	0x192[0]
1	0x193[7:4]	0x193[3:0]	0x194[7]	0x195[0]
2	0x196[7:4]	0x196[3:0]	0x197[7]	0x198[0]

Note that the value stored in the register equals the number of cycles minus one. For example, 0x190[7:4] = 0001b equals two low cycles (M = 2) for Divider 0.

Channel Frequency Division (0, 1, and 2)

For each channel (where the channel number is x: 0, 1, or 2), the frequency division, D_X, is set by the values of M and N (four bits each, representing decimal 0 to 15), where

$$Number\ of\ Low\ Cycles = M + 1$$

$$Number\ of\ High\ Cycles = N + 1$$

The cycles are cycles of the clock signal currently routed to the input of the channel dividers (VCO divider out or CLK).

When a divider is bypassed, $D_X = 1$.

Otherwise, $D_X = (N + 1) + (M + 1) = N + M + 2$. This allows each channel divider to divide by any integer from 1 to 32.

Duty Cycle and Duty-Cycle Correction (0, 1, and 2)

The duty cycle of the clock signal at the output of a channel is a result of some or all of the following conditions:

- What the M and N values for the channel are.
- If the DCC is enabled.
- If the VCO divider is used.
- The CLK input duty cycle.

The DCC function is enabled by default for each channel divider. However, the DCC function can be disabled individually for each channel divider by setting the DCCOFF bit for that channel.

Certain M and N values for a channel divider result in a non-50% duty cycle. A non-50% duty cycle can also result with an even division, if M ≠ N. The duty-cycle correction function automatically corrects non-50% duty cycles at the channel divider output to 50% duty cycle. Duty-cycle correction requires the following channel divider conditions:

- An even division must be set as M = N
- An odd division must be set as M = N + 1

When not bypassed or corrected by the DCC function, the duty cycle of each channel divider output is the numerical value of (N + 1)/(N + M + 2) expressed as a %.

The duty cycle at the output of the channel divider for various configurations is shown in Table 30 to Table 32.

Table 30. Duty Cycle with VCO Divider, Input Duty Cycle Is 50%

VCO Divider	D_X	Output Duty Cycle	
	N + M + 2	DCCOFF = 1	DCCOFF = 0
Even	1 (divider bypassed)	50%	50%
Odd = 3	1 (divider bypassed)	33.3%	50%
Odd = 5	1 (divider bypassed)	40%	50%
Even, Odd	Even	(N + 1)/(N + M + 2)	50%, requires M = N
Even, Odd	Odd	(N + 1)/(N + M + 2)	50%, requires M = N + 1

Table 31. Duty Cycle with VCO Divider, Input Duty Cycle Is X%

VCO Divider	D_X	Output Duty Cycle	
	N + M + 2	DCCOFF = 1	DCCOFF = 0
Even	1 (divider bypassed)	50%	50%
Odd = 3	1 (divider bypassed)	33.3%	(1 + X%)/3
Odd = 5	1 (divider bypassed)	40%	(2 + X%)/5
Even	Even	(N + 1)/(N + M + 2)	50%, requires M = N
	Odd	(N + 1)/(N + M + 2)	50%, requires M = N + 1
Odd = 3	Even	(N + 1)/(N + M + 2)	50%, requires M = N
Odd = 3	Odd	(N + 1)/(N + M + 2)	(3N + 4 + X%)/(6N + 9), requires M = N + 1
Odd = 5	Even	(N + 1)/(N + M + 2)	50%, requires M = N
Odd = 5	Odd	(N + 1)/(N + M + 2)	(5N + 7 + X%)/(10N + 15), requires M = N + 1

Table 32. Channel Divider Output Duty Cycle When the VCO Divider Is Not Used

Input Clock Duty Cycle	D_X	Output Duty Cycle	
	N + M + 2	DCCOFF = 1	DCCOFF = 0
Any	Channel divider bypassed	1 (divider bypassed)	Same as input duty cycle
Any	Even	(N + 1)/(M + N + 2)	50%, requires M = N
50%	Odd	(N + 1)/(M + N + 2)	50%, requires M = N + 1
X%	Odd	(N + 1)/(M + N + 2)	(N + 1 + X%)/(2 × N + 3), requires M = N + 1

If the CLK input is routed directly to the output, the duty cycle of the output is the same as the CLK input.

Phase Offset or Coarse Time Delay (0, 1, and 2)

Each channel divider allows for a phase offset, or a coarse time delay, to be programmed by setting register bits (see Table 33). These settings determine the number of cycles (successive rising edges) of the channel divider input frequency by which to offset, or delay, the rising edge of the output of the divider. This delay is with respect to a nondelayed output (that is, with a phase offset of zero). The amount of the delay is set by five bits loaded into the phase offset (PO) register plus the start high (SH) bit for each channel divider. When the start high bit is set, the delay is also affected by the number of low cycles (M) programmed for the divider.

It is necessary to use the SYNC function to make phase offsets effective (see the Synchronizing the Outputs—SYNC Function section).

Table 33. Setting Phase Offset and Division for Divider 0, Divider 1, and Divider 2

Divider	Start High (SH)	Phase Offset (PO)	Low Cycles M	High Cycles N
0	0x191[4]	0x191[3:0]	0x190[7:4]	0x190[3:0]
1	0x194[4]	0x194[3:0]	0x193[7:4]	0x193[3:0]
2	0x197[4]	0x197[3:0]	0x196[7:4]	0x196[3:0]

Note that the value stored in the register equals the number of cycles minus one. For example, 0x190[7:4] = 0001b equals two low cycles (M = 2) for Divider 0.

Let
Δ_t = delay (in seconds).
Δ_c = delay (in cycles of clock signal at input to D_X).
T_X = period of the clock signal at the input of the divider, D_X (in seconds).
Φ =
$16 \times SH[4] + 8 \times PO[3] + 4 \times PO[2] + 2 \times PO[1] + 1 \times PO[0]$

The channel divide-by is set as N = high cycles and M = low cycles.

Case 1

For $\Phi \leq 15$:
$\Delta_t = \Phi \times T_X$
$\Delta_c = \Delta_t/T_X = \Phi$

Case 2

For $\Phi \geq 16$:
$\Delta_t = (\Phi - 16 + M + 1) \times T_X$
$\Delta_c = \Delta_t/T_X$

By giving each divider a different phase offset, output-to-output delays can be set in increments of the channel divider input clock cycle. Figure 42 shows the results of setting such a coarse offset between outputs.

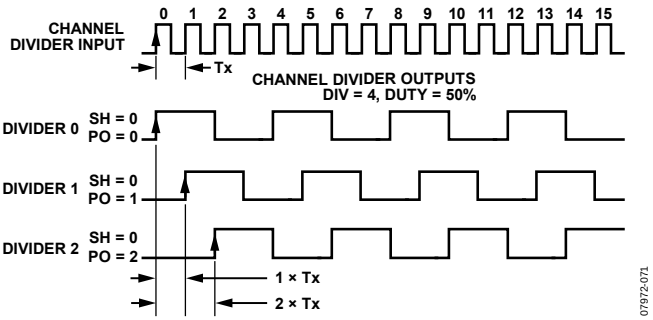

Figure 42. Effect of Coarse Phase Offset (or Delay)

Channel Dividers—LVDS/CMOS Outputs

Channel Divider 3 and Channel Divider 4 each drive a pair of LVDS outputs, giving four LVDS outputs (OUT6 to OUT9). Alternatively, each of these LVDS differential outputs can be configured individually as a pair (A and B) of CMOS single-ended outputs, providing for up to eight CMOS outputs. By default, the B output of each pair is off but can be turned on as desired.

Channel Divider 3 and Channel Divider 4 each consist of two cascaded, 1 to 32, frequency dividers. The channel frequency division is $D_{X.1} \times D_{X.2}$ or up to 1024. Both of the dividers also have DCC enabled by default, but this function can be disabled, if desired, by setting the DCCOFF bit of the channel. A coarse phase offset or delay is also programmable (see the Phase Offset or Coarse Time Delay (Divider 3 and Divider 4) section). The channel dividers operate up to 1600 MHz. The features and settings of the dividers are selected by programming the appropriate setup and control registers (see Table 47 and Table 48 through Table 57).

Table 34. Setting Division (D_X) for Divider 3 and Divider 4

Divider		M	N	Bypass	DCCOFF
3	3.1	0x199[7:4]	0x199[3:0]	0x19C[4]	0x19D[0]
	3.2	0x19B[7:4]	0x19B[3:0]	0x19C[5]	0x19D[0]
4	4.1	0x19E[7:4]	0x19E[3:0]	0x1A1[4]	0x1A2[0]
	4.2	0x1A0[7:4]	0x1A0[3:0]	0x1A1[5]	0x1A2[0]

Note that the value stored in the register equals the number of cycles minus one. For example, 0x199[7:4] = 0001b equals two low cycles (M = 2) for Divider 3.1.

Channel Frequency Division (Divider 3 and Divider 4)

The division for each channel divider is set by the bits in the registers for the individual dividers (X.Y = 3.1, 3.2, 4.1, and 4.2).

Number of Low Cycles = $M_{X.Y} + 1$

Number of High Cycles = $N_{X.Y} + 1$

When both X.1 and X.2 are bypassed, $D_X = 1 \times 1 = 1$.

When only X.2 is bypassed, $D_X = (N_{X.1} + M_{X.1} + 2) \times 1$.

When both X.1 and X.2 are not bypassed, $D_X = (N_{X.1} + M_{X.1} + 2) \times (N_{X.2} + M_{X.2} + 2)$.

By cascading the dividers, channel division up to 1024 can be obtained. However, not all integer value divisions from 1 to 1024 are obtainable; only the values that are the product of the separate divisions of the two dividers ($D_{X.1} \times D_{X.2}$) can be realized.

If only one divider is needed when using Divider 3 and Divider 4, use the first one (X.1) and bypass the second one (X.2). Do not bypass X.1 and use X.2.

Duty Cycle and Duty-Cycle Correction (Divider 3 and Divider 4)

The same duty cycle and DCC considerations apply to Divider 3 and Divider 4 as to Divider 0, Divider 1, and Divider 2 (see Duty Cycle and Duty-Cycle Correction (0, 1, and 2)); however, with these channel dividers, the number of possible configurations is more complex.

Duty-cycle correction on Divider 3 and Divider 4 requires the following channel divider conditions:

- An even $D_{X.Y}$ must be set as $M_{X.Y} = N_{X.Y}$ (low cycles = high cycles).
- An odd $D_{X.Y}$ must be set as $M_{X.Y} = N_{X.Y} + 1$ (the number of low cycles must be one greater than the number of high cycles).
- If only one divider is bypassed, it must be the second divider, X.2.
- If only one divider has an even divide by, it must be the second divider, X.2.

The possibilities for the duty cycle of the output clock from Divider 3 and Divider 4 are shown in Table 35 through Table 39.

Table 35. Divider 3 and Divider 4 Duty Cycle; VCO Divider Used; Duty Cycle Correction Off (DCCOFF = 1)

VCO Divider	$D_{X.1}$ $N_{X.1} + M_{X.1} + 2$	$D_{X.2}$ $N_{X.2} + M_{X.2} + 2$	Output Duty Cycle
Even	Bypassed	Bypassed	50%
Odd = 3	Bypassed	Bypassed	33.3%
Odd = 5	Bypassed	Bypassed	40%
Even	Even, Odd	Bypassed	$(N_{X.1} + 1)/(N_{X.1} + M_{X.1} + 2)$
Odd	Even, Odd	Bypassed	$(N_{X.1} + 1)/(N_{X.1} + M_{X.1} + 2)$
Even	Even, Odd	Even, Odd	$(N_{X.2} + 1)/(N_{X.2} + M_{X.2} + 2)$
Odd	Even, Odd	Even, Odd	$(N_{X.2} + 1)/(N_{X.2} + M_{X.2} + 2)$

Table 36. Divider 3 and Divider 4 Duty Cycle; VCO Divider Not Used; Duty Cycle Correction Off (DCCOFF = 1)

Input Clock Duty Cycle	$D_{X.1}$ $N_{X.1} + M_{X.1} + 2$	$D_{X.2}$ $N_{X.2} + M_{X.2} + 2$	Output Duty Cycle
50%	Bypassed	Bypassed	50%
X%	Bypassed	Bypassed	X%
50%	Even, Odd	Bypassed	$(N_{X.1} + 1)/(N_{X.1} + M_{X.1} + 2)$
X%	Even, Odd	Bypassed	$(N_{X.1} + 1)/(N_{X.1} + M_{X.1} + 2)$
50%	Even, Odd	Even, Odd	$(N_{X.2} + 1)/(N_{X.2} + M_{X.2} + 2)$
X%	Even, Odd	Even, Odd	$(N_{X.2} + 1)/(N_{X.2} + M_{X.2} + 2)$

Table 37. Divider 3 and Divider 4 Duty Cycle; VCO Divider Used; Duty Cycle Correction On (DCCOFF = 0); VCO Divider Input Duty Cycle = 50%

VCO Divider	$D_{X.1}$ $N_{X.1} + M_{X.1} + 2$	$D_{X.2}$ $N_{X.2} + M_{X.2} + 2$	Output Duty Cycle
Even	Bypassed	Bypassed	50%
Odd	Bypassed	Bypassed	50%
Even	Even ($N_{X.1} = M_{X.1}$)	Bypassed	50%
Odd	Even ($N_{X.1} = M_{X.1}$)	Bypassed	50%
Even	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	50%
Odd	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	50%
Even	Even ($N_{X.1} = M_{X.1}$)	Even ($N_{X.2} = M_{X.2}$)	50%
Odd	Even ($N_{X.1} = M_{X.1}$)	Even ($N_{X.2} = M_{X.2}$)	50%
Even	Odd ($M_{X.1} = N_{X.1} + 1$)	Even ($N_{X.2} = M_{X.2}$)	50%
Odd	Odd ($M_{X.1} = N_{X.1} + 1$)	Even ($N_{X.2} = M_{X.2}$)	50%
Even	Odd ($M_{X.1} = N_{X.1} + 1$)	Odd ($M_{X.2} = N_{X.2} + 1$)	50%
Odd	Odd ($M_{X.1} = N_{X.1} + 1$)	Odd ($M_{X.2} = N_{X.2} + 1$)	50%

Table 38. Divider 3 and Divider 4 Duty Cycle; VCO Divider Used; Duty Cycle Correction On (DCCOFF = 0); VCO Divider Input Duty Cycle = X%

VCO Divider	$D_{X.1}$ $N_{X.1} + M_{X.1} + 2$	$D_{X.2}$ $N_{X.2} + M_{X.2} + 2$	Output Duty Cycle
Even	Bypassed	Bypassed	50%
Odd = 3	Bypassed	Bypassed	(1 + X%)/3
Odd = 5	Bypassed	Bypassed	(2 + X%)/5
Even	Even ($N_{X.1} = M_{X.1}$)	Bypassed	50%
Odd	Even ($N_{X.1} = M_{X.1}$)	Bypassed	50%
Even	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	50%
Odd = 3	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	$(3N_{X.1} + 4 + X\%)/(6N_{X.1} + 9)$
Odd = 5	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	$(5N_{X.1} + 7 + X\%)/(10N_{X.1} + 15)$
Even	Even ($N_{X.1} = M_{X.1}$)	Even ($N_{X.2} = M_{X.2}$)	50%
Odd	Even ($N_{X.1} = M_{X.1}$)	Even ($N_{X.2} = M_{X.2}$)	50%
Even	Odd ($M_{X.1} = N_{X.1} + 1$)	Even ($N_{X.2} = M_{X.2}$)	50%
Odd	Odd ($M_{X.1} = N_{X.1} + 1$)	Even ($N_{X.2} = M_{X.2}$)	50%
Even	Odd ($M_{X.1} = N_{X.1} + 1$)	Odd ($M_{X.2} = N_{X.2} + 1$)	50%
Odd = 3	Odd ($M_{X.1} = N_{X.1} + 1$)	Odd ($M_{X.2} = N_{X.2} + 1$)	$(6N_{X.1}N_{X.2} + 9N_{X.1} + 9N_{X.2} + 13 + X\%)/(3(2N_{X.1} + 3)(2N_{X.2} + 3))$
Odd = 5	Odd ($M_{X.1} = N_{X.1} + 1$)	Odd ($M_{X.2} = N_{X.2} + 1$)	$(10N_{X.1}N_{X.2} + 15N_{X.1} + 15N_{X.2} + 22 + X\%)/(5(2N_{X.1} + 3)(2N_{X.2} + 3))$

Table 39. Divider 3 and Divider 4 Duty Cycle; VCO Divider Not Used; Duty Cycle Correction On (DCCOFF = 0)

Input Clock Duty Cycle	$D_{X.1}$ $N_{X.1} + M_{X.1} + 2$	$D_{X.2}$ $N_{X.2} + M_{X.2} + 2$	Output Duty Cycle
50%	Bypassed	Bypassed	50%
50%	Even ($N_{X.1} = M_{X.1}$)	Bypassed	50%
X%	Bypassed	Bypassed	X% (High)
X%	Even ($N_{X.1} = M_{X.1}$)	Bypassed	50%
50%	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	50%
X%	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	$(N_{X.1} + 1 + X\%)/(2N_{X.1} + 3)$
	Odd ($M_{X.1} = N_{X.1} + 1$)	Bypassed	$(N_{X.1} + 1 + X\%)/(2N_{X.1} + 3)$
50%	Even ($N_{X.1} = M_{X.1}$)	Even ($N_{X.2} = M_{X.2}$)	50%
X%	Even ($N_{X.1} = M_{X.1}$)	Even ($N_{X.2} = M_{X.2}$)	50%
50%	Odd ($M_{X.1} = N_{X.1} + 1$)	Even ($N_{X.2} = M_{X.2}$)	50%
X%	Odd ($M_{X.1} = N_{X.1} + 1$)	Even ($N_{X.2} = M_{X.2}$)	50%
50%	Odd ($M_{X.1} = N_{X.1} + 1$)	Odd ($M_{X.2} = N_{X.2} + 1$)	50%
X%	Odd ($M_{X.1} = N_{X.1} + 1$)	Odd ($M_{X.2} = N_{X.2} + 1$)	$(2N_{X.1}N_{X.2} + 3N_{X.1} + 3N_{X.2} + 4 + X\%)/((2N_{X.1} + 3)(2N_{X.2} + 3))$

Phase Offset or Coarse Time Delay (Divider 3 and Divider 4)

Divider 3 and Divider 4 can be set to have a phase offset or delay. The phase offset is set by a combination of the bits in the phase offset and start high registers (see Table 40).

Table 40. Setting Phase Offset and Division for Divider 3 and Divider 4

Divider		Start High (SH)	Phase Offset (PO)	Low Cycles M	High Cycles N
3	3.1	0x19C[0]	0x19A[3:0]	0x199[7:4]	0x199[3:0]
	3.2	0x19C[1]	0x19A[7:4]	0x19B[7:4]	0x19B[3:0]
4	4.1	0x1A1[0]	0x19F[3:0]	0x19E[7:4]	0x19E[3:0]
	4.2	0x1A1[1]	0x19F[7:4]	0x1A0[7:4]	0x1A0[3:0]

Note that the value stored in the register equals the number of cycles minus one. For example, 0x199[7:4] = 0001b equals two low cycles (M = 2) for Divider 3.1.

Let:
Δ_t = delay (in seconds).
$\Phi_{x.y} = 16 \times SH[0] + 8 \times PO[3] + 4 \times PO[2] + 2 \times PO[1] + 1 \times PO[0]$.
$T_{X.1}$ = period of the clock signal at the input to $D_{X.1}$ (in seconds).
$T_{X.2}$ = period of the clock signal at the input to $D_{X.2}$ (in seconds).

Case 1

When $\Phi_{x.1} \le 15$ and $\Phi_{x.2} \le 15$:
$\Delta_t = \Phi_{x.1} \times T_{X.1} + \Phi_{X.2} \times T_{x.2}$

Case 2

When $\Phi_{x.1} \le 15$ and $\Phi_{x.2} \ge 16$:
$\Delta_t = \Phi_{X.1} \times T_{X.1} + (\Phi_{X.2} - 16 + M_{X.2} + 1) \times T_{X.2}$

Case 3

When $\Phi_{X.1} \ge 16$ and $\Phi_{X.2} \le 15$:
$\Delta_t = (\Phi_{X.1} - 16 + M_{X.1} + 1) \times T_{X.1} + \Phi_{X.2} \times T_{X.2}$

Case 4

When $\Phi_{X.1} \ge 16$ and $\Phi_{X.2} \ge 16$:
$\Delta_t =$
$(\Phi_{X.1} - 16 + M_{X.1} + 1) \times T_{X.1} + (\Phi_{X.2} - 16 + M_{X.2} + 1) \times T_{X.2}$

Fine Delay Adjust (Divider 3 and Divider 4)

Each AD9516 LVDS/CMOS output (OUT6 to OUT9) includes an analog delay element that can be programmed to give variable time delays (Δ_t) in the clock signal at that output.

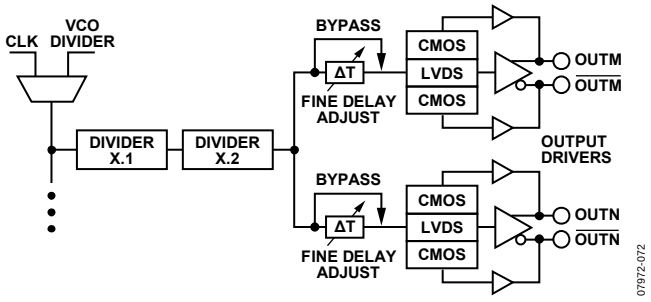

Figure 43. Fine Delay (OUT6 to OUT9)

The amount of delay applied to the clock signal is determined by programming four registers per output (see Table 41).

Table 41. Setting Analog Fine Delays

OUTPUT (LVDS/CMOS)	Ramp Capacitors	Ramp Current	Delay Fraction	Delay Bypass
OUT6	0x0A1[5:3]	0x0A1[2:0]	0x0A2[5:0]	0x0A0[0]
OUT7	0x0A4[5:3]	0x0A4[2:0]	0x0A5[5:0]	0x0A3[0]
OUT8	0x0A7[5:3]	0x0A7[2:0]	0x0A8[5:0]	0x0A6[0]
OUT9	0x0AA[5:3]	0x0AA[2:0]	0x0AB[5:0]	0x0A9[0]

Calculating the Fine Delay

The following values and equations are used to calculate the delay of the delay block.

I_{RAMP} (µA) = 200 × (*Ramp Current* + 1)

Number of Capacitors = *Number of Bits* = 0 in *Ramp Capacitor*s + 1

Example: 101 = 1 + 1 = 2; 110 = 1 + 1 = 2; 100 = 2 + 1 = 3; 001 = 2 + 1 = 3; 111 = 0 + 1 = 1.

Delay Range (ns) = 200 × ((*No. of Caps* + 3)/(I_{RAMP})) × 1.3286

$$Offset\ (\text{ns}) = 0.34 + \left(1600 - I_{RAMP}\right) \times 10^{-4} + \left(\frac{No.\ of\ Caps - 1}{I_{RAMP}}\right) \times 6$$

Delay Full Scale (ns) = *Delay Range* + *Offset*

Fine Delay (ns) = *Delay Range* × *Delay Fraction* × (1/63) + *Offset*

Note that only delay fraction values up to 47 decimal (101111b; 0x02F) are supported.

In no case can the fine delay exceed one-half of the output clock period. If a delay longer than half of the clock period is attempted, the output stops clocking.

The delay function adds some jitter greater than that specified for the nondelayed output. This means that the delay function should be used primarily for clocking digital chips, such as FPGA, ASIC, DUC, and DDC. An output with this delay enabled may not be suitable for clocking data converters. The jitter is higher for long full scales because the delay block uses a ramp and trip points to create the variable delay. A slower ramp time produces more time jitter.

Synchronizing the Outputs—SYNC Function

The AD9516 clock outputs can be synchronized to each other. Outputs can be individually excluded from synchronization. Synchronization consists of setting the nonexcluded outputs to a preset set of static conditions and subsequently releasing these outputs to continue clocking at the same instant with the preset conditions applied. This allows for the alignment of the edges of two or more outputs or for the spacing of edges according to the coarse phase offset settings for two or more outputs.

Synchronization of the outputs is executed in several ways:

- The $\overline{\text{SYNC}}$ pin is forced low and then released (manual sync).
- By setting and then resetting any one of the following three bits: the soft SYNC bit (0x230[0]), the soft reset bit (0x000[5] [mirrored]), and the power-down distribution reference bit (0x230[1]).
- Synchronization of the outputs can be executed as part of the chip power-up sequence.
- The $\overline{\text{RESET}}$ pin is forced low and then released (chip reset).
- The $\overline{\text{PD}}$ pin is forced low and then released (chip power-down).

The most common way to execute the SYNC function is to use the $\overline{\text{SYNC}}$ pin to do a manual synchronization of the outputs. This requires a low going signal on the $\overline{\text{SYNC}}$ pin, which is held low and then released when synchronization is desired. The timing of the SYNC operation is shown in Figure 44 (using VCO divider) and Figure 45 (VCO divider not used). There is an uncertainty of up to one cycle of the clock at the input to the channel divider due to the asynchronous nature of the SYNC signal with respect to the clock edges inside the AD9516. The delay from the $\overline{\text{SYNC}}$ rising edge to the beginning of synchronized output clocking is between 14 and 15 cycles of clock at the channel divider input, plus either one cycle of the VCO divider input (see Figure 44), or one cycle of the CLK input (see Figure 45), depending on whether the VCO divider is used. Cycles are counted from the rising edge of the signal.

Another common way to execute the SYNC function is by setting and resetting the soft SYNC bit at 0x230[0] (see Table 47 through Table 57 for details). Both setting and resetting of the soft SYNC bit require an update all registers (0x232[0] = 1) operation to take effect.

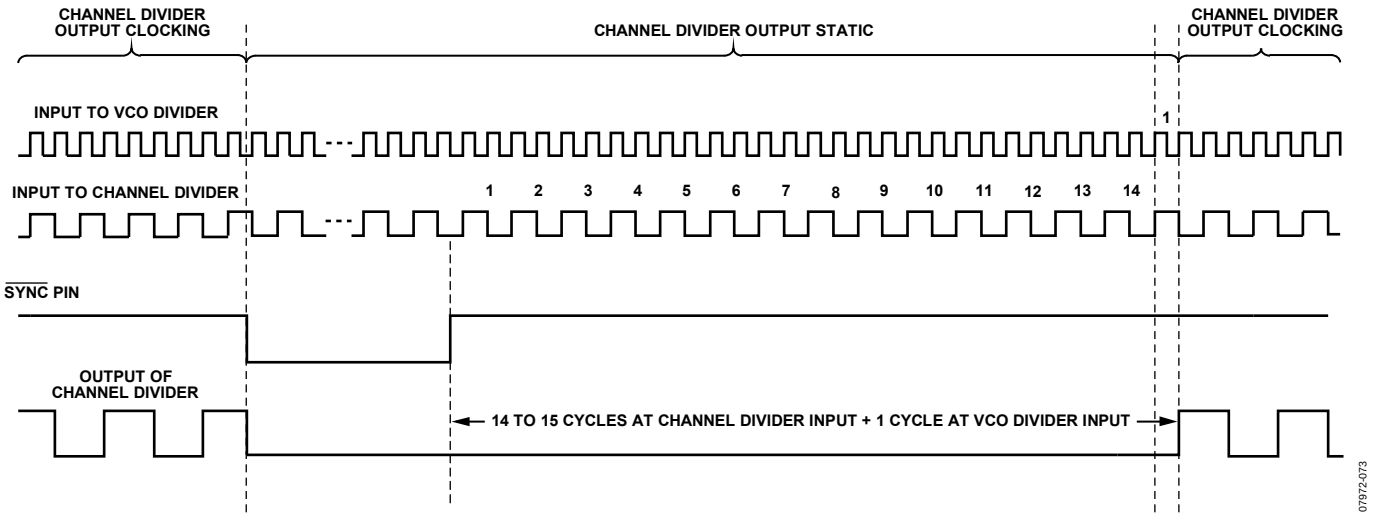

Figure 44. SYNC Timing when VCO Divider Is Used—CLK or VCO Is Input

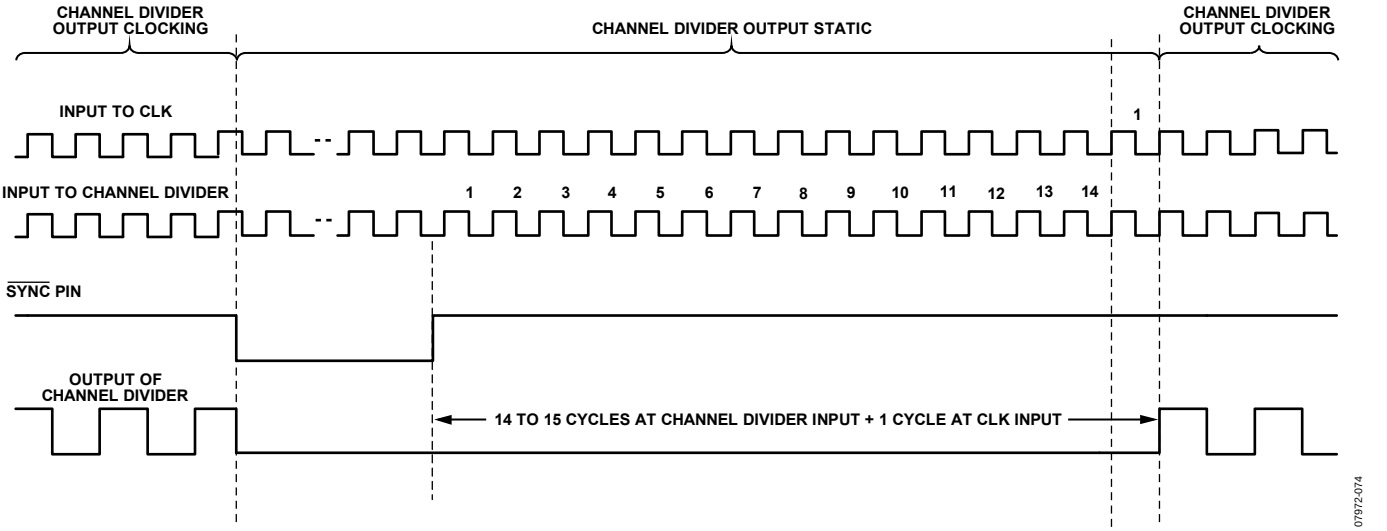

Figure 45. SYNC Timing when VCO Divider Is Not Used—CLK Input Only

A SYNC operation brings all outputs that have not been excluded (by the nosync bit) to a preset condition before allowing the outputs to begin clocking in synchronicity. The preset condition takes into account the settings in each of the channel's start high bit and its phase offset. These settings govern both the static state of each output when the SYNC operation is happening and the state and relative phase of the outputs when they begin clocking again upon completion of the SYNC operation. Between outputs and after synchronization, this allows for the setting of phase offsets.

The AD9516 outputs are in pairs, sharing a channel divider per pair (two pairs of pairs, four outputs, in the case of CMOS). The synchronization conditions apply to both outputs of a pair.

Each channel (a divider and its outputs) can be excluded from any SYNC operation by setting the nosync bit of the channel. Channels that are set to ignore SYNC (excluded channels) do not set their outputs static during a SYNC operation, and their outputs are not synchronized with those of the nonexcluded channels.

Clock Outputs

The AD9516 offers three output level choices: LVPECL, LVDS, and CMOS. OUT0 to OUT5 are LVPECL differential outputs; and OUT6 to OUT9 are LVDS/CMOS outputs. These outputs can be configured as either LVDS differential or as pairs of single-ended CMOS outputs.

LVPECL Outputs: OUT0 to OUT5

The LVPECL differential voltage (V_{OD}) is selectable (from 400 mV to 960 mV, see 0x0F0:5[3:2]. The LVPECL outputs have dedicated pins for power supply (VS_LVPECL), allowing a separate power supply to be used. VS_LVPECL can be from 2.5 V to 3.3 V.

The LVPECL output polarity can be set as noninverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without requiring a board layout change. Each LVPECL output can be powered down or powered up as needed. Because of the architecture of the LVPECL output stages, there is the possibility of electrical overstress and breakdown under certain power-down conditions.

For this reason, the LVPECL outputs have several power-down modes. This includes a safe power-down mode that continues to protect the output devices while powered down, although it consumes somewhat more power than a total power-down. If the LVPECL output pins are terminated, it is best to select the safe power-down mode. If the pins are not connected (unused), it is acceptable to use the total power-down mode.

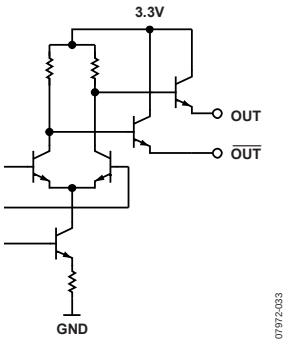

Figure 46. LVPECL Output Simplified Equivalent Circuit

LVDS/CMOS Outputs: OUT6 to OUT9

OUT6 to OUT9 can be configured as either an LVDS differential output or as a pair of CMOS single-ended outputs. The LVDS outputs allow for selectable output current from ~1.75 mA to ~7 mA.

The LVDS output polarity can be set as noninverting or inverting, which allows for the adjustment of the relative polarity of outputs within an application without requiring a board layout change. Each LVDS output can be powered down if not needed to save power.

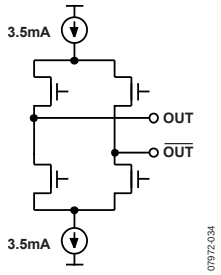

Figure 47. LVDS Output Simplified Equivalent Circuit with 3.5 mA Typical Current Source

OUT6 to OUT9 can also be CMOS outputs. Each LVDS output can be configured to be two CMOS outputs. This provides for up to eight CMOS outputs: OUT6A, OUT6B, OUT7A, OUT7B, OUT8A, OUT8B, OUT9A, and OUT9B. When an output is configured as CMOS, the CMOS Output A is automatically turned on. The CMOS Output B can be turned on or off independently. The relative polarity of the CMOS outputs can also be selected for any combination of inverting and noninverting. See Table 52, 0x140[7:5], 0x141[7:5], 0x142[7:5], and 0x143[7:5].

Each LVDS/CMOS output can be powered down as needed to save power. The CMOS output power-down is controlled by the same bit that controls the LVDS power-down for that output. This power-down control affects both the CMOS A and CMOS B outputs. However, when the CMOS A output is powered up, the CMOS B output can be powered on or off separately.

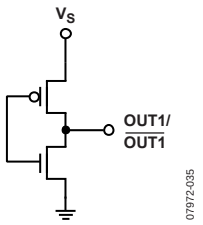

Figure 48. CMOS Equivalent Output Circuit

RESET MODES

The AD9516 has several ways to force the chip into a reset condition that restores all registers to their default values and makes these settings active.

Power-On Reset—Start-Up Conditions When VS Is Applied

A power-on reset (POR) is issued when the VS power supply is turned on. The POR pulse duration is <100 ms and initializes the chip to the power-on conditions that are determined by the default register settings. These are indicated in the Default Value (Hex) column of Table 47. At power-on, the AD9516 also executes a SYNC operation, which brings the outputs into phase alignment according to the default settings. It is recommended that the user not toggle SCLK during the reset pulse.

Asynchronous Reset via the $\overline{\text{RESET}}$ Pin

An asynchronous hard reset is executed by momentarily pulling $\overline{\text{RESET}}$ low. A reset restores the chip registers to the default settings. It is recommended that the user not toggle SCLK for 20 ns after $\overline{\text{RESET}}$ goes high.

Soft Reset via 0x000[5]

A soft reset is executed by writing 0x000[5] and 0x000[2] = 1b. This bit is not self-clearing; therefore, it must be cleared by writing 0x000[5] and 0x000[2] = 0b to reset it and complete the soft reset operation. A soft reset restores the default values to the internal registers. The soft reset bit does not require an update registers command (0x232 = 0x01) to be issued.

POWER-DOWN MODES

Chip Power-Down via $\overline{\text{PD}}$

The AD9516 can be put into a power-down condition by pulling the $\overline{\text{PD}}$ pin low. Power-down turns off most of the functions and currents inside the AD9516. The chip remains in this power-down state until $\overline{\text{PD}}$ is brought back to logic high. When woken up, the AD9516 returns to the settings programmed into its registers prior to the power-down, unless the registers are changed by new programming while the $\overline{\text{PD}}$ pin is held low.

The $\overline{\text{PD}}$ power-down shuts down the currents on the chip, except the bias current necessary to maintain the LVPECL outputs in a safe shutdown mode. This is needed to protect the LVPECL output circuitry from damage that can be caused by certain termination and load configurations when tristated. Because this is not a complete power-down, it can be called sleep mode.

When the AD9516 is in a $\overline{PD}$ power-down, the chip is in the following state:

- The PLL is off (asynchronous power-down).
- The CLK input buffer is off.
- All dividers are off.
- All LVDS/CMOS outputs are off.
- All LVPECL outputs are in safe off mode.
- The serial port is active and responds to commands.

If the AD9516 clock outputs must be synchronized to each other, a SYNC is required upon exiting power-down (see the Synchronizing the Outputs—SYNC Function section).

PLL Power-Down

The PLL section of the AD9516 can be selectively powered down. There are three PLL operating modes set by 0x010[1:0], as shown in Table 49.

In asynchronous power-down mode, the device powers down as soon as the registers are updated.

In synchronous power-down mode, the PLL power-down is gated by the charge pump to prevent unwanted frequency jumps. The device goes into power-down on the occurrence of the next charge pump event after the registers are updated.

Distribution Power-Down

The distribution section can be powered down by writing 0x230[1] = 1b. This turns off the bias to the distribution section. If the LVPECL power-down mode is normal operation (00b), it is possible for a low impedance load on that LVPECL output to draw significant current during this power-down. If the LVPECL power-down mode is set to 11b, the LVPECL output is not protected from reverse bias and can be damaged under certain termination conditions.

Individual Clock Output Power-Down

Any of the clock distribution outputs can be powered down individually by writing to the appropriate registers. The register map details the individual power-down settings for each output. The LVDS/CMOS outputs can be powered down, regardless of their output load configuration.

The LVPECL outputs have multiple power-down modes (see Table 53) that give some flexibility in dealing with the various output termination conditions. When the mode is set to 10b, the LVPECL output is protected from reverse bias to 2 VBE + 1 V. If the mode is set to 11b, the LVPECL output is not protected from reverse bias and can be damaged under certain termination conditions. This setting also affects the operation when the distribution block is powered down with 0x230[1] = 1b (see the Distribution Power-Down section).

Individual Circuit Block Power-Down

Other AD9516 circuit blocks (such as CLK, REF1, and REF2) can be powered down individually. This gives flexibility in configuring the part for power savings whenever certain chip functions are not needed.

SERIAL CONTROL PORT

The AD9516 serial control port is a flexible, synchronous, serial communications port that allows an easy interface with many industry-standard microcontrollers and microprocessors. The AD9516 serial control port is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR® protocols. The serial control port allows read/write access to all registers that configure the AD9516. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9516 serial control port can be configured for a single bidirectional I/O pin (SDIO only) or for two unidirectional I/O pins (SDIO/SDO). By default, the AD9516 is in bidirectional mode, long instruction (long instruction is the only instruction mode supported).

SERIAL CONTROL PORT PIN DESCRIPTIONS

SCLK (serial clock) is the serial shift clock. This pin is an input. SCLK is used to synchronize serial control port reads and writes. Write data bits are registered on the rising edge of this clock, and read data bits are registered on the falling edge. This pin is internally pulled down by a 30 kΩ resistor to ground.

SDIO (serial data input/output) is a dual-purpose pin and acts as an input only (unidirectional mode) or as both an input/output (bidirectional mode). The AD9516 defaults to the bidirectional I/O mode (0x000[7] = 0).

SDO (serial data output) is used only in the unidirectional I/O mode (0x000[7]) as a separate output pin for reading back data.

$\overline{CS}$ (chip select bar) is an active low control that gates the read and write cycles. When $\overline{CS}$ is high, SDO and SDIO are in a high impedance state. This pin is internally pulled up by a 30 kΩ resistor to VS.

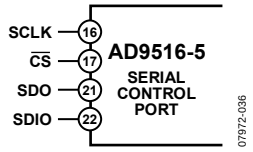

Figure 49. Serial Control Port

GENERAL OPERATION OF SERIAL CONTROL PORT

A write or a read operation to the AD9516 is initiated by pulling $\overline{CS}$ low.

$\overline{CS}$ stall high is supported in modes where three or fewer bytes of data (plus instruction data) are transferred (see Table 42). In these modes, $\overline{CS}$ can temporarily return high on any byte boundary, allowing time for the system controller to process the next byte. $\overline{CS}$ can go high on byte boundaries only and during either part (instruction or data) of the transfer.

During this period, the serial control port state machine enters a wait state until all data is sent. If the system controller decides to abort the transfer before all of the data is sent, the state machine must be reset by either completing the remaining transfers or by returning the $\overline{CS}$ low for at least one complete SCLK cycle (but less than eight SCLK cycles). Raising the $\overline{CS}$ on a nonbyte boundary terminates the serial transfer and flushes the buffer.

In streaming mode (see Table 42), any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented (see the MSB/LSB First Transfers section). $\overline{CS}$ must be raised at the end of the last byte to be transferred, thereby ending the stream mode.

Communication Cycle—Instruction Plus Data

There are two parts to a communication cycle with the AD9516. The first writes a 16-bit instruction word into the AD9516, coincident with the first 16 SCLK rising edges. The instruction word provides the AD9516 serial control port with information regarding the data transfer, which is the second part of the communication cycle. The instruction word defines whether the upcoming data transfer is a read or a write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer.

Write

If the instruction word is for a write operation, the second part is the transfer of data into the serial control port buffer of the AD9516. Data bits are registered on the rising edge of SCLK.

The length of the transfer (1, 2, or 3 bytes or streaming mode) is indicated by two bits (W1:W0) in the instruction byte. When the transfer is 1, 2, or 3 bytes, but not streaming, $\overline{CS}$ can be raised after each sequence of eight bits to stall the bus (except after the last byte, where it ends the cycle). When the bus is stalled, the serial transfer resumes when $\overline{CS}$ is lowered. Raising $\overline{CS}$ on a nonbyte boundary resets the serial control port. During a write, streaming mode does not skip over reserved or unused registers; therefore, the user must know what bit pattern to write to the reserved registers to preserve proper operation of the part. It does not matter what data is written to unused registers.

Because data is written into a serial control port buffer area, not directly into the actual control registers of the AD9516, an additional operation is needed to transfer the serial control port buffer contents to the actual control registers of the AD9516, thereby causing them to become active. The update registers operation consists of setting 0x232[0] = 1b (this bit is self-clearing). Any number of bytes of data can be changed before executing an update registers. The update registers simultaneously actuates all register changes that have been written to the buffer since any previous update.

Read

If the instruction word is for a read operation, the next N × 8 SCLK cycles clock out the data from the address specified in the instruction word, where N is 1 to 3 as determined by W1:W0. If N = 4, the read operation is in streaming mode, continuing until $\overline{CS}$ is raised. Streaming mode does not skip over reserved or blank registers. The readback data is valid on the falling edge of SCLK.

The default mode of the AD9516 serial control port is the bidirectional mode. In bidirectional mode, both the sent data and the readback data appear on the SDIO pin. It is also possible to set the AD9516 to unidirectional mode (SDO enable register, 0x000[7]). In unidirectional mode, the readback data appears on the SDO pin.

A readback request reads the data that is in the serial control port buffer area, or the data in the active registers (see Figure 50). Readback of the buffer or active registers is controlled by 0x004[0].

The AD9516 supports only the long instruction mode; therefore, 0x000[4:3] must be set to 11b (this register uses mirrored bits). Long instruction mode is the default at power-up or reset.

The AD9516 uses Register Address 0x000 to Register Address 0x232.

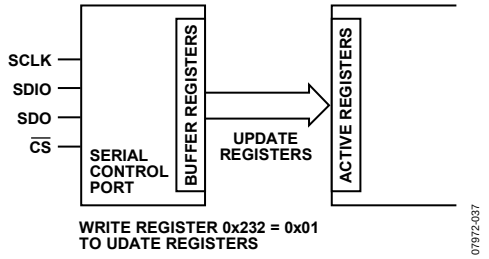

Figure 50. Relationship Between Serial Control Port Buffer Registers and Active Registers of the AD9516

INSTRUCTION WORD (16 BITS)

The MSB of the instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next two bits [W1:W0] indicate the length of the transfer in bytes. The final 13 bits are the address [A12:A0] at which to begin the read or write operation.

For a write, the instruction word is followed by the number of bytes of data indicated by Bits[W1:W0], see Table 42.

Table 42. Byte Transfer Count

W1	W0	Bytes to Transfer
0	0	1
0	1	2
1	0	3
1	1	Streaming mode

Bits[A12:A0] select the address within the register map that is written to or read from during the data transfer portion of the communications cycle. Only Bits[A9:A0] are needed to cover the range of the 0x232 registers used by the AD9516. Bits[A12:A10] must always be 0b. For multibyte transfers, this address is the starting byte address. In MSB first mode, subsequent bytes increment the address.

MSB/LSB FIRST TRANSFERS

The AD9516 instruction word and byte data can be MSB first or LSB first. Any data written to 0x000 must be mirrored; the upper four bits ([7:4]) must mirror the lower four bits ([3:0]). This makes it irrelevant whether LSB first or MSB first is in effect. As an example of this mirroring, see the default setting for this register: 0x000, which mirrors Bit 4 and Bit 3. This sets the long instruction mode (default, and is the only mode supported).

The default for the AD9516 is MSB first.

When LSB first is set by 0x000[1] and 0x000[6], it takes effect immediately, because it only affects the operation of the serial control port and does not require that an update be executed.

When MSB first mode is active, the instruction and data bytes must be written from MSB to LSB. Multibyte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes must follow in order from the high address to the low address. In MSB first mode, the serial control port internal address generator decrements for each data byte of the multibyte transfer cycle.

When LSB first is active, the instruction and data bytes must be written from LSB to MSB. Multibyte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The internal byte address generator of the serial control port increments for each byte of the multibyte transfer cycle.

The AD9516 serial control port register address decrements from the register address just written toward 0x000 for multibyte I/O operations if the MSB first mode is active (default). If the LSB first mode is active, the register address of the serial control port increments from the address just written toward 0x232 for multibyte I/O operations.

Streaming mode always terminates when it hits Address 0x232. Note that unused addresses are not skipped during multibyte I/O operations.

Table 43. Streaming Mode (No Addresses Are Skipped)

Write Mode	Address Direction	Stop Sequence
LSB first	Increment	0x230, 0x231, 0x232, stop
MSB first	Decrement	0x001, 0x000, 0x232, stop

Table 44. Serial Control Port, 16-Bit Instruction Word, MSB First

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	W1	W0	A12 = 0	A11 = 0	A10 = 0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

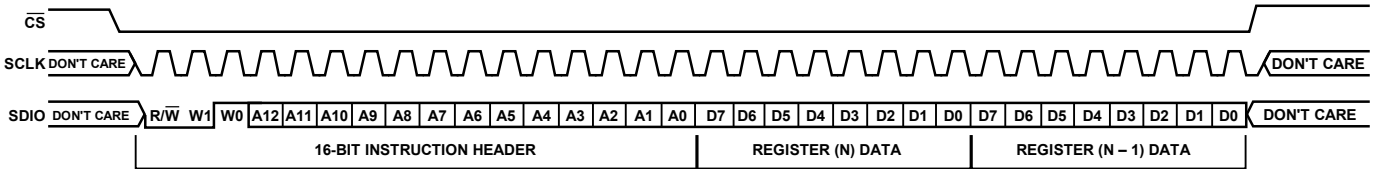

Figure 51. Serial Control Port Write—MSB First, 16-Bit Instruction, Two Bytes of Data

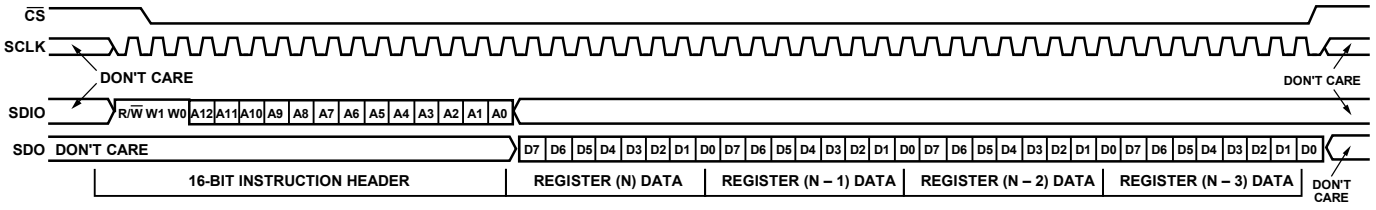

Figure 52. Serial Control Port Read—MSB First, 16-Bit Instruction, Four Bytes of Data

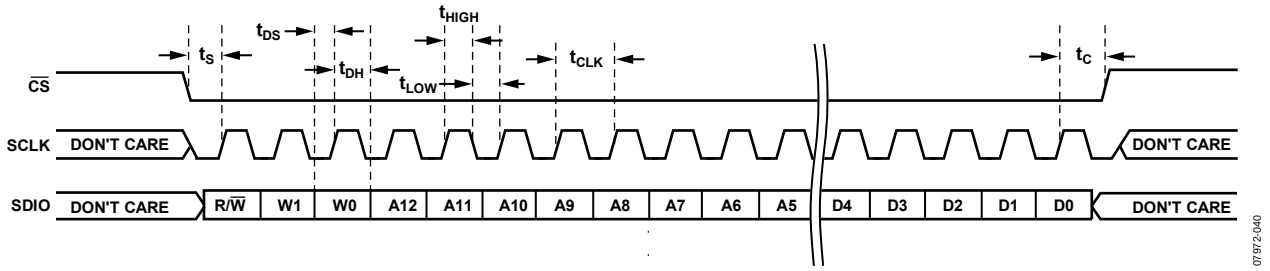

Figure 53. Serial Control Port Write—MSB First, 16-Bit Instruction, Timing Measurements

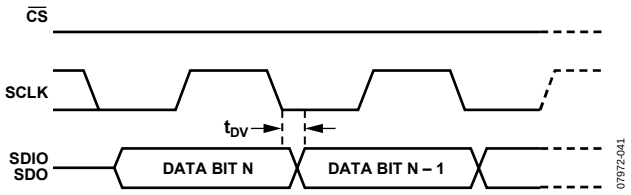

Figure 54. Timing Diagram for Serial Control Port Register Read

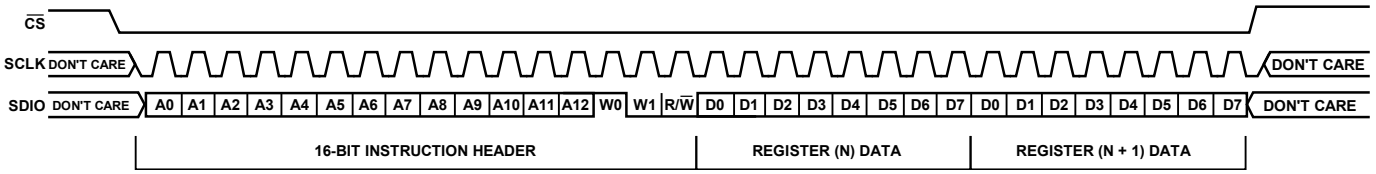

Figure 55. Serial Control Port Write—LSB First, 16-Bit Instruction, Two Bytes of Data

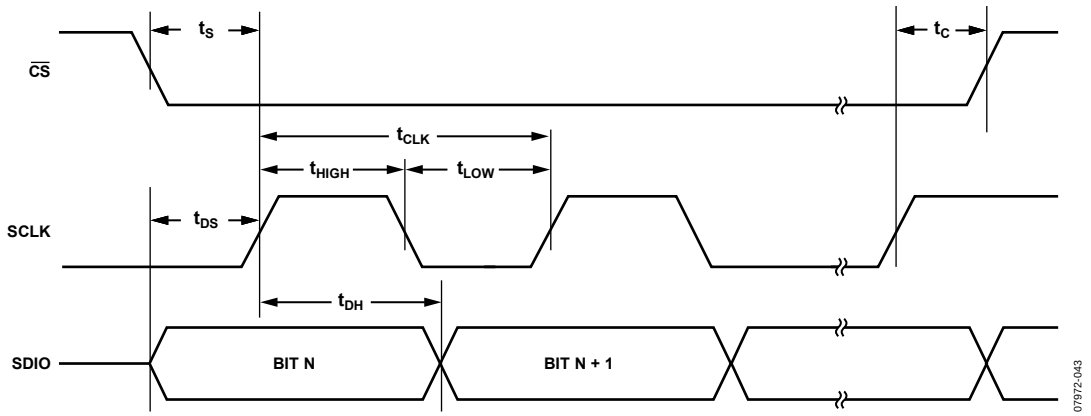

Figure 56. Serial Control Port Timing—Write

Table 45. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and the rising edge of SCLK
t_{DH}	Hold time between data and the rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of communication cycle)
t_C	Setup time between the SCLK rising edge and the $\overline{CS}$ rising edge (end of communication cycle)
t_{HIGH}	Minimum period that SCLK should be in a logic high state
t_{LOW}	Minimum period that SCLK should be in a logic low state
t_{DV}	SCLK to valid SDIO and SDO (see Figure 54)

THERMAL PERFORMANCE

Table 46. Thermal Parameters for 64-Lead LFCSP

Symbol	Thermal Characteristic Using a JEDEC JESD51-7 Plus JEDEC JESD51-5 2S2P Test Board	Value (°C/W)
θ_{JA}	Junction-to-ambient thermal resistance, 0.0 m/sec airflow per JEDEC JESD51-2 (still air)	22.0
θ_{JMA}	Junction-to-ambient thermal resistance, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air)	19.2
θ_{JMA}	Junction-to-ambient thermal resistance, 2.0 m/sec airflow per JEDEC JESD51-6 (moving air)	17.2
Ψ_{JB}	Junction-to-board characterization parameter, 1.0 m/sec airflow per JEDEC JESD51-6 (moving air) and JEDEC JESD51-8	11.6
θ_{JC}	Junction-to-case thermal resistance (die-to-heat sink) per MIL-Std 883, Method 1012.1	1.3
Ψ_{JT}	Junction-to-top-of-package characterization parameter, 0 m/sec airflow per JEDEC JESD51-2 (still air)	0.1

The AD9516 is specified for a case temperature (T_{CASE}). To ensure that T_{CASE} is not exceeded, an airflow source can be used.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured by the user at the top center of the package.
Ψ_{JT} is the value from Table 46.
PD is the power dissipation (see the total power dissipation in Table 14.)

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of Ψ_{JB} are provided for package comparison and PCB design considerations.

REGISTER MAP OVERVIEW

Register addresses that are not listed in Table 47 (as well as ones marked unused) are not used and writing to those registers has no effect. The user should only write the default value to the register addresses marked reserved.

Table 47. Register Map Overview

Addr (Hex)	Parameter	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
Serial Port Configuration										
000	Serial port configuration	SDO active	LSB first	Soft reset	Long instruction	Long instruction	Soft reset	LSB first	SDO active	18
001	Unused									
002 to 003	Reserved (Read-only)									
004	Read back control	Unused							Read back active registers	00
PLL										
010	PFD and charge pump	PFD polarity	Charge pump current			Charge pump mode		PLL power-down		7D
011	R Counter	14-Bit R Divider Bits[7:0] (LSB)								01
012		Unused		14-Bit R Divider Bits[13:8] (MSB)						00
013	A counter	Unused		6-Bit A counter						00
014	B counter	13-Bit B Counter Bits[7:0] (LSB)								03
015		Unused			13-Bit B Counter Bits[12:8] (MSB)					00
016	PLL Control 1	Set CP pin to VCP/2	Reset R counter	Reset A and B counters	Reset all counters	B counter bypass	Prescaler P			06
017	PLL Control 2	STATUS pin control						Antibacklash pulse width		00
018	PLL Control 3	Unused	Lock detect counter		Digital lock detect window	Disable digital lock detect	Reserved			06
019	PLL Control 4	R, A, B counters $\overline{\text{SYNC}}$ pin reset		R path delay			N path delay			00
01A	PLL Control 5	Unused	Reference frequency monitor threshold	LD pin control						00
01B	PLL Control 6	CLK frequency monitor	REF2 ($\overline{\text{REFIN}}$) frequency monitor	REF1 (REFIN) frequency monitor	REFMON pin control					00
01C	PLL Control 7	Disable switchover deglitch	Select REF2	Use REF_SEL pin	Automatic reference switchover	Stay on REF2	REF2 power on	REF1 power on	Differential reference	00
01D	PLL Control 8	Unused			PLL status register disable	LD pin comparator enable	Holdover enable	External holdover control	Holdover enable	00
01E	PLL Control 9	Unused								00
01F	PLL Readback (read-only)	Unused		Holdover active	REF2 selected	CLK frequency > threshold	REF2 frequency > threshold	REF1 frequency > threshold	Digital lock detect	--
020 to 04F	Unused									

Addr (Hex)	Parameter	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
Fine Delay Adjust: OUT6 to OUT9										
0A0	OUT6 delay bypass	Unused							OUT6 delay bypass	01
0A1	OUT6 delay full-scale	Unused		OUT6 ramp capacitors			OUT6 ramp current			00
0A2	OUT6 delay fraction	Unused		OUT6 delay fraction						00
0A3	OUT7 delay bypass	Unused							OUT7 delay bypass	01
0A4	OUT7 delay full-scale	Unused		OUT7 ramp capacitors			OUT7 ramp current			00
0A5	OUT7 delay fraction	Unused		OUT7 delay fraction						00
0A6	OUT8 delay bypass	Unused							OUT8 delay bypass	01
0A7	OUT8 delay full-scale	Unused		OUT8 ramp capacitors			OUT8 ramp current			00
0A8	OUT8 delay fraction	Unused		OUT8 delay fraction						00
0A9	OUT9 delay bypass	Unused							OUT9 delay bypass	01
0AA	OUT9 delay full-scale	Unused		OUT9 ramp capacitors			OUT9 ramp current			00
0AB	OUT9 delay fraction	Unused		OUT9 delay fraction						00
0AC to 0EF	Unused									
LVPECL Outputs										
0F0	OUT0	Unused			OUT0 invert	OUT0 LVPECL differential voltage		OUT0 power-down		08
0F1	OUT1	Unused			OUT1 invert	OUT1 LVPECL differential voltage		OUT1 power-down		A
0F2	OUT2	Unused			OUT2 invert	OUT2 LVPECL differential voltage		OUT2 power-down		08
0F3	OUT3	Unused			OUT3 invert	OUT3 LVPECL differential voltage		OUT3 power-down		0A
0F4	OUT4	Unused			OUT4 invert	OUT4 LVPECL differential voltage		OUT4 power-down		08
0F5	OUT5	Unused			OUT5 invert	OUT5 LVPECL differential voltage		OUT5 power-down		0A
0F6 to 13F	Unused									
LVDS/CMOS Outputs										
140	OUT6	OUT6 CMOS output polarity			OUT6 CMOS B	OUT6 select LVDS/CMOS	OUT6 LVDS output current		OUT6 power-down	42
141	OUT7	OUT7 CMOS output polarity			OUT7 CMOS B	OUT7 select LVDS/CMOS	OUT7 LVDS output current		OUT7 power-down	43
142	OUT8	OUT8 CMOS output polarity			OUT8 CMOS B	OUT8 select LVDS/CMOS	OUT8 LVDS output current		OUT8 power-down	42
143	OUT9	OUT9 CMOS output polarity			OUT9 CMOS B	OUT9 select LVDS/CMOS	OUT9 LVDS output current		OUT9 power-down	43
144 to 18F	Unused									

Addr (Hex)	Parameter	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
LVPECL Channel Dividers										
190	Divider 0 (PECL)	Divider 0 low cycles				Divider 0 high cycles				00
191		Divider 0 bypass	Divider 0 nosync	Divider 0 force high	Divider 0 start high	Divider 0 phase offset				80
192		Unused						Divider 0 direct to output	Divider 0 DCCOFF	00
193	Divider 1 (PECL)	Divider 1 low cycles				Divider 1 high cycles				BB
194		Divider 1 bypass	Divider 1 nosync	Divider 1 force high	Divider 1 start high	Divider 1 phase offset				00
195		Unused						Divider 1 direct to output	Divider 1 DCCOFF	00
196	Divider 2 (PECL)	Divider 2 low cycles				Divider 2 high cycles				00
197		Divider 2 bypass	Divider 2 nosync	Divider 2 force high	Divider 2 start high	Divider 2 phase offset				00
198		Unused						Divider 2 direct to output	Divider 2 DCCOFF	00
LVDS/CMOS Channel Dividers										
199	Divider 3 (LVDS/CMOS)	Low Cycles Divider 3.1				High Cycles Divider 3.1				22
19A		Phase Offset Divider 3.2				Phase Offset Divider 3.1				00
19B		Low Cycles Divider 3.2				High Cycles Divider 3.2				11
19C		Reserved		Bypass Divider 3.2	Bypass Divider 3.1	Divider 3 nosync	Divider 3 force high	Start High Divider 3.2	Start High Divider 3.1	00
19D		Unused							Divider 3 DCCOFF	00
19E	Divider 4 (LVDS/CMOS)	Low Cycles Divider 4.1				High Cycles Divider 4.1				22
19F		Phase Offset Divider 4.2				Phase Offset Divider 4.1				00
1A0		Low Cycles Divider 4.2				High Cycles Divider 4.2				11
1A1		Reserved		Bypass Divider 4.2	Bypass Divider 4.1	Divider 4 nosync	Divider 4 force high	Start High Divider 4.2	Start High Divider 4.1	00
1A2		Unused							Divider 4 DCCOFF	00
1A3	Reserved (read-only)									
1A4 to 1DF	Unused									
VCO Divider and CLK Input										
1E0	VCO divider	Unused					VCO divider			02
1E1	Input CLKs	Reserved			Power-down clock input section	Reserved			Bypass VCO divider	00
1E2 to 22A	Unused									

Addr (Hex)	Parameter	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)
System										
230	Power-down and SYNC	Reserved					Power-down SYNC	Power-down distribution reference	Soft SYNC	00
231		Unused								00
Update All Registers										
232	Update all registers	Unused							Update all registers (self-clearing bit)	00

REGISTER MAP DESCRIPTIONS

Table 48 through Table 57 provide a detailed description of each of the control register functions. The registers are listed by hexadecimal address. Reference to a specific bit or range of bits within a register is indicated by the brackets. For example, [3] refers to Bit 3, and [5:2] refers to the range of bits from Bit 5 through Bit 2.

Table 48. Serial Port Configuration

Reg. Addr (Hex)	Bit(s)	Name	Description
000	[7]	SDO active	Selects unidirectional or bidirectional data transfer mode. [7] = 0; SDIO pin used for write and read; SDO set high impedance; bidirectional mode (default). [7] = 1; SDO used for read; SDIO used for write; unidirectional mode.
000	[6]	LSB first	MSB or LSB data orientation. [6] = 0; data-oriented MSB first; addressing decrements (default). [6] = 1; data-oriented LSB first; addressing increments.
000	[5]	Soft reset	Soft reset. [5] = 1 (not self-clearing). Soft reset; restores default values to internal registers. Not self-clearing. Must be cleared to 0b to complete reset operation.
000	[4]	Long instruction	Short/long instruction mode (this part uses long instruction mode only, so this bit should always be = 1). [4] = 0; 8-bit instruction (short). [4] = 1; 16-bit instruction (long) (default).
000	[3:0]	Mirror [7:4]	Bits[3:0] should always mirror [7:4] so that it does not matter whether the part is in MSB or LSB first mode (see Register 0x000[6]). User should set bits as follows: [0] = [7]. [1] = [6]. [2] = [5]. [3] = [4].
004	[0]	Read back active registers	Select register bank used for a readback. [0] = 0; read back buffer registers (default). [0] = 1; read back active registers.

Table 49. PLL

Reg. Addr (Hex)	Bit(s)	Name	Description
010	[7]	PFD polarity	Sets the PFD polarity. [7] = 0; positive (higher control voltage produces higher frequency) (default). [7] = 1; negative (higher control voltage produces lower frequency).
010	[6:4]	CP current	Charge pump current (with CPRSET = 5.1 kΩ).

[6]	[5]	[4]	I_{CP} (mA)
0	0	0	0.6
0	0	1	1.2
0	1	0	1.8
0	1	1	2.4
1	0	0	3.0
1	0	1	3.6
1	1	0	4.2
1	1	1	4.8 (default)

010	[3:2]	CP mode	Charge pump operating mode.

[3]	[2]	Charge Pump Mode
0	0	High impedance state.
0	1	Force source current (pump up).
1	0	Force sink current (pump down).
1	1	Normal operation (default).

010	[1:0]	PLL power-down	PLL operating mode.

[1]	[0]	Mode
0	0	Normal operation.
0	1	Asynchronous power-down (default).
1	0	Normal operation.
1	1	Synchronous power-down.

Reg. Addr (Hex)	Bit(s)	Name	Description
011	[7:0]	14-Bit R Divider Bits[7:0] (LSB)	R divider LSBs—lower eight bits (default: 0x01).
012	[5:0]	14-Bit R Divider Bits[13:8] (MSB)	R divider MSBs—upper six bits (default: 0x00).
013	[5:0]	6-Bit A counter	A counter (part of N divider) (default: 0x00).
014	[7:0]	13-Bit B Counter Bits[7:0] (LSB)	B counter (part of N divider)—lower eight bits (default: 0x00).
015	[4:0]	13-Bit B Counter Bits[12:8] (MSB)	B counter (part of N divider)—upper five bits (default: 0x00).
016	[7]	Set CP pin to VCP/2	Set the CP pin to one-half of the VCP supply voltage. [7] = 0; CP normal operation (default). [7] = 1; CP pin set to VCP/2.
016	[6]	Reset R counter	Reset R counter (R divider). This register is not self-clearing. [6] = 0; normal (default). [6] = 1; reset R counter.

Reg. Addr (Hex)	Bit(s)	Name	Description
016	[5]	Reset A and B counters	Reset A and B counters (part of N divider). [5] = 0; normal (default). This register is not self-clearing. [5] = 1; reset A and B counters.
016	[4]	Reset all counters	Reset R, A, and B counters. This register is not self-clearing. [4] = 0; normal (default). [4] = 1; reset R, A, and B counters.
016	[3]	B counter bypass	B counter bypass. This is valid only when operating the prescaler in FD mode. [3] = 0; normal (default). [3] = 1; B counter is set to divide-by-1. This allows the prescaler setting to determine the divide for the N divider.
016	[2:0]	Prescaler P	Prescaler: DM = dual modulus and FD = fixed divide.

[2]	[1]	[0]	Mode	Prescaler
0	0	0	FD	Divide-by-1.
0	0	1	FD	Divide-by-2.
0	1	0	DM	Divide-by-2 and divide-by-3 when A ≠ 0; divide-by-2 when A = 0.
0	1	1	DM	Divide-by-4 and divide-by-5 when A ≠ 0; divide-by-4 when A = 0.
1	0	0	DM	Divide-by-8 and divide-by-9 when A ≠ 0; divide-by-8 when A = 0.
1	0	1	DM	Divide-by-16 and divide-by-17 when A ≠ 0; divide-by-16 when A = 0.
1	1	0	DM	Divide-by-32 and divide-by-33 when A ≠ 0; divide-by-32 when A = 0 (default).
1	1	1	FD	Divide-by-3.

017 [7:2] STATUS pin control — Selects the STATUS pin signal.

[7]	[6]	[5]	[4]	[3]	[2]	Level or Dynamic Signal	Signal at STATUS Pin
0	0	0	0	0	0	LVL	Ground (dc) (default).
0	0	0	0	0	1	DYN	N divider output (after the delay).
0	0	0	0	1	0	DYN	R divider output (after the delay).
0	0	0	0	1	1	DYN	A divider output.
0	0	0	1	0	0	DYN	Prescaler output.
0	0	0	1	0	1	DYN	PFD up pulse.
0	0	0	1	1	0	DYN	PFD down pulse.
0	X	X	X	X	X	LVL	Ground (dc); for all other cases of 0x0XXXX not specified.
							The selections that follow are the same as REFMON.
1	0	0	0	0	0	LVL	Ground (dc).
1	0	0	0	0	1	DYN	REF1 clock (differential reference when in differential mode).
1	0	0	0	1	0	DYN	REF2 clock (N/A in differential mode).
1	0	0	0	1	1	DYN	Selected reference to PLL (differential reference when in differential mode).
1	0	0	1	0	0	DYN	Unselected reference to PLL (not available in differential mode).
1	0	0	1	0	1	LVL	Status of selected reference (status of differential reference); active high.
1	0	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active high.
1	0	0	1	1	1	LVL	Status REF1 frequency (active high).
1	0	1	0	0	0	LVL	Status REF2 frequency (active high).
1	0	1	0	0	1	LVL	(Status REF1 frequency) AND (status REF2 frequency).
1	0	1	0	1	0	LVL	(DLD) AND (status of selected reference) AND (status of CLK).
1	0	1	0	1	1	LVL	Status of CLK frequency (active high).
1	0	1	1	0	0	LVL	Selected reference (low = REF1, high = REF2).
1	0	1	1	0	1	LVL	Digital lock detect (DLD); active high.
1	0	1	1	1	0	LVL	Holdover active (active high).

Reg. Addr (Hex)	Bit(s)	Name	Description							
			[7]	[6]	[5]	[4]	[3]	[2]	Level or Dynamic Signal	Signal at STATUS Pin
			1	0	1	1	1	1	LVL	LD pin comparator output (active high).
			1	1	0	0	0	0	LVL	VS (PLL supply).
			1	1	0	0	0	1	DYN	$\overline{\text{REF1 clock}}$ (differential reference when in differential mode).
			1	1	0	0	1	0	DYN	$\overline{\text{REF2 clock}}$ (not available in differential mode).
			1	1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL}}$ (differential reference when in differential mode).
			1	1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL}}$ (not available when in differential mode).
			1	1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
			1	1	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active low.
			1	1	0	1	1	1	LVL	Status of REF1 frequency (active low).
			1	1	1	0	0	0	LVL	Status of REF2 frequency (active low).
			1	1	1	0	0	1	LVL	$\overline{\text{(Status of REF1 frequency) AND (Status of REF2 frequency)}}$.
			1	1	1	0	1	0	LVL	$\overline{\text{(DLD) AND (Status of selected reference) AND (Status of CLK)}}$.
			1	1	1	0	1	1	LVL	Status of CLK Frequency (active low).
			1	1	1	1	0	0	LVL	Selected reference (low = REF2, high = REF1).
			1	1	1	1	0	1	LVL	Digital lock detect (DLD) (active low).
			1	1	1	1	1	0	LVL	Holdover active (active low).
			1	1	1	1	1	1	LVL	LD pin comparator output (active low).
017	[1:0]	Antibacklash pulse width	**[1]**	**[0]**	**Antibacklash Pulse Width (ns)**					
			0	0	2.9 (default)					
			0	1	1.3					
			1	0	6.0					
			1	1	2.9					
018	[6:5]	Lock detect counter	Required consecutive number of PFD cycles with edges inside lock detect window before the DLD indicates a locked condition.							
			[6]	**[5]**	**PFD Cycles to Determine Lock**					
			0	0	5 (default)					
			0	1	16					
			1	0	64					
			1	1	255					
018	[4]	Digital lock detect window	If the time difference of the rising edges at the inputs to the PFD are less than the lock detect window time, the digital lock detect flag is set. The flag remains set until the time difference is greater than the loss-of-lock threshold. [4] = 0; high range (default). [4] = 1; low range.							
018	[3]	Disable digital lock detect	Digital lock detect operation. [3] = 0; normal lock detect operation (default). [3] = 1; disable lock detect.							
019	[7:6]	R, A, B counters $\overline{\text{SYNC}}$ pin reset	**[7]**	**[6]**	**Action**					
			0	0	Do nothing on $\overline{\text{SYNC}}$ (default).					
			0	1	Asynchronous reset.					
			1	0	Synchronous reset.					
			1	1	Do nothing on $\overline{\text{SYNC}}$.					
019	[5:3]	R path delay	[5:3] R Path Delay, see Table 2 (default: 0x0).							
019	[2:0]	N path delay	[2:0] N Path Delay, see Table 2 (default: 0x0).							

Reg. Addr (Hex)	Bit(s)	Name	Description
01A	[6]	Reference frequency monitor threshold	Sets the reference (REF1/REF2) frequency monitor's detection threshold frequency. This does not affect the CLK frequency monitor's detection threshold (see Table 13, REF1, REF2, and CLK frequency status monitor). [6] = 0; frequency valid if frequency is above the higher frequency threshold (default). [6] = 1; frequency valid if frequency is above the lower frequency threshold.
01A	[5:0]	LD pin control	Selects the LD pin signal.

[5]	[4]	[3]	[2]	[1]	[0]	Level or Dynamic Signal	Signal at LD Pin
0	0	0	0	0	0	LVL	Digital lock detect (high = lock, low = unlock) (default).
0	0	0	0	0	1	DYN	P-channel, open-drain lock detect (analog lock detect).
0	0	0	0	1	0	DYN	N-channel, open-drain lock detect (analog lock detect).
0	0	0	0	1	1	HIZ	High-Z LD pin.
0	0	0	1	0	0	CUR	Current source lock detect (110 µA when DLD is true).
0	X	X	X	X	X	LVL	Ground (dc); for all other cases of 0x0XXXX not specified.
							The selections that follow are the same as REFMON.
1	0	0	0	0	0	LVL	Ground (dc).
1	0	0	0	0	1	DYN	REF1 clock (differential reference when in differential mode).
1	0	0	0	1	0	DYN	REF2 clock (N/A in differential mode).
1	0	0	0	1	1	DYN	Selected reference to PLL (differential reference when in differential mode).
1	0	0	1	0	0	DYN	Unselected reference to PLL (not available in differential mode).
1	0	0	1	0	1	LVL	Status of selected reference (status of differential reference); active high.
1	0	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active high.
1	0	0	1	1	1	LVL	Status REF1 frequency (active high).
1	0	1	0	0	0	LVL	Status REF2 frequency (active high).
1	0	1	0	0	1	LVL	(Status REF1 frequency) AND (status REF2 frequency).
1	0	1	0	1	0	LVL	(DLD) AND (status of selected reference) AND (status of CLK).
1	0	1	0	1	1	LVL	Status of CLK frequency (active high).
1	0	1	1	0	0	LVL	Selected reference (low = REF1, high = REF2).
1	0	1	1	0	1	LVL	Digital lock detect (DLD); active high.
1	0	1	1	1	0	LVL	Holdover active (active high).
1	0	1	1	1	1	LVL	N/A—do not use.
1	1	0	0	0	0	LVL	VS (PLL supply).
1	1	0	0	0	1	DYN	$\overline{\text{REF1 clock}}$ (differential reference when in differential mode).
1	1	0	0	1	0	DYN	$\overline{\text{REF2 clock}}$ (not available in differential mode).
1	1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL}}$ (differential reference when in differential mode).
1	1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL}}$ (not available when in differential mode).
1	1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
1	1	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active low.
1	1	0	1	1	1	LVL	Status of REF1 frequency (active low).
1	1	1	0	0	0	LVL	Status of REF2 frequency (active low).
1	1	1	0	0	1	LVL	$\overline{\text{(Status of REF1 frequency) AND (Status of REF2 frequency)}}$.
1	1	1	0	1	0	LVL	$\overline{\text{(DLD) AND (Status of selected reference) AND (Status of CLK)}}$.
1	1	1	0	1	1	LVL	Status of CLK frequency (active low).
1	1	1	1	0	0	LVL	Selected reference (low = REF2, high = REF1).
1	1	1	1	0	1	LVL	Digital lock detect (DLD); active low.

Reg. Addr (Hex)	Bit(s)	Name	Description

[5]	[4]	[3]	[2]	[1]	[0]	Level or Dynamic Signal	Signal at LD Pin
1	1	1	1	1	0	LVL	Holdover active (active low).
1	1	1	1	1	1	LVL	N/A—do not use.

Reg. Addr (Hex)	Bit(s)	Name	Description
01B	[7]	CLK frequency monitor	Enable or disable CLK frequency monitor. [7] = 0; disable CLK frequency monitor (default). [7] = 1; enable CLK frequency monitor.
01B	[6]	REF2 ($\overline{\text{REFIN}}$) frequency monitor	Enable or disable REF2 frequency monitor. [6] = 0; disable REF2 frequency monitor (default). [6] = 1; enable REF2 frequency monitor.
01B	[5]	REF1 (REFIN) frequency monitor	REF1 (REFIN) frequency monitor enable; this is for both REF1 (single-ended) and REFIN (differential) inputs (as selected by differential reference mode). [5] = 0; disable REF1 (REFIN) frequency monitor (default). [5] = 1; enable REF1 (REFIN) frequency monitor.
01B	[4:0]	REFMON pin control	Selects the REFMON pin signal.

[4]	[3]	[2]	[1]	[0]	Level or Dynamic Signal	Signal at REFMON Pin
0	0	0	0	0	LVL	Ground (dc) (default).
0	0	0	0	1	DYN	REF1 clock (differential reference when in differential mode).
0	0	0	1	0	DYN	REF2 clock (N/A in differential mode).
0	0	0	1	1	DYN	Selected reference to PLL (differential reference when in differential mode).
0	0	1	0	0	DYN	Unselected reference to PLL (not available in differential mode).
0	0	1	0	1	LVL	Status of selected reference (status of differential reference); active high.
0	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active high.
0	0	1	1	1	LVL	Status REF1 frequency (active high).
0	1	0	0	0	LVL	Status REF2 frequency (active high).
0	1	0	0	1	LVL	(Status REF1 frequency) AND (status REF2 frequency).
0	1	0	1	0	LVL	(DLD) AND (status of selected reference) AND (status of CLK).
0	1	0	1	1	LVL	Status of CLK frequency (active high).
0	1	1	0	0	LVL	Selected reference (low = REF1, high = REF2).
0	1	1	0	1	LVL	Digital lock detect (DLD); active low.
0	1	1	1	0	LVL	Holdover active (active high).
0	1	1	1	1	LVL	LD pin comparator output (active high).
1	0	0	0	0	LVL	VS (PLL supply).
1	0	0	0	1	DYN	$\overline{\text{REF1 clock}}$ (differential reference when in differential mode).
1	0	0	1	0	DYN	$\overline{\text{REF2 clock}}$ (not available in differential mode).
1	0	0	1	1	DYN	$\overline{\text{Selected reference to PLL}}$ (differential reference when in differential mode).
1	0	1	0	0	DYN	$\overline{\text{Unselected reference to PLL}}$ (not available when in differential mode).
1	0	1	0	1	LVL	Status of selected reference (status of differential reference); active low.
1	0	1	1	0	LVL	Status of unselected reference (not available in differential mode); active low.
1	0	1	1	1	LVL	Status of REF1 frequency (active low).
1	1	0	0	0	LVL	Status of REF2 frequency (active low).

Reg. Addr (Hex)	Bit(s)	Name	Description						
			[4]	[3]	[2]	[1]	[0]	Level or Dynamic Signal	Signal at REFMON Pin
			1	1	0	0	1	LVL	(Status of REF1 frequency) AND (Status of REF2 frequency).
			1	1	0	1	0	LVL	(DLD) AND (Status of selected reference) AND (Status of CLK) .
			1	1	0	1	1	LVL	Status of CLK frequency (active low).
			1	1	1	0	0	LVL	Selected reference (low = REF2, high = REF1).
			1	1	1	0	1	LVL	Digital lock detect (DLD); active low.
			1	1	1	1	0	LVL	Holdover active (active low).
			1	1	1	1	1	LVL	LD pin comparator output (active low).
01C	[7]	Disable switchover deglitch	Disable or enable the switchover deglitch circuit. [7] = 0; enable switchover deglitch circuit (default). [7] = 1; disable switchover deglitch circuit.						
01C	[6]	Select REF2	If Register 0x01C[5] = 0, select reference for PLL. [6] = 0; select REF1 (default). [6] = 1; select REF2.						
01C	[5]	Use REF_SEL pin	If Register 0x01C[4] = 0 (manual), set method of PLL reference selection. [5] = 0; use Register 0x01C[6] (default). [5] = 1; use REF_SEL pin.						
01C	[4]	Automatic reference switchover	Automatic or manual reference switchover. Single-ended reference mode must be selected by Register 0x01C[0] = 0. [4] = 0; manual reference switchover (default). [4] = 1; automatic reference switchover.						
01C	[3]	Stay on REF2	Stay on REF2 after switchover. [3] = 0; return to REF1 automatically when REF1 status is good again (default). [3] = 1; stay on REF2 after switchover. Do not automatically return to REF1.						
01C	[2]	REF2 power on	When automatic reference switchover is disabled, this bit turns the REF2 power on. [2] = 0; REF2 power off (default). [2] = 1; REF2 power on.						
01C	[1]	REF1 power on	When automatic reference switchover is disabled, this bit turns the REF1 power on. [1] = 0; REF1 power off (default). [1] = 1; REF1 power on.						
01C	[0]	Differential reference	Selects the PLL reference mode, differential or single-ended. Single-ended must be selected for the automatic switchover or REF1 and REF2 to work. [0] = 0; single-ended reference mode (default). [0] = 1; differential reference mode.						
01D	[4]	PLL status register disable	Disables the PLL status register readback. [4] = 0; PLL status register enable (default). [4] = 1; PLL status register disable.						
01D	[3]	LD pin comparator enable	Enables the LD pin voltage comparator. This is used with the LD pin current source lock detect mode. When in the internal (automatic) holdover mode, this enables the use of the voltage on the LD pin to determine if the PLL was previously in a locked state (see Figure 40). Otherwise, this can be used with the REFMON and STATUS pins to monitor the voltage on the LD pin. [3] = 0; disable LD pin comparator; internal/automatic holdover controller treats this pin as true/high (default). [3] = 1; enable LD pin comparator.						
01D	[2]	Holdover enable	Along with 0x01D[0] enables the holdover function. [2] = 0; holdover disabled (default). [2] = 1; holdover enabled.						
01D	[1]	External holdover control	Enables the external hold control through the $\overline{\text{SYNC}}$ pin. (This disables the internal holdover mode.) [1] = 0; automatic holdover mode—holdover controlled by automatic holdover circuit (default). [1] = 1; external holdover mode—holdover controlled by $\overline{\text{SYNC}}$ pin.						

Reg. Addr (Hex)	Bit(s)	Name	Description
01D	[0]	Holdover enable	Along with 0x01D[2] enables the holdover function. [0] = 0; holdover disabled (default). [0] = 1; holdover enabled.
01F	[5]	Holdover active	Readback register: indicates if the part is in the holdover state (see Figure 40). This is not the same as holdover enabled. [5] = 0; not in holdover. [5] = 1; holdover state active.
01F	[4]	REF2 selected	Readback register: indicates which PLL reference is selected as the input to the PLL. [4] = 0; REF1 selected (or differential reference if in differential mode). [4] = 1; REF2 selected.
01F	[3]	CLK frequency > threshold	Readback register: indicates if the CLK frequency is greater than the threshold (see Table 13, REF1, REF2, and CLK frequency status monitor). [3] = 0; CLK frequency is less than the threshold. [3] = 1; CLK frequency is greater than the threshold.
01F	[2]	REF2 frequency > threshold	Readback register: indicates if the frequency of the signal at REF2 is greater than the threshold frequency set by Register 0x01A[6]. [2] = 0; REF2 frequency is less than threshold frequency. [2] = 1; REF2 frequency is greater than threshold frequency.
01F	[1]	REF1 frequency > threshold	Readback register: indicates if the frequency of the signal at REF2 is greater than the threshold frequency set by Register 0x01A[6]. [1] = 0; REF1 frequency is less than threshold frequency. [1] = 1; REF1 frequency is greater than threshold frequency.
01F	[0]	Digital lock detect	Readback register: digital lock detect. [0] = 0; PLL is not locked. [0] = 1; PLL is locked.

Table 50. Fine Delay Adjust: OUT6 to OUT9

Reg. Addr (Hex)	Bit(s)	Name	Description			
0A0	[0]	OUT6 delay bypass	Bypass or use the delay function. [0] = 0; use delay function. [0] = 1; bypass delay function (default).			
0A1	[5:3]	OUT6 ramp capacitors	Selects the number of ramp capacitors used by the delay function. The combination of the number of capacitors and the ramp current sets the full-scale delay.			
			[5]	**[4]**	**[3]**	**Number of Capacitors**
			0	0	0	4 (default)
			0	0	1	3
			0	1	0	3
			0	1	1	2
			1	0	0	3
			1	0	1	2
			1	1	0	2
			1	1	1	1

Reg. Addr (Hex)	Bit(s)	Name	Description
0A1	[2:0]	OUT6 ramp current	Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the full-scale delay.
			[2] [1] [0] Current (µA)
			0 0 0 200 (default)
			0 0 1 400
			0 1 0 600
			0 1 1 800
			1 0 0 1000
			1 0 1 1200
			1 1 0 1400
			1 1 1 1600
0A2	[5:0]	OUT6 delay fraction	Selects the fraction of the full-scale delay desired (6-bit binary). 000000 gives zero delay. Only delay values up to 47 decimals (101111b; 0x02F) are supported (default: 0x00).
0A3	[0]	OUT7 delay bypass	Bypass or use the delay function. [0] = 0; use delay function. [0] = 1; bypass delay function (default).
0A4	[5:3]	OUT7 ramp capacitors	Selects the number of ramp capacitors used by the delay function. The combination of the number of the capacitors and the ramp current sets the full-scale delay.
			[5] [4] [3] Number of Capacitors
			0 0 0 4 (default)
			0 0 1 3
			0 1 0 3
			0 1 1 2
			1 0 0 3
			1 0 1 2
			1 1 0 2
			1 1 1 1
0A4	[2:0]	OUT7 ramp current	Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the full-scale delay.
			[2] [1] [0] Current (µA)
			0 0 0 200 (default)
			0 0 1 400
			0 1 0 600
			0 1 1 800
			1 0 0 1000
			1 0 1 1200
			1 1 0 1400
			1 1 1 1600
0A5	[5:0]	OUT7 delay fraction	Selects the fraction of the full-scale delay desired (6-bit binary). 000000 give zero delay. Only delay values up to 47 decimals (101111b; 0x02F) are supported (default: 0x00).
0A6	[0]	OUT8 delay bypass	Bypass or use the delay function. [0] = 0; use delay function. [0] = 1; bypass delay function (default).

Reg. Addr (Hex)	Bit(s)	Name	Description
0A7	[5:3]	OUT8 ramp capacitors	Selects the number of ramp capacitors used by the delay function. The combination of the number of capacitors and the ramp current sets the full-scale delay.

[5]	[4]	[3]	Number of Capacitors
0	0	0	4 (default)
0	0	1	3
0	1	0	3
0	1	1	2
1	0	0	3
1	0	1	2
1	1	0	2
1	1	1	1

0A7	[2:0]	OUT8 ramp current	Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the full-scale delay.

[2]	[1]	[0]	Current (µA)
0	0	0	200 (default)
0	0	1	400
0	1	0	600
0	1	1	800
1	0	0	1000
1	0	1	1200
1	1	0	1400
1	1	1	1600

0A8	[5:0]	OUT8 delay fraction	Selects the fraction of the full-scale delay desired (6-bit binary). 000000 gives zero delay. Only delay values up to 47 decimals (101111b; 0x02F) are supported (default: 0x00).
0A9	[0]	OUT9 delay bypass	Bypass or use the delay function. [0] = 0; use delay function. [0] = 1; bypass delay function (default).
0AA	[5:3]	OUT9 ramp capacitors	Selects the number of ramp capacitors used by the delay function. The combination of the number of capacitors and the ramp current sets the full-scale delay.

[5]	[4]	[3]	Number of Capacitors
0	0	0	4 (default)
0	0	1	3
0	1	0	3
0	1	1	2
1	0	0	3
1	0	1	2
1	1	0	2
1	1	1	1

0AA	[2:0]	OUT9 ramp current	Ramp current for the delay function. The combination of the number of capacitors and the ramp current sets the delay full scale.

[2]	[1]	[0]	Current Value (µA)
0	0	0	200 (default)
0	0	1	400
0	1	0	600
0	1	1	800
1	0	0	1000
1	0	1	1200
1	1	0	1400
1	1	1	1600

0AB	[5:0]	OUT9 delay fraction	Selects the fraction of the full-scale delay desired (6-bit binary). 000000 gives zero delay. Only delay values up to 47 decimals (101111b; 0x02F) are supported (default: 0x00).

Table 51. LVPECL Outputs

Reg. Addr (Hex)	Bit(s)	Name	Description			
0F0	[4]	OUT0 invert	Sets the output polarity. [4] = 0; noninverting (default). [4] = 1; inverting.			
0F0	[3:2]	OUT0 LVPECL differential voltage	Sets the LVPECL output differential voltage (V_{OD}).			
			[3]	**[2]**	**V_{OD} (mV)**	
			0	0	400	
			0	1	600	
			1	0	780 (default)	
			1	1	960	
0F0	[1:0]	OUT0 power-down	LVPECL power-down modes.			
			[1]	**[0]**	**Mode**	**Output**
			0	0	Normal operation (default).	On
			0	1	Partial power-down, reference on; use only if there are no external load resistors.	Off
			1	0	Partial power-down, reference on, safe LVPECL power-down.	Off
			1	1	Total power-down, reference off; use only if there are no external load resistors.	Off
0F1	[4]	OUT1 invert	Sets the output polarity. [4] = 0; noninverting (default). [4] = 1; inverting.			
0F1	[3:2]	OUT1 LVPECL differential voltage	Sets the LVPECL output differential voltage (V_{OD}).			
			[3]	**[2]**	**V_{OD} (mV)**	
			0	0	400	
			0	1	600	
			1	0	780 (default)	
			1	1	960	
0F1	[1:0]	OUT1 power-down	LVPECL power-down modes.			
			[1]	**[0]**	**Mode**	**Output**
			0	0	Normal operation.	On
			0	1	Partial power-down, reference on; use only if there are no external load resistors.	Off
			1	0	Partial power-down, reference on, safe LVPECL power-down (default).	Off
			1	1	Total power-down, reference off; use only if there are no external load resistors.	Off
0F2	[4]	OUT2 invert	Sets the output polarity. [4] = 0; noninverting (default). [4] = 1; inverting.			
0F2	[3:2]	OUT2 LVPECL differential voltage	Sets the LVPECL output differential voltage (V_{OD}).			
			[3]	**[2]**	**V_{OD} (mV)**	
			0	0	400	
			0	1	600	
			1	0	780 (default)	
			1	1	960	
0F2	[1:0]	OUT2 power-down	LVPECL power-down modes.			
			[1]	**[0]**	**Mode**	**Output**
			0	0	Normal operation (default).	On
			0	1	Partial power-down, reference on; use only if there are no external load resistors.	Off
			1	0	Partial power-down, reference on, safe LVPECL power-down.	Off
			1	1	Total power-down, reference off; use only if there are no external load resistors.	Off
0F3	[4]	OUT3 invert	Sets the output polarity. [4] = 0; noninverting (default). [4] = 1; inverting.			

Reg. Addr (Hex)	Bit(s)	Name	Description			
0F3	[3:2]	OUT3 LVPECL differential voltage	Sets the LVPECL output differential voltage (V_{OD}).			
			[3]	**[2]**	**V_{OD} (mV)**	
			0	0	400	
			0	1	600	
			1	0	780 (default)	
			1	1	960	
0F3	[1:0]	OUT3 power-down	LVPECL power-down modes.			
			[1]	**[0]**	**Mode**	**Output**
			0	0	Normal operation.	On
			0	1	Partial power-down, reference on; use only if there are no external load resistors.	Off
			1	0	Partial power-down, reference on, safe LVPECL power-down (default).	Off
			1	1	Total power-down, reference off; use only if there are no external load resistors.	Off
0F4	[4]	OUT4 invert	Sets the output polarity. [4] = 0; noninverting (default). [4] = 1; inverting.			
0F4	[3:2]	OUT4 LVPECL differential voltage	Sets the LVPECL output differential voltage (V_{OD}).			
			[3]	**[2]**	**V_{OD} (mV)**	
			0	0	400	
			0	1	600	
			1	0	780 (default)	
			1	1	960	
0F4	[1:0]	OUT4 power-down	LVPECL power-down modes.			
			[1]	**[0]**	**Mode**	**Output**
			0	0	Normal operation.	On
			0	1	Partial power-down, reference on; use only if there are no external load resistors.	Off
			1	0	Partial power-down, reference on, safe LVPECL power-down.	Off
			1	1	Total power-down, reference off; use only if there are no external load resistors.	Off
0F5	[4]	OUT5 invert	Sets the output polarity. [4] = 0; noninverting (default). [4] = 1; inverting.			
0F5	[3:2]	OUT5 LVPECL differential voltage	Sets the LVPECL output differential voltage (V_{OD}).			
			[3]	**[2]**	**V_{OD} (mV)**	
			0	0	400	
			0	1	600	
			1	0	780 (default)	
			1	1	960	
0F5	[1:0]	OUT5 power-down	LVPECL power-down modes.			
			[1]	**[0]**	**Mode**	**Output**
			0	0	Normal operation.	On
			0	1	Partial power-down, reference on; use only if there are no external load resistors.	Off
			1	0	Partial power-down, reference on, safe LVPECL power-down (default).	Off
			1	1	Total power-down, reference off; use only if there are no external load resistors.	Off

Table 52. LVDS/CMOS Outputs

Reg. Addr (Hex)	Bit(s)	Name	Description
140	[7:5]	OUT6 output polarity	In CMOS mode, [7:5] select the output polarity of each CMOS output. In LVDS mode, only [5] determines LVDS polarity.

[7]	[6]	[5]	OUT6A (CMOS)	OUT6B (CMOS)	OUT6 (LVDS)
0	0	0	Noninverting	Inverting	Noninverting
0	1	0	Noninverting	Noninverting	Noninverting (default)
1	0	0	Inverting	Inverting	Noninverting
1	1	0	Inverting	Noninverting	Noninverting
0	0	1	Inverting	Noninverting	Inverting
0	1	1	Inverting	Inverting	Inverting
1	0	1	Noninverting	Noninverting	Inverting
1	1	1	Noninverting	Inverting	Inverting

Reg. Addr (Hex)	Bit(s)	Name	Description
140	[4]	OUT6 CMOS B	In CMOS mode, turn on/off the CMOS B output. There is no effect in LVDS mode. [4] = 0; turn off the CMOS B output (default). [4] = 1; turn on the CMOS B output.
140	[3]	OUT6 select LVDS/CMOS	Select LVDS or CMOS logic levels. [3] = 0; LVDS (default). [3] = 1; CMOS.
140	[2:1]	OUT6 LVDS output current	Set output current level in LVDS mode. This has no effect in CMOS mode.

[2]	[1]	Current (mA)	Recommended Termination (Ω)
0	0	1.75	100
0	1	3.5	100 (default)
1	0	5.25	50
1	1	7	50

Reg. Addr (Hex)	Bit(s)	Name	Description
140	[0]	OUT6 power-down	Power-down output (LVDS/CMOS). [0] = 0; power on (default). [0] = 1; power off.
141	[7:5]	OUT7 output polarity	In CMOS mode, [7:5] select the output polarity of each CMOS output. In LVDS mode, only [5] determines LVDS polarity.

[7]	[6]	[5]	OUT7A (CMOS)	OUT7B (CMOS)	OUT7 (LVDS)
0	0	0	Noninverting	Inverting	Noninverting
0	1	0	Noninverting	Noninverting	Noninverting (default)
1	0	0	Inverting	Inverting	Noninverting
1	1	0	Inverting	Noninverting	Noninverting
0	0	1	Inverting	Noninverting	Inverting
0	1	1	Inverting	Inverting	Inverting
1	0	1	Noninverting	Noninverting	Inverting
1	1	1	Noninverting	Inverting	Inverting

Reg. Addr (Hex)	Bit(s)	Name	Description
141	[4]	OUT7 CMOS B	In CMOS mode, turn on/off the CMOS B output. There is no effect in LVDS mode. [4] = 0; turn off the CMOS B output (default). [4] = 1; turn on the CMOS B output.
141	[3]	OUT7 select LVDS/CMOS	Select LVDS or CMOS logic levels. [3] = 0; LVDS (default). [3] = 1; CMOS.
141	[2:1]	OUT7 LVDS output current	Set output current level in LVDS mode. This has no effect in CMOS mode.

[2]	[1]	Current (mA)	Recommended Termination (Ω)
0	0	1.75	100
0	1	3.5	100 (default)
1	0	5.25	50
1	1	7	50

<table>
<tr><th>Reg. Addr (Hex)</th><th>Bit(s)</th><th>Name</th><th>Description</th></tr>
<tr><td>141</td><td>[0]</td><td>OUT7 power-down</td><td>Power-down output (LVDS/CMOS).
[0] = 0; power on.
[0] = 1; power off (default).</td></tr>
<tr><td>142</td><td>[7:5]</td><td>OUT8 output polarity</td><td>In CMOS mode, [7:5] select the output polarity of each CMOS output.
In LVDS mode, only [5] determines LVDS polarity.
<table>
<tr><th>[7]</th><th>[6]</th><th>[5]</th><th>OUT8A (CMOS)</th><th>OUT8B (CMOS)</th><th>OUT8 (LVDS)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Noninverting</td><td>Inverting</td><td>Noninverting</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Noninverting</td><td>Noninverting</td><td>Noninverting (default)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Inverting</td><td>Inverting</td><td>Noninverting</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Inverting</td><td>Noninverting</td><td>Noninverting</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Inverting</td><td>Noninverting</td><td>Inverting</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Inverting</td><td>Inverting</td><td>Inverting</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Noninverting</td><td>Noninverting</td><td>Inverting</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Noninverting</td><td>Inverting</td><td>Inverting</td></tr>
</table></td></tr>
<tr><td>142</td><td>[4]</td><td>OUT8 CMOS B</td><td>In CMOS mode, turn on/off the CMOS B output. There is no effect in LVDS mode.
[4] = 0; turn off the CMOS B output (default).
[4] = 1; turn on the CMOS B output.</td></tr>
<tr><td>142</td><td>[3]</td><td>OUT8 select LVDS/CMOS</td><td>Select LVDS or CMOS logic levels.
[3] = 0; LVDS (default).
[3] = 1; CMOS.</td></tr>
<tr><td>142</td><td>[2:1]</td><td>OUT8 LVDS output current</td><td>Set output current level in LVDS mode. This has no effect in CMOS mode.
<table>
<tr><th>[2]</th><th>[1]</th><th>Current (mA)</th><th>Recommended Termination (Ω)</th></tr>
<tr><td>0</td><td>0</td><td>1.75</td><td>100</td></tr>
<tr><td>0</td><td>1</td><td>3.5</td><td>100 (default)</td></tr>
<tr><td>1</td><td>0</td><td>5.25</td><td>50</td></tr>
<tr><td>1</td><td>1</td><td>7</td><td>50</td></tr>
</table></td></tr>
<tr><td>142</td><td>[0]</td><td>OUT8 power-down</td><td>Power-down output (LVDS/CMOS).
[0] = 0; power on (default).
[0] = 1; power off.</td></tr>
<tr><td>143</td><td>[7:5]</td><td>OUT9 output polarity</td><td>In CMOS mode, [7:5] select the output polarity of each CMOS output.
In LVDS mode, only [5] determines LVDS polarity.
<table>
<tr><th>[7]</th><th>[6]</th><th>[5]</th><th>OUT9A (CMOS)</th><th>OUT9B (CMOS)</th><th>OUT9 (LVDS)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Noninverting</td><td>Inverting</td><td>Noninverting</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Noninverting</td><td>Noninverting</td><td>Noninverting (default)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Inverting</td><td>Inverting</td><td>Noninverting</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Inverting</td><td>Noninverting</td><td>Noninverting</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Inverting</td><td>Noninverting</td><td>Inverting</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Inverting</td><td>Inverting</td><td>Inverting</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Noninverting</td><td>Noninverting</td><td>Inverting</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Noninverting</td><td>Inverting</td><td>Inverting</td></tr>
</table></td></tr>
<tr><td>143</td><td>[4]</td><td>OUT9 CMOS B</td><td>In CMOS mode, turn on/off the CMOS B output. There is no effect in LVDS mode.
[4] = 0; turn off the CMOS B output (default).
[4] = 1; turn on the CMOS B output.</td></tr>
<tr><td>143</td><td>[3]</td><td>OUT9 select LVDS/CMOS</td><td>Select LVDS or CMOS logic levels.
[3] = 0; LVDS (default).
[3] = 1; CMOS.</td></tr>
</table>

Reg. Addr (Hex)	Bit(s)	Name	Description
143	[2:1]	OUT9 LVDS output current	Set output current level in LVDS mode. This has no effect in CMOS mode.

[2]	[1]	Current (mA)	Recommended Termination (Ω)
0	0	1.75	100
0	1	3.5	100 (default)
1	0	5.25	50
1	1	7	50

143	[0]	OUT9 power-down	Power-down output (LVDS/CMOS). [0] = 0; power on. [0] = 1; power off (default).

Table 53. LVPECL Channel Dividers

Reg. Addr (Hex)	Bit(s)	Name	Description
190	[7:4]	Divider 0 low cycles	Number of clock cycles (minus 1) of the Divider 0 input during which the Divider 0 output stays low. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x0).
190	[3:0]	Divider 0 high cycles	Number of clock cycles (minus 1) of the Divider 0 input during which the Divider 0 output stays high. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x0).
191	[7]	Divider 0 bypass	Bypass and power-down the divider; route input to divider output. [7] = 0; use divider. [7] = 1; bypass divider (default).
191	[6]	Divider 0 nosync	Nosync. [6] = 0; obey chip-level SYNC signal (default). [6] = 1; ignore chip-level SYNC signal.
191	[5]	Divider 0 force high	Force divider output to high. This requires that nosync also be set. [5] = 0; divider output forced to low (default). [5] = 1; divider output forced to high.
191	[4]	Divider 0 start high	Selects clock output to start high or start low. [4] = 0; start low (default). [4] = 1; start high.
191	[3:0]	Divider 0 phase offset	Phase offset (default: 0x0).
192	[1]	Divider 0 direct to output	Connect OUT0 and OUT1 to Divider 0 or directly to CLK input. [1] = 0: OUT0 and OUT1 are connected to Divider 0 (default). [1] = 1; If 0x1E1[0] = 0, the CLK is routed directly to OUT0 and OUT1. If 0x1E1[0] = 1, there is no effect.
192	[0]	Divider 0 DCCOFF	Duty-cycle correction function. [0] = 0; enable duty-cycle correction (default). [0] = 1; disable duty-cycle correction.
193	[7:4]	Divider 1 low cycles	Number of clock cycles (minus 1) of the Divider 1 input during which the Divider 1 output stays low. A value of 0x7 means the divider is low for eight input clock cycles (default: 0xB).
193	[3:0]	Divider 1 high cycles	Number of clock cycles (minus 1) of the Divider 1 input during which the Divider 1 output stays high. A value of 0x7 means the divider is low for eight input clock cycles (default: 0xB).
194	[7]	Divider 1 bypass	Bypass and power-down the divider; route input to divider output. [7] = 0; use divider (default). [7] = 1; bypass divider.
194	[6]	Divider 1 nosync	Nosync. [6] = 0; obey chip-level SYNC signal (default). [6] = 1; ignore chip-level SYNC signal.

Reg. Addr (Hex)	Bit(s)	Name	Description
194	[5]	Divider 1 force high	Force divider output to high. This requires that nosync also be set. [5] = 0; divider output forced to low (default). [5] = 1; divider output forced to high.
194	[4]	Divider 1 start high	Selects clock output to start high or start low. [4] = 0; start low (default). [4] = 1; start high.
194	[3:0]	Divider 1 phase offset	Phase offset (default: 0x0).
195	[1]	Divider 1 direct to output	Connect OUT2 and OUT3 to Divider 1 or directly to CLK input. [1] = 0; OUT2 and OUT3 are connected to Divider 1 (default). [1] = 1; If 0x1E1[0] = 0, the CLK is routed directly to OUT2 and OUT3. If 0x1E1[0] = 1, there is no effect.
195	[0]	Divider 1 DCCOFF	Duty-cycle correction function. [0] = 0; enable duty-cycle correction (default). [0] = 1; disable duty-cycle correction.
196	[7:4]	Divider 2 low cycles	Number of clock cycles (minus 1) of the Divider 2 input during which the Divider 2 output stays low. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x0).
196	[3:0]	Divider 2 high cycles	Number of clock cycles (minus 1) of the Divider 2 input during which the Divider 2 output stays high. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x0).
197	[7]	Divider 2 bypass	Bypass and power down the divider; route input to divider output. [7] = 0; use divider (default). [7] = 1; bypass divider.
197	[6]	Divider 2 nosync	Nosync. [6] = 0; obey chip-level SYNC signal (default). [6] = 1; ignore chip-level SYNC signal.
197	[5]	Divider 2 force high	Force divider output to high. This requires that nosync also be set. [5] = 0; divider output forced to low (default). [5] = 1; divider output forced to high.
197	[4]	Divider 2 start high	Selects clock output to start high or start low. [4] = 0; start low (default). [4] = 1; start high.
197	[3:0]	Divider 2 phase offset	Phase offset (default: 0x0).
198	[1]	Divider 2 direct to output	Connect OUT4 and OUT5 to Divider 2 or directly to CLK input. [1] = 0; OUT4 and OUT5 are connected to Divider 2 (default). [1] = 1; If 0x1E1[0] = 0, the CLK is routed directly to OUT4 and OUT5. If 0x1E1[0] = 1, there is no effect.
198	[0]	Divider 2 DCCOFF	Duty-cycle correction function. [0] = 0; enable duty-cycle correction (default). [0] = 1; disable duty-cycle correction.

Table 54. LVDS/CMOS Channel Dividers

Reg. Addr (Hex)	Bit(s)	Name	Description
199	[7:4]	Low Cycles Divider 3.1	Number of clock cycles (minus 1) of the Divider 3.1 input during which the Divider 3.1 output stays low. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x2).
199	[3:0]	High Cycles Divider 3.1	Number of clock cycles (minus 1) of the Divider 3.1 input during which the Divider 3.1 output stays high. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x2).
19A	[7:4]	Phase Offset Divider 3.2	Refer to LVDSCMOS channel divider function description (default: 0x0).
19A	[3:0]	Phase Offset Divider 3.1	Refer to LVDSCMOS channel divider function description (default: 0x0).

Reg. Addr (Hex)	Bit(s)	Name	Description
19B	[7:4]	Low Cycles Divider 3.2	Number of clock cycles (minus 1) of the Divider 3.2 input during which the Divider 3.2 output stays low. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x1).
19B	[3:0]	High Cycles Divider 3.2	Number of clock cycles (minus 1) of the Divider 3.2 input during which the Divider 3.2 output stays high. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x1).
19C	[5]	Bypass Divider 3.2	Bypass (and power-down) 3.2 divider logic, route clock to 3.2 output. [5] = 0; do not bypass (default). [5] = 1; bypass.
19C	[4]	Bypass Divider 3.1	Bypass (and power-down) 3.1 divider logic, route clock to 3.1 output. [4] = 0; do not bypass (default). [4] = 1; bypass.
19C	[3]	Divider 3 nosync	Nosync. [3] = 0; obey chip-level SYNC signal (default). [3] = 1; ignore chip-level SYNC signal.
19C	[2]	Divider 3 force high	Force Divider 3 output high. Requires that nosync also be set. [2] = 0; force low (default). [2] = 1; force high.
19C	[1]	Start High Divider 3.2	Divider 3.2 start high/low. [1] = 0; start low (default). [1] = 1; start high.
19C	[0]	Start High Divider 3.1	Divider 3.1 start high/low. [0] = 0; start low (default). [0] = 1; start high.
19D	[0]	Divider 3 DCCOFF	Duty-cycle correction function. [0] = 0; enable duty-cycle correction (default). [0] = 1; disable duty-cycle correction.
19E	[7:4]	Low Cycles Divider 4.1	Number of clock cycles (minus 1) of the Divider 4.1 input during which the Divider 4.1 output stays low. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x2).
19E	[3:0]	High Cycles Divider 4.1	Number of clock cycles (minus 1) of the Divider 4.1 input during which the Divider 4.1 output stays high. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x2).
19F	[7:4]	Phase Offset Divider 4.2	Refer to LVDSCMOS channel divider function description (default: 0x0).
19F	[3:0]	Phase Offset Divider 4.1	Refer to LVDSCMOS channel divider function description (default: 0x0).
1A0	[7:4]	Low Cycles Divider 4.2	Number of clock cycles (minus 1) of the Divider 4.2 input during which the Divider 4.2 output stays low. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x1).
1A0	[3:0]	High Cycles Divider 4.2	Number of clock cycles (minus 1) of the Divider 4.2 input during which the Divider 4.2 output stays high. A value of 0x7 means the divider is low for eight input clock cycles (default: 0x1).
1A1	[5]	Bypass Divider 4.2	Bypass (and power down) 4.2 divider logic, route clock to 4.2 output. [5] = 0; do not bypass (default). [5] = 1; bypass.
1A1	[4]	Bypass Divider 4.1	Bypass (and power down) 4.1 divider logic, route clock to 4.1 output. [4] = 0; do not bypass (default). [4] = 1; bypass.
1A1	[3]	Divider 4 nosync	Nosync. [3] = 0; obey chip-level SYNC signal (default). [3] = 1; ignore chip-level SYNC signal.
1A1	[2]	Divider 4 force high	Force Divider 4 output high. Requires that nosync also be set. [2] = 0; force low (default). [2] = 1; force high.
1A1	[1]	Start High Divider 4.2	Divider 4.2 start high/low. [1] = 0; start low (default). [1] = 1; start high.

Reg. Addr (Hex)	Bit(s)	Name	Description
1A1	[0]	Start High Divider 4.1	Divider 4.1 start high/low. [0] = 0; start low (default). [0] = 1; start high.
1A2	[0]	Divider 4 DCCOFF	Duty-cycle correction function. [0] = 0; enable duty-cycle correction (default). [0] = 1; disable duty-cycle correction.

Table 55. VCO Divider and CLK Input

Reg. Addr (Hex)	Bit(s)	Name	Description			
1E0	[2:0]	VCO divider	**[2]**	**[1]**	**[0]**	**Divide**
			0	0	0	2
			0	0	1	3
			0	1	0	4 (default)
			0	1	1	5
			1	0	0	6
			1	0	1	Output static
			1	1	0	Output static
			1	1	1	Output static
1E1	[4]	Power-down clock input section	Power down the clock input section (including CLK buffer, VCO divider, and CLK tree). [4] = 0; normal operation (default). [4] = 1; power-down.			
1E1	[0]	Bypass VCO divider	Bypass or use the VCO divider. [0] = 0; use VCO divider (default). [0] = 1; bypass VCO divider.			

Table 56. System

Reg. Addr (Hex)	Bit(s)	Name	Description
230	[2]	Power-down SYNC	Power down the SYNC function. [2] = 0; normal operation of the SYNC function (default). [2] = 1; power-down SYNC circuitry.
230	[1]	Power-down distribution reference	Power down the reference for distribution section. [1] = 0; normal operation of the reference for the distribution section (default). [1] = 1; power down the reference for the distribution section.
230	[0]	Soft SYNC	The soft SYNC bit works the same as the $\overline{\text{SYNC}}$ pin, except that the polarity of the bit is reversed; that is, a high level forces selected channels into a predetermined static state, and a 1-to-0 transition triggers a SYNC. [0] = 0; same as $\overline{\text{SYNC}}$ high (default). [0] = 1; same as $\overline{\text{SYNC}}$ low.

Table 57. Update All Registers

Reg. Addr (Hex)	Bit(s)	Name	Description
232	[0]	Update all registers	This bit must be set to 1 to transfer the contents of the buffer registers into the active registers. This happens on the next SCLK rising edge. This bit is self-clearing; that is, it does not have to be set back to 0. [0] = 1 (self-clearing); update all active registers to the contents of the buffer registers.

APPLICATION NOTES

USING THE AD9516 OUTPUTS FOR ADC CLOCK APPLICATIONS

Any high speed ADC is extremely sensitive to the quality of its sampling clock. An ADC can be thought of as a sampling mixer, and any noise, distortion, or timing jitter on the clock is combined with the desired signal at the analog-to-digital output. Clock integrity requirements scale with the analog input frequency and resolution, with higher analog input frequency applications at ≥14-bit resolution being the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock. Considering an ideal ADC of infinite resolution where the step size and quantization error can be ignored, the available SNR can be expressed approximately by

$$SNR(\text{dB}) = 20 \times \log\left(\frac{1}{2\pi f_A t_J}\right)$$

where:
f_A is the highest analog frequency being digitized.
t_J is the rms jitter on the sampling clock.

Figure 57 shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB).

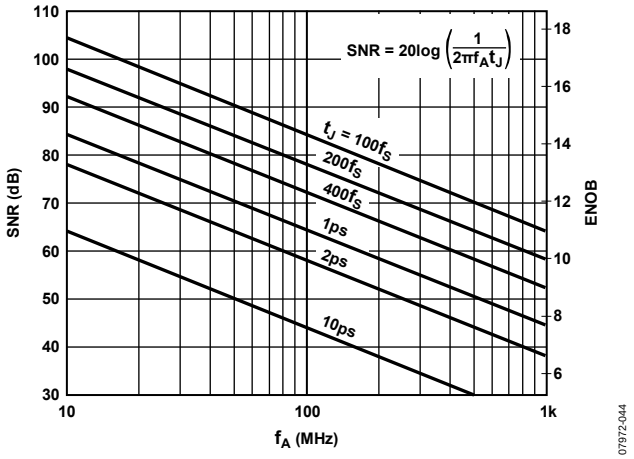

Figure 57. SNR and ENOB vs. Analog Input Frequency

See the AN-756 Application Note and the AN-501 Application Note at www.analog.com.

Many high performance ADCs feature differential clock inputs to simplify the task of providing the required low jitter clock on a noisy PCB. (Distributing a single-ended clock on a noisy PCB can result in coupled noise on the sample clock. Differential distribution has inherent common-mode rejection that can provide superior clock performance in a noisy environment.) The AD9516 features both LVPECL and LVDS outputs that provide differential clock outputs, which enable clock solutions that maximize converter SNR performance. The input requirements of the ADC (differential or single-ended, logic level, and termination) should be considered when selecting the best clocking/converter solution.

LVPECL CLOCK DISTRIBUTION

The LVPECL outputs of the AD9520 provide the lowest jitter clock signals available from the AD9520. The LVPECL outputs (because they are open emitter) require a dc termination to bias the output transistors. The simplified equivalent circuit in Figure 46 shows the LVPECL output stage.

In most applications, a LVPECL far-end Thevenin termination (see Figure 58) or Y-termination (see Figure 59) is recommended. In both cases, V_S of the receiving buffer should match VS_LVPECL. If it does not match, ac coupling is recommended (see Figure 60).

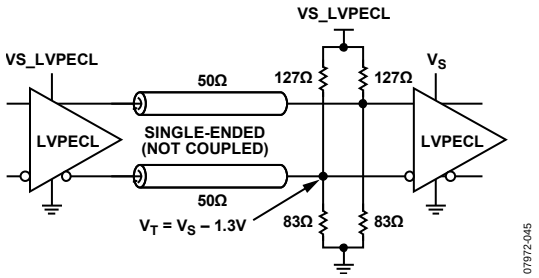

Figure 58. DC-Coupled 3.3 V LVPECL Far-End Thevenin Termination

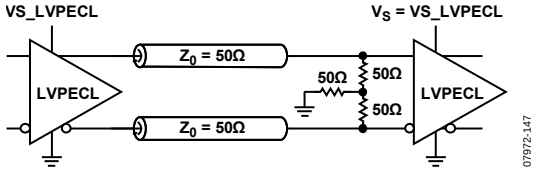

Figure 59. DC-Coupled 3.3 V LVPECL Y-Termination

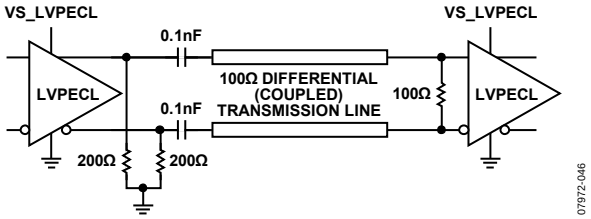

Figure 60. AC-Coupled LVPECL with Parallel Transmission Line

LVPECL Y-termination is an elegant termination scheme that uses the fewest components and offers both odd- and even-mode impedance matching. Even-mode impedance matching is an important consideration for closely coupled transmission lines at high frequencies. Its main drawback is that it offers limited flexibility for varying the drive strength of the emitter-follower LVPECL driver. This can be an important consideration when driving long trace lengths but is usually not an issue. In the case where VS_LVPECL = 2.5 V, the 50 Ω termination resistor connected to ground in Figure 59 should be changed to 19 Ω.

Thevenin-equivalent termination uses a resistor network to provide 50 Ω termination to a dc voltage that is below V_{OL} of the LVPECL driver. In this case, VS_LVPECL on the AD9520 should equal V_S of the receiving buffer. Although the resistor combination shown results in a dc bias point of VS_LVPECL – 2 V, the actual common-mode voltage is VS_LVPECL – 1.3 V because there is additional current flowing from the AD9520 LVPECL driver through the pull-down resistor.

The circuit is identical for the case where VS_LVPECL = 2.5 V, except that the pull-down resistor is 62.5 Ω and the pull-up is 250 Ω.

LVDS CLOCK DISTRIBUTION

The AD9516 provides four clock outputs (OUT6 to OUT9) that are selectable as either CMOS or LVDS level outputs. LVDS is a differential output option that uses a current mode output stage. The nominal current is 3.5 mA, which yields 350 mV of output swing across a 100 Ω resistor. The LVDS output meets or exceeds all ANSI/TIA/EIA-644 specifications.

A recommended termination circuit for the LVDS outputs is shown in Figure 61.

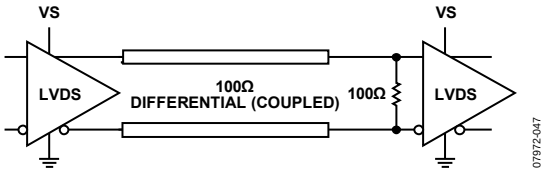

Figure 61. LVDS Output Termination

See the AN-586 Application Note at www.analog.com for more information on LVDS.

CMOS CLOCK DISTRIBUTION

The AD9516 provides four clock outputs (OUT6 to OUT9) that are selectable as either CMOS or LVDS level outputs. When selected as CMOS, each output becomes a pair of CMOS outputs, each of which can be individually turned on or off and set as noninverting or inverting. These outputs are 3.3 V CMOS compatible.

Whenever single-ended CMOS clocking is used, some general guidelines should be followed.

Point-to-point nets should be designed such that a driver has only one receiver on the net, if possible. This allows for simple termination schemes and minimizes ringing due to possible mismatched impedances on the net. Series termination at the source is generally required to provide transmission line matching and/or to reduce current transients at the driver. The value of the resistor is dependent on the board design and timing requirements (typically 10 Ω to 100 Ω is used). CMOS outputs are also limited in terms of the capacitive load or trace length that they can drive. Typically, trace lengths less than 3 inches are recommended to preserve signal rise/fall times and preserve signal integrity.

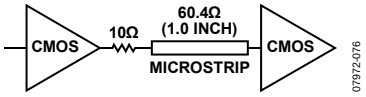

Figure 62. Series Termination of CMOS Output

Termination at the far end of the PCB trace is a second option. The CMOS outputs of the AD9516 do not supply enough current to provide a full voltage swing with a low impedance resistive, far-end termination, as shown in Figure 63. The far-end termination network should match the PCB trace impedance and provide the desired switching point. The reduced signal swing may still meet receiver input requirements in some applications. This can be useful when driving long trace lengths on less critical nets.

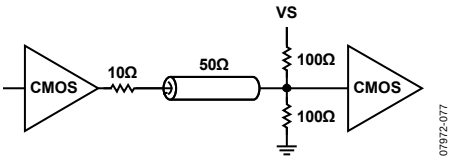

Figure 63. CMOS Output with Far-End Termination

Because of the limitations of single-ended CMOS clocking, consider using differential outputs when driving high speed signals over long traces. The AD9516 offers both LVPECL and LVDS outputs that are better suited for driving long traces where the inherent noise immunity of differential signaling provides superior performance for clocking converters.

OUTLINE DIMENSIONS

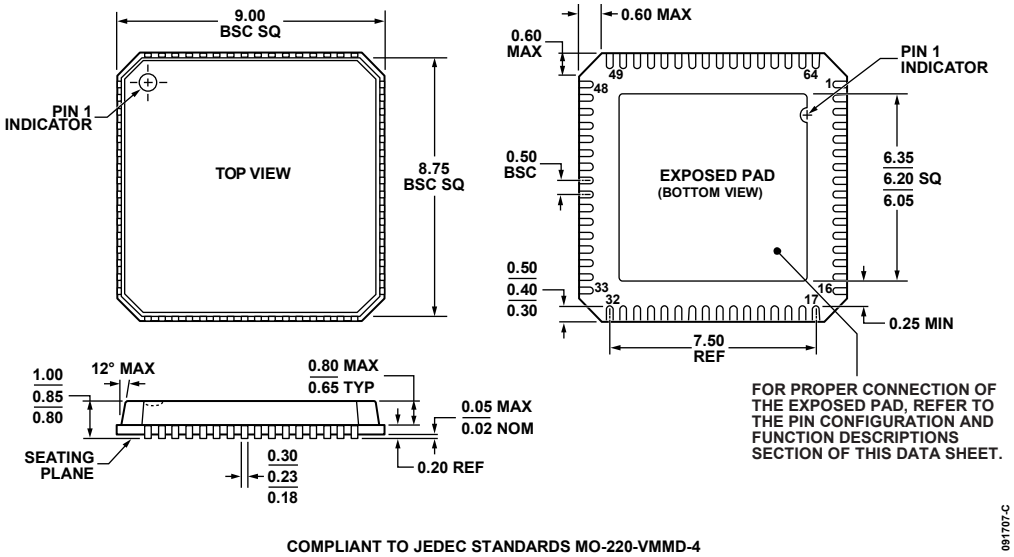

Figure 64. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9516-5BCPZ[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-4
AD9516-5BCPZ-REEL7[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-4
AD9516-5/PCBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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