CY7B9910
CY7B9920

Low Skew Clock Buffer

Features

- **All outputs skew <100 ps typical (250 max.)**
- **15- to 80-MHz output operation**
- **Zero input to output delay**
- **50% duty-cycle outputs**
- **Outputs drive 50Ω terminated lines**
- **Low operating current**
- **24-pin SOIC package**
- **Jitter: <200 ps peak to peak, <25 ps RMS**
- **Compatible with Pentium™-based processors**

Functional Description

The CY7B9910 and CY7B9920 Low Skew Clock Buffers offer low-skew system clock distribution. These multiple-output clock drivers optimize the timing of high-performance computer systems. Eight individual drivers can each drive terminated transmission lines with impedances as low as 50Ω while delivering minimal and specified output skews and full-swing logic levels (CY7B9910 TTL or CY7B9920 CMOS).

The completely integrated PLL allows "zero delay" capability. External divide capability, combined with the internal PLL, allows distribution of a low-frequency clock that can be multiplied by virtually any factor at the clock destination. This facility minimizes clock distribution difficulty while allowing maximum system clock speed and flexibility.

Block Diagram Description

Phase Frequency Detector and Filter

These two blocks accept inputs from the reference frequency (REF) input and the feedback (FB) input and generate correction information to control the frequency of the Voltage-Controlled Oscillator (VCO). These blocks, along with the VCO, form a Phase-Locked Loop (PLL) that tracks the incoming REF signal.

VCO

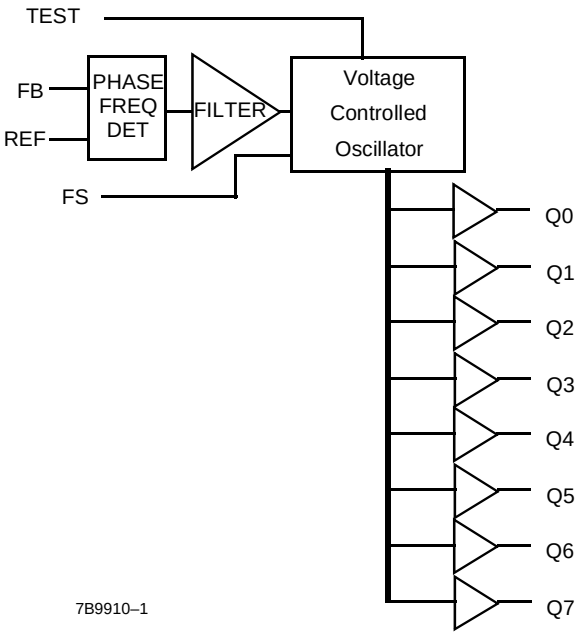
The VCO accepts analog control inputs from the PLL filter block and generates a frequency. The operational range of the VCO is determined by the FS control pin.

Test Mode

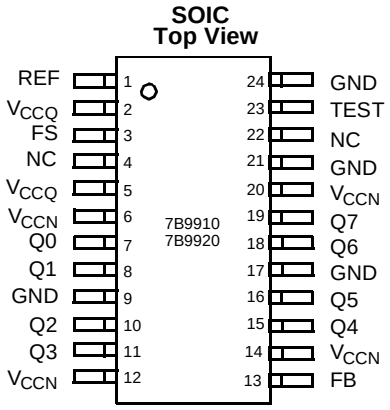
The TEST input is a three-level input. In normal system operation, this pin is connected to ground, allowing the CY7B9910/CY7B9920 to operate as explained above. (For testing purposes, any of the three-level inputs can have a removable jumper to ground, or be tied LOW through a 100Ω resistor. This will allow an external tester to change the state of these pins.)

If the TEST input is forced to its MID or HIGH state, the device will operate with its internal phase-locked loop disconnected, and input levels supplied to REF will directly control all outputs. Relative output to output functions are the same as in normal mode.

Logic Block Diagram



Pin Configuration



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Pin Definitions

Signal Name	I/O	Description
REF	I	Reference frequency input. This input supplies the frequency and timing against which all functional variation is measured.
FB	I	PLL feedback input (typically connected to one of the eight outputs).
FS[9,10,11]	I	Three-level frequency range select.
TEST	I	Three-level select. See Test Mode section.
Q[0..7]	O	Clock outputs.
V_{CCN}	PWR	Power supply for output drivers.
V_{CCQ}	PWR	Power supply for internal circuitry.
GND	PWR	Ground.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +7.0V

DC Input Voltage ..... –0.5V to +7.0V

Output Current into Outputs (LOW) .....64 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY7B9910		CY7B9920		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –16 mA	2.4				V
		V_{CC} = Min., I_{OH} =–40 mA			V_{CC}–0.75		
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 46 mA		0.45			V
		V_{CC} = Min., I_{OL} = 46 mA				0.45	
V_{IH}	Input HIGH Voltage (REF and FB inputs only)		2.0	V_{CC}	V_{CC} – 1.35	V_{CC}	V
V_{IL}	Input LOW Voltage (REF and FB inputs only)		–0.5	0.8	–0.5	1.35	V
V_{IHH}	Three-Level Input HIGH Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	V_{CC} – 1V	V_{CC}	V_{CC} – 1V	V_{CC}	V
V_{IMM}	Three-Level Input MID Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	V_{CC}/2 – 500 mV	V_{CC}/2 + 500 mV	V_{CC}/2 – 500 mV	V_{CC}/2 + 500 mV	V
V_{ILL}	Three-Level Input LOW Voltage (Test, FS)[1]	Min. ≤ V_{CC} ≤ Max.	0.0	1.0	0.0	1.0	V
I_{IH}	Input HIGH Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = Max.		10		10	µA
I_{IL}	Input LOW Leakage Current (REF and FB inputs only)	V_{CC} = Max., V_{IN} = 0.4V	–500		–500		µA
I_{IHH}	Input HIGH Current (Test, FS)	V_{IN} = V_{CC}		200		200	µA
I_{IMM}	Input MID Current (Test, FS)	V_{IN} = V_{CC}/2	–50	50	–50	50	µA

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions		CY7B9910 Min.	CY7B9910 Max.	CY7B9920 Min.	CY7B9920 Max.	Unit
I_{ILL}	Input LOW Current (Test, FS)	V_{IN} = GND			–200		–200	µA
I_{OS}	Output Short Circuit Current[2]	V_{CC} = Max., V_{OUT} = GND (25°C only)			–250		N/A	mA
I_{CCQ}	Operating Current Used by Internal Circuitry	V_{CCN}=V_{CCQ}=Max., All Input Selects Open	Com'l		85		85	mA
			Mil/Ind		90		90	
I_{CCN}	Output Buffer Current per Output Pair[3]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}			14		19	mA
PD	Power Dissipation per Output Pair[4]	V_{CCN} = V_{CCQ} = Max., I_{OUT} = 0 mA Input Selects Open, f_{MAX}			78		104[5]	mW

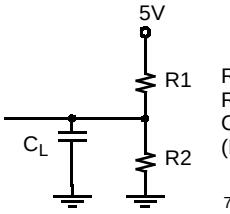
Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF

Notes:

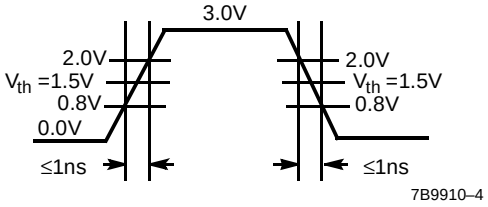
1. These inputs are normally wired to V_{CC}, GND, or left unconnected (actual threshold voltages vary as a percentage of V_{CC}). Internal termination resistors hold unconnected inputs at V_{CC}/2. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional t_{LOCK} time before all data sheet limits are achieved.
2. Tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only. CY7B9920 outputs are not short circuit protected.
3. Total output current per output pair can be approximated by the following expression that includes device current plus load current:
   CY7B9910:
   I_{CCN} = [(4 + 0.11F) + [((835 – 3F)/Z) + (.0022FC)]N] x 1.1
   CY7B9920:
   I_{CCN} = [(3.5+ .17F) + [((1160 – 2.8F)/Z) + (.0025FC)]N] x 1.1
   Where
   F = frequency in MHz
   C = capacitive load in pF
   Z = line impedance in ohms
   N = number of loaded outputs; 0, 1, or 2
   FC = F < C
4. Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:
   CY7B9910:
   PD = [(22 + 0.61F) + [((1550 – 2.7F)/Z) + (.0125FC)]N] x 1.1
   CY7B9920:
   PD = [(19.25+ 0.94F) + [((700 + 6F)/Z) + (.017FC)]N] x 1.1
   See note 3 for variable definition.
5. CMOS output buffer current and power dissipation specified at 50-MHz reference frequency.
6. Applies to REF and FB inputs only. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

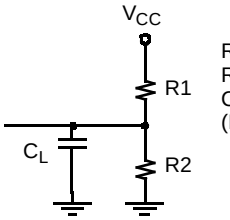


R1=130
R2=91
C_L = 50 pF (C_L = 30pF for –5 and – 2 devices)
(Includes fixture and probe capacitance)

TTL AC Test Load (CY7B9910)

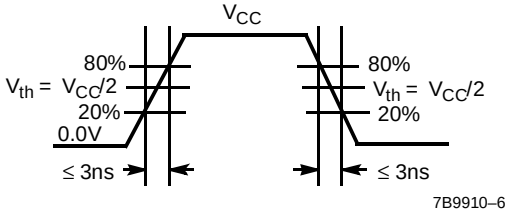


TTL Input Test Waveform (Cy7B9910)



R1=100
R2=100
C_L = 50 pF (C_L =30 pF for –5 and – 2devices)
(Includes fixture and probe capacitance)

CMOS AC Test Load (CY7B9920)



CMOS Input Test Waveform (CY7B9920)

Switching Characteristics Over the Operating Range[7]

Parameter	Description		CY7B9910–2[8] Min.	Typ.	Max.	CY7B9920–2[8] Min.	Typ.	Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[9, 10]	15		30	15		30	MHz
		FS = MID[9, 10]	25		50	25		50	
		FS = HIGH[9, 10, 11]	40		80	40		80[12]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[13, 14]			0.1	0.25		0.1	0.25	ns
t_{DEV}	Device-to-Device Skew[14, 15]				0.75			0.75	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.25	0.0	+0.25	–0.25	0.0	+0.25	ns
t_{ODCV}	Output Duty Cycle Variation[16]		–0.65	0.0	+0.65	–0.65	0.0	+0.65	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.0	1.2	0.5	2.0	2.5	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak			200			200	ps
		RMS			25			25	ps

Parameter	Description		CY7B9910–5 Min.	Typ.	Max.	CY7B9920–5 Min.	Typ.	Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[9, 10]	15		30	15		30	MHz
		FS = MID[9, 10]	25		50	25		50	
		FS = HIGH[9, 10, 11]	40		80	40		80[12]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[13, 14]			0.25	0.5		0.25	0.5	ns
t_{DEV}	Device-to-Device Skew[8, 15]				1.0			1.0	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.5	0.0	+0.5	–0.5	0.0	+0.5	ns
t_{ODCV}	Output Duty Cycle Variation[16]		–1.0	0.0	+1.0	–1.0	0.0	+1.0	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.0	1.5	0.5	2.0	3.0	ns

Parameter	Description		CY7B9910–5 Min.	CY7B9910–5 Typ.	CY7B9910–5 Max.	CY7B9920–5 Min.	CY7B9920–5 Typ.	CY7B9920–5 Max.	Unit
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.0	1.5	0.5	2.0	3.0	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak[8]			200			200	ps
		RMS[8]			25			25	ps

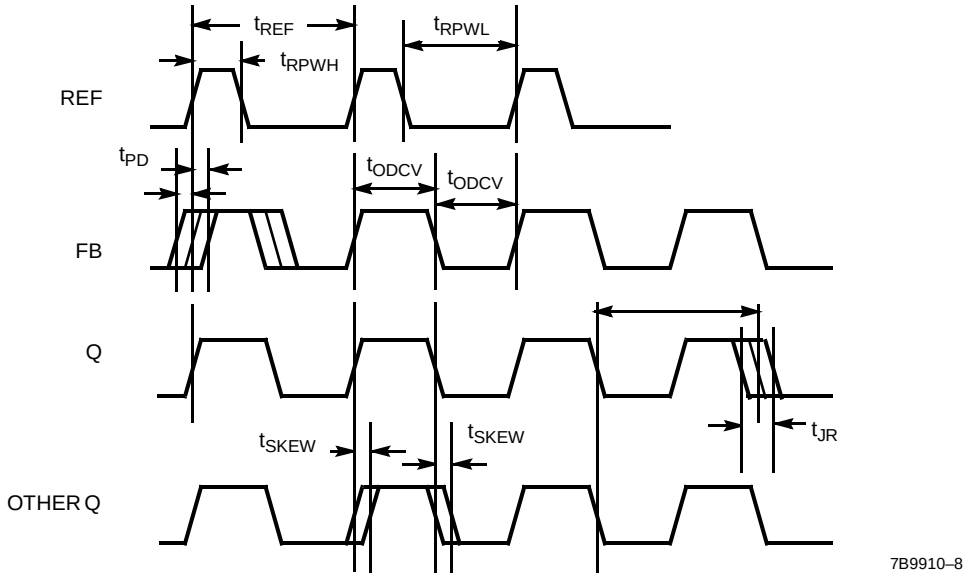
Notes:

7. Test measurement levels for the CY7B9910 are TTL levels (1.5V to 1.5V). Test measurement levels for the CY7B9920 are CMOS levels ($V_{CC}/2$ to $V_{CC}/2$). Test conditions assume signal transition times of 2ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.
8. Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.
9. For all three-state inputs, HIGH indicates a connection to V_{CC}, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.
10. The level to be set on FS is determined by the "normal" operating frequency (f_{NOM}) of the VCO (see Logic Block Diagram). The frequency appearing at the REF and FB inputs will be f_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be f_{NOM}/X when the device is configured for a frequency multiplication by using external division in the feedback path of value X.
11. When the FS pin is selected HIGH, the REF input must not transition upon power-up until V_{CC} has reached 4.3V.
12. Except as noted, all CY7B9920–2 and –5 timing parameters are specified to 80-MHz with a 30-pF load.
13. t_{SKEW} is defined as the time between the earliest and the latest output transition among all outputs when all are loaded with 50 pF and terminated with 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
14. t_{SKEW} is defined as the skew between outputs.
15. t_{DEV} is the output-to-output skew between any two outputs on separate devices operating under the same conditions (V_{CC}, ambient temperature, air flow, etc.).
16. t_{ODCV} is the deviation of the output from a 50% duty cycle.
17. Specified with outputs loaded with 30 pF for the CY7B99X0–2 and –5 devices and 50 pF for the CY7B99X0–7 devices. Devices are terminated through 50Ω to 2.06V (CY7B9910) or $V_{CC}/2$ (CY7B9920).
18. t_{ORISE} and t_{OFALL} measured between 0.8V and 2.0V for the CY7B9910 or $0.8V_{CC}$ and $0.2V_{CC}$ for the CY7B9920.
19. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{CC} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

Switching Characteristics Over the Operating Range[7] (continued)

Parameter	Description		CY7B9910–7 Min.	CY7B9910–7 Typ.	CY7B9910–7 Max.	CY7B9920–7 Min.	CY7B9920–7 Typ.	CY7B9920–7 Max.	Unit
f_{NOM}	Operating Clock Frequency in MHz	FS = LOW[9, 10]	15		30	15		30	MHz
		FS = MID[9, 10]	25		50	25		50	
		FS = HIGH[9, 10, 11]	40		80	40		80[12]	
t_{RPWH}	REF Pulse Width HIGH		5.0			5.0			ns
t_{RPWL}	REF Pulse Width LOW		5.0			5.0			ns
t_{SKEW}	Zero Output Skew (All Outputs)[13, 14]			0.3	0.75		0.3	0.75	ns
t_{DEV}	Device-to-Device Skew[8, 15]				1.5			1.5	ns
t_{PD}	Propagation Delay, REF Rise to FB Rise		–0.7	0.0	+0.7	–0.7	0.0	+0.7	ns
t_{ODCV}	Output Duty Cycle Variation[16]		–1.2	0.0	+1.2	–1.2	0.0	+1.2	ns
t_{ORISE}	Output Rise Time[17, 18]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{OFALL}	Output Fall Time[17, 18]		0.15	1.5	2.5	0.5	3.0	5.0	ns
t_{LOCK}	PLL Lock Time[19]				0.5			0.5	ms
t_{JR}	Cycle-to-Cycle Output Jitter	Peak to Peak[8]			200			200	ps
t_{JR}		RMS[8]			25			25	ps

AC Timing Diagrams



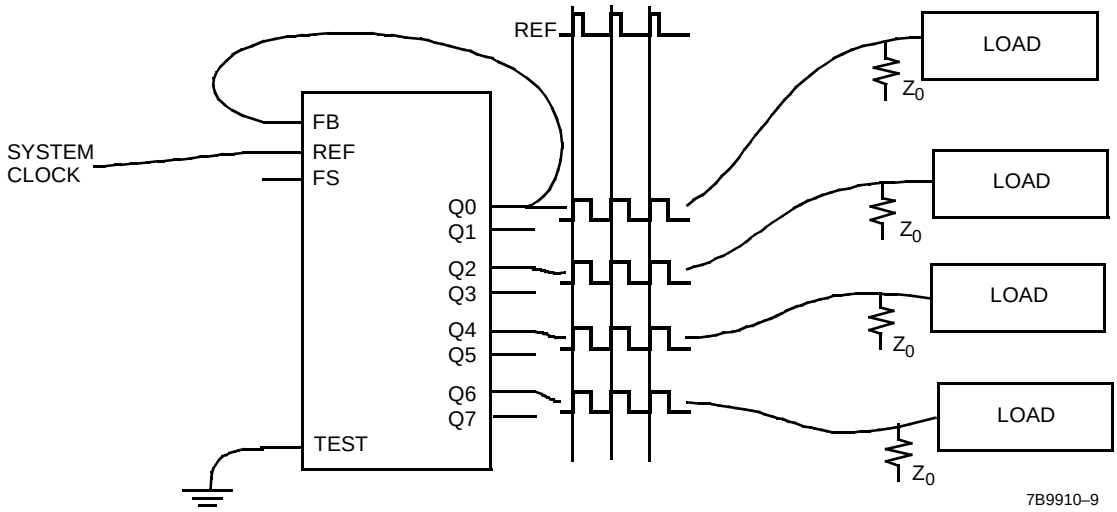


Figure 1. Zero-Skew and/or Zero-Delay Clock Driver

Operational Mode Descriptions

Figure 1 shows the device configured as a zero-skew clock buffer. In this mode the 7B9910/9920 can be used as the basis for a low-skew clock distribution tree. The outputs are aligned and may each drive a terminated transmission line to an independent load. The FB input can be tied to any output and the operating frequency range is selected with the FS pin. The low-skew specification, coupled with the ability to drive terminated transmission lines (with impedances as low as 50 ohms), allows efficient printed circuit board design.

Figure 2 shows the CY7B9910/9920 connected in series to construct a zero-skew clock distribution tree between boards. Cascaded clock buffers will accumulate low-frequency jitter because of the non-ideal filtering characteristics of the PLL filter. It is not recommended that more than two clock buffers be connected in series.

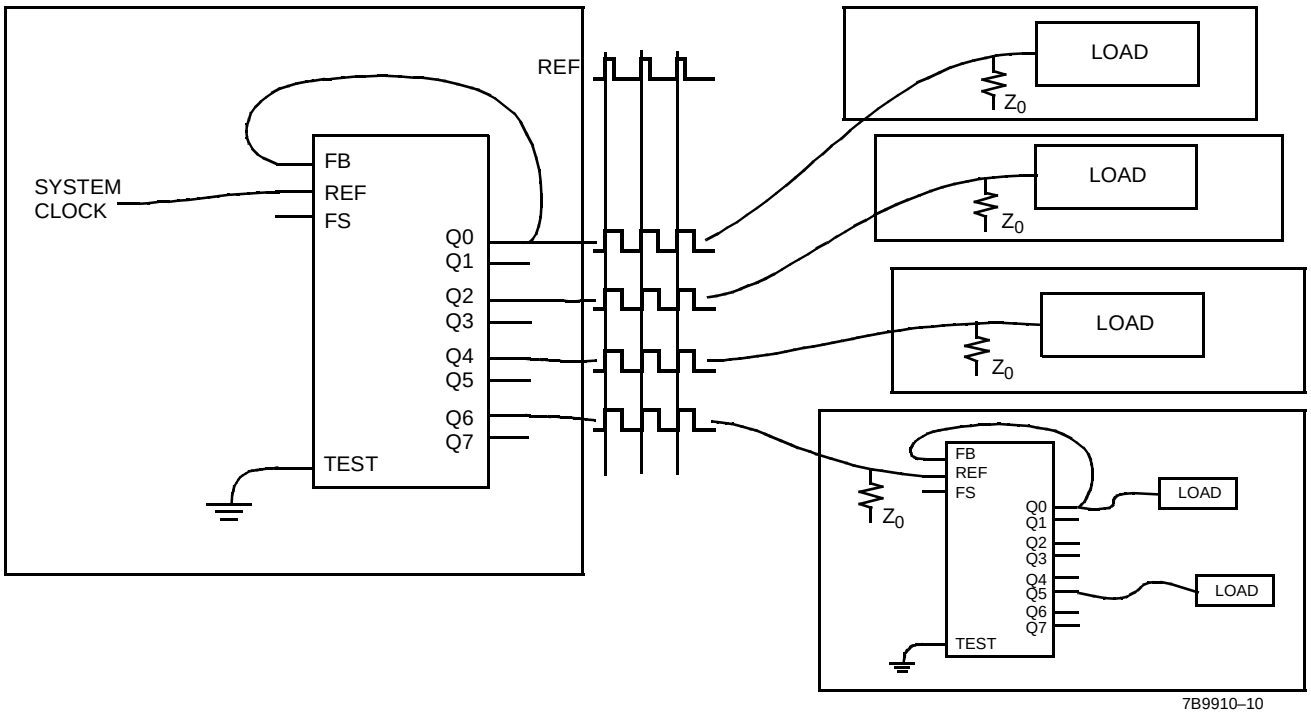


Figure 2. Board-to-Board Clock Distribution

Ordering Information

Accuracy (ps)	Ordering Code	Package Name	Package Type	Operating Range
250	CY7B9910–2SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–2SC	S13	24-Lead Small Outline IC	
500	CY7B9910–5SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9910–5SI	S13	24-Lead Small Outline IC	Industrial
	CY7B9920–5SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–5SI	S13	24-Lead Small Outline IC	Industrial
750	CY7B9910–7SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9910–7SI	S13	24-Lead Small Outline IC	Industrial
	CY7B9920–7SC	S13	24-Lead Small Outline IC	Commercial
	CY7B9920–7SI	S13	24-Lead Small Outline IC	Industrial

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Package Diagram

24-Lead (300-Mil) Molded SOIC S13