

Frequency Multiplier and Zero Delay Buffer

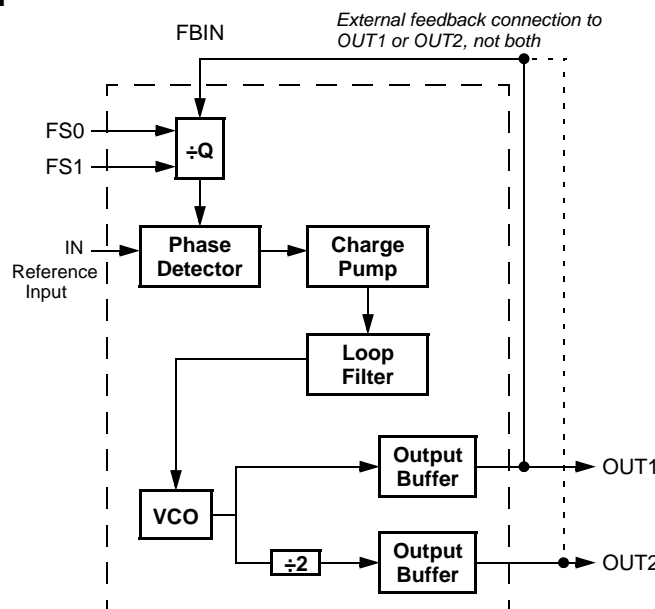
Features

- 90 ps Typical Jitter OUT2
- 200 ps Typical Jitter OUT1
- 65 ps Typical Output-to-output Skew
- 90ps Typical Propagation Delay
- Voltage range: 3.3V±5%, or 5V±10%
- Output Frequency Range: 5 MHz to 133 MHz
- Two Outputs
- Configuration options allow various multiplications of the reference frequency—refer to [Table 1](#) to determine the specific option which meets your multiplication needs
- Available in 8-pin SOIC Package

Table 1. Configuration Options

FBIN	FS0	FS1	OUT1	OUT2
OUT1	0	0	2 X REF	REF
OUT1	1	0	4 X REF	2 X REF
OUT1	0	1	REF	REF/2
OUT1	1	1	8 X REF	4 X REF
OUT2	0	0	4 X REF	2 X REF
OUT2	1	0	8 X REF	4 X REF
OUT2	0	1	2 X REF	REF
OUT2	1	1	16 X REF	8 X REF

Logic Block Diagram



Pinouts

Figure 1. Pin Configuration – 8-Pin SOIC Package

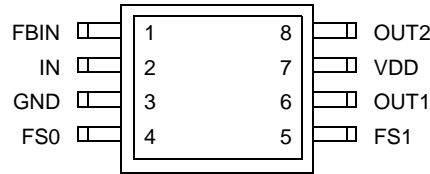


Table 2. Pin Definition

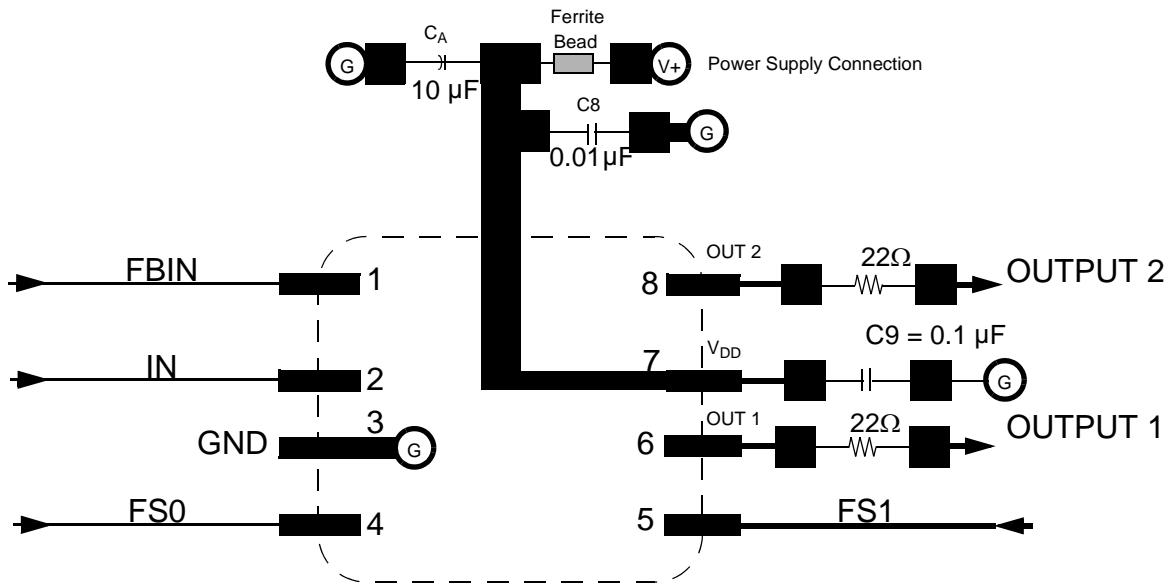
Pin Name	Pin No	Pin Type	Pin Description
IN	2	I	Reference Input: The output signals are synchronized to this signal.
FBIN	1	I	Feedback Input: This input must be fed by one of the outputs (OUT1 or OUT2) to ensure proper functionality. If the trace between FBIN and the output pin being used for feedback is equal in length to the traces between the outputs and the signal destinations, then the signals received at the destinations are synchronized to the REF signal input (IN).
OUT1	6	O	Output 1: The frequency of the signal provided by this pin is determined by the feedback signal connected to FBIN, and the FS0:1 inputs (see Table 1).
OUT2	8	O	Output 2: The frequency of the signal provided by this pin is one-half of the frequency of OUT1. See Table 1.
VDD	7	P	Power Connections: Connect to 3.3V or 5V. This pin should be bypassed with a 0.1- μ F decoupling capacitor. Use ferrite beads to help reduce noise for optimal jitter performance.
GND	3	P	Ground Connection: Connect all grounds to the common system ground plane.
FS0:1	4, 5	I	Function Select Inputs: Tie to V_{DD} (HIGH, 1) or GND (LOW, 0) as desired per Table 1.

Overview

The CY2302 is a two-output zero delay buffer and frequency multiplier. It provides an external feedback path allowing maximum flexibility when implementing the Zero Delay feature. This is explained further in the sections of this datasheet titled “How to Implement Zero Delay,” and “Inserting Other Devices in Feedback Path.”

The CY2302 is a pin-compatible upgrade of the Cypress W42C70-01. The CY2302 addresses some application dependent problems experienced by users of the older device.

Figure 2. Schematic/Suggested Layout



How to Implement Zero Delay

Typically, Zero Delay Buffers (ZDBs) are used because a designer wants to provide multiple copies of a clock signal in phase with each other. The whole concept behind ZDBs is that the signals at the destination chips are all going HIGH at the same time as the input to the ZDB. In order to achieve this, layout must compensate for trace length between the ZDB and the target devices. The method of compensation is described as follows.

External feedback is the trait that allows for this compensation. The PLL on the ZDB causes the feedback signal to be in phase with the reference signal. When laying out the board, match the trace lengths between the output being used for feedback and the FBIN input to the PLL.

If it is desirable to either add a little delay, or slightly precede the input signal, this may also be implemented by either making the trace to the FBIN pin a little shorter or a little longer than the traces to the devices being clocked.

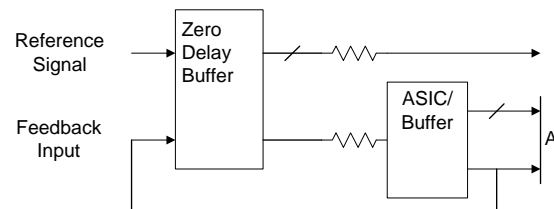
Inserting Other Devices in Feedback Path

Another nice feature available due to the external feedback is the ability to synchronize signals to the signal coming from some other device. This implementation can be applied to any device (ASIC, multiple output clock buffer/driver, etc.) that is put into the feedback path.

Referring to Figure 2, if the traces between the ASIC/Buffer and the destination of the clock signal(s) (A) are equal in length to the

trace between the buffer and the FBIN pin, the signals at the destination(s) device is driven HIGH at the same time when the Reference clock provided to the ZDB goes HIGH. Synchronizing the other outputs of the ZDB to the outputs from the ASIC/Buffer is more complex however, as any propagation delay from the ZDB output to the ASIC/Buffer output must be accounted for.

Figure 3. Six Output Buffer in the Feedback Path



Phase Alignment

In cases where OUT1 (i.e., the higher frequency output) is connected to FBIN input pin the output OUT2 rising edges may be either 0 or 180° phase aligned to the IN input waveform (as set randomly when the input and/or power is supplied). If OUT2 is desired to be rising-edge aligned to the IN input’s rising edge, then connect the OUT2 (i.e., the lowest frequency output) to the FBIN pin. This set-up provides a consistent input-output phase relationship.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on Any Pin with Respect to GND	-0.5 to +7.0	V
T_{STG}	Storage Temperature	-65 to +150	°C
T_A	Ambient Operating Temperature, Commercial	0 to +70	°C
	Ambient Operating Temperature, Industrial	-40 to +85	°C
T_B	Ambient Temperature under Bias	-55 to +125	°C
P_D	Power Dissipation	0.5	W

DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C or -40° to 85°C , $V_{DD} = 3.3\text{V} \pm 5\%$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current	Unloaded, 100 MHz	—	17	35	mA
V_{IL}	Input Low Voltage		—	—	0.8	V
V_{IH}	Input High Voltage		2.0	—		V
V_{OL}	Output Low Voltage	$I_{OL} = 12\text{ mA}$	—	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -12\text{ mA}$	2.4	—	—	V
I_{IL}	Input Low Current	$V_{IN} = 0\text{V}$	-40	—	5	μA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$	—	—	5	μA

DC Electrical Characteristics

$T_A = 0^\circ\text{C}$ to 70°C or -40° to 85°C , $V_{DD} = 5\text{V} \pm 10\%$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
I_{DD}	Supply Current	Unloaded, 100 MHz	—	37	50	mA
V_{IL}	Input Low Voltage		—	—	0.8	V
V_{IH}	Input High Voltage		2.0	—		V
V_{OL}	Output Low Voltage	$I_{OL} = 12\text{ mA}$	—	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -12\text{ mA}$	2.4	—		V
I_{IL}	Input Low Current	$V_{IN} = 0\text{V}$	-80	—	5	μA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$		—	5	μA

AC Electrical Characteristics

 $T_A = 0^\circ\text{C to } +70^\circ\text{C or } -40^\circ\text{ to } 85^\circ\text{C, } V_{DD} = 3.3\text{V } \pm 5\%^{[3]}$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency ^[1]		5	—	133	MHz
f_{OUT}	Output Frequency	OUT1 15-pF load	10	—	133	MHz
t_R	Output Rise Time	0.8V to 2.0V, 15-pF load	—	—	3.5	ns
t_F	Output Fall Time	2.0V to 0.8V, 15-pF load	—	—	2.5	ns
t_{CLKR}	Input Clock Rise Time ^[2]		—	—	10	ns
t_{CLKF}	Input Clock Fall Time ^[2]		—	—	10	ns
t_D	Duty Cycle	15-pF load ^[5]	40	50	60	%
t_{LOCK}	PLL Lock Time	Power supply stable	—	—	1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle	OUT1, $f_{OUT} > 30$ MHz	—	200	300	ps
		OUT2, $f_{OUT} > 30$ MHz	—	90	300	ps
t_{DC}	Die Out Time ^[6]		100	—	—	Clock Cycles
t_{SKEW}	Output-output Skew ^[4]		—	65	250	ps
t_{PD}	Propagation Delay ^[4]		-350	90	350	ps

AC Electrical Characteristics

 $T_A = 0^\circ\text{C to } +70^\circ\text{C or } -40^\circ\text{ to } 85^\circ\text{C, } V_{DD} = 5.0\text{V } \pm 10\%^{[3]}$

Parameter	Description	Test Condition	Min	Typ	Max	Unit
f_{IN}	Input Frequency ^[1]		5	—	133	MHz
f_{OUT}	Output Frequency	OUT1 15-pF load	10	—	133	MHz
t_R	Output Rise Time	0.8V to 2.0V, 15-pF load	—	—	2.5	ns
t_F	Output Fall Time	2.0V to 0.8V, 15-pF load	—	—	1.5	ns
t_{CLKR}	Input Clock Rise Time ^[2]		—	—	10	ns
t_{CLKF}	Input Clock Fall Time ^[2]		—	—	10	ns
t_D	Duty Cycle	15-pF load ^[5, 7]	40	50	60	%
t_{LOCK}	PLL Lock Time	Power supply stable	—	—	1.0	ms
t_{JC}	Jitter, Cycle-to-Cycle	OUT1, $f_{OUT} > 30$ MHz	—	200	300	ps
		OUT2, $f_{OUT} > 30$ MHz	—	90	300	ps
t_{DC}	Die out time ^[6]		100	—	—	Clock cycles
t_{SKEW}	Output-output Skew ^[4]		—	65	250	ps
t_{PD}	Propagation Delay ^[4]		-350	90	350	ps

Notes

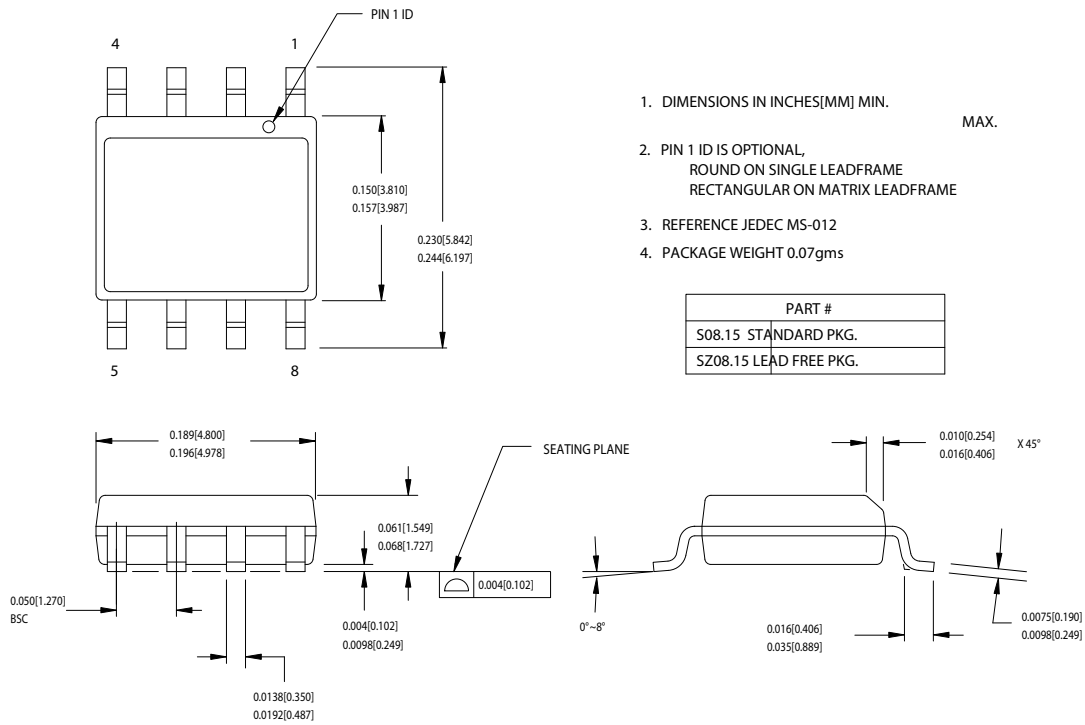
1. Input frequency is limited by output frequency range and input to output frequency multiplication factor (which is determined by circuit configuration).
2. Longer input rise and fall time degrades skew and jitter performance.
3. All AC specifications are measured with a 50Ω transmission line, load terminated with 50Ω to 1.4V.
4. Skew is measured at 1.4V on rising edges.
5. Duty cycle is measured at 1.4V.
6. 33 MHz reference input suddenly stopped (0 MHz). Number of cycles provided prior to output falling to <16 MHz.
7. Duty Cycle measured at 120 MHz. For 133 MHz, degrades to 35/65 worst case.

Ordering Information

Ordering Code	Package Type	Temperature Grade
CY2302SC-1	8-pin SOIC	Commercial (0° to 70°C)
CY2302SC-1T	8-pin SOIC – Tape and Reel	Commercial (0° to 70°C)
CY2302SI-1 ^[8]	8-pin SOIC	Industrial (-40° to 85°C)
Pb-free		
CY2302SXC-1	8-pin SOIC	Commercial (0° to 70°C)
CY2302SXC-1T	8-pin SOIC – Tape and Reel	Commercial (0° to 70°C)
CY2302SXI-1	8-pin SOIC	Industrial (-40° to 85°C)
CY2302SXI-1T	8-pin SOIC – Tape and Reel	Industrial (-40° to 85°C)

Package Diagram

Figure 4. 8-Pin (150-Mil) SOIC S8



51-85066-°C

Note

8. Not recommended for new designs. New designs should use the CY2302SXI-1.

Document History Page

Document Title: CY2302 Frequency Multiplier and Zero Delay Buffer Document Number: 38-07154				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	110264	SZV	12/18/01	Change from Spec number: 38-00794 to 38-07154
*A	394695	RGL	See ECN	Added typical char data Added Pb-free devices Added phase alignment paragraph
*B	2761988	KVM	09/10/09	Removed CY2302SI-1T from the Ordering Information table Added temperature values to Ordering Information table and to Absolute Maximum Table

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