NB6N239S

3.3 V, 3.0 GHz Any Differential Clock IN to LVDS OUT ÷1/2/4/8, ÷2/4/8/16 Clock Divider

Description

The NB6N239S is a high−speed, low skew clock divider with two divider circuits, each having selectable clock divide ratios; ÷1/2/4/8 and ÷2/4/8/16. Both divider circuits drive LVDS compatible outputs. (More device information on page 7). The NB6N239S is a member of the ECLinPS MAX™ family of high performance clock products.

Features

- Maximum Clock Input Frequency, 3.0 GHz (1.5 GHz with ÷1)
- Input Compatibility with LVDS/LVPECL/CML/HSTL
- Rise/Fall Time 120 ps Typical
- < 5 ps Typical Within Device Output Skew
- Example; 622.08 MHz Input Generates 38.88 MHz to 622.08 MHz Outputs
- Internal 50 Ω Termination Provided
- Random Clock Jitter < 2 ps RMS
- QA ÷1 Edge Aligned to QB ÷n Edge
- Operating Range: V_{CC} = 3.0 V to 3.465 V with GND = 0 V
- Master Reset for Synchronization of Multiple Chips
- V_{BBAC} Reference Output
- Synchronous Output Enable/Disable
- TIA/EIA – 644 Compliant
- Pb−Free Packages are Available

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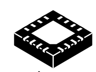
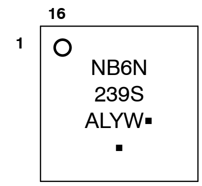
MARKING DIAGRAM*



Bottom View

QFN−16
MN SUFFIX
CASE 485G



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

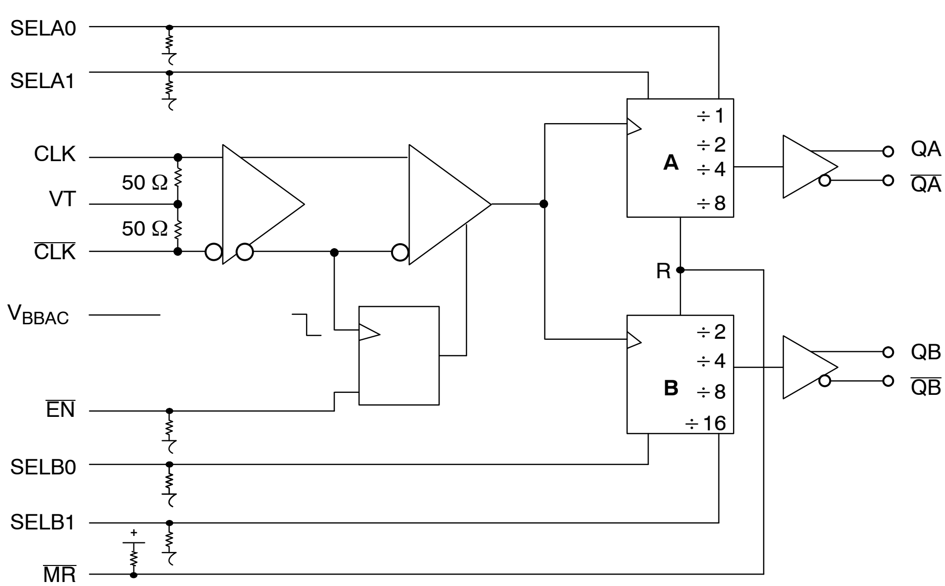


Figure 1. Simplified Logic Diagram

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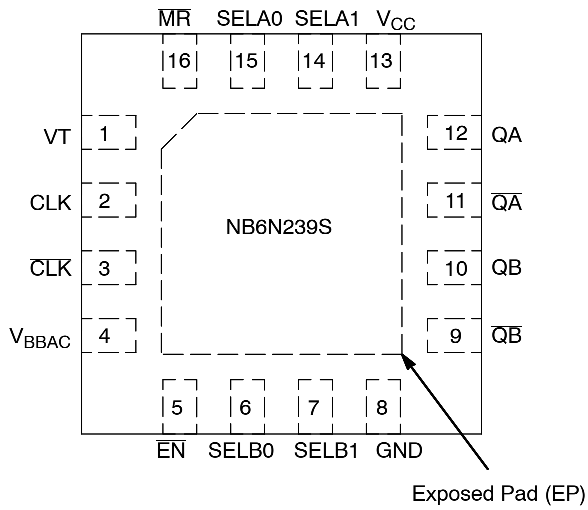

Figure 2. Pinout: QFN−16 (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VT		Internal 100 Ω Center−Tapped Termination Pin for CLK and $\overline{\text{CLK}}$.
2	CLK	LVDS, LVPECL, CML, HSTL Input	Noninverted Differential CLOCK Input.
3	$\overline{\text{CLK}}$	LVDS, LVPECL, CML, HSTL Input	Inverted Differential CLOCK Input.
4	V_{BBAC}		Output Voltage Reference for Capacitor Coupled Inputs, only.
5	$\overline{\text{EN}}$*	LVCMOS/LVTTL Input	Synchronous Output Enable
6	SELB0*	LVCMOS/LVTTL Input	Clock Divide Select Pin
7	SELB1*	LVCMOS/LVTTL Input	Clock Divide Select Pin
8	GND	Power Supply	Negative Supply Voltage
9	$\overline{\text{QB}}$	LVDS Output	Inverted Differential Output. Typically terminated with 100 Ω across differential outputs.
10	QB	LVDS Output	Noninverted Differential Output. Typically terminated with 100 Ω across differential outputs.
11	$\overline{\text{QA}}$	LVDS Output	Inverted Differential Output. Typically terminated with 100 Ω across differential outputs.
12	QA	LVDS Output	Noninverted Differential Output. Typically terminated with 100 Ω across differential outputs.
13	V_{CC}	Power Supply	Positive Supply Voltage.
14	SELA1*	LVCMOS/LVTTL Input	Clock Divide Select Pin
15	SELA0*	LVCMOS/LVTTL Input	Clock Divide Select Pin
16	$\overline{\text{MR}}$**	LVCMOS/LVTTL Input	Master Reset Asynchronous, Default Open High, Asserted LOW
	EP	Power Supply (OPT)	The Exposed Pad on the QFN−16 package bottom is thermally connected to the die for improved heat transfer out of package. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board.

*Pins will default LOW when left OPEN.
**Pins will default HIGH when left OPEN.

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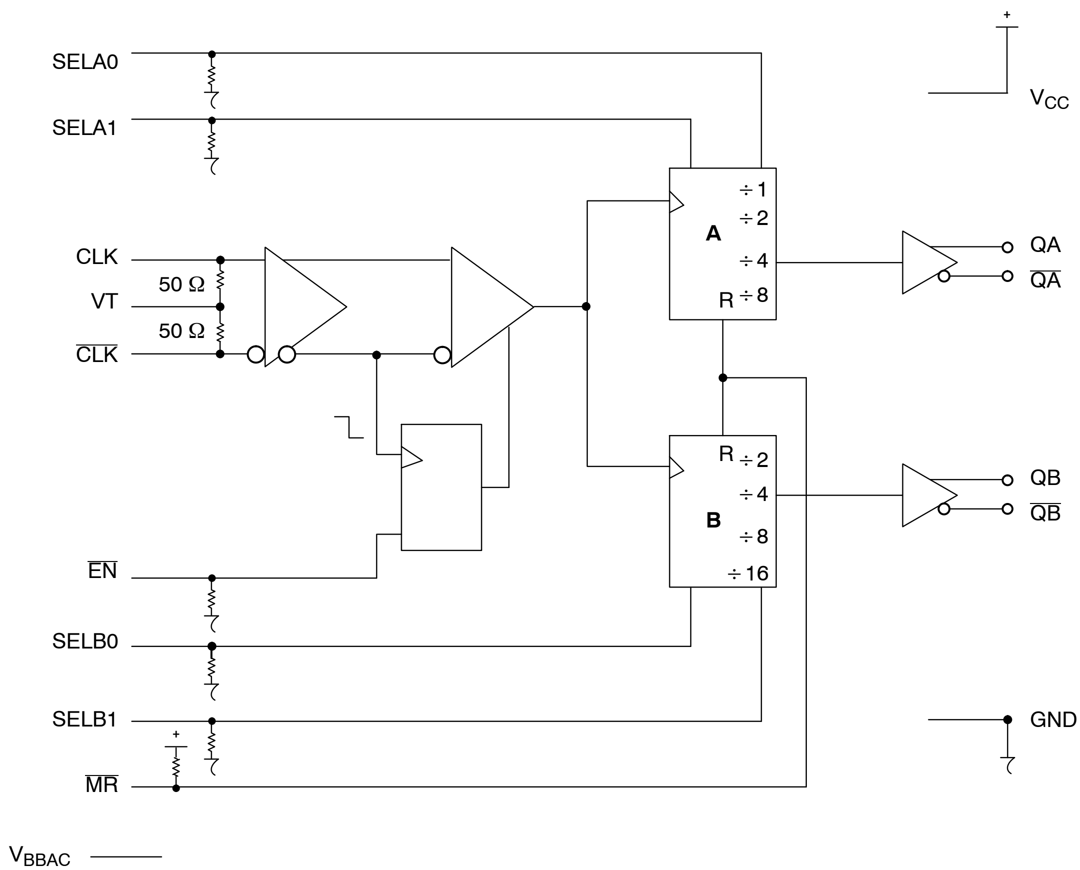

Figure 3. Logic Diagram

Table 2. FUNCTION TABLE

CLK	$\overline{EN}$*	$\overline{MR}$**	FUNCTION
_|‾	L	H	Divide
‾|_	H	H	Hold Q
X	X	L	Reset Q

Table 3. CLOCK DIVIDE SELECT, QA OUTPUTS

SELA1*	SELA0*		QA Outputs
L	L		Divide by 1
L	H		Divide by 2
H	L		Divide by 4
H	H		Divide by 8

Table 4. CLOCK DIVIDE SELECT, QB OUTPUTS

SELB1*	SELB0*		QB Outputs
L	L		Divide by 2
L	H		Divide by 4
H	L		Divide by 8
H	H		Divide by 16

_|‾ = Low−to−High Transition
‾|_ = High−to−Low Transition
X = Don’t Care
*Pins will default LOW when left OPEN.
**Pins will default HIGH when left OPEN.

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Table 5. ATTRIBUTES

Characteristics		Value	
Internal Input Pulldown Resistor Internal Input Pullup Resistor		75 kΩ 75 kΩ	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1500 V > 100 V > 1000 V	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Pb Pkg	Pb−Free Pkg
	QFN−16	Level 1	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
Transistor Count		370	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test			

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 6. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Mode Power Supply	GND = 0 V		3.6	V
V_I	Input Voltage	GND = 0 V	GND ≤ V_I ≤ V_{CC}	3.6	V
I_{SC}	Output Short Circuit Current Line−to−Line Line−to−GND TIA/EIA − 644 Compliant			12 24	mA mA
I_{BBAC}	V_{BBAC} Sink/Source Current			± 0.5	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 lfpm 500 lfpm		41.6 35.2	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board		4.0	°C/W
T_{sol}	Wave Solder Pb Pb−Free			265 265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 7. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS
(V_{CC} = 3.0 V to 3.465 V, GND = 0 V)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current (Inputs and Outputs OPEN)				35	45	55				mA
V_{OH}	Output HIGH Voltage (Notes 2)			1600			1600			1600	mV
V_{OL}	Output LOW Voltage (Notes 2)	900			900			900			mV
V_{OD}	Differential Output Voltage (Figure 21)	250		450	250		450	250		450	mV
ΔV_{OD}	V_{OD} Magnitude Change	0		50	0		50	0		50	mV
V_{OS}	Offset Voltage (Figure 21)	1125		1375	1125		1375	1125		1375	mV
ΔV_{OS}	V_{OS} Magnitude Change	0		50	0		50	0		50	mV
DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED (Figures 7, 10)											
V_{th}	Input Threshold Reference Voltage (Note 3)	100		V_{CC} − 100	100		V_{CC} − 100	100		V_{CC} − 100	mV
V_{IH}	Single−ended Input HIGH Voltage	V_{th} + 100		V_{CC}	V_{th} + 100		V_{CC}	V_{th} + 100		V_{CC}	mV
V_{IL}	Single−ended Input LOW Voltage	GND		V_{th} − 100	GND		V_{th} − 100	GND		V_{th} − 100	mV
V_{BBAC}	Output Voltage Reference @ 100 μA (Note 6) V_{CC} = 3.3 V	V_{CC}−1460 1840	V_{CC}−1330 1970	V_{CC}−1200 2100	V_{CC}−1460 1840	V_{CC}−1340 1960	V_{CC}−1200 2100	V_{CC}−1460 1840	V_{CC}−1350 1950	V_{CC}−1200 2100	mV
DIFFERENTIAL INPUT DRIVEN DIFFERENTIALLY (Figures 8, 9, 11) (Note 5)											
V_{IHD}	Differential Input HIGH Voltage	100		V_{CC}	100		V_{CC}	100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{CC} − 100	GND		V_{CC} − 100	GND		V_{CC} − 100	mV
V_{CMR}	Input Common Mode Range (Differential Cross−point Voltage) (Note 4)	50		V_{CC} – 50	50		V_{CC} – 50	50		V_{CC} – 50	mV
V_{ID}	Differential Input Voltage ($V_{IHD(CLK)}$ − $V_{ILD(CLK)}$) and ($\overline{V_{IHD(CLK)}}$ − $\overline{V_{ILD(CLK)}}$)	100		V_{CC} − GND	100		V_{CC} − GND	100		V_{CC} − GND	mV
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

2. Outputs loaded with 100 Ω across LVDS outputs.
3. V_{th} is applied to the complementary input when operating in single−ended mode.
4. $VCMR_{MIN}$ varies 1:1 with GND, $VCMR_{MAX}$ varies 1:1 with V_{CC}.
5. Input and output voltage swing is a single−ended measurement operating in differential mode.
6. V_{BBAC} used to rebias capacitor−coupled inputs only (see Figures 16 and 17).

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Table 8. DC CHARACTERISTICS, LVTTL/LVCMOS INPUTS (V_{CC} = 3.0 V to 3.465 V, GND = 0 V, T_A = −40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage (LVCMOS/LVTTL)	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage (LVCMOS/LVTTL)	GND		0.8	V
I_{IH}	Input HIGH Current	−150		150	μA
I_{IL}	Input LOW Current	−150		150	μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 9. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.465 V; GND = 0 V (Note 7)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{inMAX}	Maximum Input CLOCK Frequency QA/QB = (÷2, ÷4, ÷8, ÷16) QA = (÷1)	 3.0 1.5			 3.0 1.5			 3.0 1.5			GHz
V_{OUTPP}	Output Voltage Amplitude (Notes 9, 10) QA(÷2, 4, 8), QB(÷n) $f_{in} \le$ 3.0 GHz QA(÷1), QB(÷n) $f_{in} \le$ 1.5 GHz	 200 200	 350 350	 450 450	 200 200	 350 350	 450 450	 200 200	 350 350	 450 450	mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential @ 50 MHz CLK, Qn $\overline{MR}$, Qn	550 420		780 660	550 420		780 660	550 420		780 660	ps
t_{RR}	Reset Recovery	0	−90		0	−90		0	−90		ps
t_s	Setup Time @ 50 MHz $\overline{EN}$, CLK SELA/B, CLK	0 0	−60 −300		0 0	−60 −300		0 0	−60 −300		ps
t_h	Hold Time @ 50 MHz CLK, $\overline{EN}$ CLK, SELA/B	150 700	65 200		150 700	65 200		150 700	65 200		ps
t_{skew}	Within−Device Skew @ 50 MHz (Note 8) Device−to−Device Skew (Note 8) Duty Cycle Skew (Note 8)		5 25 25	30 80 40		5 30 30	30 90 45		6 30 30	35 90 45	ps
t_{PW}	Minimum Pulse Width $\overline{MR}$	550			550			550			ps
t_{JITTER}	RMS Random Clock Jitter			2			2			2	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 9)	100		V_{CC} −GND	100		V_{CC} −GND	100		V_{CC} −GND	mV
t_r t_f	Output Rise/Fall Times @ 50 MHz Qn, $\overline{Qn}$ (20% − 80%)	70	120	190	70	120	190	70	120	190	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Measured using a 750 mV, 50% duty cycle clock source. All loading with 100 Ω across LVDS outputs.
8. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.
9. Input and output voltage swing is a single−ended measurement operating in differential mode.
10. Output Voltage Amplitude ($V_{OHCLK} - V_{OLCLK}$) at input CLOCK frequency, f_{in}. The output frequency, f_{out}, is the input CLOCK frequency divided by n, $f_{out} = f_{in} \div n$. Input CLOCK frequency is ≤3.0 GHz.

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Application Information

The NB6N239S is a high−speed, low skew clock divider with two divider circuits, each having selectable clock divide ratios; ÷1/2/4/8 and ÷2/4/8/16. Both divider circuits drive differential LVDS compatible outputs. The internal dividers are synchronous to each other. Therefore, the common output edges are precisely aligned.

The NB6N239S clock inputs can be driven by a variety of differential signal level technologies including LVDS, LVPECL, HSTL, or CML. The differential clock input buffer employs a pair of internal 50 Ω termination resistors in a 100 Ω center−tapped configuration and accessible via the VT pin. This feature provides transmission line termination on−chip, at the receiver end, eliminating external components. The V_{BBAC} reference output is recommended to be used to rebias differential or single−ended input capacitor−coupled CLOCK signals. For the capacitor−coupled CLK and/or $\overline{CLK}$ inputs, V_{BBAC} should be connected to the V_T pin and bypassed to ground with a 0.01 μF capacitor. Inputs CLK and $\overline{CLK}$ must be signal driven or auto oscillation may result.

The common enable ($\overline{EN}$) is synchronous so that the internal divider flip−flops will only be enabled/disabled when the internal clock is in the LOW state. This avoids any chance of generating a runt pulse on the internal clock when the device is enabled/disabled, as can happen with an asynchronous control. The internal enable flip−flop is clocked on the falling edge of the input clock. Therefore, all associated specification limits are referenced to the negative edge of the clock input.

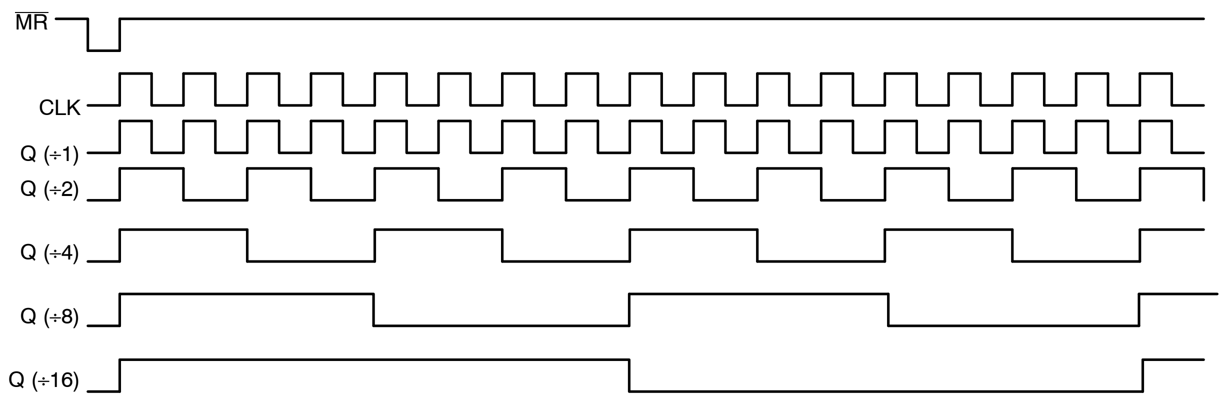
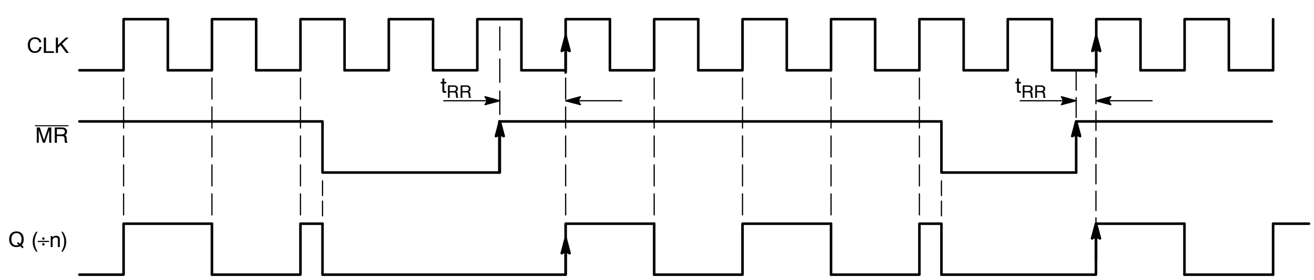


Figure 4. Timing Diagram



NOTE: On the rising edge of $\overline{MR}$, Q goes HIGH after the first rising edge of CLK.

Figure 5. Master Reset Timing Diagram

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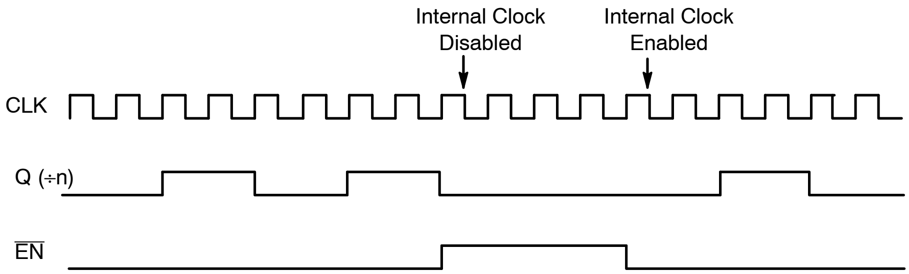

Figure 6. Output Enable Timing Diagrams

The $\overline{EN}$ signal will "freeze" the internal divider flip−flops on the first falling edge of CLK after its assertion. The internal divider flip−flops will maintain their state during the freeze. When $\overline{EN}$ is deasserted (LOW), and after the next falling edge of CLK, then the internal divider flip−flops will "unfreeze" and continue to their next state count with proper phase relationships.

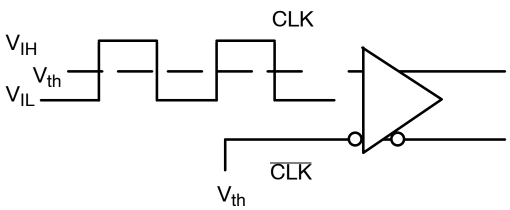

Figure 7. Differential Input Driven Single−Ended

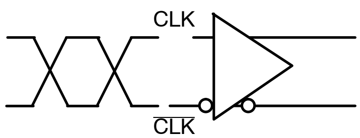

Figure 8. Differential Inputs Driven Differentially

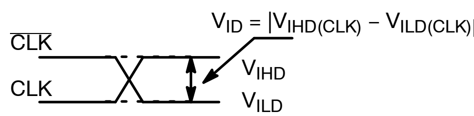

Figure 9. Differential Inputs Driven Differentially

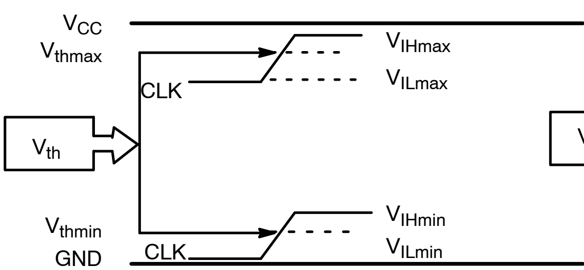

Figure 10. V_{th} Diagram

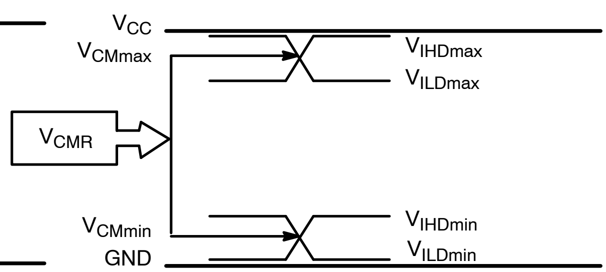

Figure 11. V_{CMR} Diagram

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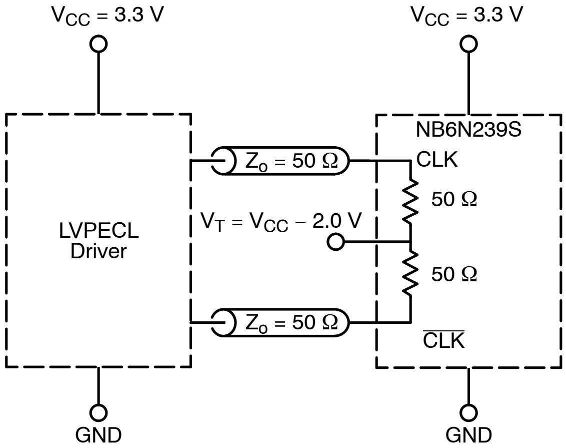

Figure 12. LVPECL Interface

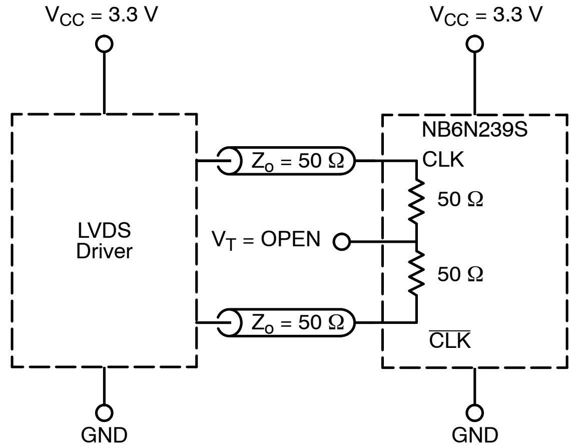

Figure 13. LVDS Interface

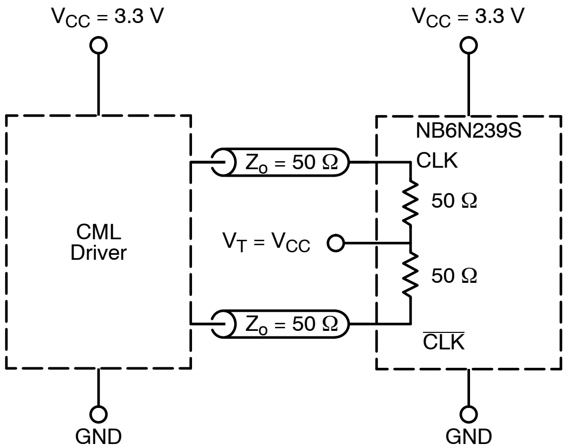

Figure 14. Standard 50 Ω Load CML Interface

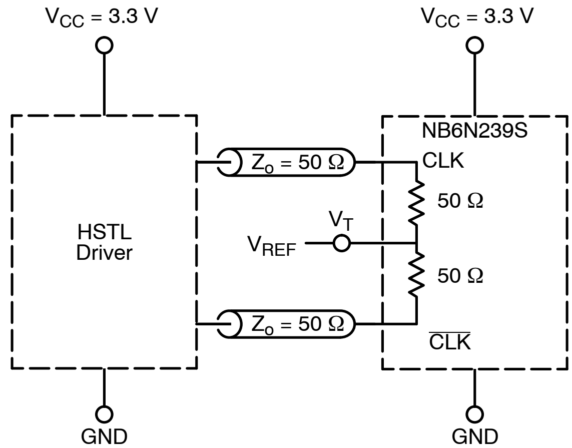

Figure 15. Standard 50 Ω Load HSTL Interface

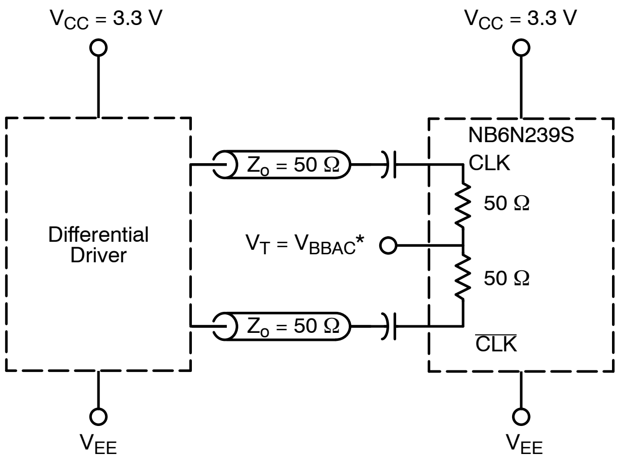

Figure 16. Capacitor−Coupled Differential Interface (V_T Connected to V_{BBAC})

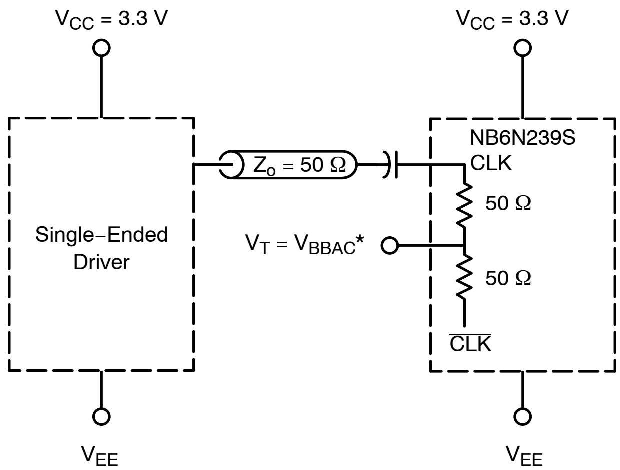

Figure 17. Capacitor−Coupled Single−Ended Interface (V_T Connected to V_{BBAC})

*V_{BBAC} bypassed to ground with a 0.01 μF capacitor.

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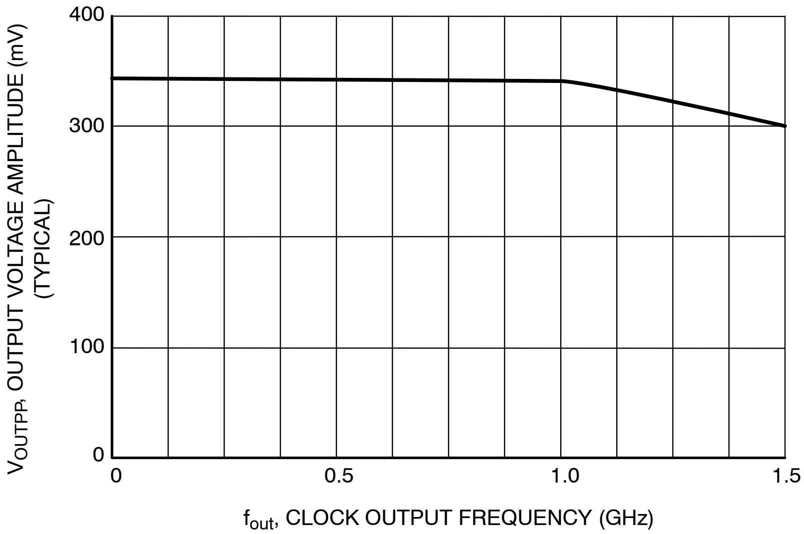

Figure 18. Output Voltage Amplitude (V_{OUTPP}) versus Output Clock Frequency at 25°C (Typical)
f_{out} (QA/QB) = f_{in} ÷ n;
For n = 2, 4, 8, 16; $f_{in} \leq$ 3.0 GHz
For n = 1; $f_{in} \leq$ 1.5 GHz

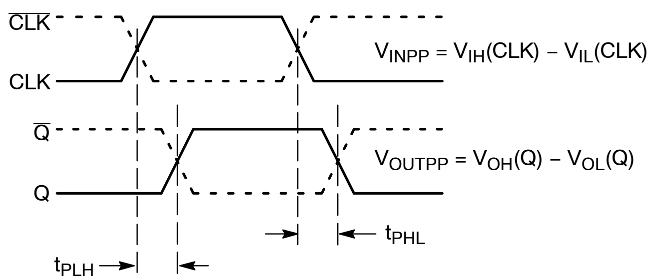

Figure 19. AC Reference Measurement

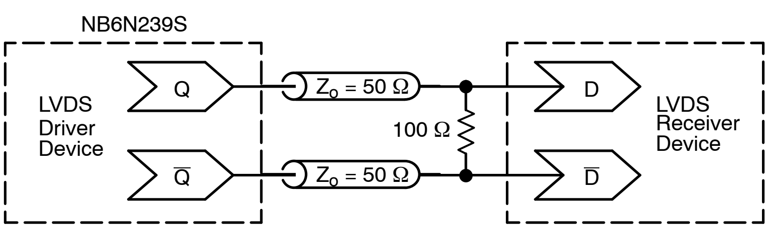

Figure 20. Typical LVDS Termination for Output Driver and Device Evaluation,
If Receiver Has On−chip Termination, 100 Ω Resistor is Not Needed

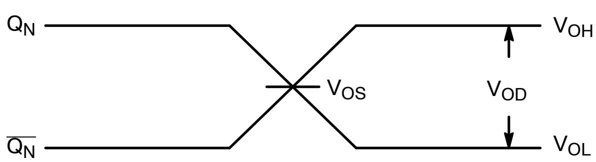

Figure 21. LVDS Output

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ORDERING INFORMATION

Device	Package	Shipping†
NB6N239SMN	QFN−16, 3 x 3 mm	123 Units / Rail
NB6N239SMNG	QFN−16, 3 x 3 mm (Pb−Free)	123 Units / Rail
NB6N239SMNR2	QFN−16, 3 x 3 mm	3000 / Tape & Reel
NB6N239SMNR2G	QFN−16, 3 x 3 mm (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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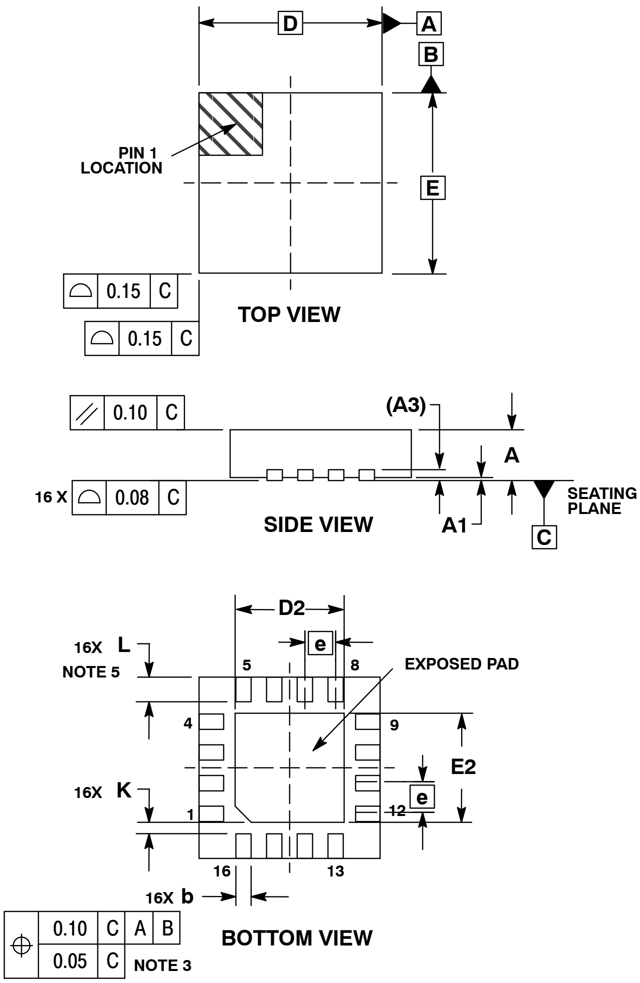
PACKAGE DIMENSIONS

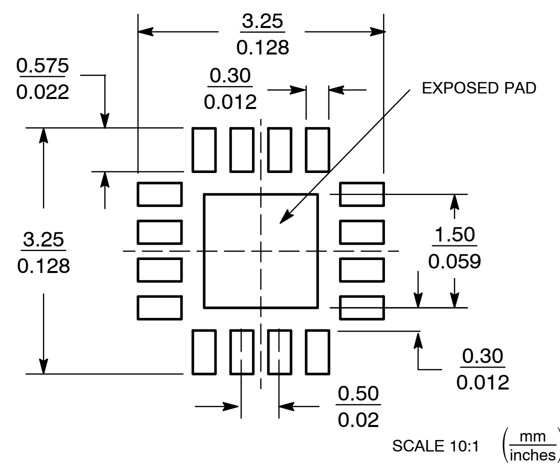
16 PIN QFN
CASE 485G−01
ISSUE C



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	3.00 BSC	
D2	1.65	1.85
E	3.00 BSC	
E2	1.65	1.85
e	0.50 BSC	
K	0.18 TYP	
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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