



# ICS8761

LOW VOLTAGE, LOW SKEW,  
PCI / PCI-X CLOCK GENERATOR

## GENERAL DESCRIPTION

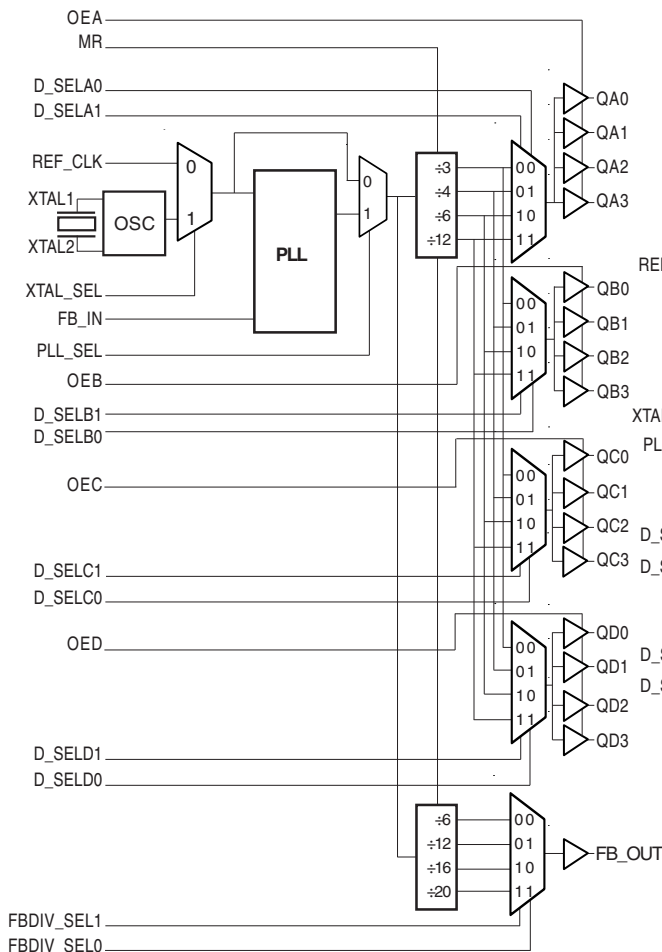
The ICS8761 is a low voltage, low skew PCI / PCI-X Clock Generator. The ICS8761 has a selectable REF\_CLK or crystal input. The REF\_CLK input accepts LVCMOS or LVTTTL input levels. The ICS8761 has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiplying and regenerating clocks with “zero delay”. Using a 20MHz or 25MHz crystal or a 33.333MHz or 66.666MHz reference frequency, the ICS8761 will generate output frequencies of 33.333MHz, 66.666MHz, 100MHz and 133.333MHz simultaneously.

The low impedance LVCMOS/LVTTTL outputs of the ICS8761 are designed to drive 50Ω series or parallel terminated transmission lines.

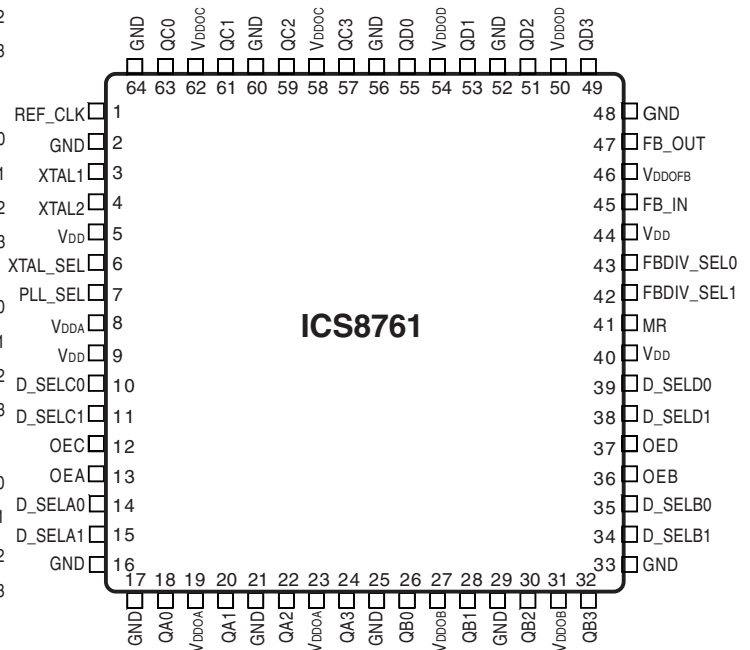
## FEATURES

- Fully integrated PLL
- Seventeen LVCMOS/LVTTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS/LVTTTL REF\_CLK
- Maximum output frequency: 166.67MHz
- Maximum crystal input frequency: 38MHz
- Maximum REF\_CLK input frequency: 83.333MHz
- Individual banks with selectable output dividers for generating 33.333MHz, 66.66MHz, 100MHz and 133.333MHz simultaneously
- Separate feedback control for generating PCI / PCI-X frequencies from a 20MHz or 25MHz crystal or 33.333MHz or 66.666MHz reference frequency
- Cycle-to-cycle jitter: 70ps (maximum)
- Period jitter, RMS: 17ps (maximum)
- Output skew: 230ps (maximum)
- Bank skew: 40ps (maximum)
- Static phase offset:  $0 \pm 150$ ps (maximum)
- Full 3.3V or 3.3V core, 2.5V multiple output supply modes
- 0°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**ICS8761**  
64-Lead LQFP  
10mm x 10mm x 1.4mm package body  
Y package  
Top View



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**TABLE 1. PIN DESCRIPTIONS**

| Number   | Name                  | Type   |          | Description  |
|--|-----------------------|--------|----------|--|
| 1  | REF_CLK               | Input  | Pulldown | Reference clock input. LVCMOS / LVTTTL interface levels.   |
| 2, 16, 17,<br>21, 25, 29,<br>33, 48, 52,<br>56, 60, 64 | GND                   | Power  |          | Power supply ground.   |
| 3, 4   | XTAL1,<br>XTAL2       | Input  |          | Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.   |
| 5, 9, 40, 44   | V <sub>DD</sub>       | Power  |          | Core supply pins.  |
| 6  | XTAL_SEL              | Input  | Pullup   | Selects between crystal oscillator or reference clock as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_CLK when LOW. LVCMOS / LVTTTL interface levels.                                  |
| 7  | PLL_SEL               | Input  | Pullup   | Selects between PLL and bypass mode. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTTL interface levels.  |
| 8  | V <sub>DDA</sub>      | Power  |          | Analog supply pin. See Applications Note for filtering.  |
| 10, 11   | D_SELCO,<br>D_SELCO1  | Input  | Pulldown | Selects divide value for Bank C outputs as described in Table 3. LVCMOS / LVTTTL interface levels.   |
| 12   | OEC                   | Input  | Pullup   | Determines state of Bank C outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTTL interface levels.  |
| 13   | OEA                   | Input  | Pullup   | Determines state of Bank A outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTTL interface levels.  |
| 14, 15   | D_SELA0,<br>D_SELA1   | Input  | Pulldown | Selects divider value for Bank A outputs as described in Table 3. LVCMOS / LVTTTL interface levels.  |
| 18, 20,<br>22, 24                                      | QA0, QA1,<br>QA2, QA3 | Output |          | Bank A clock outputs. 15Ω typical output impedance. LVCMOS / LVTTTL interface levels.  |
| 19, 23   | V <sub>DDOA</sub>     | Power  |          | Output supply pins for Bank A outputs.   |
| 26, 28,<br>30, 32                                      | QB0, QB1,<br>QB2, QB3 | Output |          | Bank B clock outputs. 15Ω typical output impedance. LVCMOS / LVTTTL interface levels.  |
| 27, 31   | V <sub>DDOB</sub>     | Power  |          | Output supply pins for Bank B outputs.   |
| 34, 35   | D_SELB1,<br>D_SELB0   | Input  | Pulldown | Selects divider value for Bank B outputs as described in Table 3. LVCMOS / LVTTTL interface levels.  |
| 36   | OEB                   | Input  | Pullup   | Determines state of Bank B outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTTL interface levels.  |
| 37   | OED                   | Input  | Pullup   | Determines state of Bank D outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTTL interface levels.  |
| 38, 39   | D_SELD1,<br>D_SELD0   | Input  | Pulldown | Selects divider value for Bank D outputs as described in Table 3. LVCMOS / LVTTTL interface levels.  |
| 41   | MR                    | Input  | Pulldown | Active HIGH Master reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels. |
| 42   | FBDIV_SEL1            | Input  | Pulldown | Selects divider value for bank feedback output as described in Table 3. LVCMOS / LVTTTL interface levels.  |
| 43   | FBDIV_SEL0            | Input  | Pullup   | Selects divider value for bank feedback output as described in Table 3. LVCMOS / LVTTTL interface levels.  |
| 45   | FB_IN                 | Input  | Pulldown | Feedback input to phase detector for generating clocks with "zero delay". LVCMOS / LVTTTL interface levels.  |



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| Number         | Name                          | Type   | Description  |
|----------------|-------------------------------|--------|--|
| 46             | V <sub>DDO<sub>FB</sub></sub> | Power  | Output supply pin for FB_Out output.   |
| 47             | FB_OUT                        | Output | Feedback output. Connect to FB_IN. 15Ω typical output impedance. LVCMOS / LVTTTL interface levels. |
| 49, 51, 53, 55 | QD3, QD2, QD1, QD0            | Output | Bank D clock outputs. 15Ω typical output impedance. LVCMOS / LVTTTL interface levels.              |
| 50, 54         | V <sub>DDOD</sub>             | Power  | Output supply pins for Bank D outputs.   |
| 57, 59, 61, 63 | QC3, QC2, QC1, QC0            | Output | Bank C clock outputs. 15Ω typical output impedance. LVCMOS / LVTTTL interface levels.              |
| 58, 62         | V <sub>DDOC</sub>             | Power  | Output supply pins for Bank C outputs.   |

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

| Symbol                | Parameter  | Test Conditions   | Minimum | Typical | Maximum | Units |
|-----------------------|--|---|---------|---------|---------|-------|
| C <sub>IN</sub>       | Input Capacitance                                  |   |         | 4       |         | pF    |
| R <sub>PULLUP</sub>   | Input Pullup Resistor                              |   |         |         | 51      | kΩ    |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor                            |   |         |         | 51      | kΩ    |
| C <sub>PD</sub>       | Power Dissipation Capacitance (per output); NOTE 1 | V <sub>DD</sub> , V <sub>DDA</sub> = 3.465V; V <sub>DDOx</sub> = 3.465V |         |         | 9       | pF    |
|                       |  | V <sub>DD</sub> , V <sub>DDA</sub> = 3.465V; V <sub>DDOx</sub> = 2.625V |         |         | 11      | pF    |
| R <sub>OUT</sub>      | Output Impedance                                   |   |         | 15      |         | Ω     |

NOTE 1: V<sub>DDOx</sub> denotes V<sub>DDOA</sub>, V<sub>DDOB</sub>, V<sub>DDOC</sub>, V<sub>DDOD</sub>, V<sub>DDO<sub>FB</sub></sub>.

TABLE 3A. OUTPUT CONTROL PIN FUNCTION TABLE

| Inputs |     |     |     |     | Outputs |         |         |         |
|--------|-----|-----|-----|-----|---------|---------|---------|---------|
| MR     | OEA | OEB | OEC | OED | QA0:QA3 | QB0:QB3 | QC0:QC3 | QD0:QD3 |
| 1      | 1   | 1   | 1   | 1   | LOW     | LOW     | LOW     | LOW     |
| 0      | 1   | 1   | 1   | 1   | Active  | Active  | Active  | Active  |
| X      | 0   | 0   | 0   | 0   | HiZ     | HiZ     | HiZ     | HiZ     |

TABLE 3B. OPERATING MODE FUNCTION TABLE

| Inputs  | Operating Mode |
|---------|----------------|
| PLL_SEL |                |
| 0       | Bypass         |
| 1       | PLL            |

TABLE 3C. PLL INPUT FUNCTION TABLE

| Inputs   |                 |
|----------|-----------------|
| XTAL_SEL | PLL Input       |
| 0        | REF_CLK         |
| 1        | XTAL Oscillator |



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**TABLE 3D. CONTROL FUNCTION TABLE**

| Inputs  |         |            |            |                                 | Outputs    |                |               |
|---------|---------|------------|------------|---------------------------------|------------|----------------|---------------|
|         |         |            |            |                                 | PLL_SEL =1 | Frequency      |               |
| D_SELx1 | D_SELx0 | FBDIV_SEL1 | FBDIV_SEL0 | Reference Frequency Range (MHz) | QX0:QX3    | QX0:QX3 (MHz)  | FB_OUT (MHz)  |
| 0       | 0       | 0          | 0          | 41.6 - 83.33                    | x 2        | 83.33 - 166.67 | 41.6 - 83.33  |
| 0       | 0       | 0          | 1          | 20.83 - 41.67                   | x 4        | 83.33 - 166.67 | 20.83 - 41.67 |
| 0       | 0       | 1          | 0          | 15.62 - 31.25                   | x 5.33     | 83.33 - 166.67 | 15.62 - 31.25 |
| 0       | 0       | 1          | 1          | 12.5 - 25                       | x 6.67     | 83.33 - 166.67 | 12.5 - 25     |
| 0       | 1       | 0          | 0          | 41.6 - 83.33                    | x 1.5      | 62.4 - 125     | 41.6 - 83.33  |
| 0       | 1       | 0          | 1          | 20.83 - 41.67                   | x 3        | 62.4 - 125     | 20.83 - 41.67 |
| 0       | 1       | 1          | 0          | 15.62 - 31.25                   | x 4        | 62.4 - 125     | 15.62 - 31.25 |
| 0       | 1       | 1          | 1          | 12.5 - 25                       | x 5        | 62.4 - 125     | 12.5 - 25     |
| 1       | 0       | 0          | 0          | 41.6 - 83.33                    | x 1        | 41.6 - 83.33   | 41.6 - 83.33  |
| 1       | 0       | 0          | 1          | 20.83 - 41.67                   | x 2        | 41.6 - 83.33   | 20.83 - 41.67 |
| 1       | 0       | 1          | 0          | 15.62 - 31.25                   | x 2.67     | 41.6 - 83.33   | 15.62 - 31.25 |
| 1       | 0       | 1          | 1          | 12.5 - 25                       | x 3.33     | 41.6 - 83.33   | 12.5 - 25     |
| 1       | 1       | 0          | 0          | 41.6 - 83.33                    | ÷ 2        | 20.8 - 41.67   | 41.6 - 83.33  |
| 1       | 1       | 0          | 1          | 20.83 - 41.67                   | ÷ 1        | 20.8 - 41.67   | 20.83 - 41.67 |
| 1       | 1       | 1          | 0          | 15.62 - 31.25                   | x 1.33     | 20.8 - 41.67   | 15.62 - 31.25 |
| 1       | 1       | 1          | 1          | 12.5 - 25                       | x 1.67     | 20.8 - 41.67   | 12.5 - 25     |

NOTE: D\_SELx1 denotes D\_SELA1, D\_SELB1, D\_SELc1, and D\_SELD1. D\_SELx0 denotes D\_SELA0, D\_SELB0, D\_SELc0, and D\_SELD0. QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.

**TABLE 3E. CONTROL FUNCTION TABLE (PCI CONFIGURATION)**

| Inputs  |         |            |            |                           | Outputs     |               |              |
|---------|---------|------------|------------|---------------------------|-------------|---------------|--------------|
|         |         |            |            |                           | PLL_SEL = 1 | Frequency     |              |
| D_SELx1 | D_SELx0 | FBDIV_SEL1 | FBDIV_SEL0 | Reference Frequency (MHz) | QX0:QX3     | QX0:QX3 (MHz) | FB_OUT (MHz) |
| 0       | 0       | 0          | 0          | 66.67                     | x 2         | 133           | 66.67        |
| 0       | 0       | 0          | 1          | 33.33                     | x 4         | 133           | 33.33        |
| 0       | 0       | 1          | 0          | 25                        | x 5.33      | 133           | 25           |
| 0       | 0       | 1          | 1          | 20                        | x 6.67      | 133           | 20           |
| 0       | 1       | 0          | 0          | 66.67                     | x 1.5       | 100           | 66.67        |
| 0       | 1       | 0          | 1          | 33.33                     | x 3         | 100           | 33.33        |
| 0       | 1       | 1          | 0          | 25                        | x 4         | 100           | 25           |
| 0       | 1       | 1          | 1          | 20                        | x 5         | 100           | 20           |
| 1       | 0       | 0          | 0          | 66.67                     | x 1         | 66.67         | 66.67        |
| 1       | 0       | 0          | 1          | 33.33                     | x 2         | 66.67         | 33.33        |
| 1       | 0       | 1          | 0          | 25                        | x 2.67      | 66.67         | 25           |
| 1       | 0       | 1          | 1          | 20                        | x 3.33      | 66.67         | 20           |
| 1       | 1       | 0          | 0          | 66.67                     | ÷ 2         | 33.33         | 66.67        |
| 1       | 1       | 0          | 1          | 33.33                     | ÷ 1         | 33.33         | 33.33        |
| 1       | 1       | 1          | 0          | 25                        | x 1.33      | 33.33         | 25           |
| 1       | 1       | 1          | 1          | 20                        | x 1.67      | 33.33         | 20           |

NOTE: D\_SELx1 denotes D\_SELA1, D\_SELB1, D\_SELc1, and D\_SELD1. D\_SELx0 denotes D\_SELA0, D\_SELB0, D\_SELc0, and D\_SELD0. QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.



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## ABSOLUTE MAXIMUM RATINGS

|  |                            |
|--|----------------------------|
| Supply Voltage, $V_{DD}$                 | 4.6V                       |
| Inputs, $V_I$                            | -0.5V to $V_{DD} + 0.5V$   |
| Outputs, $V_O$                           | -0.5V to $V_{DDOX} + 0.5V$ |
| Package Thermal Impedance, $\theta_{JA}$ | 41.1°C/W (0 lfpm)          |
| Storage Temperature, $T_{STG}$           | -65°C to 150°C             |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

| Symbol     | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$   | Core Supply Voltage           |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDA}$  | Analog Supply Voltage         |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDOX}$ | Output Supply Voltage; NOTE 1 |                 | 3.135   | 3.3     | 3.465   | V     |
| $I_{DD}$   | Power Supply Current          |                 |         |         | 175     | mA    |
| $I_{DDA}$  | Analog Supply Current         |                 |         |         | 55      | mA    |
| $I_{DDOX}$ | Output Supply Current; NOTE 2 |                 |         |         | 25      | mA    |

NOTE 1:  $V_{DDOX}$  denotes  $V_{DDOA}$ ,  $V_{DDOB}$ ,  $V_{DDOC}$ ,  $V_{DDOD}$ , and  $V_{DDOFB}$ .

NOTE 2:  $I_{DDOX}$  denotes  $I_{DDOA}$ ,  $I_{DDOB}$ ,  $I_{DDOC}$ ,  $I_{DDOD}$ , and  $I_{DDOFB}$ .

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDOX} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

| Symbol     | Parameter                     | Test Conditions | Minimum | Typical | Maximum | Units |
|------------|-------------------------------|-----------------|---------|---------|---------|-------|
| $V_{DD}$   | Core Supply Voltage           |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDA}$  | Analog Supply Voltage         |                 | 3.135   | 3.3     | 3.465   | V     |
| $V_{DDOX}$ | Output Supply Voltage; NOTE 1 |                 | 2.375   | 2.5     | 2.625   | V     |
| $I_{DD}$   | Power Supply Current          |                 |         |         | 160     | mA    |
| $I_{DDA}$  | Analog Supply Current         |                 |         |         | 50      | mA    |
| $I_{DDOX}$ | Output Supply Current; NOTE 2 |                 |         |         | 210     | mA    |

NOTE 1:  $V_{DDOX}$  denotes  $V_{DDOA}$ ,  $V_{DDOB}$ ,  $V_{DDOC}$ ,  $V_{DDOD}$ , and  $V_{DDOFB}$ .

NOTE 2:  $I_{DDOX}$  denotes  $I_{DDOA}$ ,  $I_{DDOB}$ ,  $I_{DDOC}$ ,  $I_{DDOD}$ , and  $I_{DDOFB}$ .



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**TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

| Symbol    | Parameter                    | Test Conditions   | Minimum                             | Typical | Maximum        | Units   |
|-----------|------------------------------|---|-------------------------------------|---------|----------------|---------|
| $V_{IH}$  | Input High Voltage           | OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1:D_SELD1, PLL_SEL, FBDIV_SEL0, FBDIV_SEL1 | 2                                   |         | $V_{DD} + 0.3$ | V       |
|           |                              | REF_CLK   | 2                                   |         | $V_{DD} + 0.3$ | V       |
| $V_{IL}$  | Input Low Voltage            | OEA:OED, XTAL_SEL, MR, D_SELA0:D_SELD0, FB_IN, D_SELA1, D_SELD1, PLL_SEL                        | -0.3                                |         | 0.8            | V       |
|           |                              | REF_CLK   | -0.3                                |         | 1.3            | V       |
| $I_{IH}$  | Input High Current           | D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL1                                | $V_{DD} = V_{IN} = 3.465V$          |         | 150            | $\mu A$ |
|           |                              | XTAL_SEL, PLL_SEL, FBDIV_SEL0, OEA:OED  | $V_{DD} = V_{IN} = 3.465V$          |         | 5              | $\mu A$ |
| $I_{IL}$  | Input Low Current            | D_SELA0:D_SELD0, FB_IN, MR, D_SELA1:D_SELD1, REF_CLK, FBDIV_SEL1                                | $V_{DD} = 3.465V,$<br>$V_{IN} = 0V$ |         | -5             | $\mu A$ |
|           |                              | XTAL_SEL, PLL_SEL, FBDIV_SEL0, OEA:OED  | $V_{DD} = 3.465V,$<br>$V_{IN} = 0V$ |         | -150           | $\mu A$ |
| $V_{OH}$  | Output High Voltage; NOTE 1  |   | $V_{DDOX} = 3.465V$                 |         | 2.6            | V       |
|           |                              |   | $V_{DDOX} = 2.625V$                 |         | 1.8            | V       |
| $V_{OL}$  | Output Low Voltage; NOTE 1   |   | $V_{DDOX} = 3.465V$<br>or $2.625V$  |         | 0.5            | V       |
| $I_{OZL}$ | Output Tristate Current Low  |   | -5                                  |         |                | $\mu A$ |
| $I_{OZH}$ | Output Tristate Current High |   |                                     |         | 5              | $\mu A$ |

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDOX}/2$ . See Parameter Measurement Information section, "Output Load Test Circuit" Diagrams.

**TABLE 5. CRYSTAL CHARACTERISTICS**

| Parameter                          | Test Conditions | Minimum     | Typical | Maximum | Units    |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation                |                 | Fundamental |         |         |          |
| Frequency                          |                 | 10          |         | 38      | MHz      |
| Equivalent Series Resistance (ESR) |                 |             |         | 70      | $\Omega$ |
| Shunt Capacitance                  |                 |             | 7       |         | pF       |
| Drive Level                        |                 |             |         | 1       | mW       |

**TABLE 6. PLL INPUT REFERENCE CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

| Symbol    | Parameter           | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|---------------------|-----------------|---------|---------|---------|-------|
| $f_{REF}$ | Reference Frequency |                 | 10      |         | 83.33   | MHz   |



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**TABLE 7A. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

| Symbol         | Parameter                           | Test Conditions                   | Minimum | Typical | Maximum | Units |
|----------------|-------------------------------------|-----------------------------------|---------|---------|---------|-------|
| $f_{MAX}$      | Output Frequency                    |                                   |         |         | 166.67  | MHz   |
| $t(\emptyset)$ | Static Phase Offset; NOTE 1, 7      | $f = 50MHz$                       | -150    |         | 150     | ps    |
| $tsk(b)$       | Bank Skew; NOTE 2, 6                |                                   |         |         | 40      | ps    |
| $tsk(o)$       | Output Skew; NOTE 3, 6              |                                   |         |         | 230     | ps    |
| $f_{jit(cc)}$  | Cycle-to-Cycle Jitter; 6            | $f = 50MHz$ ; NOTE 4, 7           |         |         | 70      | ps    |
|                |                                     | $f = 25MHz$ XTAL,<br>133.3MHz out |         |         | 190     | ps    |
| $f_{jit(per)}$ | Period Jitter, RMS; NOTE 4, 6, 7, 8 |                                   |         |         | 17      | ps    |
| $t_L$          | PLL Lock Time                       |                                   |         |         | 1       | ms    |
| $t_R$          | Output Rise Time                    | 20% to 80%                        | 300     |         | 800     | ps    |
| $t_F$          | Output Fall Time                    | 20% to 80%                        | 300     |         | 800     | ps    |
| odc            | Output Duty Cycle; NOTE 5, 7        |                                   | 45      |         | 55      | %     |

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured from  $V_{DD}/2$  of the input to  $V_{DDOX}/2$  of the output.

NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDOX}/2$ .

NOTE 4: Jitter performance using LVCMOS inputs.

NOTE 5: Measured using REF\_CLK. For XTAL input, refer to Application Note.

NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 7: Tested with  $D\_SELXX = 10$  (divide by 6);  $FBDIV\_SEL = 00$  (divide by 6).

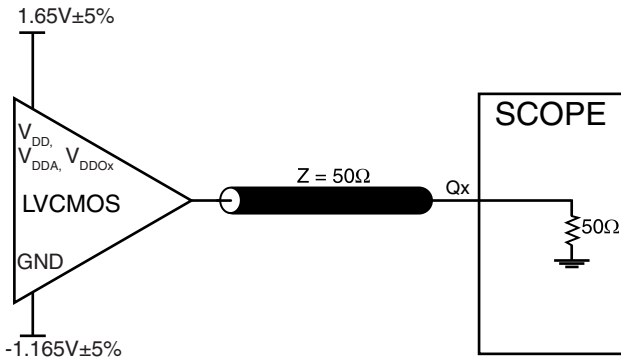
NOTE 8: This parameter is defined as an RMS value.

**TABLE 7B. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDOX} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $85^\circ C$**

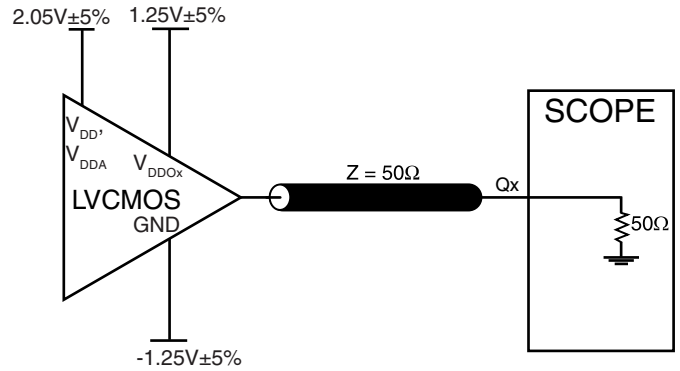
| Symbol         | Parameter                           | Test Conditions                   | Minimum | Typical | Maximum | Units |
|----------------|-------------------------------------|-----------------------------------|---------|---------|---------|-------|
| $f_{MAX}$      | Output Frequency                    |                                   |         |         | 166.67  | MHz   |
| $t(\emptyset)$ | Static Phase Offset; NOTE 1, 7      | $f = 50MHz$                       | -350    |         | 20      | ps    |
| $tsk(b)$       | Bank Skew; NOTE 2, 6                |                                   |         |         | 40      | ps    |
| $tsk(o)$       | Output Skew; NOTE 3, 6              |                                   |         |         | 230     | ps    |
| $f_{jit(cc)}$  | Cycle-to-Cycle Jitter; NOTE 6       | $f = 50MHz$ ; NOTE 4, 7           |         |         | 70      | ps    |
|                |                                     | $f = 25MHz$ XTAL,<br>133.3MHz out |         |         | 190     | ps    |
| $f_{jit(per)}$ | Period Jitter, RMS; NOTE 4, 6, 7, 8 |                                   |         |         | 17      | ps    |
| $t_L$          | PLL Lock Time                       |                                   |         |         | 1       | ms    |
| $t_R$          | Output Rise Time                    | 20% to 80%                        | 300     |         | 800     | ps    |
| $t_F$          | Output Fall Time                    | 20% to 80%                        | 300     |         | 800     | ps    |
| odc            | Output Duty Cycle; NOTE 5, 7        |                                   | 45      |         | 55      | %     |

See notes in Table 7A above.

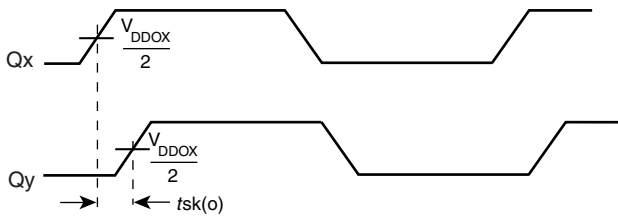
## PARAMETER MEASUREMENT INFORMATION



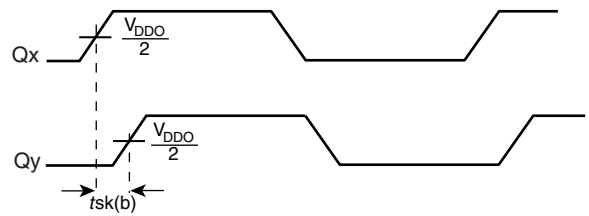
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



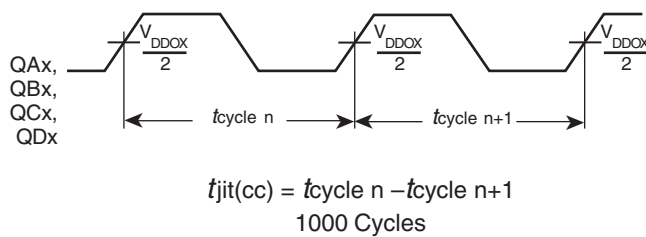
**3.3V/2.5V OUTPUT LOAD AC TEST CIRCUIT**



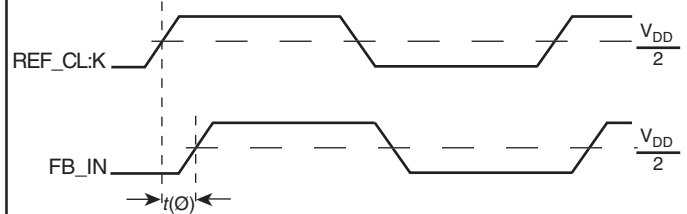
**OUTPUT SKEW**



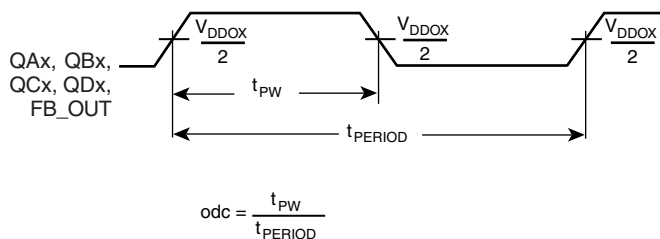
**BANK SKEW (Where X denotes outputs in the same Bank)**



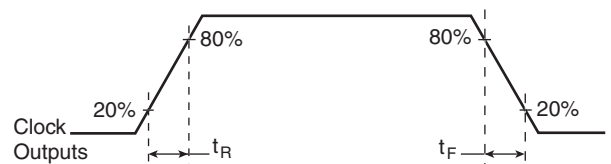
**CYCLE-TO-CYCLE JITTER**



**STATIC PHASE OFFSET**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



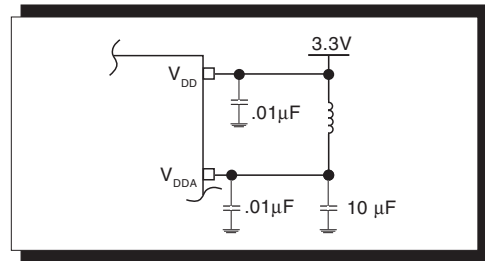
**OUTPUT RISE/FALL TIME**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8761 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDOX}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a ferrite bead along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$ .

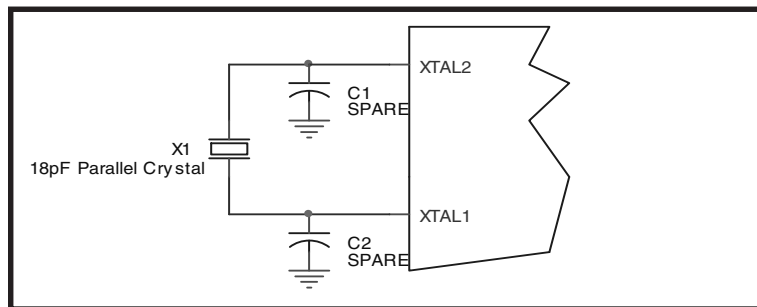


**FIGURE 1. POWER SUPPLY FILTERING**

### CRYSTAL INPUT INTERFACE

The ICS8761 crystal interface is shown in *Figure 2*. While layout the PC Board, it is recommended to provide C1 and C2 spare footprints for frequency fine tuning. For an 18pF

parallel resonant crystal, the C1 and C2 are expected to be  $\sim 10\text{pF}$  and  $\sim 5\text{pF}$  respectively.



**FIGURE 2. CRYSTAL INPUT INTERFACE**



## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### CRYSTAL INPUT:

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

#### REF\_CLK INPUT:

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the REF\_CLK to ground.

#### LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

### OUTPUTS:

#### LVC MOS OUTPUT:

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.

## SCHEMATIC EXAMPLE

Figure 3 shows a schematic example of the ICS8761. In this example, the input is driven by an ICS LVHSTL driver. The decoupling capacitors should be physically located near the

power pin. For ICS8761, the unused clock outputs can be left floating. The optional C1 and C2 are spare footprints for frequency fine tuning.

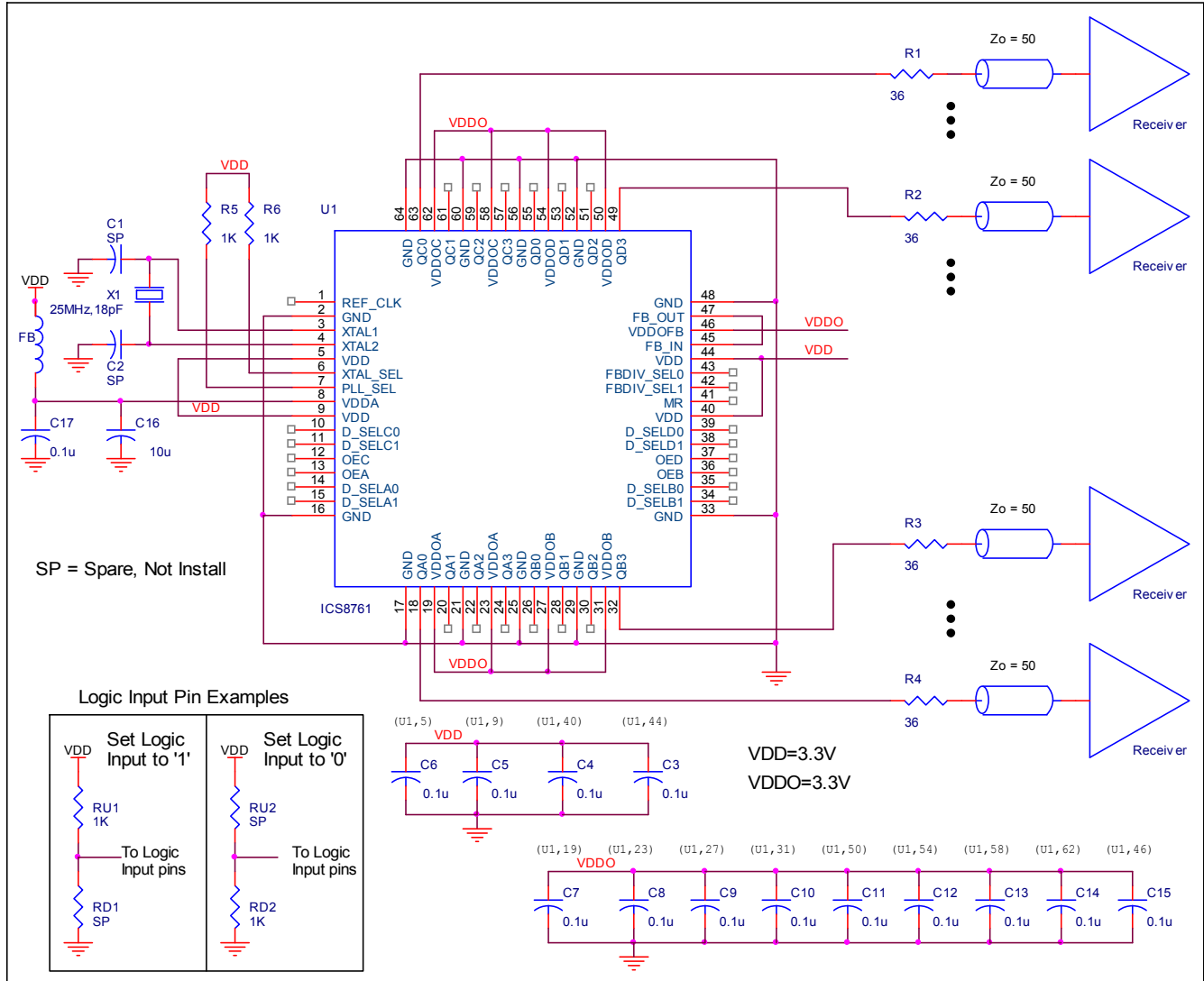


FIGURE 3. ICS8761 CLOCK GENERATOR SCHEMATIC EXAMPLE

## RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 64 LEAD TSSOP

| $\theta_{JA}$ by Velocity (Linear Feet per Minute) |          |          |          |
|--|----------|----------|----------|
|  | 0        | 200      | 500      |
| Single-Layer PCB, JEDEC Standard Test Boards       | 58.8°C/W | 48.5°C/W | 43.2°C/W |
| Multi-Layer PCB, JEDEC Standard Test Boards        | 41.1°C/W | 35.8°C/W | 33.6°C/W |

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8761 is: 6040

PACKAGE OUTLINE - Y SUFFIX FOR 64 LEAD TSSOP

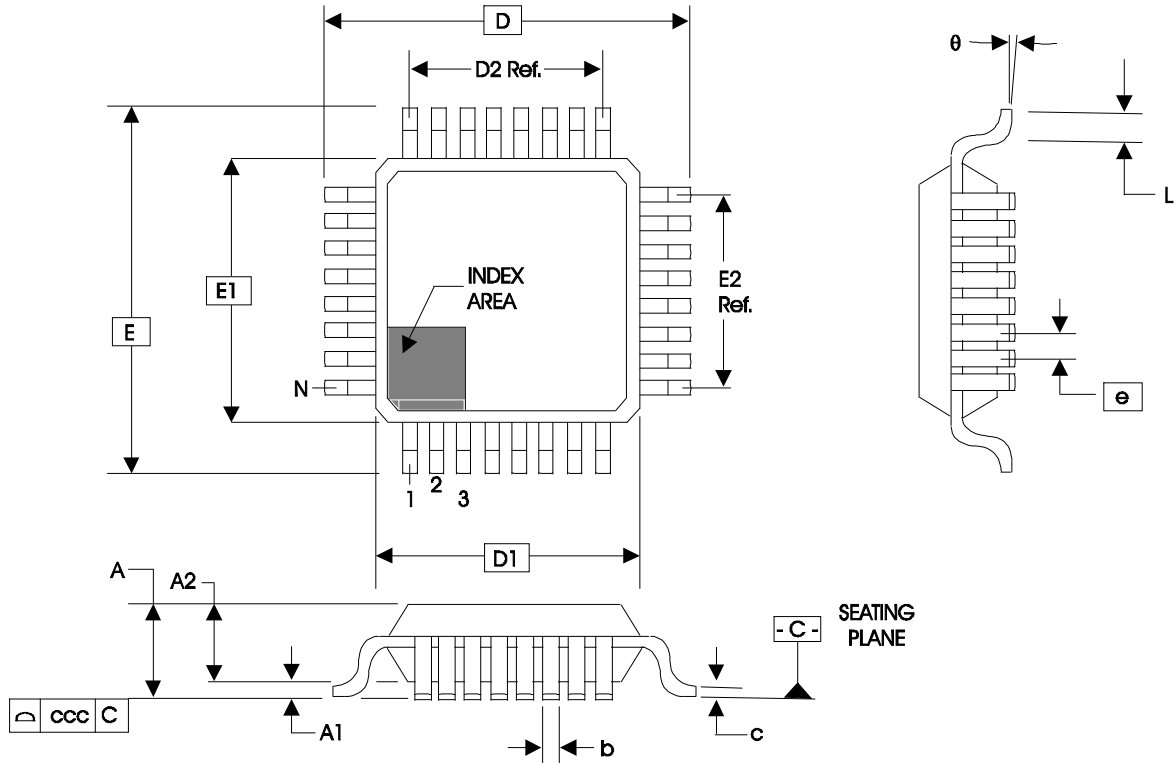


TABLE 9. PACKAGE DIMENSIONS

| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS |             |         |         |
|--|-------------|---------|---------|
| SYMBOL   | BCD         |         |         |
|  | MINIMUM     | NOMINAL | MAXIMUM |
| N  | 64          |         |         |
| A  | --          | --      | 1.60    |
| A1   | 0.05        | --      | 0.15    |
| A2   | 1.35        | 1.40    | 1.45    |
| b  | 0.17        | --      | 0.27    |
| c  | 0.09        | --      | 0.20    |
| D  | 12.00 BASIC |         |         |
| D1   | 10.00 BASIC |         |         |
| D2   | 7.50 Ref.   |         |         |
| E  | 12.00 BASIC |         |         |
| E1   | 10.00 BASIC |         |         |
| E2   | 7.50 Ref.   |         |         |
| e  | 0.50 BASIC  |         |         |
| L  | 0.45        | --      | 0.75    |
| theta  | 0°          | --      | 7°      |
| ccc  | --          | --      | 0.08    |

Reference Document: JEDEC Publication 95, MS-026



# ICS8761

LOW VOLTAGE, LOW SKEW,  
PCI / PCI-X CLOCK GENERATOR

**TABLE 10. ORDERING INFORMATION**

| Part/Order Number | Marking     | Package                           | Shipping Packaging | Temperature |
|-------------------|-------------|-----------------------------------|--------------------|-------------|
| 8761CY            | ICS8761CY   | 64 Lead LQFP                      | tray               | 0°C to 85°C |
| 8761CYT           | ICS8761CY   | 64 Lead LQFP                      | 500 tape & reel    | 0°C to 85°C |
| 8761CYLN          | ICS8761CYLN | 64 Lead "Lead-Free/Annealed" LQFP | tray               | 0°C to 85°C |
| 8761CYLNT         | ICS8761CYLN | 64 Lead "Lead-Free/Annealed" LQFP | 500 tape & reel    | 0°C to 85°C |
| 8761CYLF          | ICS8761CYLF | 64 Lead "Lead-Free" LQFP          | tray               | 0°C to 85°C |
| 8761CYLFT         | ICS8761CYLF | 64 Lead "Lead-Free" LQFP          | 500 tape & reel    | 0°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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| REVISION HISTORY SHEET |           |       |   |          |
|------------------------|-----------|-------|---|----------|
| Rev                    | Table     | Page  | Description of Change   | Date     |
| A                      | T1        | 2     | Pin Description Table, revised Master Reset description.  | 8/15/02  |
| A                      | T1        | 2     | Pin Description Table, pin 43 should be labeled at a PULLUP instead of a PULLDOWN.  | 11/05/02 |
|                        | T4B, T4D  | 6, 8  | LVC MOS DC Characteristics table - in the $I_{IH}$ and $I_{IL}$ rows, FBDIV_SEL0 was deleted from the "pulldown" row and was added to the "pullup" row.   |          |
| B                      | T3D       | 1     | Features section, changed max. output frequency from 200MHz to 183.3MHz, and max. REF_CLK input frequency from 100MHz to 91.6MHz.   | 11/06/02 |
|                        |           | 4     | Control Function Table - revised Reference Frequency Range column and Frequency columns to reflect the output frequency change.   |          |
|                        | T5A, T5B  | 7, 9  | AC Characteristics tables - changed Output Frequency from 200MHz max. to 183.3MHz max.  |          |
| B                      | T1        | 2     | Pin Description Table, revised crystal description.   | 1/20/03  |
|                        | T5A, T5B  | 7, 9  | AC Characteristics tables - changed Period Jitter measurement to Period Jitter, RMS and added NOTE 8.   |          |
|                        |           | 10    | Added Crystal information.  |          |
|                        |           | 11    | Added Schematic Example in the Application Information Section.   |          |
| B                      | T1        | 2     | Pin Description Table - revised MR description.   | 3/25/03  |
|                        | T4A, T4C  | 5, 7  | Power Supply Tables - changed $V_{DD}$ parameter to read "Core Supply Voltage" from "Positive Supply Voltage".  |          |
|                        |           | 10    | Deleted Crystal Input Interface section.  |          |
|                        |           | 10    | Updated Schematic Example diagram.  |          |
| C                      | T3D       | 1     | Updated Features to reflect T5A, 3.3V AC Characteristics (see below).   | 4/10/03  |
|                        |           | 4     | Adjusted Ref. Frequency Range and Frequency columns.  |          |
|                        | T4A       | 5     | Changed $I_{DD}$ max. from 150mA to 175mA, $I_{DDA}$ max. from 50mA to 55mA, and $I_{DDO}$ max. from 330mA to 25mA.   |          |
|                        | T5A & T5B | 6 & 8 | Changed $f_{MAX}$ from 183.3MHz max. to 166.67MHz max.  |          |
|                        |           |       | Changed RMS tjit(per) from 20ps max. to 17ps max.   |          |
| C                      |           | 1     | Features Section - added Lead-Free bullet.  | 8/2/04   |
|                        |           | 10    | Added Crystal Section.  |          |
|                        |           | 14    | Ordering Information Table - added Lead-Free/Annealed Part Number.  |          |
| C                      |           | 14    | Ordering Information Table - added Lead-Free Part Number.   | 8/7/04   |
| D                      | T2        | 3     | Pin Characteristics Table - changed CIN from 4pF max. to 4pF typical.   | 1/13/06  |
|                        |           | T5    | 6   |          |
|                        |           | 9     | Power Supply Filtering Techniques - corrected last sentence in the paragraph to read ""Figure 1 illustrates how a ferrite bead along..." from ""Figure 1 illustrates how a 10W resistor along..." |          |
|                        |           |       | Corrected Power Supply Filtering diagram.   |          |
|                        |           |       | Added Recommendations for Unused Input and Output Pins.   |          |
|                        | T10       | 10    | Corrected Schematic Example diagram.  |          |
|                        |           | 11    | Ordering Information Table - added Lead-Free note.  |          |
| E                      | T10       | 14    | Updated datasheet's header/footer with IDT from ICS.  | 7/26/10  |
|                        |           | 14    | Removed ICS prefix from Part/Order Number column.   |          |
|                        |           | 16    | Added Contact Page.   |          |



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