

3.3 V Zero Delay Clock Buffer

Features

- 10 MHz to 100–133 MHz operating range
- Zero input and output propagation delay
- Multiple low skew outputs
- One input drives five outputs (CY2305C)
- One input drives nine outputs, grouped as 4 + 4 + 1 (CY2309C)
- 50 ps typical cycle-to-cycle jitter (15 pF, 66 MHz)
- Test mode to bypass phase locked loop (PLL) (CY2309C) only, see [Select Input Decoding for CY2309C on page 5](#)
- Available in space saving 16-pin 150 Mil small outline integrated circuit (SOIC) or 4.4 mm thin shrunk small outline package (TSSOP) packages (CY2309C), and 8-pin, 150 Mil SOIC package (CY2305C)
- 3.3 V operation
- Commercial, industrial and automotive-A flows available

Functional Description

The CY2305C and CY2309C are die replacement parts for CY2305 and CY2309.

The CY2309C is a low-cost 3.3 V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC or TSSOP package. The CY2305C is an 8-pin version of the CY2309C. It accepts one reference input and drives out five low skew clocks. The -1H versions of each device operate up to

100–133 MHz frequencies and have higher drive than the -1 devices. All parts have on-chip phase locked loops (PLLs) which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

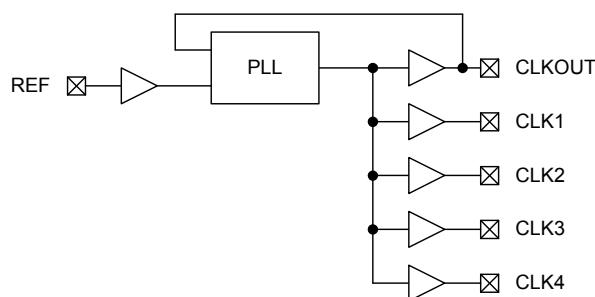
The CY2309C has two banks of four outputs each that are controlled by the select inputs as shown in the [Select Input Decoding for CY2309C on page 5](#). If all output clocks are not required, Bank B is three-stated. The input clock is directly applied to the outputs by the select inputs for chip and system testing purposes.

The CY2305C and CY2309C PLLs enter a power down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off. This results in less than 12.0 μ A of current draw for commercial temperature devices and 25.0 μ A for industrial and automotive-A temperature parts. The CY2309C PLL shuts down in one additional case as shown in the [Select Input Decoding for CY2309C on page 5](#).

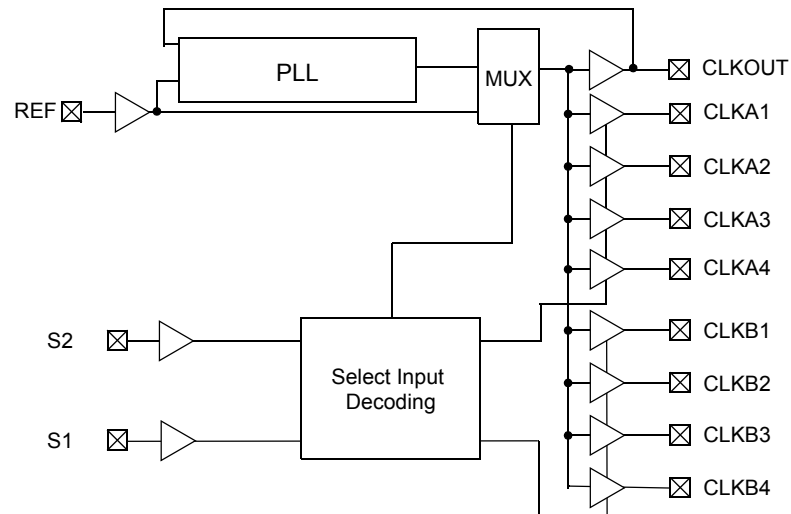
In the special case when S2:S1 is 1:0, the PLL is bypassed and REF is output from DC to the maximum allowable frequency. The part behaves as a non-zero delay buffer in this mode and the outputs are not three-stated.

The CY2305C or CY2309C is available in two or three different configurations as shown in the [Ordering Information on page 11](#). The CY2305C-1 or CY2309C-1 is the base part. The CY2305-1H or CY2309-1H is the high drive version of the -1. Its rise and fall times are much faster than the -1.

Logic Block Diagram for CY2305C



Logic Block Diagram for CY2309C



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Pinouts

CY2305C

Figure 1. Pin Diagram - 8 Pin SOIC (Top View)

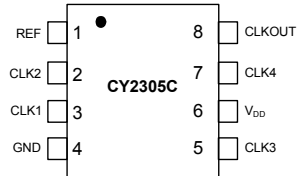


Table 1. Pin Description - 8 Pin SOIC

| Pin | Signal | Description |
|-----|-----------------------|--|
| 1 | REF ^[1] | Input reference frequency |
| 2 | CLK2 ^[2] | Buffered clock output |
| 3 | CLK1 ^[2] | Buffered clock output |
| 4 | GND | Ground |
| 5 | CLK3 ^[2] | Buffered clock output |
| 6 | V _{DD} | 3.3 V supply |
| 7 | CLK4 ^[2] | Buffered clock output |
| 8 | CLKOUT ^[2] | Buffered clock output, internal feedback on this pin |

CY2309C

Figure 2. Pin Diagram - 16 Pin SOIC/TSSOP (Top View)

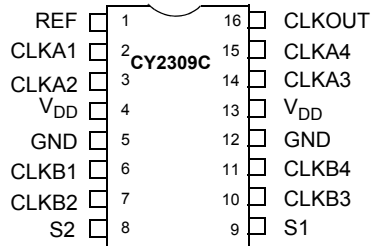


Table 2. Pin Definition - 16 Pin SOIC/TSSOP

| Pin | Signal | Description |
|-----|----------------------|-------------------------------|
| 1 | REF ^[1] | Input reference frequency |
| 2 | CLKA1 ^[2] | Buffered clock output, Bank A |
| 3 | CLKA2 ^[2] | Buffered clock output, Bank A |
| 4 | V _{DD} | 3.3 V supply |
| 5 | GND | Ground |
| 6 | CLKB1 ^[2] | Buffered clock output, Bank B |
| 7 | CLKB2 ^[2] | Buffered clock output, Bank B |
| 8 | S2 ^[3] | Select input, bit 2 |

Notes

1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs

Table 2. Pin Definition - 16 Pin SOIC/TSSOP (continued)

| Pin | Signal | Description |
|-----|-----------------------|--|
| 9 | S1 ^[4] | Select input, bit 1 |
| 10 | CLKB3 ^[5] | Buffered clock output, Bank B |
| 11 | CLKB4 ^[5] | Buffered clock output, Bank B |
| 12 | GND | Ground |
| 13 | V _{DD} | 3.3 V supply |
| 14 | CLKA3 ^[5] | Buffered clock output, Bank A |
| 15 | CLKA4 ^[5] | Buffered clock output, Bank A |
| 16 | CLKOUT ^[5] | Buffered output, internal feedback on this pin |

Table 3. Select Input Decoding for CY2309C

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | CLKOUT ^[6] | Output Source | PLL Shutdown |
|----|----|-------------|-------------|-----------------------|---------------|--------------|
| 0 | 0 | Three state | Three state | Driven | PLL | N |
| 0 | 1 | Driven | Three state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input or output delay.

For applications requiring zero input or output delay, all outputs including CLKOUT are equally loaded. Even if CLKOUT is not

used, it must have a capacitive load equal to that on other outputs for obtaining zero input or output delay.

For zero output to output skew, all outputs must be loaded equally.

Notes

4. Weak pull ups on these inputs.
5. Weak pull down on all outputs.
6. This output is driven and has an internal feedback for the PLL. The load on this output is adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Supply voltage to ground potential -0.5 V to +4.6 V
 DC input voltage (Except REF) -0.5 V to $V_{DD} + 0.5$ V
 DC input voltage REF -0.5 V to $V_{DD} + 0.5$ V

Storage temperature -65 °C to +150 °C
 Junction temperature 150 °C
 Static discharge voltage
 (per MIL-STD-883, Method 3015) > 2,000 V

Operating Conditions for CY2305CSXC-XX and CY2309CSXC-XX

Operating conditions table for CY2305CSXC-XX and CY2309CSXC-XX commercial temperature devices.

| Parameter | Description | Min | Max | Unit |
|-----------|---|------|-----|------|
| V_{DD} | Supply voltage | 3.0 | 3.6 | V |
| T_A | Operating temperature (ambient temperature) | 0 | 70 | °C |
| C_L | Load capacitance, below 100 MHz | – | 30 | pF |
| C_L | Load capacitance, from 100 MHz to 133 MHz | – | 10 | pF |
| C_{IN} | Input capacitance | – | 7 | pF |
| t_{PU} | Power-up time for all V_{DD} s to reach minimum specified voltage (power ramps are monotonic) | 0.05 | 50 | ms |

Operating Conditions for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX

Operating conditions table for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX industrial/automotive-A temperature devices.

| Parameter | Description | Min | Max | Unit |
|-----------|---|------|-----|------|
| V_{DD} | Supply voltage | 3.0 | 3.6 | V |
| T_A | Operating temperature (ambient temperature) | -40 | 85 | °C |
| C_L | Load capacitance, below 100 MHz | – | 30 | pF |
| C_L | Load capacitance, from 100 MHz to 133 MHz | – | 10 | pF |
| C_{IN} | Input capacitance | – | 7 | pF |
| t_{PU} | Power-up time for all V_{DD} s to reach minimum specified voltage (power ramps are monotonic) | 0.05 | 50 | ms |

Electrical Characteristics for CY2305CSXC-XX and CY2309CSXC-XX

Electrical characteristics table for CY2305CSXC-XX and CY2309CSXC-XX commercial temperature devices.

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--------------------|------------------------------------|--|-----|-----|------|
| V_{IL} | Input LOW voltage ^[7] | | – | 0.8 | V |
| V_{IH} | Input HIGH voltage ^[7] | | 2.0 | – | V |
| I_{IL} | Input LOW current | $V_{IN} = 0$ V | – | 50 | μA |
| I_{IH} | Input HIGH current | $V_{IN} = V_{DD}$ | – | 100 | μA |
| V_{OL} | Output LOW voltage ^[8] | $I_{OL} = 8$ mA (–1) $I_{OH} = 12$ mA (–1H) | – | 0.4 | V |
| V_{OH} | Output HIGH voltage ^[8] | $I_{OH} = -8$ mA (–1) $I_{OL} = -12$ mA (–1H) | 2.4 | – | V |
| I_{DD} (PD mode) | Power-down supply current | REF = 0 MHz | – | 12 | μA |
| I_{DD} | Supply current | Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD} | – | 32 | mA |

Notes

7. REF input has a threshold voltage of $V_{DD}/2$.
 8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX

Electrical characteristics table for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX industrial/automotive-A temperature devices.

| Parameter | Description | Test Conditions | Min | Max | Unit |
|--------------------|-------------------------------------|--|-----|-----|---------------|
| V_{IL} | Input LOW voltage ^[9] | | – | 0.8 | V |
| V_{IH} | Input HIGH voltage ^[9] | | 2.0 | – | V |
| I_{IL} | Input LOW current | $V_{IN} = 0\text{ V}$ | – | 50 | μA |
| I_{IH} | Input HIGH current | $V_{IN} = V_{DD}$ | – | 100 | μA |
| V_{OL} | Output LOW voltage ^[10] | $I_{OL} = 8\text{ mA (-1)}$ $I_{OH} = 12\text{ mA (-1H)}$ | – | 0.4 | V |
| V_{OH} | Output HIGH voltage ^[10] | $I_{OH} = -8\text{ mA (-1)}$ $I_{OL} = -12\text{ mA (-1H)}$ | 2.4 | – | V |
| I_{DD} (PD mode) | Power-down supply current | REF = 0 MHz | – | 25 | μA |
| I_{DD} | Supply current | Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD} | – | 35 | mA |

Switching Characteristics for CY2305CSXC-XX and CY2309CSXC-XX

Switching characteristics table for CY2305CSXC-1 and CY2309CSXC-1 commercial temperature devices. All parameters are specified with loaded outputs.

| Parameter | Name | Test Conditions | Min | Typ | Max | Unit |
|------------|--|--|----------|-----|---------------|------------|
| t_1 | Output frequency | 30 pF load 10 pF load | 10 10 | – | 100 133.33 | MHz MHz |
| t_{DC} | Output duty cycle ^[10] = $t_2 \div t_1$ | Measured at 1.4 V, $F_{out} > 50\text{ MHz}$ | 40 | 50 | 60 | % |
| | | Measured at 1.4 V, $F_{out} \leq 50\text{ MHz}$ | 45 | 50 | 55 | % |
| t_3 | Rise time ^[10] | Measured between 0.8 V and 2.0 V | – | – | 2.25 | ns |
| t_4 | Fall time ^[10] | Measured between 0.8 V and 2.0 V | – | – | 2.25 | ns |
| t_5 | Output-to-output skew ^[10] | All outputs equally loaded | – | – | 200 | ps |
| t_{6A} | Delay, REF rising edge to CLKOUT rising edge ^[10] | Measured at $V_{DD}/2$ | – | 0 | ± 350 | ps |
| t_{6B} | Delay, REF rising edge to CLKOUT rising edge ^[10] | Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only. | 1 | 5 | 8.7 | ns |
| t_7 | Device-to-device skew ^[10] | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | – | 0 | 700 | ps |
| t_J | Cycle-to-cycle jitter, peak ^[10] | Measured at 66.67 MHz, loaded outputs | – | 50 | 175 | ps |
| t_{LOCK} | PLL lock time ^[10] | Stable power supply, valid clock presented on REF pin | – | – | 1.0 | ms |

Notes

9. .REF input has a threshold voltage of $V_{DD}/2$.

10. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching Characteristics for CY2305CSXC-XX and CY2309CSXC-XX

Switching characteristics table for CY2305CSXC-1H and CY2309CSXC-1H commercial temperature devices. All parameters are specified with loaded outputs.

| Parameter | Name | Description | Min | Typ | Max | Unit |
|------------|--|--|----------|-----|---------------|------------|
| t_1 | Output frequency | 30-pF load 10-pF load | 10 10 | — | 100 133.33 | MHz MHz |
| t_{DC} | Output duty cycle ^[11] = $t_2 \div t_1$ | Measured at 1.4 V, $F_{out} > 50$ MHz | 40 | 50 | 60 | % |
| | | Measured at 1.4 V, $F_{out} \leq 50$ MHz | 45 | 50 | 55 | % |
| t_3 | Rise time ^[11] | Measured between 0.8 V and 2.0 V | — | — | 1.5 | ns |
| t_4 | Fall time ^[11] | Measured between 0.8 V and 2.0 V | — | — | 1.5 | ns |
| t_5 | Output-to-output skew ^[11] | All outputs equally loaded | — | — | 200 | ps |
| t_{6A} | Delay, REF rising edge to CLKOUT rising edge ^[11] | Measured at $V_{DD}/2$ | — | 0 | ± 350 | ps |
| t_{6B} | Delay, REF rising edge to CLKOUT rising edge ^[11] | Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only. | 1 | 5 | 8.7 | ns |
| t_7 | Device-to-device skew ^[11] | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | — | 0 | 700 | ps |
| t_8 | Output slew rate ^[11] | Measured between 0.8 V and 2.0 V using Test circuit #2 | 1 | — | — | V/ns |
| t_J | Cycle-to-cycle jitter, peak ^[11] | Measured at 66.67 MHz, loaded outputs | — | — | 175 | ps |
| t_{LOCK} | PLL lock time ^[11] | Stable power supply, valid clock presented on REF pin | — | — | 1.0 | ms |

Switching Characteristics for CY2305CSXI-XX, CY2305CSXA-XX and CY2309CSXI-XX

Switching characteristics table for CY2305CSXI-1, CY2305CSXA-1, and CY2309CSXI-1 industrial temperature devices. All parameters are specified with loaded outputs.

| Parameter | Name | Test Conditions | Min | Typ | Max | Unit |
|------------|--|--|----------|-----|---------------|------------|
| t_1 | Output frequency | 30 pF load 10 pF load | 10 10 | — | 100 133.33 | MHz MHz |
| t_{DC} | Output duty cycle ^[11] = $t_2 \div t_1$ | Measured at 1.4 V, $F_{out} > 50$ MHz | 40 | 50 | 60 | % |
| | | Measured at 1.4 V, $F_{out} \leq 50$ MHz | 45 | 50 | 55 | % |
| t_3 | Rise time ^[11] | Measured between 0.8 V and 2.0 V | — | — | 2.25 | ns |
| t_4 | Fall time ^[11] | Measured between 0.8 V and 2.0 V | — | — | 2.25 | ns |
| t_5 | Output-to-output skew ^[11] | All outputs equally loaded | — | — | 200 | ps |
| t_{6A} | Delay, REF rising edge to CLKOUT rising edge ^[11] | Measured at $V_{DD}/2$ | — | 0 | ± 350 | ps |
| t_{6B} | Delay, REF rising edge to CLKOUT rising edge ^[11] | Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only. | 1 | 5 | 8.7 | ns |
| t_7 | Device-to-device skew ^[11] | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | — | 0 | 700 | ps |
| t_J | Cycle-to-cycle jitter, peak ^[11] | Measured at 66.67 MHz, loaded outputs | — | 50 | 175 | ps |
| t_{LOCK} | PLL lock time ^[11] | Stable power supply, valid clock presented on REF pin | — | — | 1.0 | ms |

Note

11. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Switching characteristics table for CY2305CSXI-1H, CY2305CSXA-1H and CY2309CSXI-1H

Switching characteristics table for CY2305CSXI-1H, CY2305CSXA-1H and CY2309CSXI-1H industrial/automotive-A temperature device. All parameters are specified with loaded outputs.

| Parameter | Name | Description | Min | Typ | Max | Unit |
|------------|--|--|----------|-----|---------------|------------|
| t_1 | Output frequency | 30 pF load 10 pF load | 10 10 | – | 100 133.33 | MHz MHz |
| t_{DC} | Output duty cycle ^[12] = $t_2 \div t_1$ | Measured at 1.4 V, $F_{out} > 50$ MHz | 40 | 50 | 60 | % |
| | | Measured at 1.4 V, $F_{out} \leq 50$ MHz | 45 | 50 | 55 | % |
| t_3 | Rise time ^[12] | Measured between 0.8 V and 2.0 V | – | – | 1.5 | ns |
| t_4 | Fall time ^[12] | Measured between 0.8 V and 2.0 V | – | – | 1.5 | ns |
| t_5 | Output-to-output skew ^[12] | All outputs equally loaded | – | – | 200 | ps |
| t_{6A} | Delay, REF rising edge to CLKOUT rising edge ^[12] | Measured at $V_{DD}/2$ | – | 0 | ± 350 | ps |
| t_{6B} | Delay, REF rising edge to CLKOUT rising edge ^[12] | Measured at $V_{DD}/2$. Measured in PLL Bypass mode, CY2309C device only. | 1 | 5 | 8.7 | ns |
| t_7 | Device-to-device skew ^[12] | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | – | 0 | 700 | ps |
| t_8 | Output slew rate ^[12] | Measured between 0.8 V and 2.0 V using Test circuit #2 | 1 | – | – | V/ns |
| t_J | Cycle-to-cycle jitter, peak ^[12] | Measured at 66.67 MHz, loaded outputs | – | – | 175 | ps |
| t_{LOCK} | PLL lock time ^[12] | Stable power supply, valid clock presented on REF pin | – | – | 1.0 | ms |

Switching Waveforms

Figure 3. Duty Cycle Timing

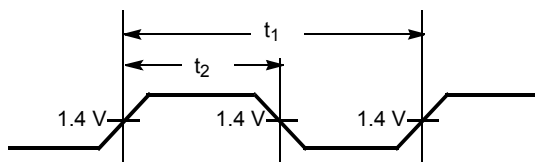
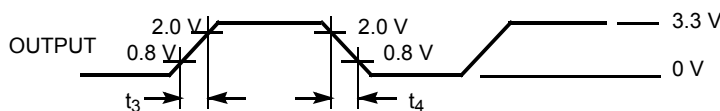


Figure 4. All Outputs Rise/Fall Time



Note

12. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Figure 5. Output-Output Skew

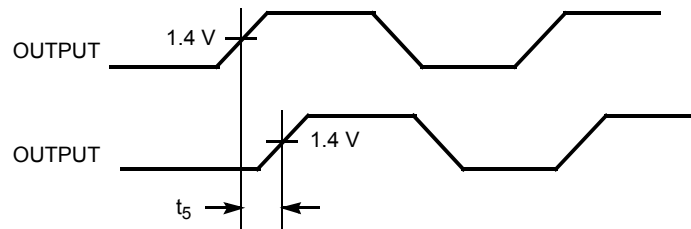


Figure 6. Input-Output Propagation Delay

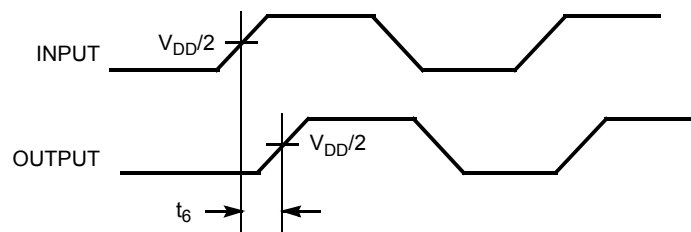
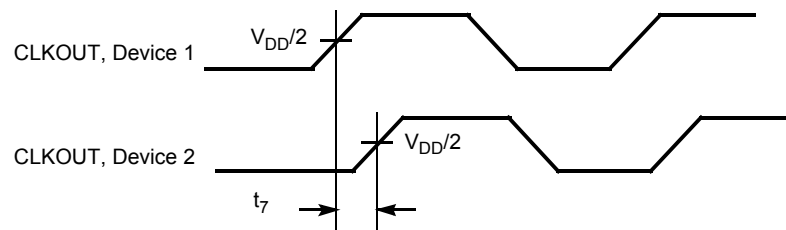
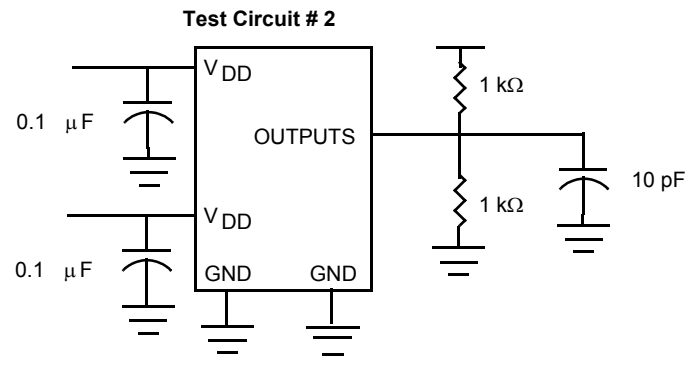
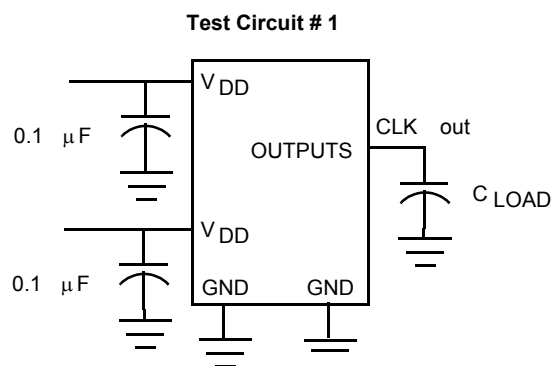


Figure 7. Device-Device Skew



Test Circuits

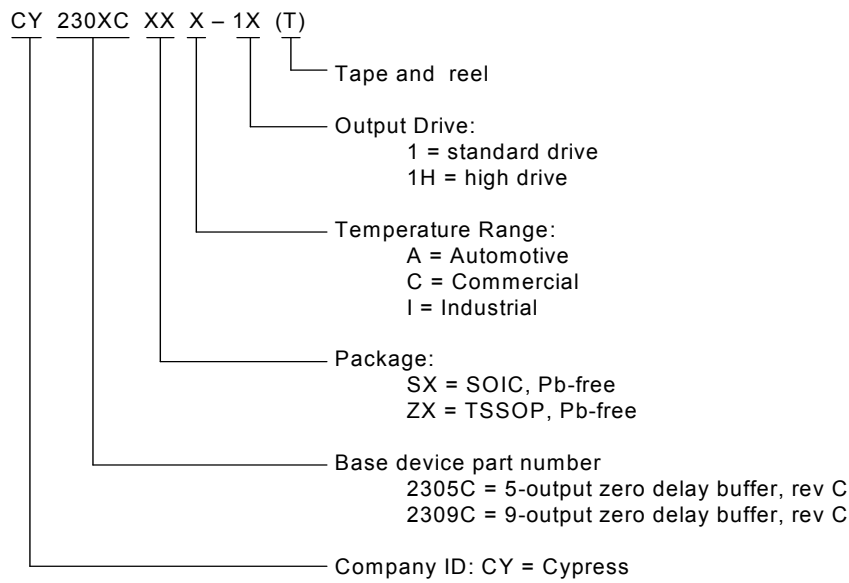


For parameter t_8 (output slew rate) on -1H devices

Ordering Information

| Ordering Code | Package Type | Operating Range |
|--------------------------|-------------------------------------|-----------------|
| Pb-free - CY2305C | | |
| CY2305CSXC-1 | 8-pin 150 Mil SOIC | Commercial |
| CY2305CSXC-1T | 8-pin 150 Mil SOIC – Tape and reel | Commercial |
| CY2305CSXC-1H | 8-pin 150 Mil SOIC | Commercial |
| CY2305CSXC-1HT | 8-pin 150 Mil SOIC – Tape and reel | Commercial |
| CY2305CSXI-1 | 8-pin 150 Mil SOIC | Industrial |
| CY2305CSXI-1T | 8-pin 150 Mil SOIC – Tape and reel | Industrial |
| CY2305CSXI-1H | 8-pin 150 Mil SOIC | Industrial |
| CY2305CSXI-1HT | 8-pin 150 Mil SOIC – Tape and reel | Industrial |
| CY2305CSXA-1H | 8-pin 150 Mil SOIC | Automotive-A |
| CY2305CSXA-1HT | 8-pin 150 Mil SOIC – Tape and reel | Automotive-A |
| Pb-free - CY2309C | | |
| CY2309CSXC-1 | 16-pin 150 Mil SOIC | Commercial |
| CY2309CSXC-1T | 16-pin 150 Mil SOIC – Tape and reel | Commercial |
| CY2309CSXC-1H | 16-pin 150 Mil SOIC | Commercial |
| CY2309CSXC-1HT | 16-pin 150 Mil SOIC – Tape and reel | Commercial |
| CY2309CSXI-1 | 16-pin 150 Mil SOIC | Industrial |
| CY2309CSXI-1T | 16-pin 150 Mil SOIC – Tape and reel | Industrial |
| CY2309CSXI-1H | 16-pin 150 Mil SOIC | Industrial |
| CY2309CSXI-1HT | 16-pin 150 Mil SOIC – Tape and reel | Industrial |
| CY2309CZXC-1 | 16-pin 4.4 mm TSSOP | Commercial |
| CY2309CZXC-1T | 16-pin 4.4 mm TSSOP – Tape and reel | Commercial |
| CY2309CZXC-1H | 16-pin 4.4 mm TSSOP | Commercial |
| CY2309CZXC-1HT | 16-pin 4.4 mm TSSOP – Tape and reel | Commercial |
| CY2309CZXI-1 | 16-pin 4.4 mm TSSOP | Industrial |
| CY2309CZXI-1T | 16-pin 4.4 mm TSSOP – Tape and reel | Industrial |
| CY2309CZXI-1H | 16-pin 4.4 mm TSSOP | Industrial |
| CY2309CZXI-1HT | 16-pin 4.4 mm TSSOP – Tape and reel | Industrial |

Ordering Code Definition



Package Drawing and Dimensions

Figure 8. 8-Pin (150 Mil) SOIC SZ08.15

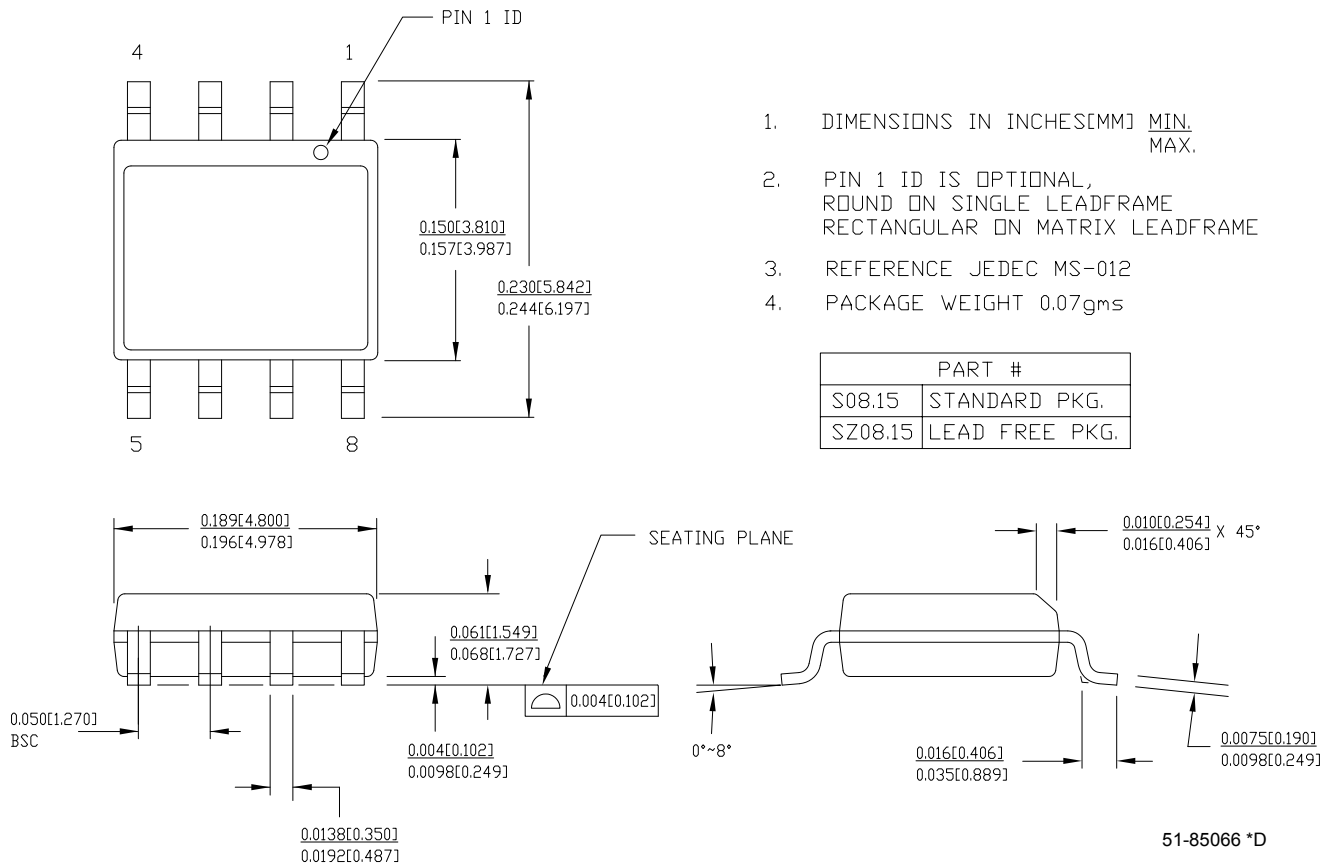
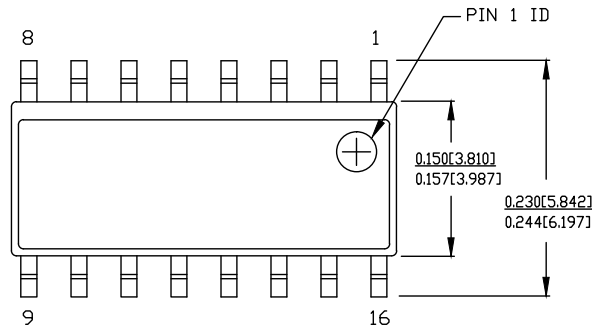


Figure 9. 16-Pin (150 Mil) SOIC SZ16.15



DIMENSIONS IN INCHES[MM] MIN.
MAX.

REFERENCE JEDEC MS-012

PACKAGE WEIGHT 0.15gms

| PART # | |
|---------|----------------|
| S16.15 | STANDARD PKG. |
| SZ16.15 | LEAD FREE PKG. |

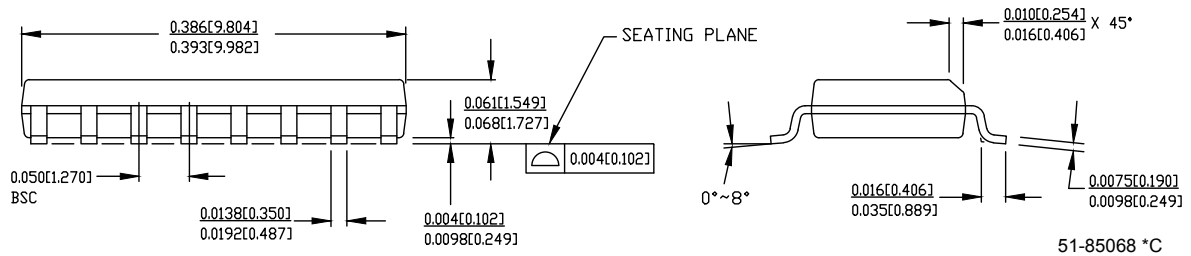


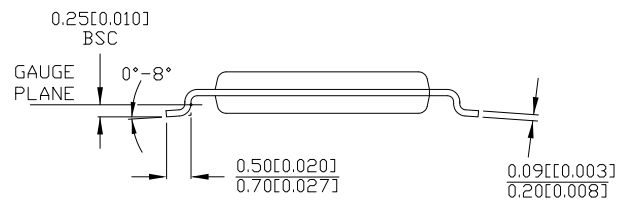
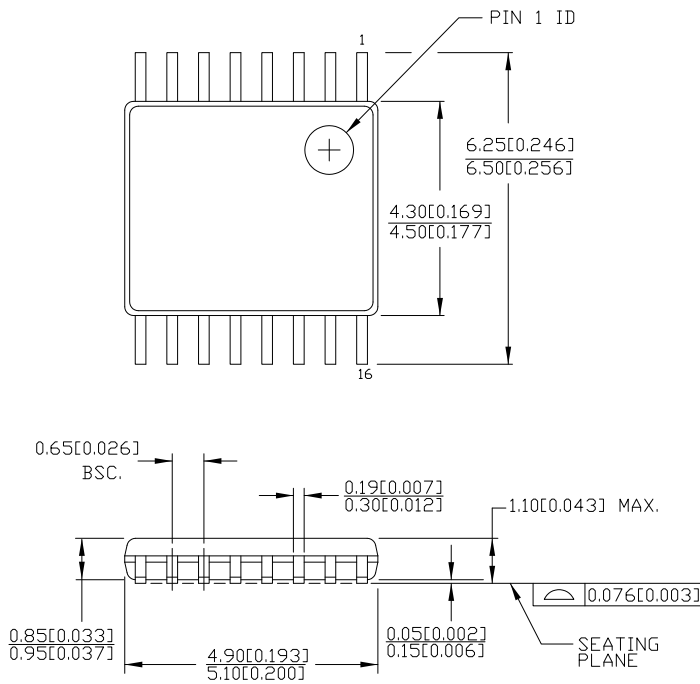
Figure 10. 16-Pin TSSOP 4.40 mm Body ZZ16.173

DIMENSIONS IN MM[INCHES] MIN.
MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

| PART # | |
|----------|----------------|
| Z16.173 | STANDARD PKG. |
| ZZ16.173 | LEAD FREE PKG. |



51-85091 °C

Acronyms

| Acronym | Description |
|---------|---|
| CMOS | Complementary metal oxide semiconductor |
| PLL | phase locked loop |
| SOIC | small outline integrated circuit |
| TSSOP | thin shrunk small outline package |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degrees Celsius |
| V | Volts |
| kHz | Kilohertz |
| MHz | megahertz |
| μA | microamperes |
| mA | milliamperes |
| ms | milliseconds |
| ns | nanoseconds |
| pF | picofarads |
| ps | picoseconds |

Document History Page

| Document Title: CY2305C CY2309C 3.3 V ZERO DELAY CLOCK BUFFER Document Number: 38-07672 | | | | |
|--|-----------|------------|-----------------|--|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 224421 | See ECN | RGL | New data sheet |
| *A | 268571 | See ECN | RGL | Added bullet for 5 V tolerant inputs in the features |
| *B | 276453 | See ECN | RGL | Minor Change: Moved one sentence from the features to the Functional Description |
| *C | 303063 | See ECN | RGL | Updated data sheet as per characterization data |
| *D | 318315 | See ECN | RGL | Data sheet rewrite |
| *E | 344815 | See ECN | RGL | Minor Error: Corrected the header of all the AC/DC tables with the right part numbers. |
| *F | 127988938 | See ECN | KVM | Changed title from ,low Cost 3.3 V Zero Delay Buffer to 3.3 V Zero Delay Clock Buffer Specified the VIL minimum value to -0.3 V Specified the VIH maximum value to VDD + 0.3 V Changed DC Input Voltage (REF) maximum value in Absolute Maximum section Removed references to 5 V tolerant inputs (pages 1 and 2) Removed Pentium compatibility reference Added CY2305C block diagram Added ,peak to the jitter specifications Changed typical jitter from 75 ps to 50 ps for standard drive devices For standard drive devices, tightened rise/fall times from 2.5 ns to 2.25 ns Tightened cycle-to-cycle jitter from 200 ps to 175 ps Tightened output-to-output skew from 250 ps to 200 ps |
| *G | 1561504 | See ECN | KVM/NSI /AESAs | Added CY2305C Automotive-A grade devices Extended duty cycle specs to cover entire frequency range Changed from Preliminary to Final |
| *H | 2558537 | 08/27/08 | KVM/AESA | Added CY2305CSXA-1 and CY2305CSXA-1T parts in Ordering Information table under Pb-free CY2305C |
| *I | 2901743 | 03/30/2010 | VIVG | Updated Package Drawing and Dimensions . Added Ordering Code Definition Added Sales, Solutions, and Legal Information URLs. |
| *J | 3080990 | 11/10/2010 | BASH | Modified pin diagram of Figure 1. Updated as per new template Added Acronyms and Units of Measure table Added TOC |
| *K | 3160535 | 02/03/2011 | BASH | Removed min value of V_{IL} and max value of V_{IH} from Electrical Characteristics Table on page 6 and page 7. Removed Prune parts CY2305CSXA-1 and CY2305CSXA-1T from the datasheet. |

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