CY2308

3.3 V Zero Delay Buffer

Features

- Zero input-output propagation delay, adjustable by capacitive load on FBK input
- Multiple configurations, see Available CY2308 Configurations on page 4 for more details
- Multiple low skew outputs
- Two banks of four outputs, three-stateable by two select inputs
- 10 MHz to 133 MHz operating range
- 75 ps typical cycle-to-cycle jitter (15 pF, 66 MHz)
- Space saving 16-pin 150 mil SOIC package or 16-pin TSSOP
- 3.3 V operation
- Industrial temperature available

Functional Description

The CY2308 is a 3.3 V Zero Delay Buffer designed to distribute high speed clocks in PC, workstation, datacom, telecom, and other high performance applications.

The part has an on-chip PLL that locks to an input clock presented on the REF pin. The PLL feedback is driven from external FBK pin, so user has flexibility to choose any one of the outputs as feedback input and connect it to FBK pin. The input-to-output skew is less than 250 ps and output-to-output skew is less than 200 ps.

The CY2308 has two banks of four outputs each that is controlled by the select inputs as shown in the table Select Input Decoding on page 3. If all output clocks are not required, Bank B is three-stated. The input clock is directly applied to the output for chip and system testing purposes by the select inputs.

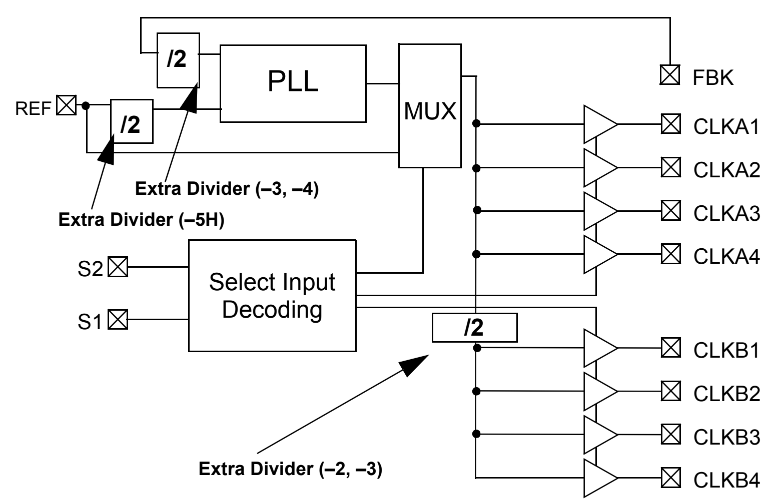
The CY2308 PLL enters a power down state when there are no rising edges on the REF input. In this mode, all outputs are three-stated and the PLL is turned off resulting in less than 25 μA of current draw. The PLL shuts down in two additional cases as shown in the table Select Input Decoding on page 3.

Multiple CY2308 devices accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is less than 700 ps.

The CY2308 is available in five different configurations as shown in the table Available CY2308 Configurations on page 4.

- The CY2308–1 is the base part where the output frequencies equal the reference if there is no counter in the feedback path. The CY2308–1H is the high drive version of the –1 and rise and fall times on this device are much faster.
- The CY2308–2 enables the user to obtain 2x and 1x frequencies on each output bank. The exact configuration and output frequencies depend on the user's selection of output that drives the feedback pin.
- The CY2308–3 enables the user to obtain 4x and 2x frequencies on the outputs.
- The CY2308–4 enables the user to obtain 2x clocks on all outputs. Thus, the part is extremely versatile and is used in a variety of applications.
- The CY2308–5H is a high drive version with REF/2 on both banks.

Logic Block Diagram



 [+] Feedback

Contents

Pinouts

Figure 1. Pin Diagram - 16 Pin SOIC (Top view)

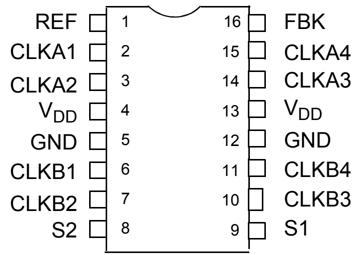


Table 1. Pin Definitions - 16 Pin SOIC

Pin	Signal	Description
1	REF[1]	Input reference frequency
2	CLKA1[2]	Clock output, Bank A
3	CLKA2[2]	Clock output, Bank A
4	V_{DD}	Power supply voltage
5	GND	Power supply ground
6	CLKB1[2]	Clock output, Bank B
7	CLKB2[2]	Clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Clock output, Bank B
11	CLKB4[2]	Clock output, Bank B
12	GND	Power supply ground
13	V_{DD}	Power supply voltage
14	CLKA3[2]	Clock output, Bank A
15	CLKA4[2]	Clock output, Bank A
16	FBK	PLL feedback input

Select Input Decoding

S2	S1	CLOCK A1–A4	CLOCK B1–B4	Output Source	PLL Shutdown
0	0	Tri-state	Tri-state	PLL	Y
0	1	Driven	Tri-state	PLL	N
1	0	Driven[4]	Driven[4]	Reference	Y
1	1	Driven	Driven	PLL	N

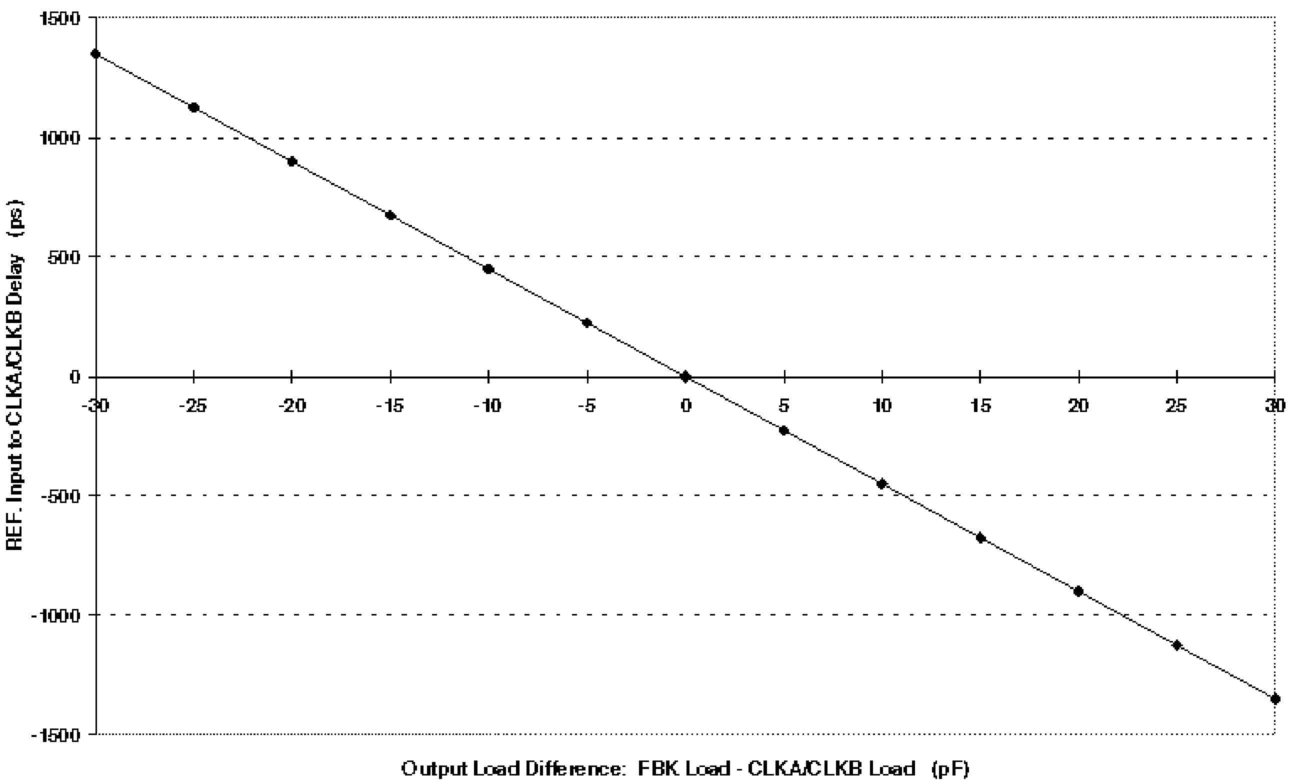
Notes
1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull ups on these inputs.
4. Outputs inverted and PLL bypass mode for 2308–2 and 2308–3, S2 = 1 and S1 = 0.

Available CY2308 Configurations

Device	Feedback From[5]	Bank A Frequency	Bank B Frequency
CY2308–1	Bank A or Bank B	Reference	Reference
CY2308–1H	Bank A or Bank B	Reference	Reference
CY2308–2	Bank A	Reference	Reference/2
CY2308–2	Bank B	2 x Reference	Reference
CY2308–3	Bank A	2 x Reference	Reference[6]
CY2308–3	Bank B	4 x Reference	2 x Reference
CY2308–4	Bank A or Bank B	2 x Reference	2 x Reference
CY2308–5H	Bank A or Bank B	Reference /2	Reference /2

Zero Delay and Skew Control

Figure 2. REF. Input to CLKA/CLKB Delay Versus Difference in Loading Between FBK Pin and CLKA/CLKB Pins



To close the feedback loop of the CY2308, the user has to connect any one of the eight available output pins to FBK pin. The output driving the FBK pin drives a total load of 7 pF plus any additional load that it drives. The relative loading of this output to the remaining outputs adjusts the input-output delay as shown in the Figure 2.

For applications requiring zero input-output delay, all outputs including the one providing feedback is equally loaded.

If input-output delay adjustments are required, use the Zero Delay and Skew Control graph to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, outputs are loaded equally. For further information on using CY2308, refer to the application note CY2308: Zero Delay Buffer-AN1234.

Notes

5. User has to select one of the available outputs that drive the feedback pin and need to connect selected output pin to FBK pin externally.
6. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use CY2308–2.

Maximum Ratings

Supply voltage to ground potential ....–0.5 V to +7.0 V

DC input voltage (except REF)...........–0.5 V to V_{DD} + 0.5 V

DC input voltage REF ....–0.5 V to 7 V

Storage temperature .... –65 °C to +150 °C

Junction temperature... 150 °C

Static discharge voltage (MIL-STD-883, Method 3015).................................. >2000 V

Operating Conditions for Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	0	70	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
	Load capacitance, from 100 MHz to 133 MHz	–	15	pF
C_{IN}	Input capacitance[7]	–	7	pF
t_{PU}	Power up time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for Commercial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	µA
I_{IH}	Input HIGH current	V_{IN} = V_{DD}	–	100.0	µA
V_{OL}	Output LOW voltage[8]	I_{OL} = 8 mA (–1, –2, –3, –4) I_{OL} = 12 mA (–1H, –5H)	–	0.4	V
V_{OH}	Output HIGH voltage[8]	I_{OH} = –8 mA (–1, –2, –3, –4) I_{OH} = –12 mA (–1H, –5H)	2.4	–	V
I_{DD} (PD mode)	Power down supply current	REF = 0 MHz	–	12.0	µA
I_{DD}	Supply current	Unloaded outputs, 100 MHz REF, select inputs at V_{DD} or GND	–	45.0	mA
			–	70.0 (–1H, –5H)	mA
		Unloaded outputs, 66 MHz REF (–1, –2, –3, –4)	–	32.0	mA
		Unloaded outputs, 33 MHz REF (–1, –2, –3, –4)	–	18.0	mA

Switching Characteristics for Commercial Temperature Devices

Parameter[9]	Name	Test Conditions	Min	Typ.	Max	Unit
F_{in}	Input frequency	–	10	–	133.3	MHz
t_1	Output frequency	30 pF load	10	–	100 (–1, –2, –3, –4) 66.67 (–5H)	MHz
t_1	Output frequency	20 pF load, –1H, –5H devices	10	–	133.3 (–1H) 66.67 (–5H)	MHz
t_1	Output frequency	15 pF load, –1, –2, –3, –4 devices	10	–	133.3	MHz

Notes
7. Applies to both Ref clock and FBK.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.
9. All parameters are specified with loaded outputs.

Switching Characteristics for Commercial Temperature Devices (continued)

Parameter[9]	Name	Test Conditions	Min	Typ.	Max	Unit
t_{PD}	Duty cycle[10, 12] = $t_2 \div t_1$ (–1, –2, –3, –4, –1H, –5H)	Measured at 1.4 V, F_{OUT} = 66.66 MHz, 30 pF load	40.0	50.0	60.0	%
t_{PD}	Duty cycle[10, 12] = $t_2 \div t_1$ (–1, –2, –3, –4, –1H, –5H)	Measured at 1.4 V, F_{OUT} < 50 MHz, 15 pF load	45.0	50.0	55.0	%
t_3	Rise time[10, 12] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	2.20	ns
t_3	Rise time[10, 12] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 15 pF load	–	–	1.50	ns
t_3	Rise time[10, 12] (–1H, –5H)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	1.50	ns
t_4	Fall time[10, 12] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	2.20	ns
t_4	Fall time[10, 12] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 15 pF load	–	–	1.50	ns
t_4	Fall time[10, 12] (–1H, –5H)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	1.25	ns
t_5	Output to output skew on same Bank (–1, –2, –3, –4)[10, 12]	All outputs equally loaded	–	–	200	ps
	Output to output skew (–1H, –5H)	All outputs equally loaded	–	–	200	ps
	Output Bank A to output Bank B skew (–1, –4, –5H)	All outputs equally loaded	–	–	200	ps
	Output Bank A to output Bank B skew (–2, –3)	All outputs equally loaded	–	–	400	ps
t_6	Delay, REF rising edge to FBK rising edge[10, 12]	Measured at $V_{DD}/2$	–	0	±250	ps
t_7	Device to device skew[10, 12]	Measured at $V_{DD}/2$ on the FBK pins of devices	–	0	700	ps
t_8	Output slew rate[10, 12]	Measured between 0.8 V and 2.0 V on –1H, –5H device using Test Circuit 2	1	–		V/ns
t_J	Cycle to cycle Jitter[10, 12] (–1, –1H, –4, –5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load	–	75	200	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load	–	–	200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load	–	–	100	ps
t_J	Cycle to cycle Jitter[10, 12] (–2, –3)	Measured at 66.67 MHz, loaded outputs, 30 pF load	–	–	400	ps
		Measured at 66.67 MHz, loaded outputs, 15 pF load	–	–	400	ps
t_{LOCK}	PLL lock time[10, 12]	Stable power supply, valid clocks presented on REF and FBK pins	–	–	1.0	ms

Notes

10. All parameters are specified with loaded outputs.
11. Parameter is guaranteed by design and characterization. Not 100% tested in production.
12. All parameters are specified with loaded outputs.

Operating Conditions for Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply voltage	3.0	3.6	V
T_A	Operating temperature (ambient temperature)	–40	85	°C
C_L	Load capacitance, below 100 MHz	–	30	pF
	Load capacitance, from 100 MHz to 133 MHz	–	15	pF
C_{IN}	Input capacitance[13]	–	7	pF
t_{PU}	Power up time for all V_{DDs} to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW voltage		–	0.8	V
V_{IH}	Input HIGH voltage		2.0	–	V
I_{IL}	Input LOW current	V_{IN} = 0 V	–	50.0	μA
I_{IH}	Input HIGH current	$V_{IN} = V_{DD}$	–	100.0	μA
V_{OL}	Output LOW voltage[14, 15]	I_{OL} = 8 mA (–1, –2, –3, –4) I_{OL} = 12 mA (–1H, –5H)	–	0.4	V
V_{OH}	Output HIGH voltage[14, 15]	I_{OH} = –8 mA (–1, –2, –3, –4) I_{OH} = –12 mA (–1H, –5H)	2.4	–	V
I_{DD} (PD mode)	Power down supply current	REF = 0 MHz	–	25.0	μA
I_{DD}	Supply current	Unloaded outputs, 100 MHz, Select inputs at V_{DD} or GND	–	45.0	mA
			–	70(–1H, –5H)	mA
		Unloaded outputs, 66 MHz REF (–1, –2, –3, –4)	–	35.0	mA
		Unloaded outputs, 66 MHz REF (–1, –2, –3, –4)	–	20.0	mA

Switching Characteristics for Industrial Temperature Devices

Parameter[15]	Name	Test Conditions	Min	Typ	Max	Unit
F_{in}	Input frequency	-	10	-	133.3	MHz
t_1	Output frequency	30 pF load	10	–	100 (-1,-2,-3,-4) 66.67 (-5H)	MHz
t_1	Output frequency	20 pF load, –1H, –5H devices	10	–	133.3 (-1H) 66.67 (-5H)	MHz
t_1	Output frequency	15 pF load, –1, –2, –3, –4 devices	10	–	133.3	MHz
t_{PD}	Duty cycle[14, 15] = $t_2 \div t_1$ (–1, –2, –3, –4, –1H, –5H)	Measured at 1.4 V, F_{OUT} = 66.66 MHz 30 pF load	40.0	50.0	60.0	%
t_{PD}	Duty cycle[14, 15] = $t_2 \div t_1$ (–1, –2, –3, –4, –1H, –5H)	Measured at 1.4 V, F_{OUT} < 50 MHz, 15 pF load	45.0	50.0	55.0	%
t_3	Rise time[14, 15] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	2.50	ns
t_3	Rise time[14, 15] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 15 pF load	–	–	1.50	ns

Notes
13. Applies to both Ref clock and FBK.
14. Parameter is guaranteed by design and characterization. Not 100% tested in production.
15. All parameters are specified with loaded outputs.

Switching Characteristics for Industrial Temperature Devices (continued)

Parameter[15]	Name	Test Conditions	Min	Typ	Max	Unit
t_3	Rise time[16, 17] (–1H, –5H)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	1.50	ns
t_4	Fall time[16, 17] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	2.50	ns
t_4	Fall time[16, 17] (–1, –2, –3, –4)	Measured between 0.8 V and 2.0 V, 15 pF load	–	–	1.50	ns
t_4	Fall time[16, 17] (–1H, –5H)	Measured between 0.8 V and 2.0 V, 30 pF load	–	–	1.25	ns
t_5	Output to output skew on same Bank (–1, –2, –3, –4)[16, 17]	All outputs equally loaded	–	–	200	ps
	Output to output skew (–1H, –5H)	All outputs equally loaded	–	–	200	ps
	Output Bank A to output Bank B skew (–1, –4, –5H)	All outputs equally loaded	–	–	200	ps
	Output Bank A to output Bank B skew (–2, –3)	All outputs equally loaded	–	–	400	ps
t_6	Delay, REF rising edge to FBK rising edge[16, 17]	Measured at $V_{DD}/2$	–	0	±250	ps
t_7	Device to device skew[16, 17]	Measured at $V_{DD}/2$ on the FBK pins of devices	–	0	700	ps
t_8	Output slew rate[16, 17]	Measured between 0.8 V and 2.0 V on –1H, –5H device using Test Circuit 2	1	–	–	V/ns
t_J	Cycle to cycle Jitter[16, 17] (–1, –1H, –4, –5H)	Measured at 66.67 MHz, loaded outputs, 15 pF load	–	75	200	ps
		Measured at 66.67 MHz, loaded outputs, 30 pF load	–	–	200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load	–	–	100	ps
t_J	Cycle to cycle Jitter[16, 17] (–2, –3)	Measured at 66.67 MHz, loaded outputs, 30 pF load	–	–	400	ps
		Measured at 66.67 MHz, loaded outputs, 15 pF load	–	–	400	ps
t_{LOCK}	PLL lock time[16, 17]	Stable power supply, valid clocks presented on REF and FBK pins	–	–	1.0	ms

Notes
16. Parameter is guaranteed by design and characterization. Not 100% tested in production.
17. All parameters are specified with loaded outputs.

Switching Waveforms

Figure 3. Duty Cycle Timing

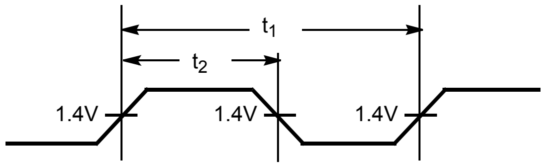


Figure 4. All Outputs Rise/Fall Time

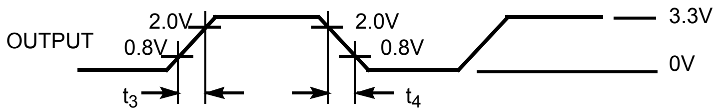


Figure 5. Output-Output Skew

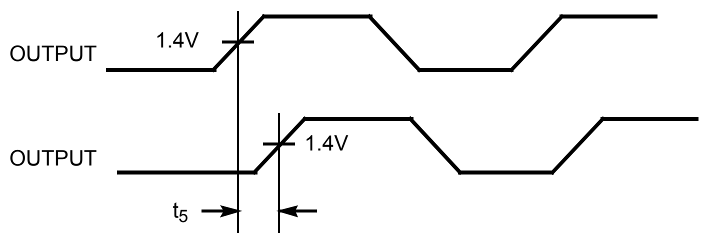


Figure 6. Input-Output Propagation Delay

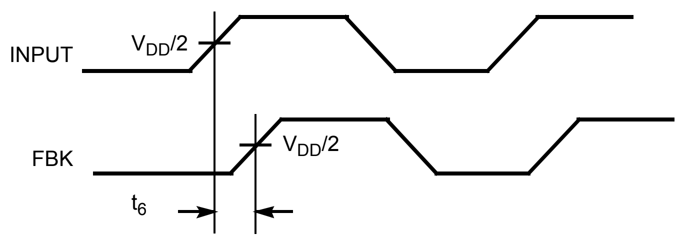
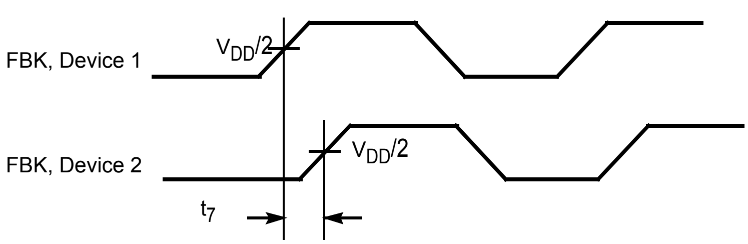
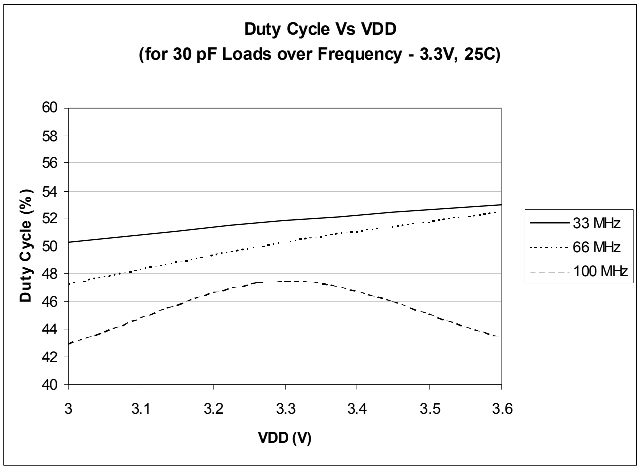
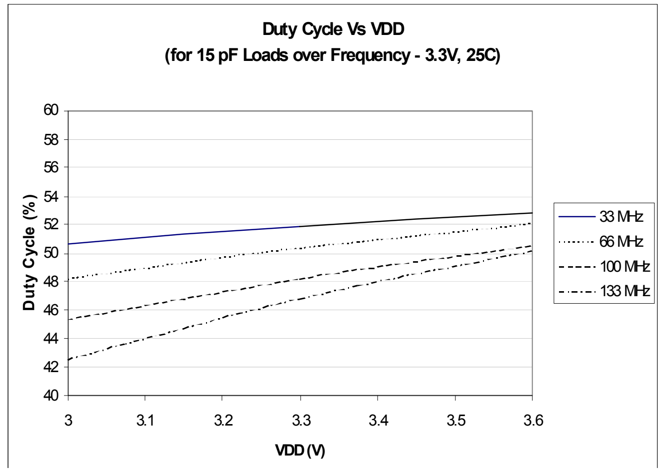


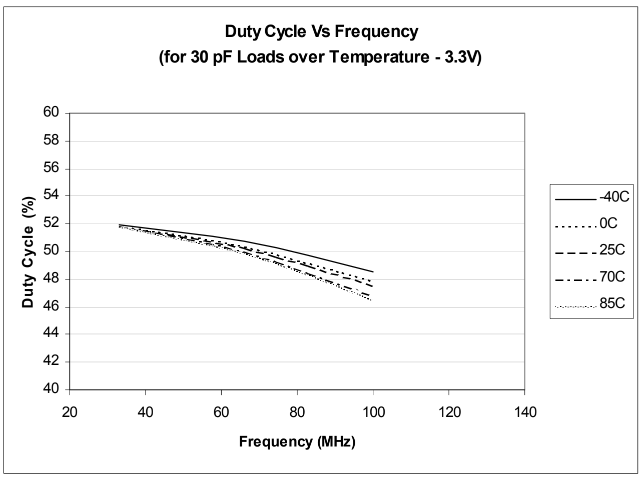
Figure 7. Device-Device Skew

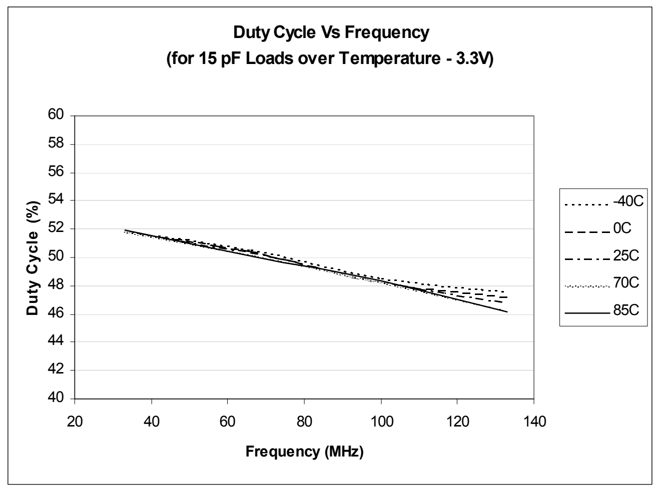


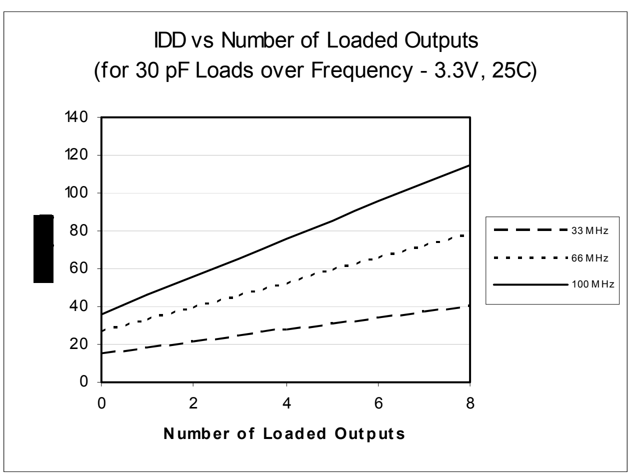
Typical Duty Cycle[18] and I_{DD} Trends[19] for CY2308–1,2,3,4

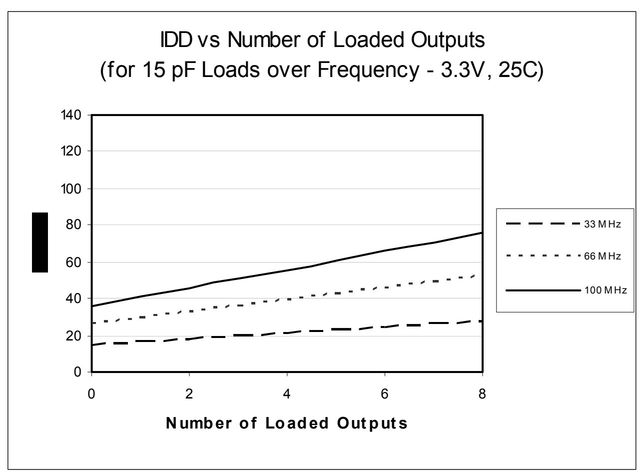








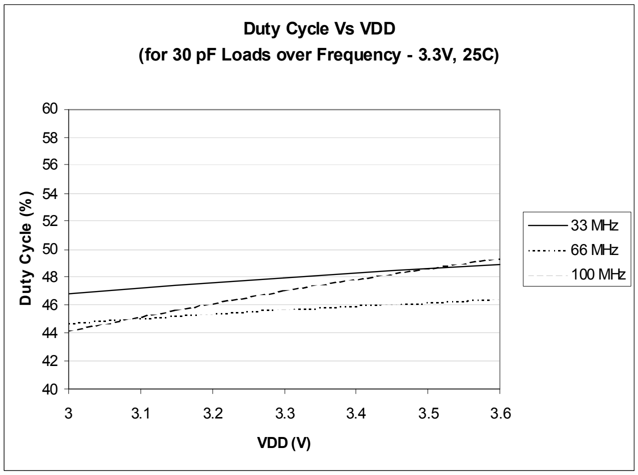


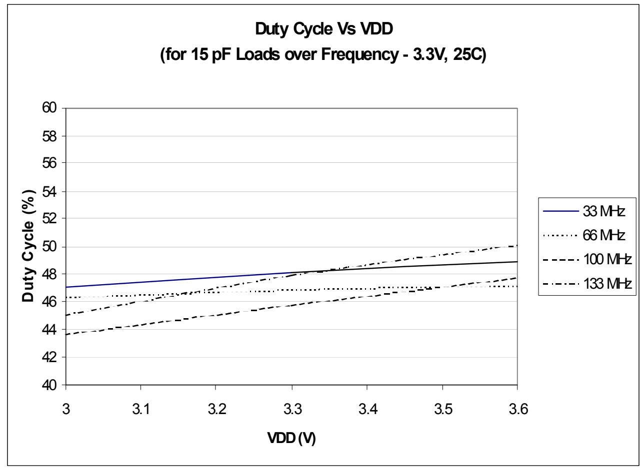


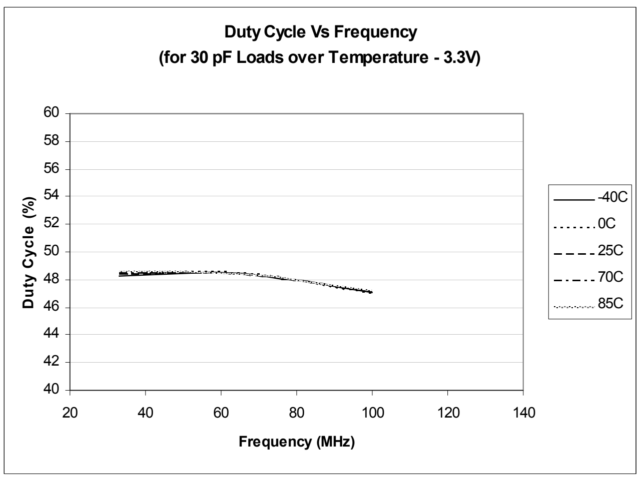
Notes

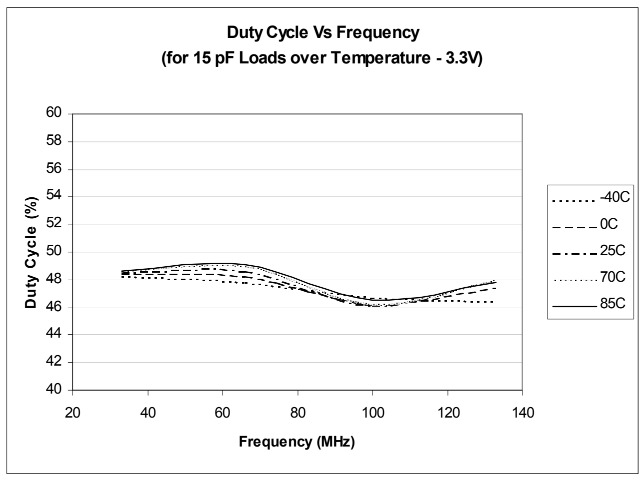
18. Duty cycle is taken from typical chip measured at 1.4 V.
19. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current.
(n = number of outputs; C = Capacitance load per output (F); V = Voltage supply (V); f = frequency (Hz).

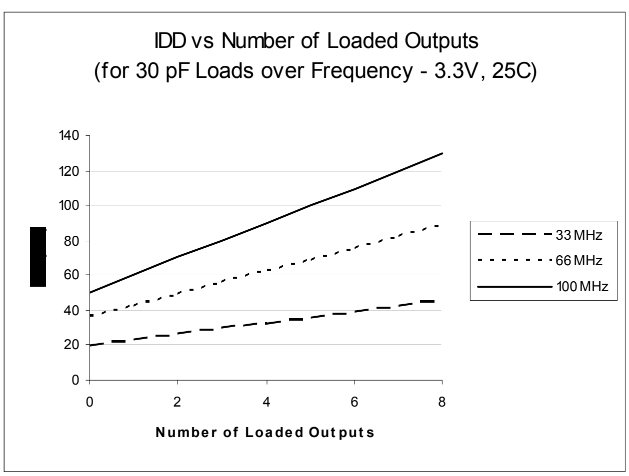
Typical Duty Cycle[20] and I_{DD} Trends[21] for CY2308–1H, 5H

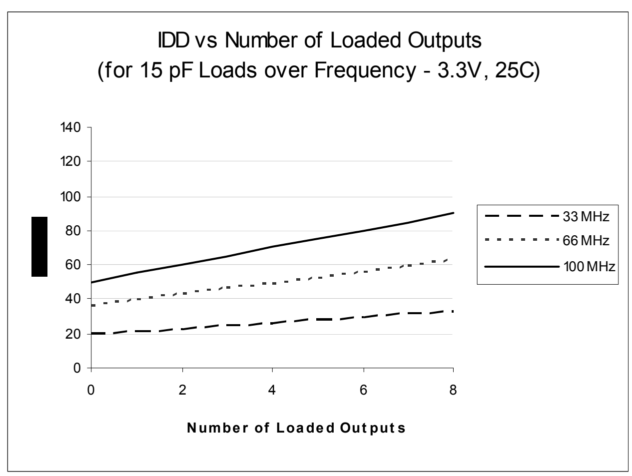










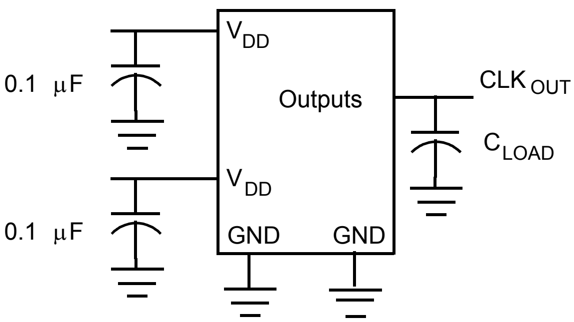


Notes

20. Duty cycle is taken from typical chip measured at 1.4 V.
21. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = number of outputs; C = Capacitance load per output (F); V = Voltage supply (V); f = frequency (Hz).

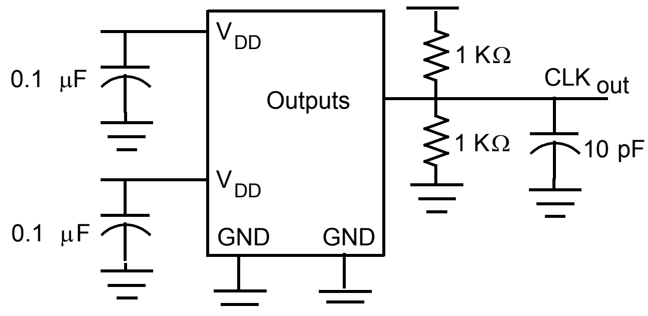
Test Circuits

Test Circuit 1



Test Circuit for all parameters except t_8

Test Circuit 2



Test Circuit for t_8, Output slew rate on –1H, –5H device

Ordering Information

Ordering Code	Package Type	Operating Range
CY2308SI–1T[22]	16-pin 150 mil SOIC – Tape and Reel	Industrial
CY2308SI–1H[22]	16-pin 150 mil SOIC	Industrial
CY2308SI–1HT[22]	16-pin 150 mil SOIC – Tape and Reel	Industrial
CY2308ZI–1H[22]	16-pin 4.4 mm TSSOP	Industrial
CY2308ZI–1HT[22]	16-pin 4.4 mm TSSOP –Tape and Reel	Industrial
CY2308SI–2[22]	16-pin 150 mil SOIC	Industrial
CY2308SI–2T[22]	16-pin 150 mil SOIC – Tape and Reel	Industrial

Note
22. Not recommended for new designs.

Ordering Information (continued)

Ordering Code	Package Type	Operating Range
Pb-free		
CY2308SXC–1	16-pin 150 mil SOIC	Commercial
CY2308SXC–1T	16-pin 150 mil SOIC – Tape and Reel	Commercial
CY2308SXI–1	16-pin 150 mil SOIC	Industrial
CY2308SXI–1T	16-pin 150 mil SOIC – Tape and Reel	Industrial
CY2308SXC–1H	16-pin 150 mil SOIC	Commercial
CY2308SXC–1HT	16-pin 150 mil SOIC –Tape and Reel	Commercial
CY2308SXI–1H	16-pin 150 mil SOIC	Industrial
CY2308SXI–1HT	16-pin 150 mil SOIC – Tape and Reel	Industrial
CY2308ZXC–1H	16-pin 4.4 mm TSSOP	Commercial
CY2308ZXC–1HT	16-pin 4.4 mm TSSOP – Tape and Reel	Commercial
CY2308ZXI–1H	16-pin 4.4 mm TSSOP	Industrial
CY2308ZXI–1HT	16-pin 4.4 mm TSSOP – Tape and Reel	Industrial
CY2308SXC–2	16-pin 150 mil SOIC	Commercial
CY2308SXC–2T	16-pin 150 mil SOIC – Tape and Reel	Commercial
CY2308SXI–2	16-pin 150 mil SOIC	Industrial
CY2308SXI–2T	16-pin 150 mil SOIC – Tape and Reel	Industrial
CY2308SXC–3	16-pin 150 mil SOIC	Commercial
CY2308SXC–3T	16-pin 150 mil SOIC – Tape and Reel	Commercial
CY2308SXI–3	16-pin 150 mil SOIC	Industrial
CY2308SXI–3T	16-pin 150 mil SOIC – Tape and Reel	Industrial
CY2308SXC–4	16-pin 150 mil SOIC	Commercia
CY2308SXC–4T	16-pin 150 mil SOIC – Tape and Reel	Commercial
CY2308SXI–4	16-pin 150 mil SOIC	Industrial
CY2308SXI–4T	16-pin 150 mil SOIC – Tape and Reel	Industrial

Ordering Code Definitions

CY xxx x X I (-x) T

T=Tape and Reel, Blank = Standard

Dash or Variant Code

Temperature Range

C = Commercial = 0 °C to +70 °C

I = Industrial = –40 °C to +85 °C

Pb Free, blank = leaded

Package Type

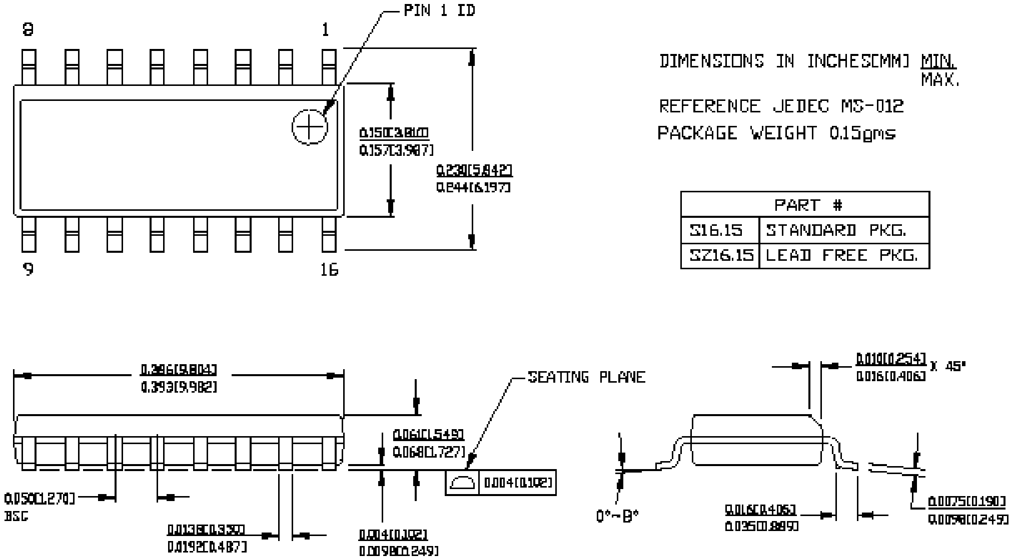
S = SOIC, Z = TSSOP

Part Identifier

Company ID: CY = Cypress

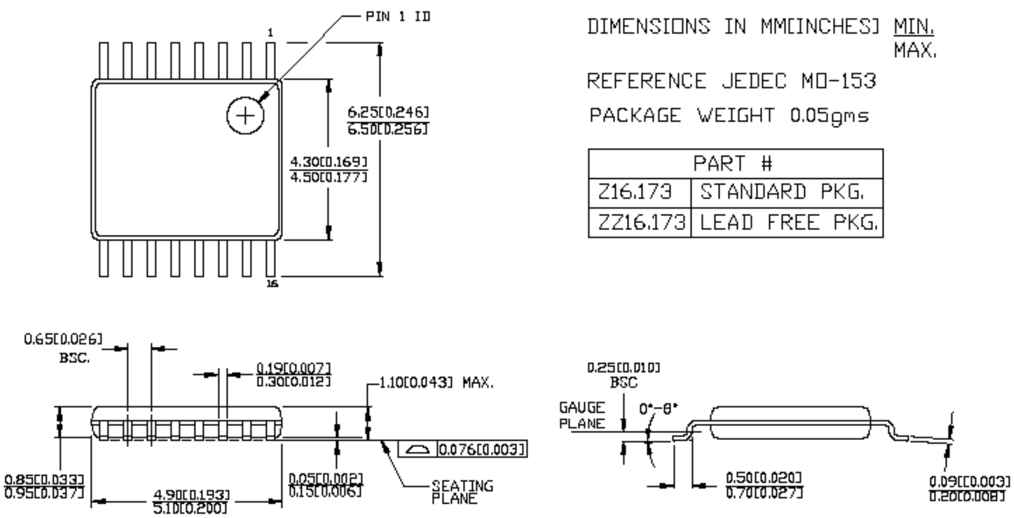
Package Drawings and Dimensions

Figure 8. 16-Pin (150 Mil) SOIC S16.15



51-85068 *C

Figure 9. 16-Pin TSSOP 4.40 mm Body Z16.173



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Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
FBK	Feedback
PLL	Phase locked loop
MUX	Multiplexer

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degrees Celsius	µW	microwatts
dB	decibels	mA	milliamperes
fC	femtoCoulomb	mm	millimeters
fF	femtofarads	ms	milliseconds
Hz	hertz	mV	millivolts
KB	1024 bytes	nA	nanoamperes
Kbit	1024 bits	ns	nanoseconds
kHz	kilohertz	nV	nanovolts
kΩ	kilohms	Ω	ohms
MHz	megahertz	pA	picoamperes
MΩ	megaohms	pF	picofarads
µA	microamperes	pp	peak-to-peak
µF	microfarads	ppm	parts per million
µH	microhenrys	ps	picoseconds
µs	microseconds	sps	samples per second
µV	microvolts	σ	sigma: one standard deviation
µVrms	microvolts root-mean-square		

Document History Page

Rev.	ECN	Orig. of Change	Submission Date	Description of Change
Document Title: CY2308 3.3V Zero Delay Buffer Document Number: 38-07146				
**	110255	SZV	12/17/01	Changed from Specification number: 38-00528 to 38-07146
*A	118722	RGL	10/31/02	Added Note 1 in page 2.
*B	121832	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*C	235854	RGL	06/24/04	Added Pb-free Devices
*D	310594	RGL	02/09/05	Removed obsolete parts in the ordering information table Specified typical value for cycle-to-cycle jitter
*E	1344343	KVM/VED	08/20/07	Brought the Ordering Information Table up to date: removed three obsolete parts and added two parts Changed titles to tables that are specific to commercial and industrial temperature ranges
*F	2568575	AESA	09/19/08	Updated template. Added Note “Not recommended for new designs.” Changed IDD (PD mode) from 12.0 to 25.0 μA for Commercial and Industrial Temperature Devices Deleted Duty Cycle parameters for F_{out} < 50 MHz Removed CY2308SI-4, CY2308SI-4T and CY2308SC-5HT.
*G	2632364	KVM	01/08/09	Corrected TSSOP package size (from 150 mil to 4.4 mm) in Ordering Information table
*H	2673353	KVM/PYRS	03/13/09	Reverted IDD (PD mode) and Duty Cycle parameters back to the values in revision *E: Changed IDD (PD mode) from 25 to 12 μA for commercial temperature devices Added Duty Cycle parameters for F_{out} < 50 MHz for commercial and industrial devices.
*I	2897373	CXQ	03/22/10	Updated ordering information table. Updated copyright section. Updated package diagrams.
*J	2971365	BASH	07/06/10	Updated input to output skew and power down current number in Functional Description, page 1 Update pin descriptions in ‘Pin Description’ column, Table1, page 2 Added ‘Input Frequency’ parameter and output frequency for –1H and –5H in ‘Switching Characteristics Table’ and removed footnote, page 4, 5, and 7. Modified Description on page-1 and page-3 to make clear that user has to select one of the outputs to drive feedback. Added footnote in ‘Available CY2308 Configurations’ Table, page-3, for clarification.
*K	3047133	CXQ	10/04/2010	Sunset Review. No change to datasheet from last revision.
*L	3055192	CXQ	10/11/2010	Removed part CY2308SXI–5H and CY2308SXI–5HI

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