High Voltage Charge Pump, PLL Synthesizer

ADF4113HV

FEATURES

- High voltage charge pump (15 V)
- 2.7 V to 5.5 V power supply
- 200 MHz to 4.0 GHz frequency range
- Pin compatible with ADF4110, ADF4111, ADF4112, ADF4113 ADF4106, and ADF4002 synthesizers
- Two selectable charge pump currents
- Digital lock detect
- Power-down mode
- Loop filter design possible with ADIsimPLL™

APPLICATIONS

- Applications using high voltage VCOs
- IF/RF local oscillator (LO) generation in base stations
- Point-to-point radio LO generation
- Clock for analog-to-digital and digital-to-analog converters
- Wireless LANs, PMR
- Communications test equipment

GENERAL DESCRIPTION

The ADF4113HV is an integer-N frequency synthesizer with a high voltage charge pump (15 V). The synthesizer is designed for use with voltage controlled oscillators (VCOs) that have high tuning voltages (up to 15 V). Active loop filters are often used to achieve high tuning voltages, but the ADF4113HV charge pump can drive a high voltage VCO directly with a passive-loop filter. The ADF4113HV can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision high voltage charge pump, a programmable reference divider, programmable A and B counters, and a dual-modulus prescaler (P/P + 1).

A simple 3-wire interface controls all of the on-chip registers. The devices operate with a power supply ranging from 2.7 V to 5.5 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

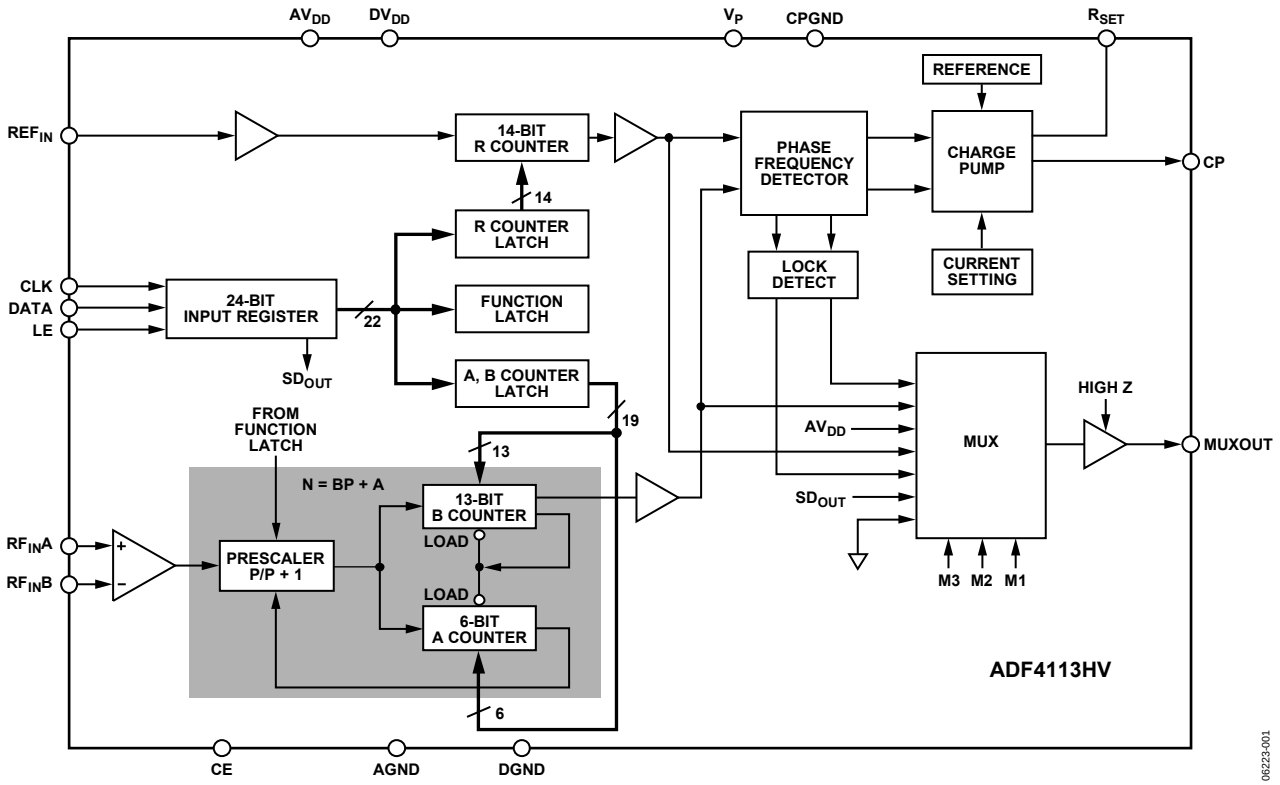

Figure 1.

Rev. A

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TABLE OF CONTENTS

REVISION HISTORY

9/08—Rev. 0 to Rev. A

Changes to Figure 22 13

1/07—Revision 0: Initial Version

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SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V ± 10%, 5 V ± 10%; 13.5 V < V_P ≤ 16.5 V; AGND = DGND = CPGND = 0 V; R_{SET} = 4.7 kΩ; dBm referred to 50 Ω; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Operating temperature range for B version: −40°C to +85°C.

Table 1.

Parameter	B Version	B Chips[1]	Unit	Test Conditions/Comments
RF CHARACTERISTICS (3 V)				
RF Input Sensitivity	−15/0	−15/0	dBm min/max	
RF Input Frequency	0.2/3.7	0.2/3.7	GHz min/max	For lower frequencies, ensure SR > 130 V/µs
Prescaler Output Frequency[2]	165	165	MHz max	
RF CHARACTERISTICS (5 V)				
RF Input Sensitivity	−10/0	−10/0	dBm min/max	
RF Input Frequency	0.2/3.7	0.2/3.7	GHz min/max	For lower frequencies, ensure SR > 130 V/µs
	0.2/4.0	0.2/4.0	GHz min/max	Input level = −5 dBm
Prescaler Output Frequency	200	200	MHz max	
REF_{IN} CHARACTERISTICS				
REF_{IN} Input Frequency	5/150	5/150	MHz min/max	For f < 5 MHz, ensure SR > 100 V/µs
Reference Input Sensitivity	0.4/AV_{DD}	0.4/AV_{DD}	V p-p min/max	AV_{DD} = 3.3 V, biased at $AV_{DD}/2$[3]
	1.0/AV_{DD}	1.0/AV_{DD}	V p-p min/max	For f ≥ 10 MHz, AV_{DD} = 5 V, biased at $AV_{DD}/2$[3, 4]
REF_{IN} Input Capacitance	10	10	pF max	
REF_{IN} Input Current	±100	±100	µA max	
PHASE DETECTOR FREQUENCY	5	5	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				R_{SET} = 4.7 kΩ
High Value	640	640	µA typ	
Low Value	80	80	µA typ	
Absolute Accuracy	2.5	2.5	% typ	
R_{SET} Range	3.9/10	3.9/10	kΩ typ	
I_{CP} Three-State Leakage Current	5	5	nA max	
Sink and Source Current Matching	3	3	% typ	1 V ≤ V_{CP} ≤ V_P − 1 V
I_{CP} vs. V_{CP}	1.5	1.5	% typ	1 V ≤ V_{CP} ≤ V_P − 1 V
I_{CP} vs. Temperature	2	2	% typ	V_{CP} = V_P/2
LOGIC INPUTS				
V_{INH}, Input High Voltage	0.8 × DV_{DD}	0.8 × DV_{DD}	V min	
V_{INL}, Input Low Voltage	0.2 × DV_{DD}	0.2 × DV_{DD}	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	DV_{DD} − 0.4	DV_{DD} − 0.4	V min	I_{OH} = 500 µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES				
AV_{DD}	2.7/5.5	2.7/5.5	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	13.5/16.5	13.5/16.5	V min/V max	
I_{DD}[5] (AI_{DD} + DI_{DD})	16	11	mA max	11 mA typical
I_P	0.25	0.25	mA max	T_A = 25°C
Low Power Sleep Mode	1	1	µA typ	
NOISE CHARACTERISTICS				
Normalized Phase Noise Floor[6]	−212	−212	dBc/Hz typ	

[1] The B chip specifications are given as typical values.
[2] This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[3] AC coupling ensures $AV_{DD}/2$ bias.
[4] Guaranteed by characterization.
[5] T_A = 25°C; AV_{DD} = DV_{DD} = 5.5 V; P = 16; RF_{IN} = 900 MHz.
[6] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO, PN_{TOT}, and subtracting 20logN (where N is the N divider value) and 10logf_{PFD}: PN_{SYNTH} = PN_{TOT} − 10logf_{PFD} − 20logN.

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TIMING CHARACTERISTICS

Guaranteed by design but not production tested. AV_{DD} = DV_{DD} = 3 V ± 10%, 5 V ± 10%; 13.5 V ≤ V_P ≤ 16.5 V; AGND = DGND = CPGND = 0 V; R_{SET} = 4.7 kΩ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Timing Diagram

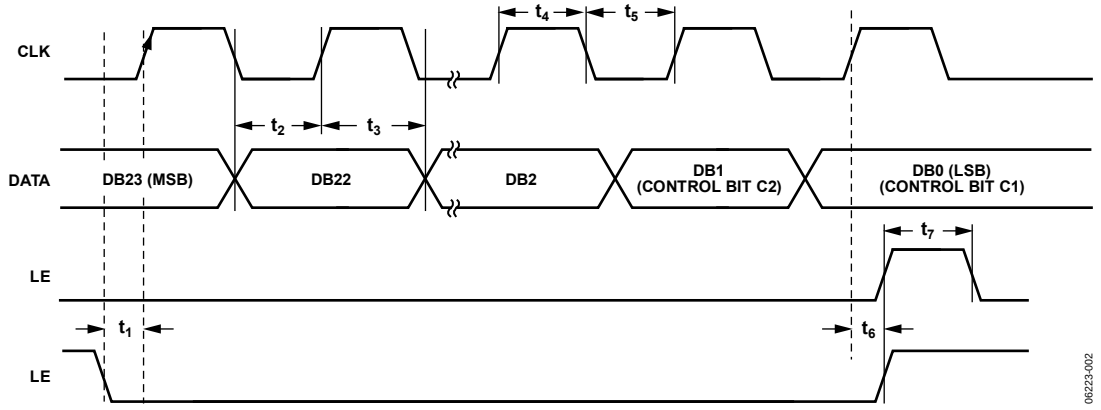

Figure 2. Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND[1]	−0.3 V to +7 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +18 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	−0.3 V to V_{DD} + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$	±320 mV
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

[1] GND = AGND = DGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <1 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

TRANSISTOR COUNT

The transistor count is 12,150 (CMOS) and 348 (bipolar).

THERMAL RESISTANCE

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
TSSOP	150.4	°C/W
LFCSP (Paddle Soldered)	122	°C/W
LFCSP (Paddle Not Soldered)	216	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

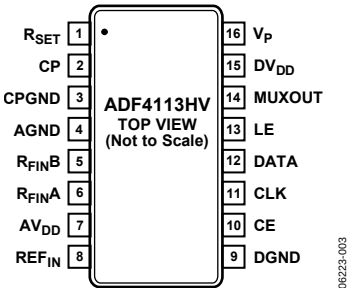

Figure 3. TSSOP Pin Configuration

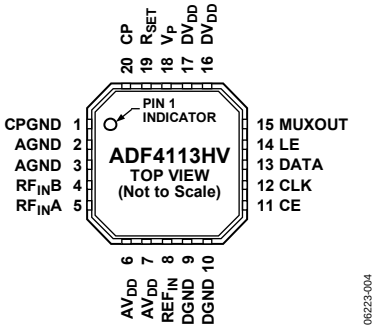

Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1	19	R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.56 V for the ADF4113HV. The relationship between I_{CP} and R_{SET} is $I_{CPmax} = 3/R_{SET}$. Therefore, with R_{SET} = 4.7 kΩ, I_{CPmax} = 640 µA.
2	20	CP	Charge Pump Output. When enabled, this pin provides ±I_{CP} to the external loop filter; in turn, this drives the external VCO.
3	1	CPGND	Charge Pump Ground. CPGND is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	$RF_{IN}B$	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	5	$RF_{IN}A$	Input to the RF Prescaler. This small-signal input is ac-coupled from the VCO.
7	6, 7	AV_{DD}	Analog Power Supply. The power supply can range from 2.7 V to 5.5 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
8	8	REF_{IN}	Reference Input. This pin is a CMOS input with a nominal threshold of $V_{DD}/2$, and an equivalent input resistance of 100 kΩ. This input can be driven from a TTL or CMOS crystal oscillator, or can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	CE	Chip Enable. A Logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high powers up the device depending on the status of the Power-Down Bit PD1.
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches; the latch is selected using the control bits.
14	15	MUXOUT	Multiplexer Output. This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be externally accessed.
15	16, 17	DV_{DD}	Digital Power Supply. This can range from 2.7 V to 5.5 V. Decoupling capacitors to the digital ground plane (1µF, 1nF) should be placed as close as possible to this pin. For best performance, the 1 µF capacitor should be placed within 2 mm of the pin. The placing of the 1nF capacitor is less critical but should still be within 5 mm of the pin. DV_{DD} must have the same value as AV_{DD}.
16	18	V_P	Charge Pump Power Supply. V_P can range from 13.5 V to 16.5 V and should be decoupled appropriately.

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TYPICAL PERFORMANCE CHARACTERISTICS

Loop bandwidth = 25 kHz, reference = 10 MHz reference from Agilent E4440A PSA, VCO = Sirenza VCO190-1500T(Y), evaluation board = EVAL-ADF4113HVEBZ1.

FREQ –UNIT	PARAM –TYPE	DATA –FORMAT	KEYWORD		IMPEDANCE –OHMS
GHz	S	MA	R		50
FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.05	0.89207	–2.0571	1.05	0.9512	–40.134
0.10	0.8886	–4.4427	1.10	0.93458	–43.747
0.15	0.89022	–6.3212	1.15	0.94782	–44.393
0.20	0.96323	–2.1393	1.20	0.96875	–46.937
0.25	0.90566	–12.13	1.25	0.92216	–49.6
0.30	0.90307	–13.52	1.30	0.93755	–51.884
0.35	0.89318	–15.746	1.35	0.96178	–51.21
0.40	0.89806	–18.056	1.40	0.94354	–53.55
0.45	0.89565	–19.693	1.45	0.95189	–56.786
0.50	0.88538	–22.246	1.50	0.97647	–58.781
0.55	0.89699	–24.336	1.55	0.98619	–60.545
0.60	0.89927	–25.948	1.60	0.95459	–61.43
0.65	0.87797	–28.457	1.65	0.97945	–61.241
0.70	0.90765	–29.735	1.70	0.98864	–64.051
0.75	0.88526	–31.879	1.75	0.97399	–66.19
0.80	0.81267	–32.681	1.80	0.97216	–63.775
0.85	0.90357	–31.522			
0.90	0.92954	–34.222			
0.95	0.92087	–36.961			
1.00	0.93788	–39.343			

06223-005

Figure 5. S-Parameter Data for the ADF4113HV RF Input (Up to 1.8 GHz)

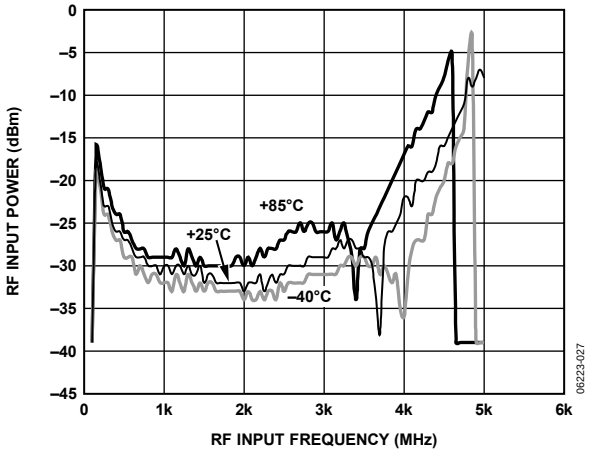

Figure 6. Input Sensitivity

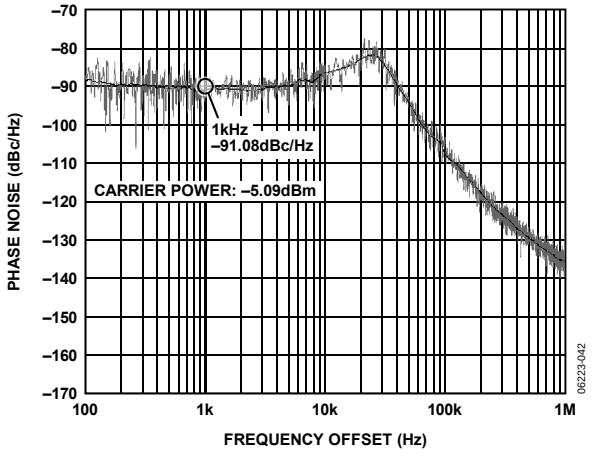

Figure 7. Integrated Phase Noise
(RF = 1000 MHz, PFD = 1 MHz, V_{TUNE} = 1.8 V, RMS Noise = 0.93°)

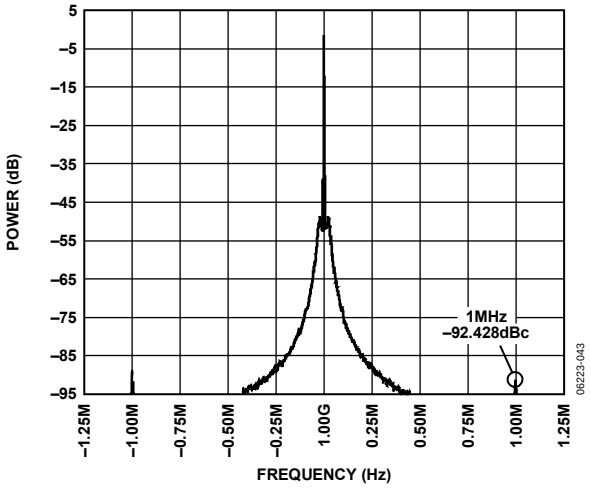

Figure 8. Reference Spurs (RF = 1000 MHz, PFD = 1 MHz)

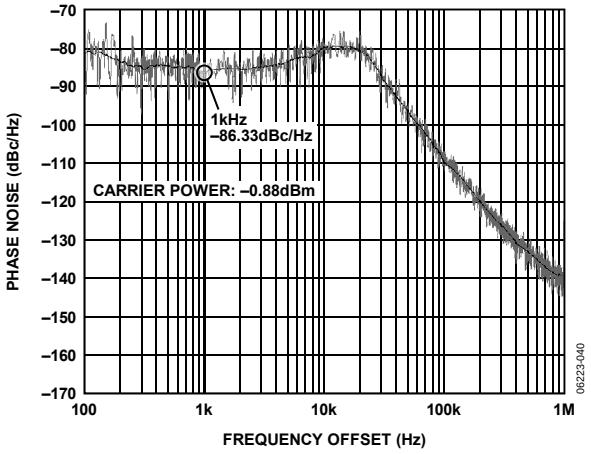

Figure 9. Integrated Phase Noise
(RF = 1800 MHz, PFD= 1 MHz, V_{TUNE} = 13.1 V, RMS Noise = 1.16°)

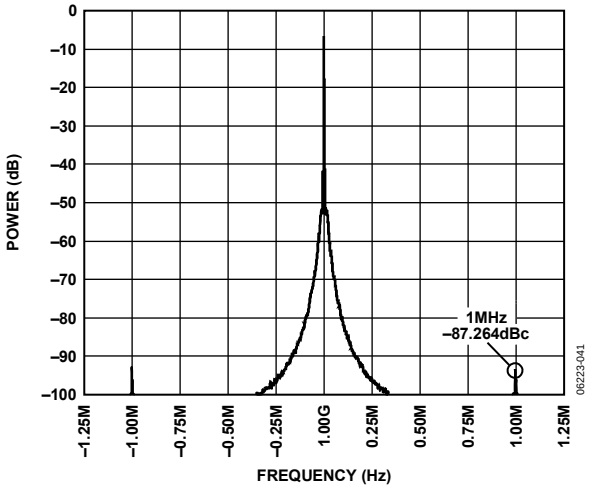

Figure 10. Reference Spurs (RF = 1800 MHz, PFD = 1 MHz)

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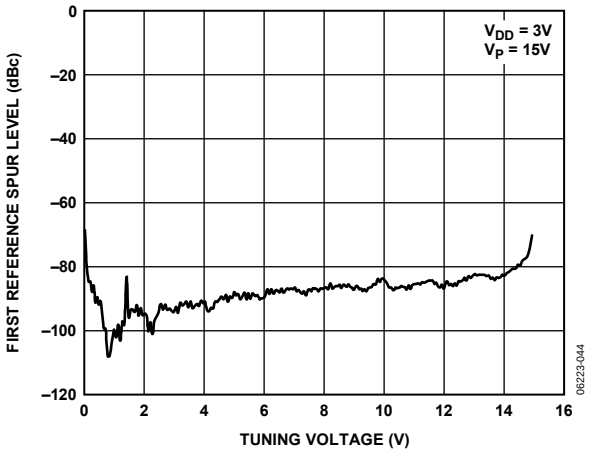

Figure 11. PFD Spurs (1 MHz) vs. V_{TUNE}

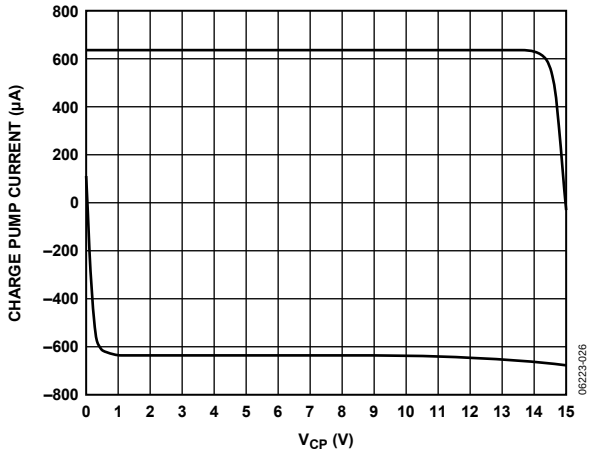

Figure 13. Charge Pump Output Characteristics

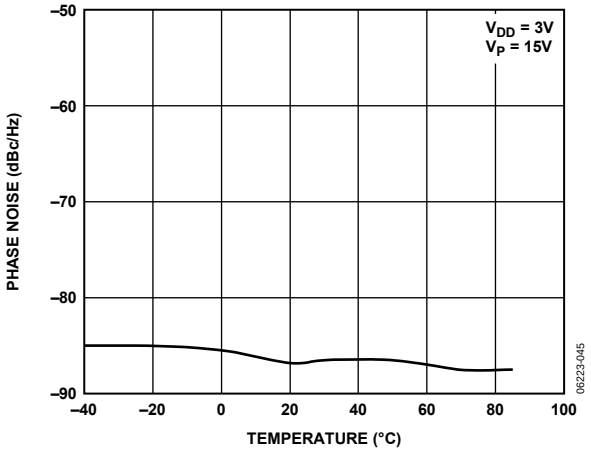

Figure 12. Phase Noise vs. Temperature (RF = 1500 MHz, PFD = 1 MHz)

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CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 14. SW1 and SW2 are normally closed switches (NC in Figure 14). SW3 is normally open (NO in Figure 14). When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

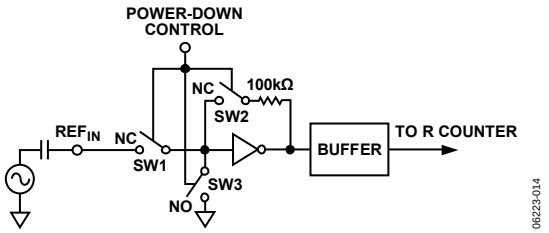

Figure 14. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 15. It is followed by a two-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

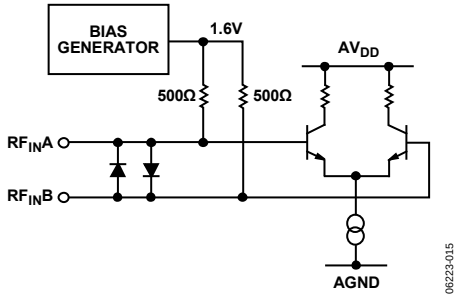

Figure 15. RF Input Stage

PRESCALER (P/P + 1)

Together with the A and B counters, the dual-modulus prescaler (P/P + 1) enables the large division ratio, N, to be realized by

$$N = BP + A$$

The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and CMOS B counters. The prescaler is programmable; it can be set in software to 8/9, 16/17, 32/33, or 64/65. It is based on a synchronous 4/5 core.

A AND B COUNTERS

The A and B CMOS counters combine with the dual-modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 200 MHz or less (for AV_{DD} = 5 V). Thus, with an RF input frequency of 2.5 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not.

Pulse Swallow Function

The A and B counters, in conjunction with the dual-modulus prescaler, make it possible to generate output frequencies that are spaced only by the reference frequency divided by R. The equation for the VCO frequency is

$$f_{VCO} = [(P \times B) + A]f_{REFIN}/R$$

where:

f_{VCO} = output frequency of external voltage controlled oscillator (VCO).

P = preset modulus of dual-modulus prescaler.

B = preset divide ratio of binary 13-bit counter (3 to 8191).

A = preset divide ratio of binary 6-bit swallow counter (0 to 63).

f_{REFIN} = output frequency of the external reference frequency oscillator.

R = preset divide ratio of binary 14-bit programmable reference counter (1 to 16,383).

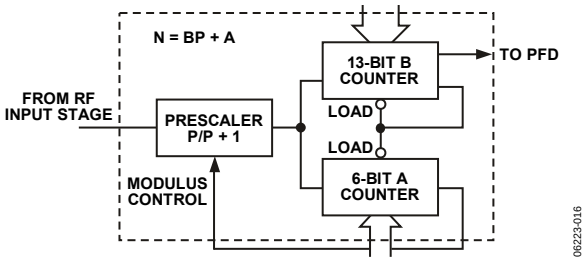

Figure 16. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

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PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 17 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse. See Figure 20. The only recommended setting for the antibacklash pulse width is 7.2 ns.

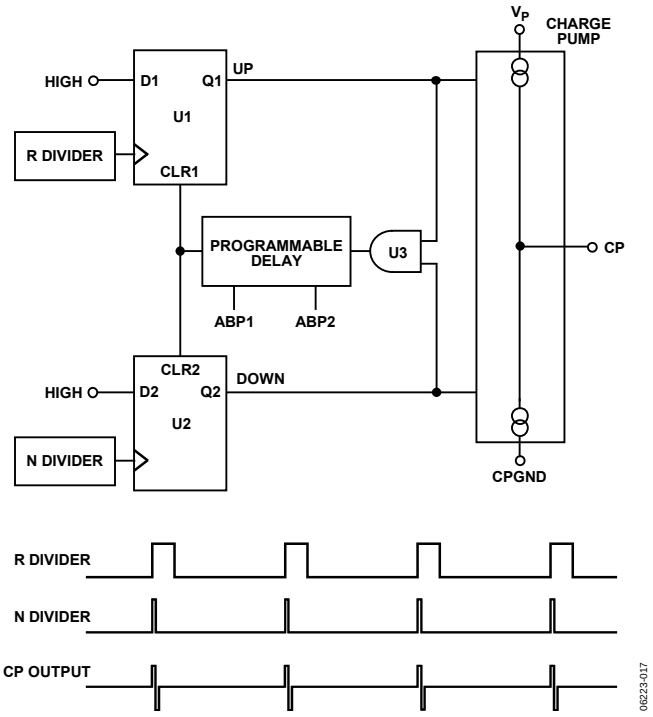

Figure 17. PFD Simplified Schematic and Timing (in Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4113HV allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Figure 22 shows the full truth table (function latch map). Figure 18 shows the MUXOUT section in block diagram form.

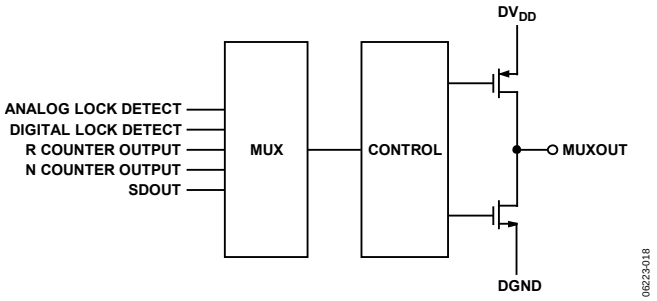

Figure 18. MUXOUT Circuit

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the AB counter latch is set to 0, digital lock detect is set high when the phase error on five consecutive phase detector (PD) cycles is less than 10 ns. With LDP set to 1, five consecutive cycles of less than 3 ns are required to set the lock detect. It stays high until a phase error greater than 25 ns is detected on any subsequent PD cycle.

Operate the N-channel, open-drain, analog lock detect with a 10 kΩ nominal external pull-up resistor. When lock has been detected, this output is high with narrow low-going pulses.

INPUT SHIFT REGISTER

The ADF4113HV digital section includes a 24-bit input shift register, a 14-bit R counter, and a 19-bit N counter comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK, MSB first. Data is transferred from the shift register to one of three latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 6. Figure 19 shows a summary of how the latches are programmed.

Table 6. C2, C1 Truth Table

Control Bits		
C2	**C1**	**Data Latch**
0	0	R counter
0	1	N counter (A and B)
1	0	Function latch (including prescaler)

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Latch Summary

REFERENCE COUNTER LATCH

RESERVED						ANTI-BACKLASH PULSE WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(0)	C1(0)

N COUNTER LATCH

RE-SERVED	LD PREC	RE-SERVED	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	L1	0	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2(0)	C1(1)

FUNCTION LATCH

PRE-SCALER VALUE		RESERVED				CURRENT SETTING			RESERVED						CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER DOWN	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	0	0	0	0	CP3	CP2	CP1	0	0	0	0	0	0	F4	F3	M3	M2	M1	F2	F1	C2(1)	C1(0)

06223-019

Figure 19. Latch Summary Tables

Reference Counter Latch Map

RESERVED						ANTI-BACKLASH PULSE WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2(0)	C1(0)

THESE BITS MUST BE SET AS INDICATED FOR NORMAL OPERATION

ABP2	ABP1	ANTI-BACKLASH PULSE WIDTH
1	0	7.2ns (ONLY ALLOWED SETTING)

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

06223-020

Figure 20. Reference Counter Latch Bit Map

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AB Counter Latch Map

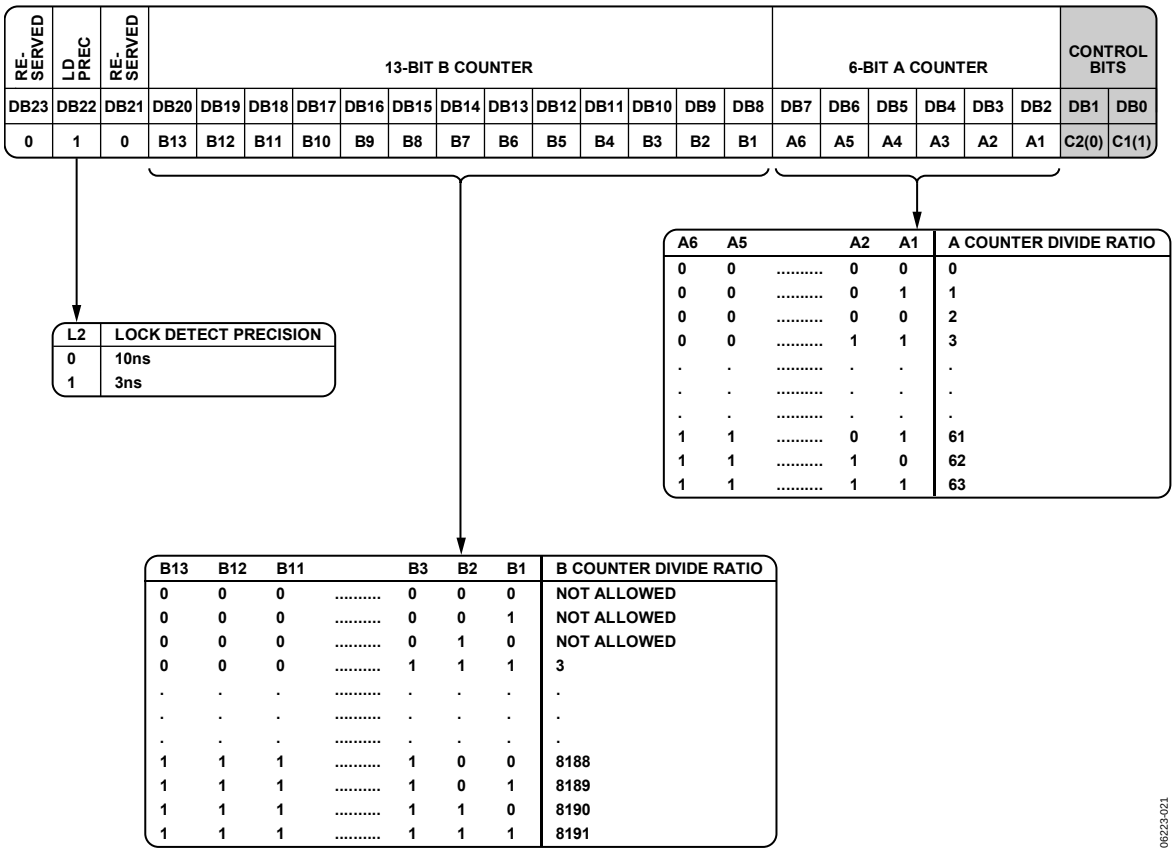

Figure 21. B Counter Latch Map

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Function Latch Map

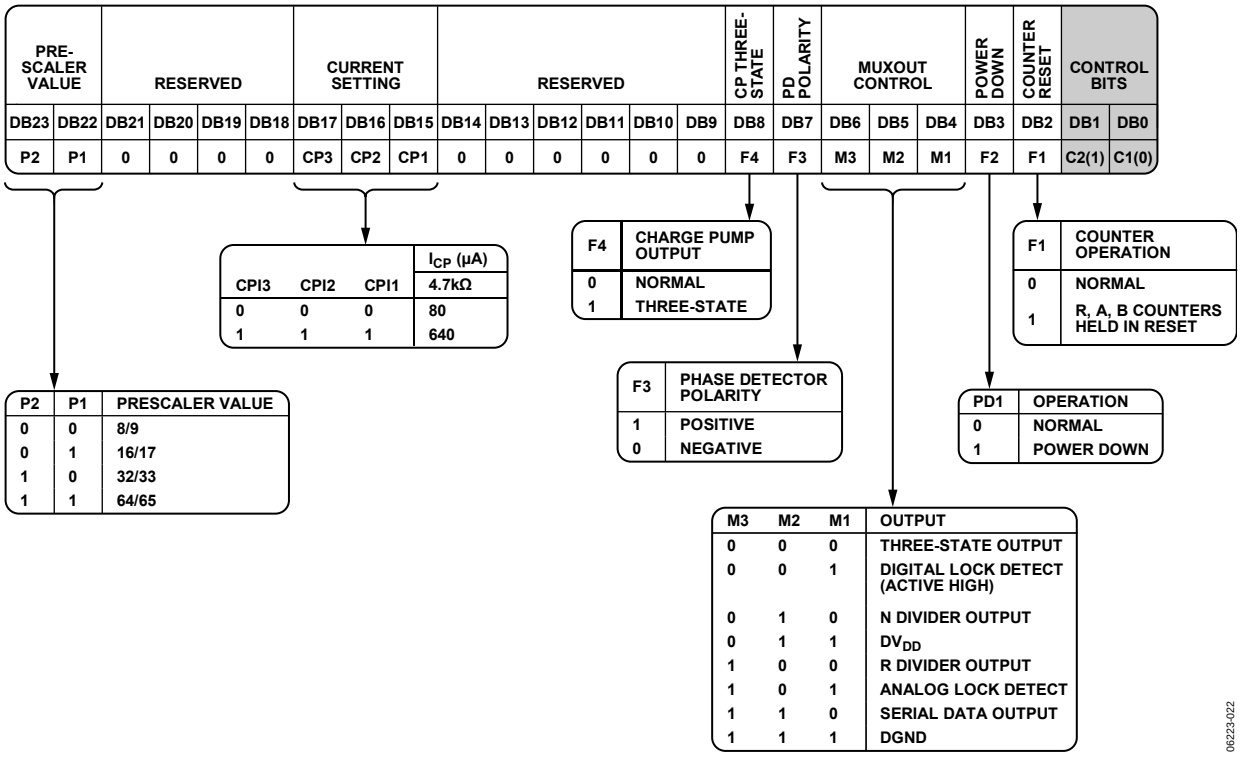

Figure 22. Function Latch Map

FUNCTION LATCH

The on-chip function latch is programmed with C2 and C1 set to 1,0, respectively. Figure 22 shows the input data format for programming the function latch.

Counter Reset

DB2 (F1) is the counter reset bit. When DB2 is 1, the R counter and the AB counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit must be disabled, and the N counter resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle.)

Power-Down

DB3 (F2) in the function latch provides a software power-down for the ADF4113HV. The device powers down immediately after latching a 1 into Bit F2.

When the CE pin is low, the device immediately powers down regardless of the state of the power-down bit (F2).

When a power-down is activated (either through software or a CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The $RF_{IN}A$ and $RF_{IN}B$ inputs are debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, and M1 on the ADF4113HV. Figure 22 shows the truth table.

Charge Pump Currents

CPI3, CPI2, and CPI1 program the current setting for the charge pump. The truth table is given in Figure 22.

Prescaler Value

P2 and P1 in the function latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 200 MHz. Thus, with an RF frequency of 2 GHz, a prescaler value of 16/17 is valid, but a value of 8/9 is not.

PD Polarity

This bit sets the phase detector polarity bit. See Figure 22.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

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DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initial power-up of the device, there are two ways to program the device.

CE Pin Method

1. Apply V_{DD}.
2. Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
3. Program the function latch (10). Program the R counter latch (00). Program the AB counter latch (01).
4. Bring CE high to take the device out of power-down. The R and AB counters resume counting in close alignment.

After CE goes high, a duration of 1 µs is sometimes required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

1. Apply V_{DD}.
2. Conduct a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.
3. Conduct an R counter load (00 in 2 LSBs).
4. Conduct an AB counter load (01 in 2 LSBs).
5. Conduct a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

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APPLICATIONS

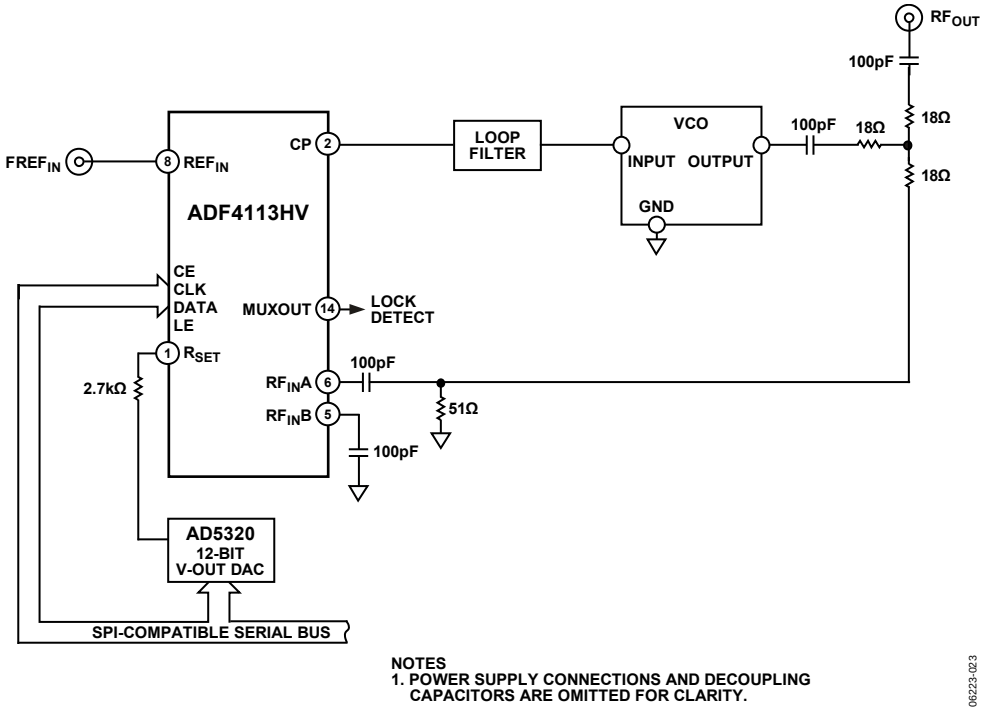

Figure 23. Driving the R_{SET} Pin with a Digital-to-Analog Converter

USING A DIGITIAL-TO-ANALOG CONVERTER TO DRIVE THE R_{SET} PIN

A digital-to-analog converter (DAC) can be used to drive the R_{SET} pin of the ADF4113HV, thus increasing the level of control over the charge pump current (I_{CP}). This can be advantageous in wideband applications where the sensitivity of the VCO varies over the tuning range. To compensate for this, I_{CP} can be varied to maintain good phase margin and ensure loop stability. See Figure 23 for this configuration.

INTERFACING

The ADF4113HV has a simple SPI®-compatible serial interface for writing to the device. CLK, DATA, and LE control the data transfer. When latch enable (LE) goes high, the 24 bits that have been clocked into the input register on each rising edge of CLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 6 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz, or one update every 1.2 µs. This rate is more than adequate for systems that have typical lock times in the hundreds of microseconds.

ADuC812 Interface

Figure 24 shows the interface between the ADF4113HV and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4113HV needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

I/O port lines on the ADuC812 are also used to control power-down (CE input), and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When the ADuC812 is operating in the SPI master mode, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 166 kHz.

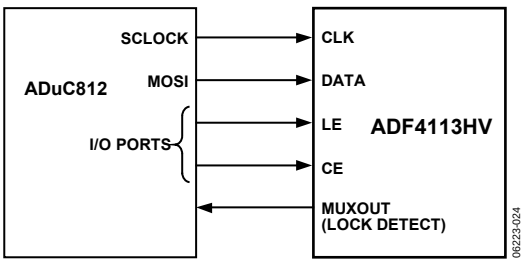

Figure 24. ADuC812 to ADF4113HV Interface

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ADSP-21xx Interface

Figure 25 shows the interface between the ADF4113HV and the ADSP-21xx digital signal processor. The ADF4113HV needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the auto buffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated.

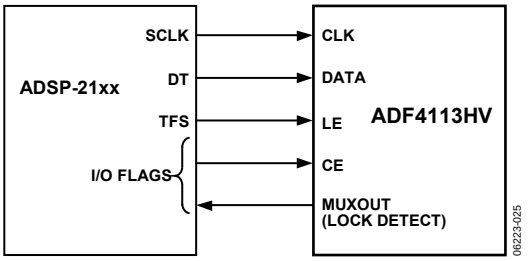

Figure 25. ADSP-21xx to ADF4113HV Interface

Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the auto buffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the chip scale package (CP-20-1) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length, and 0.05 mm wider than the package land width. The land should be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, provide a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern. This ensures that shorting is avoided.

Thermal vias can be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at a 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.

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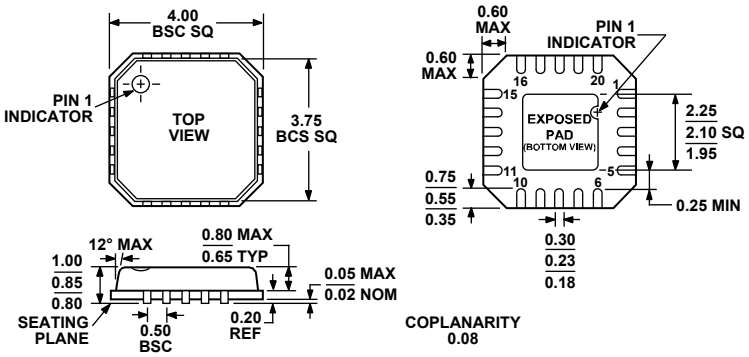
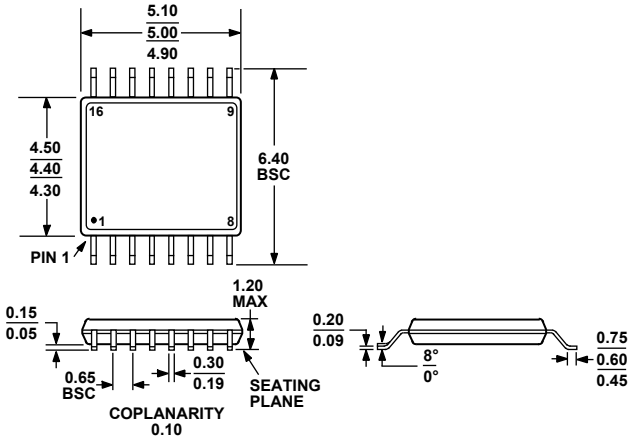
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 26. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm x 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 27. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADF4113HVBRUZ[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113HVBRUZ-RL[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113HVBRUZ-RL7[1]	−40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4113HVBCPZ[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
ADF4113HVBCPZ-RL[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
ADF4113HVBCPZ-RL7[1]	−40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-1
EVAL-ADF4113HVEB1Z[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

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