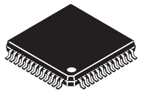
3.3V/2.5V 1:15 PECL/LVCMOS Clock Fanout Buffer

MPC9449

3.3V/2.5V 1:15 PECL/LVCMOS CLOCK FANOUT BUFFER



FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D

The MPC9449 is a 3.3V or 2.5V compatible, 1:15 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews less than 200 ps the device meets the needs of the most demanding clock applications.

Features

- 15 LVCMOS compatible clock outputs
- Two selectable LVCMOS and one differential LVPECL compatible clock inputs
- Selectable output frequency divider (divide-by-one and divide-by-two)
- Maximum clock frequency of 200 MHz
- Maximum clock skew of 200 ps
- High-impedance output control
- 3.3V or 2.5V power supply
- Drives up to 30 series terminated clock lines
- Ambient temperature range –40°C to +85°C
- 52 lead LQFP packaging
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC949

Functional Description

The MPC9449 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 200 MHz. The device has 15 identical outputs, organized in 4 output banks. Each output bank provides a retimed or frequency divided copy of the input signal with a near zero skew. The output buffer supports driving of 50Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable LVCMOS compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9449 accepts one differential PECL clock signal. The DSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the four output banks. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of –40°C to +85°C. The MPC9449 is pin and function compatible but performance-enhanced to the MPC949. The device is packaged in a 52-lead LQFP package.

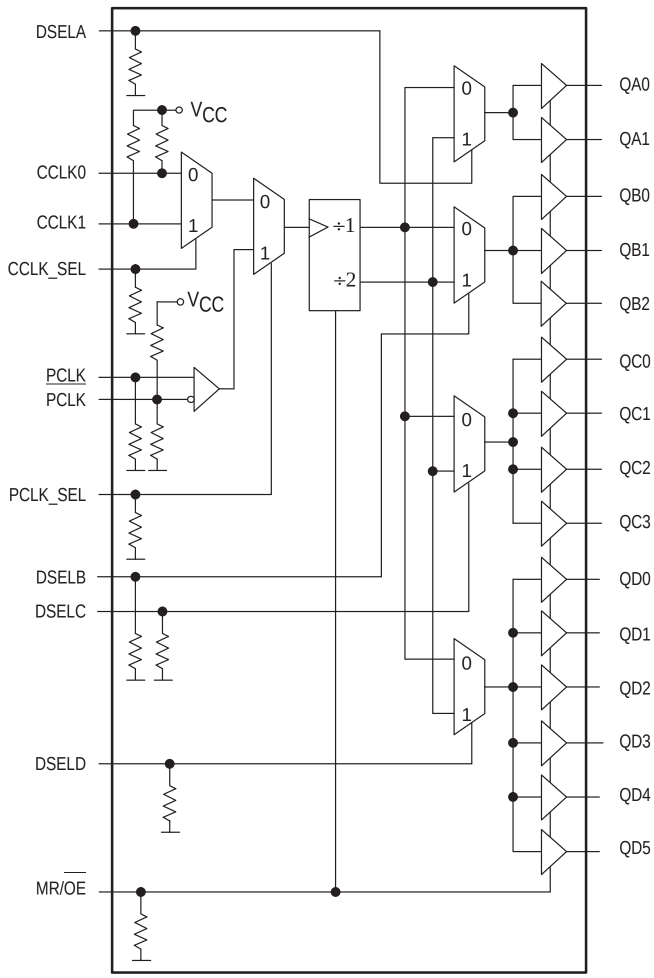


Figure 1. MPC9449 Logic Diagram

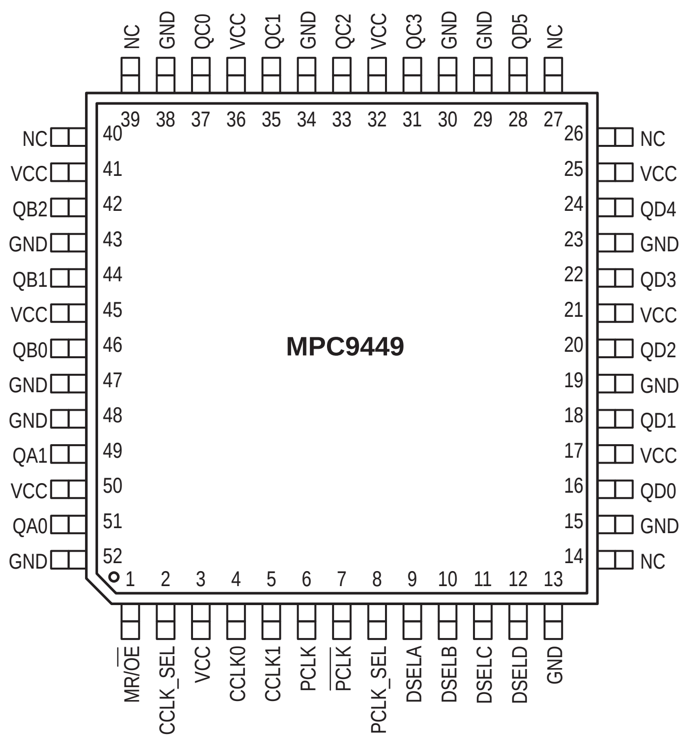


Figure 2. MPC9449 52–Lead Package Pinout (Top View)

Table 1: FUNCTION TABLE

Control	Default	0	1
PCLK_SEL	0	LVCMOS clock input selected (CCLK0 or CCLK1)	PCLK differential input selected
CCLK_SEL	0	CCLK0 selected	CCLK1 selected
DSELA, DSELB, DSELC, DSELD	0 0 0 0	÷1	÷2
MR/$\overline{OE}$	1	Outputs enabled	Outputs disabled (high impedance)

Table 2: PIN CONFIGURATION

Pin	I/O	Type	Function
PCLK, $\overline{PCLK}$	Input	LVPECL	Differential LVPECL clock input
CCLK0, CCLK1	Input	LVCMOS	LVCMOS clock inputs
PCLK_SEL	Input	LVCMOS	LVPECL clock input select
CCLK_SEL	Input	LVCMOS	LVCMOS clock input select
DSELA, DSELB, DSELC, DSELD	Input	LVCMOS	Clock divider selection
MR/$\overline{OE}$	Input	LVCMOS	Output enable/disable (high-impedance tristate)
QA0-1, QB0-2, QC0-3, QD0-5	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
VCC	Supply	VCC	Positive power supply for I/O and core. All VCC pins must be connected to the positive power supply for correct operation

Table 3: GENERAL SPECIFICATIONS

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch–Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4: ABSOLUTE MAXIMUM RATINGS[a]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.8	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

a. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5: DC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[a]
V_{PP}	Peak-to-peak input voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[b]	Common Mode Range PCLK, $\overline{PCLK}$	1.0		V_{CC}-0.6	V	LVPECL
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output impedance		14 - 17		Ω	
I_{IN}	Input Current			±200	µA	V_{IN}=V_{CC} or GND
I_{CCQ}	Maximum Quiescent Supply Current			10	mA	All V_{CC} Pins

a The MPC9449 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

b V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

Table 6: AC CHARACTERISTICS (V_{CC} = 3.3V ± 5%, T_A = –40°C to 85°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Peak-to-peak input voltage PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[c]	Common Mode Range PCLK, $\overline{PCLK}$	1.0		V_{CC}-0.6	V	LVPECL
f_{max}	Output frequency	0		200	MHz	
f_{ref}	Input Frequency	0		200	MHz	
$t_{P, REF}$	Reference Input Pulse Width	1.5			ns	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{sk(O)}$	Output-to-output Skew Qa outputs Qb outputs Qc outputs Qd outputs same frequency All outputs different frequencies All outputs			50 50 50 100 200 300	ps ps ps ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew		2.5		ns	
$t_{sk(P)}$	Output Pulse Skew			250	ps	DC_{REF} = 50%
$t_{PLH, HL}$	Propagation delay CCLK0 or CCLK1 to any Q PCLK to any Q	1.0 1.0	3.0 3.0	5.0 5.0	ns ns	
$t_{PLZ, HZ}$	Output Disable Time OE to any Q			11	ns	
$t_{PZL, LZ}$	Output Enable Time OE to any Q			11	ns	
t_r, t_f	Output Rise/Fall Time[c]	0.1		1.0	ns	0.55 to 2.4V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)		TBD		ps	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

b V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts propagation delay.

c An input rise/fall time greater than that specified may be used, but AC characteristics are not guaranteed under such a condition.

Table 7: DC CHARACTERISTICS (V_{CC} = 2.5V ± 5%, T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage	-0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-peak input voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[a]	Common Mode Range PCLK, $\overline{PCLK}$	1.0		V_{CC}-0.6	V	LVPECL
V_{OH}	Output High Voltage	1.8			V	I_{OH}=-15 mA[b]
V_{OL}	Output Low Voltage			0.6	V	I_{OL}= 15 mA
Z_{OUT}	Output impedance		17 - 20		Ω	
I_{IN}	Input Current[c]			±200	µA	V_{IN}=V_{CC} or GND
I_{CC}	Maximum Quiescent Supply Current			10	mA	All V_{CC} Pins

a V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

b The MPC9449 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}.

c Inputs have pull-down or pull-up resistors affecting the input current.

Table 8: AC CHARACTERISTICS (V_{CC} = 2.5V ± 5%, T_A = –40°C to 85°C)[a]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Peak-to-peak input voltage PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[b]	Common Mode Range PCLK, $\overline{PCLK}$	1.2		V_{CC}-0.6	V	LVPECL
f_{max}	Output frequency	0		200	MHz	
f_{ref}	Input Frequency	0		200	MHz	
$t_{P, REF}$	Reference Input Pulse Width	1.5			ns	
tr, tf	CCLK Input Rise/Fall Time			1.0	ns	0.7 to 1.7V
$t_{sk(O)}$	Output-to-output Skew Qa outputs Qb outputs Qc outputs Qd outputs same frequency All outputs different frequencies All outputs			50 50 50 100 200 300	ps ps ps ps ps ps	
$t_{sk(PP)}$	Device-to-device Skew		5.0		ns	
$t_{SK(P)}$	Output Pulse Skew			350	ps	DC_{REF} = 50%
$t_{PLH, HL}$	Propagation delay CCLK0 or CCLK1 to any Q PCLK to any Q	1.0 1.0	3.5 3.5	7.0 7.0	ns ns	
$t_{PLZ, HZ}$	Output Disable Time OE to any Q			11	ns	
$t_{PZL, LZ}$	Output Enable Time OE to any Q			11	ns	
t_r, t_f	Output Rise/Fall Time[c]	0.1		1.0	ns	0.6 to 1.8V
$t_{JIT(CC)}$	Cycle-to-cycle jitter RMS (1 σ)		TBD		ps	

a AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

b V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts propagation delay.

c An input rise/fall time greater than that specified may be used, but AC characteristics are not guaranteed under such a condition.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9449 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}÷2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9449 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3. "Single versus Dual Transmission Lines" illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9449 clock driver is effectively doubled due to its capability to drive multiple lines.

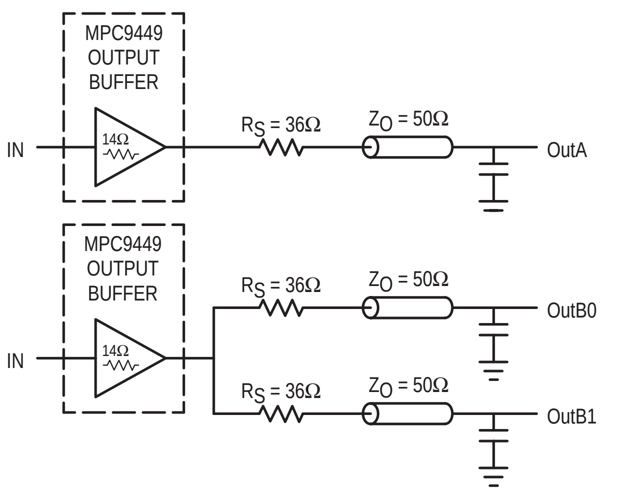


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4. "Single versus Dual Line Termination Waveforms" show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9449 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9449. The output waveform in Figure 4. "Single versus Dual Line Termination Waveforms" shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S \left(Z_0 \div (R_S + R_0 + Z_0) \right)$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 \left(25 \div (18+17+25) \right)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

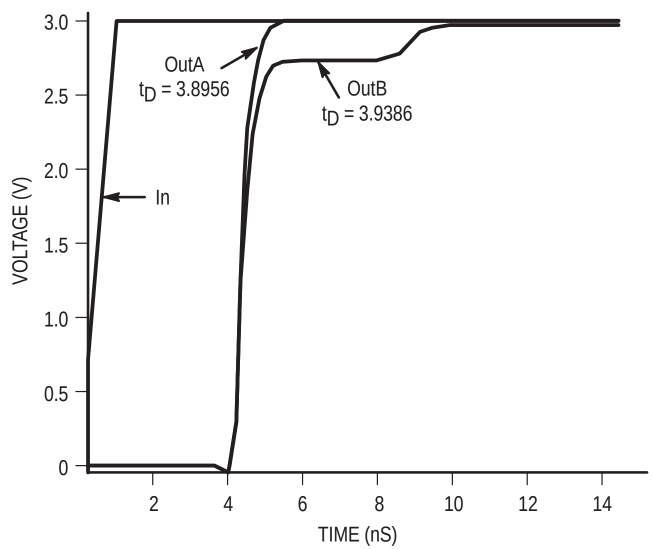
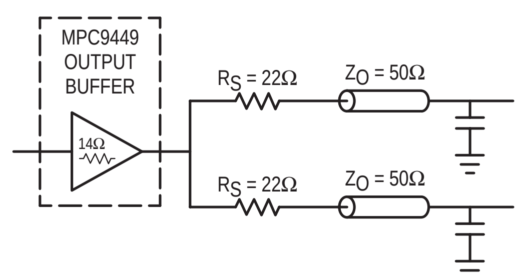


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5. "Optimized Dual Line Termination" should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$$
$$25\Omega = 25\Omega$$

Figure 5. Optimized Dual Line Termination

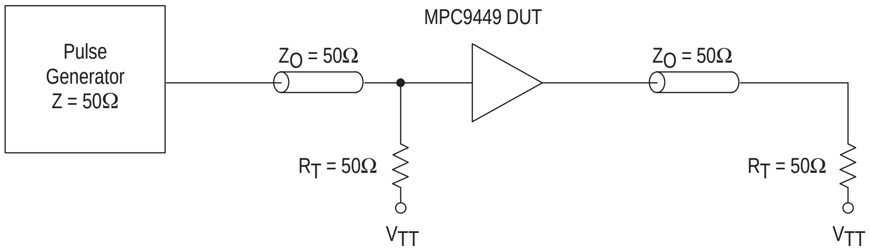


Figure 6. CCLK MPC9449 AC test reference for V_{CC} = 3.3V and V_{CC} = 2.5V

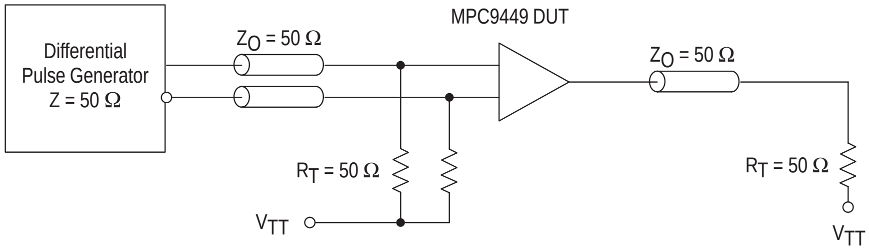
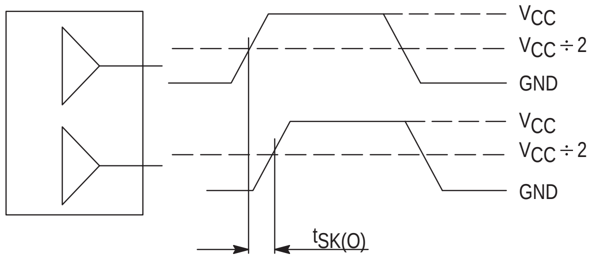


Figure 7. PCLK MPC9449 AC test reference



The pin–to–pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output–to–output Skew $t_{SK(O)}$

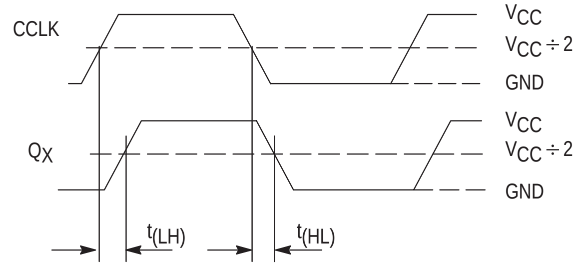


Figure 9. Propagation delay (t_{PD}) test reference

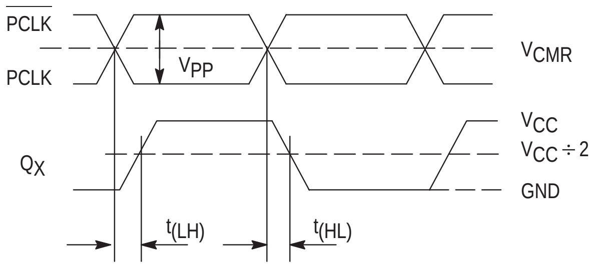
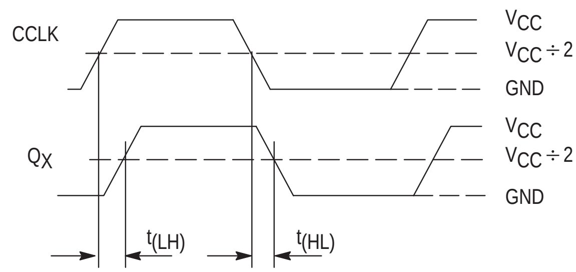
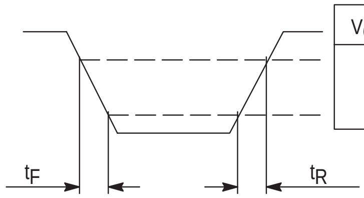


Figure 10. Propagation delay (t_{PD}) test reference



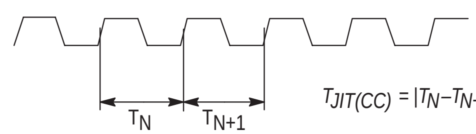
$t_{SK(P)} = | t_{PLH} - t_{PHL} |$

Figure 11. Output Pulse Skew $t_{SK(P)}$ test reference



V_{CC}=3.3V	V_{CC}=2.5V
2.4	1.8V
0.55	0.6V

Figure 12. Output Transition Time Test Reference



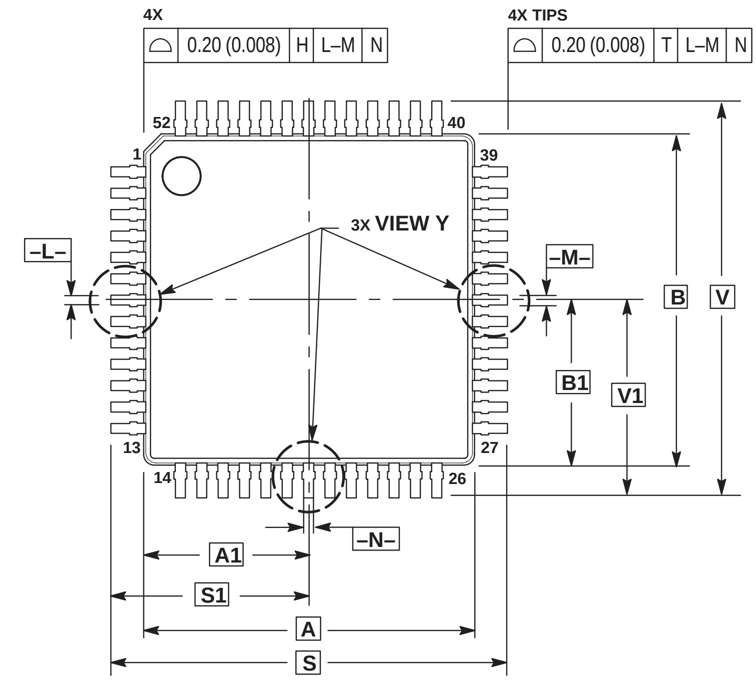
$T_{JIT(CC)} = |T_N - T_{N+1}|$

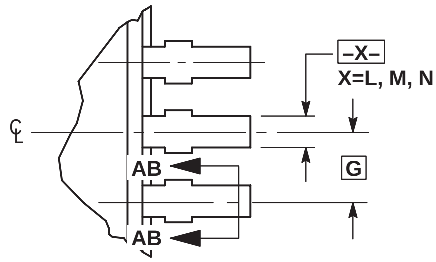
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 13. Cycle–to–cycle Jitter

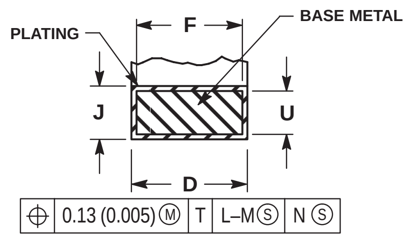
OUTLINE DIMENSIONS

FA SUFFIX
LQFP PACKAGE
CASE 848D-03
ISSUE C



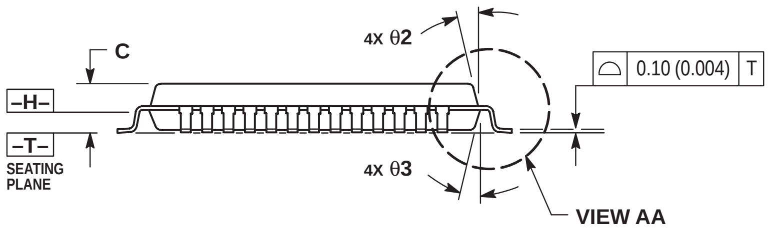


VIEW Y

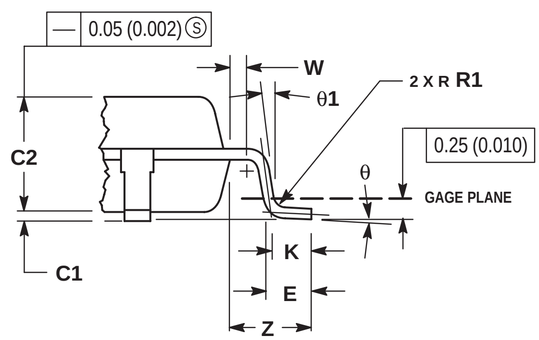


SECTION AB–AB
ROTATED 90° CLOCKWISE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –H– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –L–, –M– AND –N– TO BE DETERMINED AT DATUM PLANE –H–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –T–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 (0.003).



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	—	1.70	—	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
θ	0°	7°	0°	7°
θ1	0°	—	0°	—
θ2	12° REF		12° REF	
θ3	5°	13°	5°	13°



VIEW AA

NOTES

NOTES

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