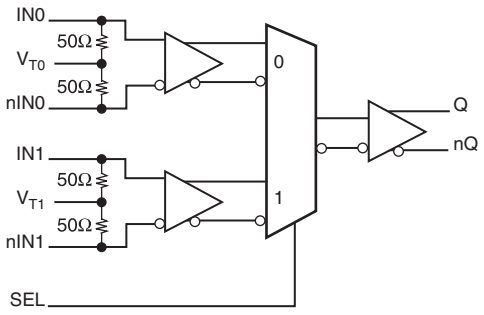
General Description

The ICS858018 is a high performance 2:1 Differential-to-LVPECL Multiplexer and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS858018 differential inputs have internal termination resistors and when used in conjunction with the V_{T0}/V_{T1} pins, allow the inputs to interface with several differential signal types. The ICS858018 is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

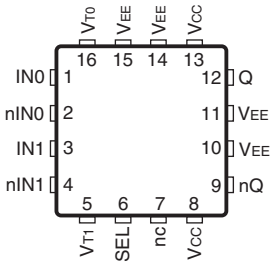
Features

- One LVPECL output
- INx/nINx pairs can accept the following differential input levels: LVPECL, LVDS, CML
- Maximum output frequency: 2GHz
- Propagation delay: 700ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Supply voltage range:
  (LVPECL) V_{CC} = 2.375V to 3.63V, V_{EE} = 0V
  (ECL) V_{CC} = 0V, V_{EE} = -3.63V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS858018

16-Lead VFQFN
3mm x 3mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	IN0	Input		Non-inverting differential LVPECL clock input.
2	nIN0	Input		Inverting differential LVPECL clock input.
3	IN1	Input		Non-inverting differential LVPECL clock input.
4	nIN1	Input		Inverting differential LVPECL clock input.
5, 16	V_{T1}, V_{T0}	Input		Input for termination. Both IN and nIN inputs are terminated to this pin. See Application Information section, *Differential Input with Built-in 50Ω Termination Interface.*
6	SEL	Input	Pullup	Select pin. LVCMOS/LVTTL interface levels.
7	nc	Unused		No connect.
8, 13	V_{CC}	Power		Power supply pins.
9, 12	nQ, Q	Output		Differential output pair. LVPECL/ECL interface levels.
10, 11, 14, 15	V_{EE}	Power		Negative supply pins.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ

Table 3. Truth Table

Inputs					Outputs	
IN0	nIN0	IN1	nIN1	SEL	Q	nQ
0	1	X	X	0	0	1
1	0	X	X	0	1	0
X	X	0	1	1	0	1
X	X	1	0	1	1	0

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	-0.5V to + 4.0V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Input Current, IN/nIN	+50mA
V_T Current, I_{VT}	+100mA
Operating Temperature Range, T_A	-40°C to 85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	88.5°C/W (0 mps)

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±10% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.63	V
I_{EE}	Power Supply Current				21	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = 3.3V±10% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°**C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{CC} = 3.3V	2		V_{CC} + 0.3	V
		V_{CC} = 2.5V	1.7		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 3.3V	-0.3		0.8	V
		V_{CC} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{CC} = V_{IN} = 3.63V or 2.625V			10	µA
I_{IL}	Input Low Current	V_{CC} = 3.63V or 2.625V, V_{IN} = 0V	-150			µA

Table 4C. DC Characteristics, V_{CC} = 3.3V±10% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°**C**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
R_{IN}	Differential Input Resistance	INx/nINx	IN to V_T	40	50	60	Ω
V_{IH}	Input High Voltage	INx/nINx		1.2		V_{CC}	V
V_{IL}	Input Low Voltage	INx/nINx		0		V_{IH} – 0.15	V
V_{IN}	Input Voltage Swing			0.15		2.8	V
V_{DIFF_IN}	Differential Input Voltage Swing			0.3		3.4	V
IN	Input Current; NOTE 1	INx/nINx				35	mA

NOTE 1: Guaranteed by design.

Table 4D. LVPECL DC Characteristics, V_{CC} = 3.3V±10% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°**C**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1			V_{CC} – 1.005		V
V_{OL}	Output Low Voltage; NOTE 1			V_{CC} – 1.78		V
V_{OUT}	Output Voltage Swing		0.6		1.0	V
V_{DIFF_OUT}	Differential Output Voltage Swing		1.2		2.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.

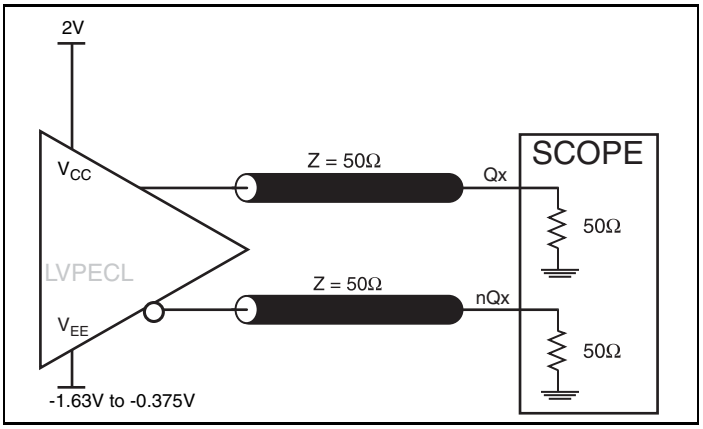
AC Electrical Characteristics

Table 3. LVPECL AC Characteristics, V_{CC} = 3.3V±10% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C

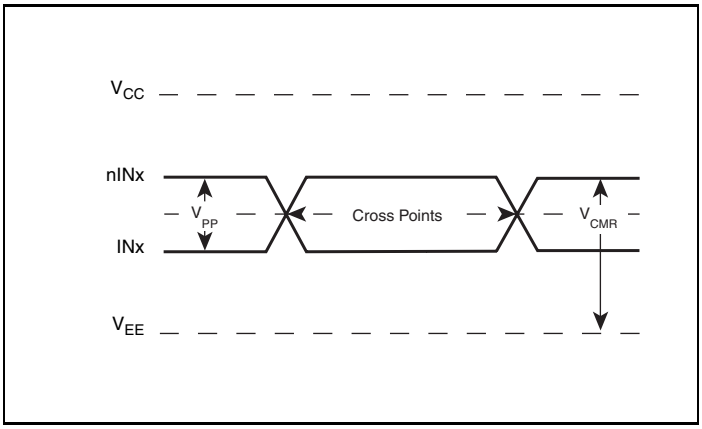
Parameter	Symbol		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency		V_{OUT} ≥ 450mV			2	GHz
t_{PD}	Propagation Delay, Differential; NOTE 1	IN0 or IN1-to-Q		350		700	ps
		SEL-to-Q		0.175		1.3	ns
*t*sk(i)	Input Skew; NOTE 2					35	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4					250	ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	75		375	ps

All parameters characterized at ≤ 1GHz unless otherwise noted
T_A, Ambient Temperature applied using forced air flow.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between inputs measured to the same output at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

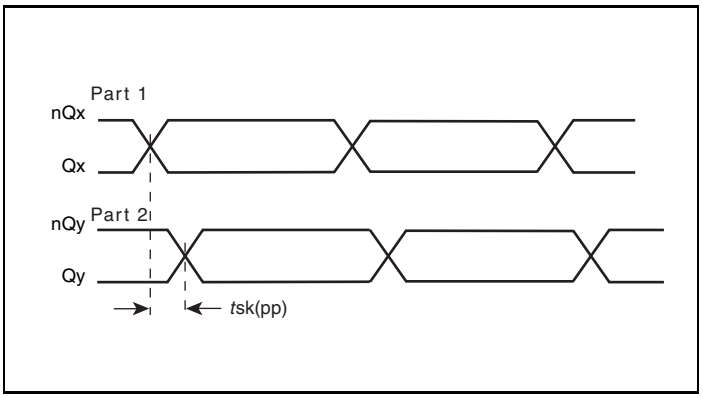
Parameter Measurement Information



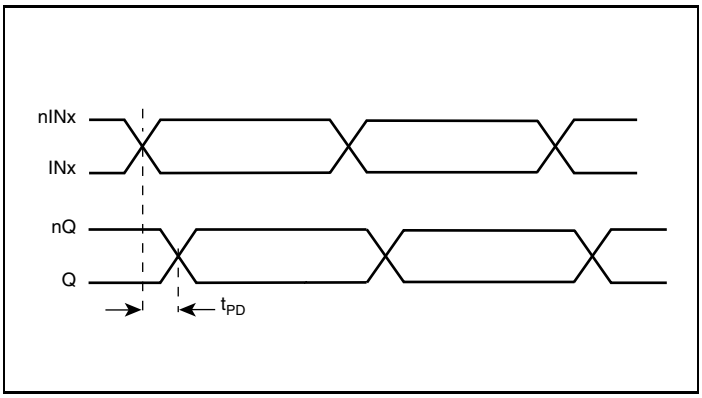
Output Load AC Test Circuit



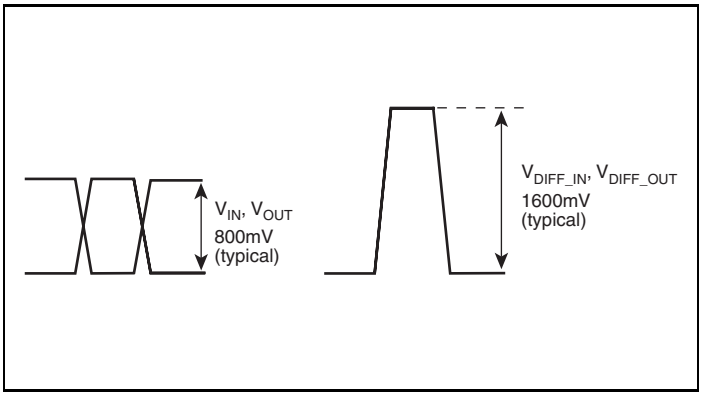
Differential Input Level



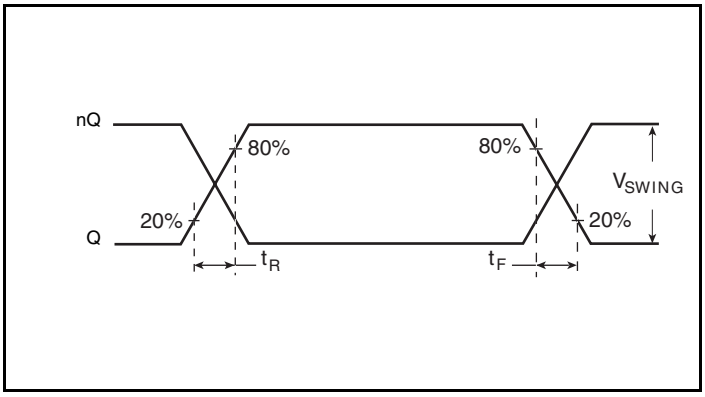
Part-to-Part Skew



Propagation Delay

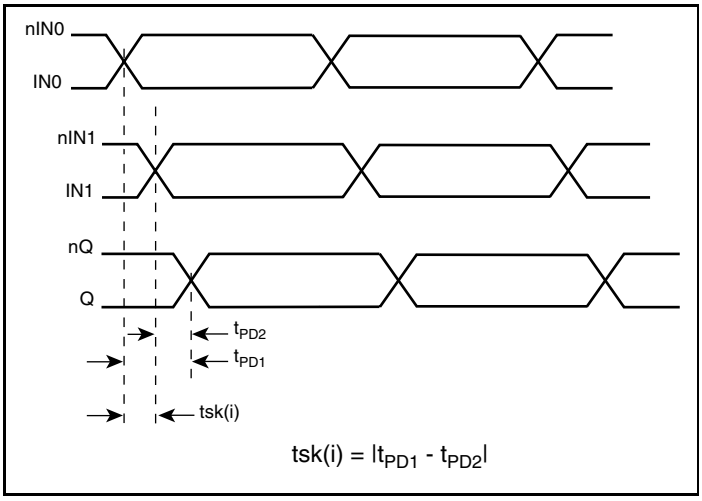


Single-ended & Differential Input Voltage Swing



Output Rise/Fall Time

Parameter Measurement Information, continued



Input Skew

Application Information

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

The control pin has an internal pullup; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

3.3V Differential Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 1A to 1D* show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most common driver types.

The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

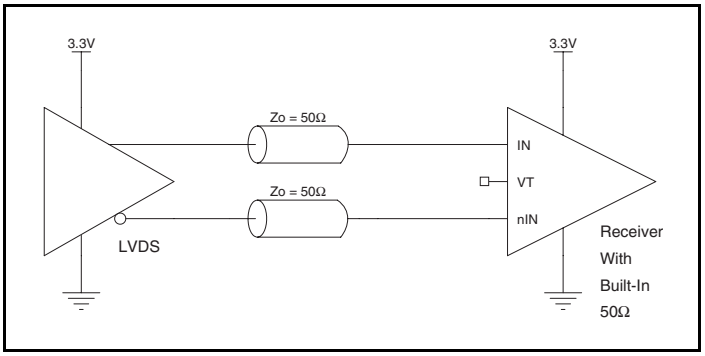


Figure 1A. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

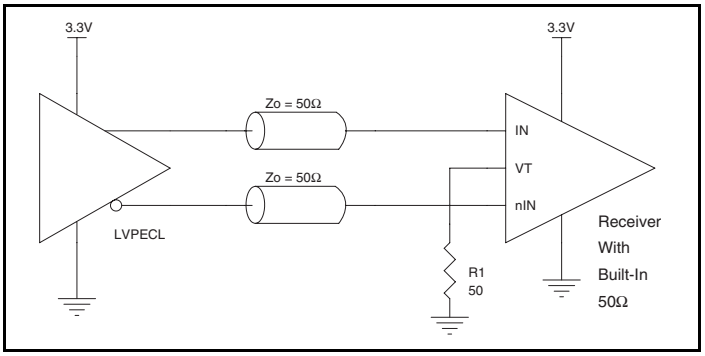


Figure 1B. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

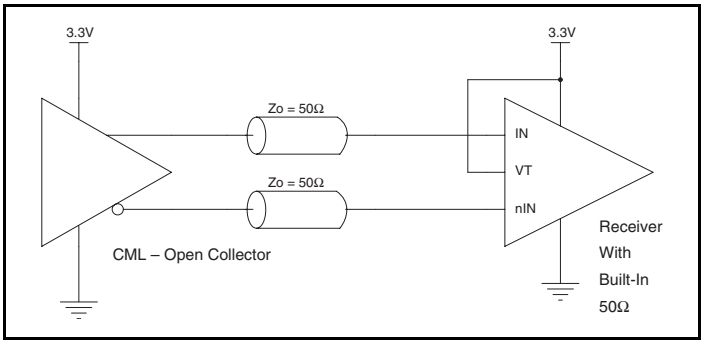


Figure 1C. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a CML Driver

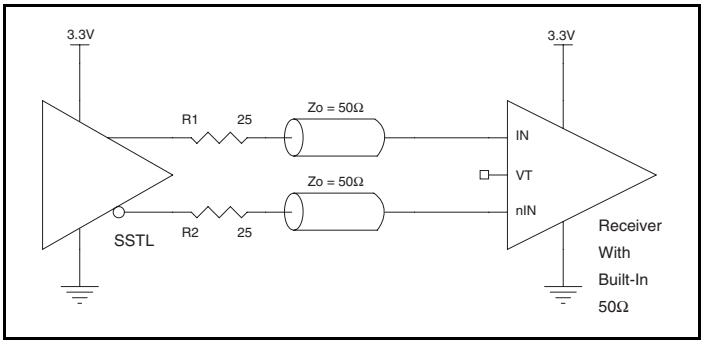


Figure 1D. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

2.5V LVPECL Input with Built-In 50Ω Termination Interface

The IN /nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML, SSTL and other differential signals. Both signals must meet the V_{IN} and V_{IH} input requirements. *Figures 2A to 2D* show interface examples for the HiPerClockS IN/nIN with built-in 50Ω termination input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

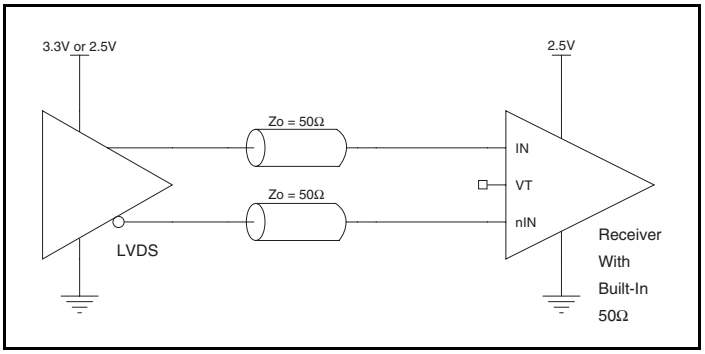


Figure 2A. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver

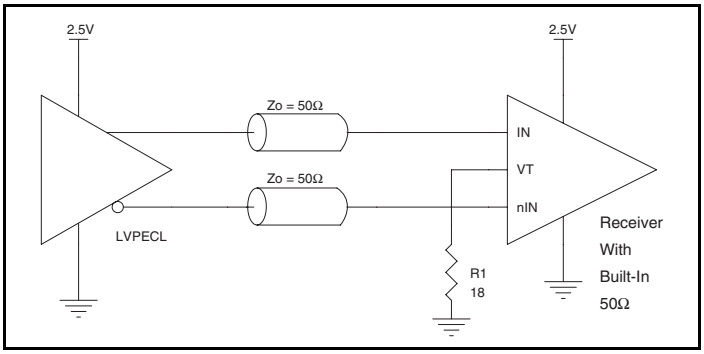


Figure 2B. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver

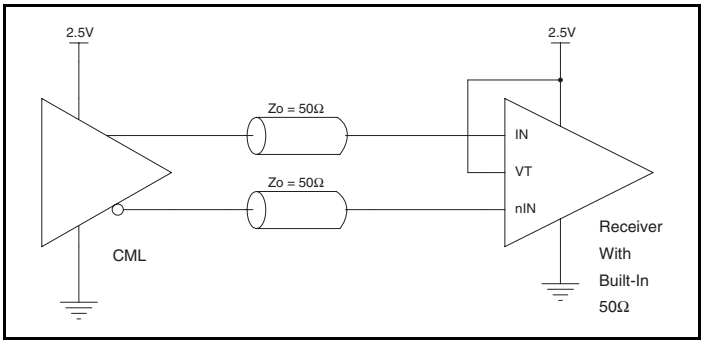


Figure 2C. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by a CML Driver

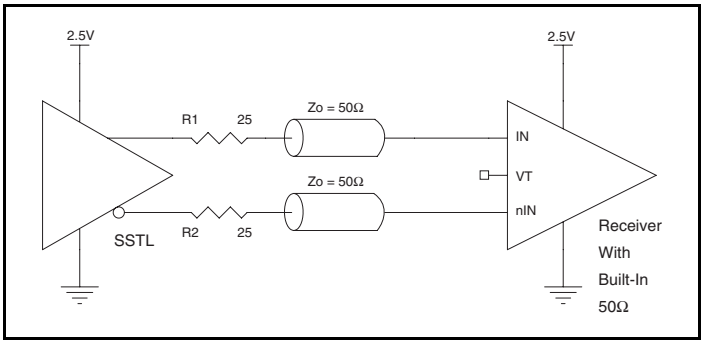


Figure 2D. HiPerClockS IN/nIN Input with Built-In 50Ω Driven by an SSTL Driver

2.5V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in Figure 3A.

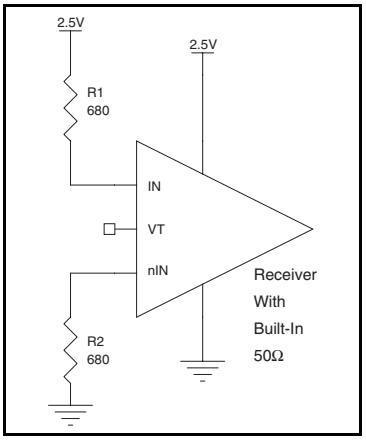


Figure 3A. Unused Input Handling

3.3V Differential Input with Built-In 50Ω Termination Unused Input Handling

To prevent oscillation and to reduce noise, it is recommended to have pullup and pulldown connect to true and compliment of the unused input as shown in Figure3B.

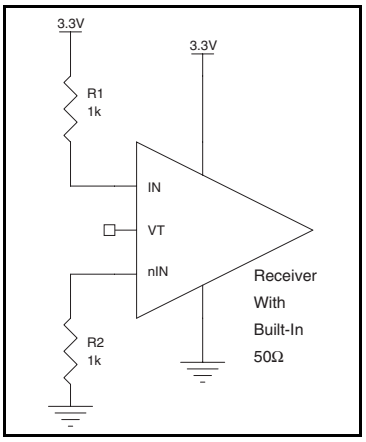


Figure 3B. Unused Input Handling

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

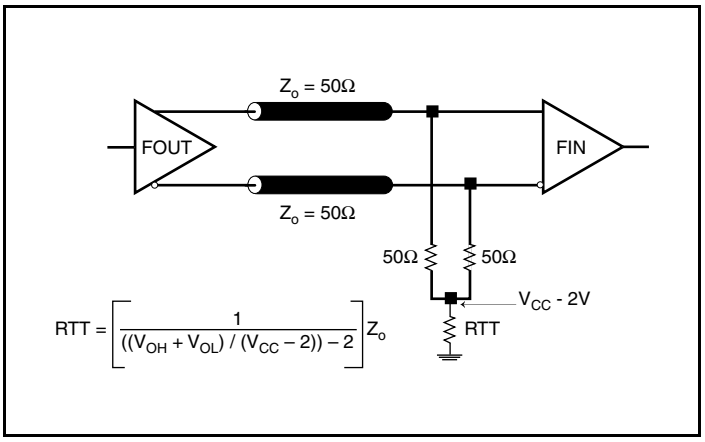


Figure 4A. 3.3V LVPECL Output Termination

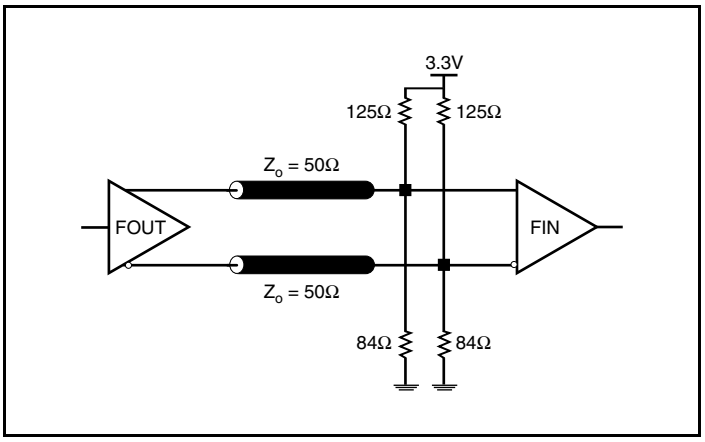


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and *Figure 5B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in *Figure 5C.*

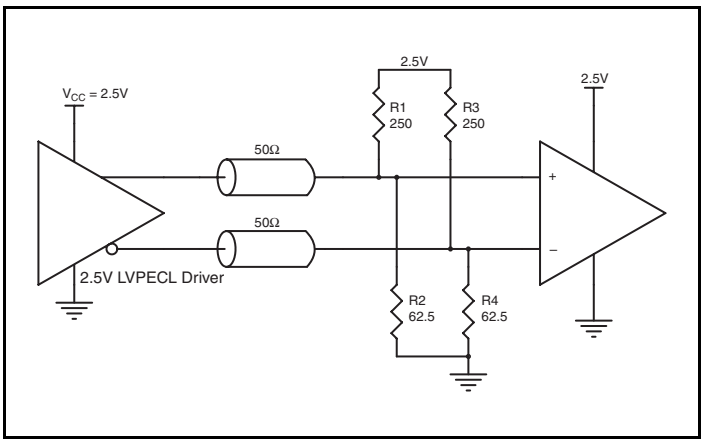


Figure 5A. 2.5V LVPECL Driver Termination Example

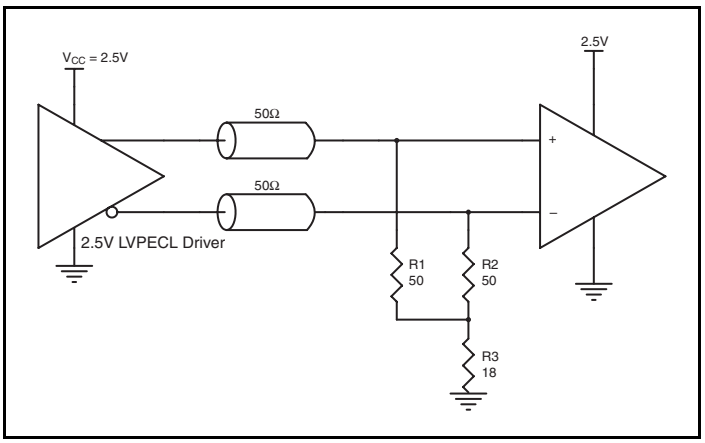


Figure 5B. 2.5V LVPECL Driver Termination Example

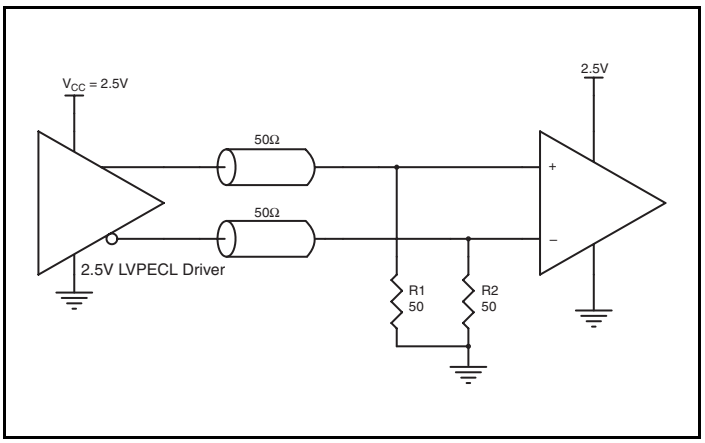


Figure 5C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

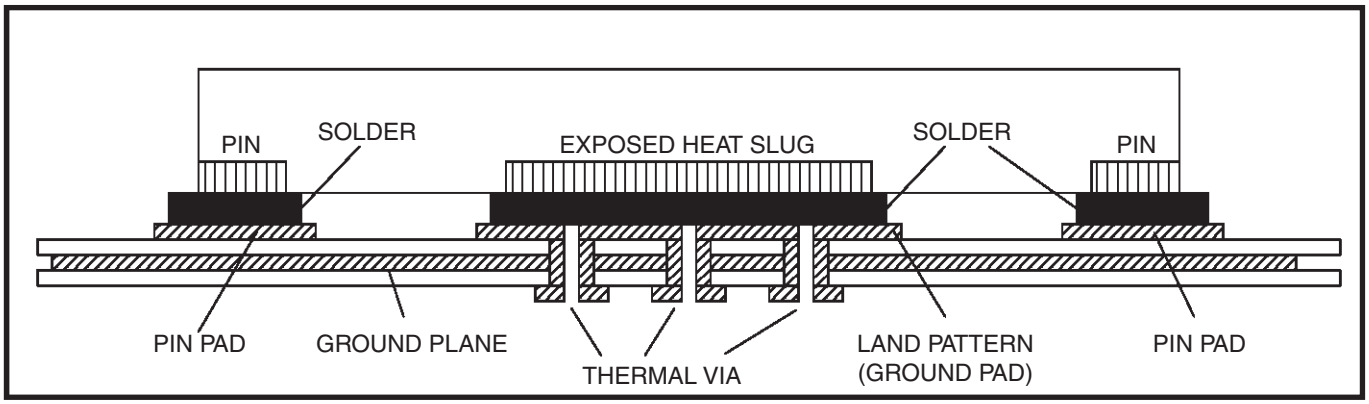


Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS858018.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS858018 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.63V * 21mA = **76.23mW**
- Power $(outputs)_{MAX}$ = **27.83mW w/Loaded Output pair**

Total Power$_{\_MAX}$ = 76.23mW + 27.83mW = **104.06mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 88.5°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.0104W * 88.5°C/W = 94.2°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead VFQFN, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	88.5°C/W	77.3°C/W	69.4°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7.*

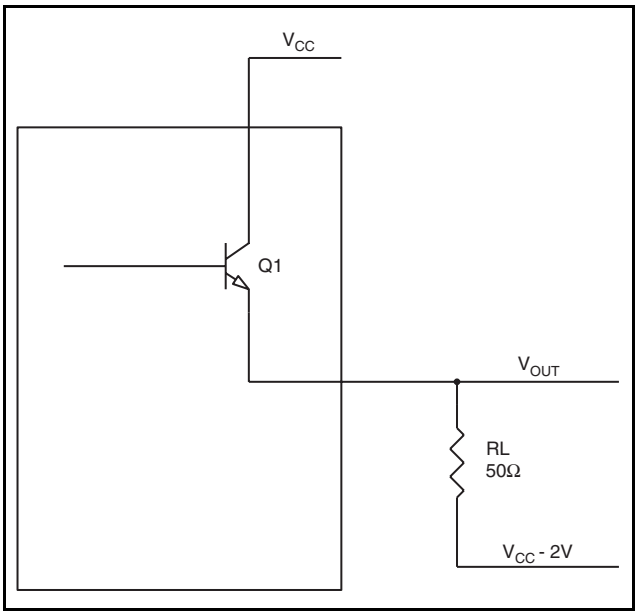


Figure 7. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX}} - \mathbf{1.005V}$
  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{1.005V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX}} - \mathbf{1.78V}$
  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.78V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 1.005V)/50Ω] * 1.005V =$ **20mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.78V)/50Ω] * 1.78V =$ **7.83mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **27.83mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	88.5°C/W	77.3°C/W	69.4°C/W

Transistor Count

The transistor count for ICS858018 is: 109

Pin Compatible with SY58011U

Package Outline and Package Dimensions

Package Outline - K Suffix for 16 Lead VFQFN

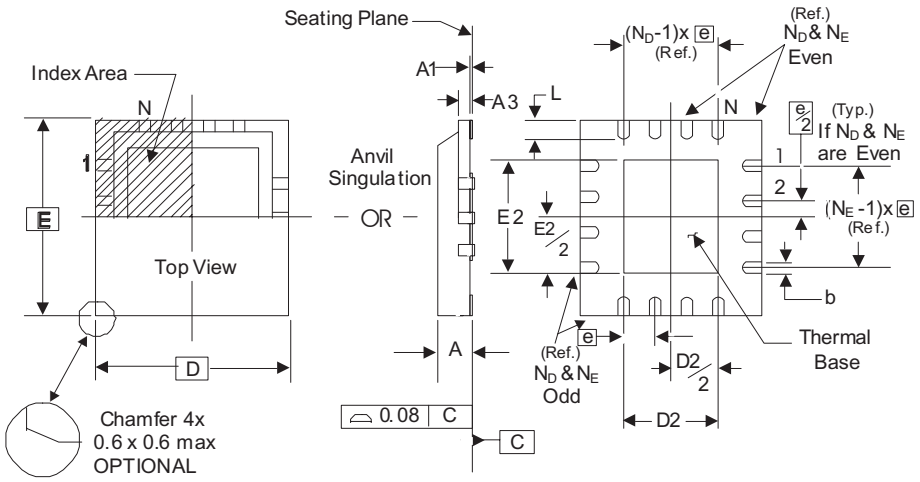


Table 8. K Package Dimensions for 16 Lead VFQFN

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 Basic	
D, E	3.0	
D2, E2	1.00	1.80
L	0.30	0.50
N_D N_E	4.0	

Reference Document: JEDEC Publication 95, MO-220

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
858018AK	018A	16 Lead VFQFN	Tube	-40°C to 85°C
858018AKT	018A	16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C
858018AKLF	18AL	“Lead-Free” 16 Lead VFQFN	Tube	-40°C to 85°C
858018AKLFT	18AL	“Lead-Free” 16 Lead VFQFN	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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