

**FEATURES**

- Input frequencies up to 80MHz
- PECL-to-TTL version of popular ECLinPS E111
- Guaranteed low skew specification
- Latched input
- Differential ECL internal design
- VBB output for single-ended operation
- Single +5V supply
- Reset/enable
- Extra TTL and ECL power/ground pins
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- ESD protection of 2000V
- Fully compatible with Motorola MC10H641/100H641
- Available in 28-pin PLCC package

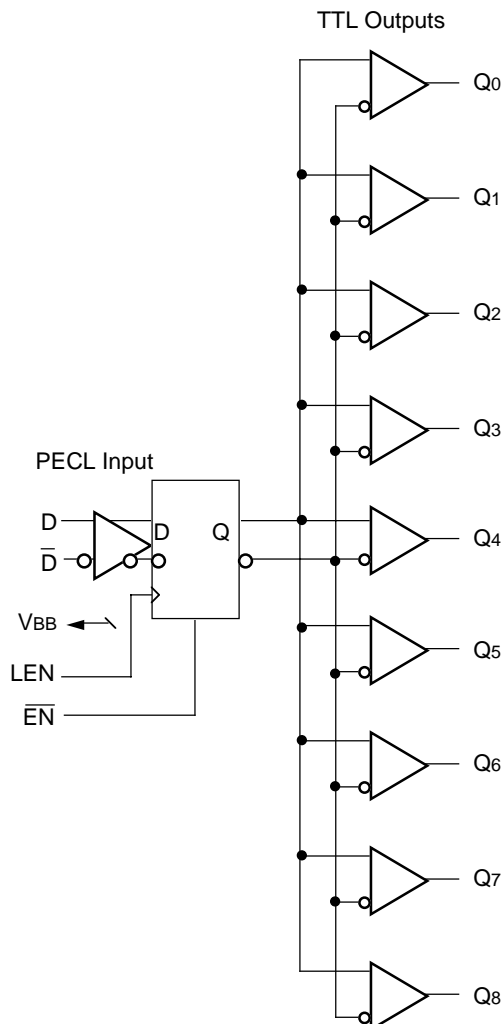
**DESCRIPTION**

The SY10/100H641A are single supply, low skew translating 1:9 clock drivers. Devices in the Synergy H600 translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

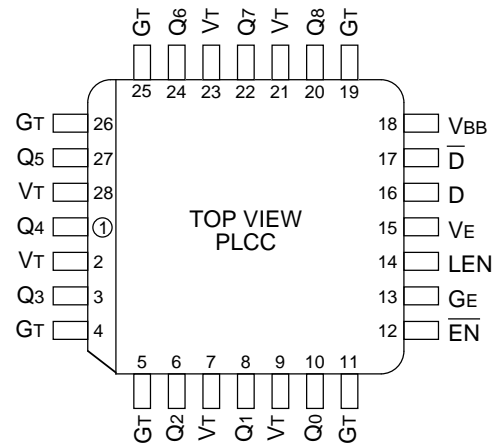
The devices feature a 24mA TTL output stage with AC performance specified into a 50pF load capacitance. A latch is provided on-chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the latch is transparent. A HIGH on the enable pin (EN) forces all outputs LOW.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

**BLOCK DIAGRAM**



**PIN CONFIGURATION**



**PIN NAMES**

Pin	Function
GT	TTL Ground (0V)
VT	TTL Vcc (+5.0V)
VE	ECL Vcc (+5.0V)
GE	ECL Ground (0V)
D, D-bar	Signal Input (PECL)
VBB	VBB Reference Output (PECL)
Q0 - Q8	Signal Outputs (TTL)
EN	Enable Input (PECL)
LEN	Latch Enable Input (PECL)

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Value	Unit
VE (ECL) VT (TTL)	Power Supply Voltage	-0.5 to +7.0 -0.5 to +7.0	V
VI (ECL)	Input Voltage	0.0 to VE	V
VOUT (TTL)	Disabled 3-State Output	0.0 to VT	V
IOUT (ECL)	Output Current - Continuous - Surge	50 100	mA
Tstore	Storage Temperature	-65 to +150	°C
TA	Operating Temperature	0 to +85	°C

### TRUTH TABLE

D	LEN	EN	Q
L	L	L	L
H	L	L	H
X	H	L	Q0
X	X	H	L

**NOTE:**

- Do not exceed.

### VCC AND CLOAD

Ranges to meet duty cycle requirement: 0°C ≤ TA ≤ 85°C. Output duty cycle measured relative to 1.5V.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
PW1	Ranges of VCC and CL to meet min. pulse width (HIGH or LOW) at fOUT ≤ 40MHz	VCC	4.75	5.0	5.25	V	All Outputs
		CL	10	—	50	pF	
		Pw	11	—	—	ns	
PW2	Ranges of VCC and CL to meet min. pulse width (HIGH or LOW) at fOUT ≤ 50MHz	VCC	4.875	5.0	5.125	V	All Outputs
		CL	15	—	27	pF	
		Pw	9.0	—	—	ns	

### DC ELECTRICAL CHARACTERISTICS

VT = VE = 5.0V ± 5%

Symbol	Parameter		TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
IEE	Power Supply Current	ECL	—	30	—	30	—	30	mA	VE Pin
ICCH		TTL	—	30	—	30	—	30		Total all VT pins
ICCL			—	37	—	37	—	37		

### TTL DC ELECTRICAL CHARACTERISTICS

VT = VE = 5.0V ± 5%

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
VOH	Output HIGH Voltage	2.5	—	2.5	—	2.5	—	V	IOH = -15mA
VOL	Output LOW Voltage	—	0.5	—	0.5	—	0.5	V	IOL = 24mA
Ios	Output Short Circuit Current	-100	-225	-100	-225	-100	-225	mA	VOUT = 0V

## 10H ECL DC ELECTRICAL CHARACTERISTICS

 $V_T = V_E = 5.0V \pm 5\%$ 

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>IH</sub>	Input HIGH Current	—	225	—	175	—	175	μA	—
I <sub>IL</sub>	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V <sub>IH</sub>	Input HIGH Voltage <sup>(1)</sup>	3.830	4.160	3.870	4.190	3.940	4.280	V	V <sub>E</sub> = 5.0V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>	3.050	3.520	3.050	3.520	3.050	3.555	V	V <sub>E</sub> = 5.0V
V <sub>BB</sub>	Output Reference Voltage <sup>(1)</sup>	3.620	3.730	3.650	3.750	3.690	3.810	V	V <sub>E</sub> = 5.0V

### NOTE:

1. V<sub>IH</sub>, V<sub>IL</sub> and V<sub>BB</sub> are referenced to V<sub>E</sub> and will vary 1:1 with the power supply. The levels shown are for V<sub>E</sub> = +5.0V.

## 100H ECL DC ELECTRICAL CHARACTERISTICS

 $V_T = V_E = 5.0V \pm 5\%$ 

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>IH</sub>	Input HIGH Current	—	225	—	175	—	175	μA	—
I <sub>IL</sub>	Input LOW Current	0.5	—	0.5	—	0.5	—	μA	—
V <sub>IH</sub>	Input HIGH Voltage <sup>(1)</sup>	3.835	4.120	3.835	4.120	3.835	4.120	V	V <sub>E</sub> = 5.0V
V <sub>IL</sub>	Input LOW Voltage <sup>(1)</sup>	3.190	3.525	3.190	3.525	3.190	3.525	V	V <sub>E</sub> = 5.0V
V <sub>BB</sub>	Output Reference Voltage <sup>(1)</sup>	3.620	3.740	3.620	3.740	3.620	3.740	V	V <sub>E</sub> = 5.0V

### NOTE:

1. V<sub>IH</sub>, V<sub>IL</sub> and V<sub>BB</sub> are referenced to V<sub>E</sub> and will vary 1:1 with the power supply. The levels shown are for V<sub>E</sub> = +5.0V.

## AC ELECTRICAL CHARACTERISTICS

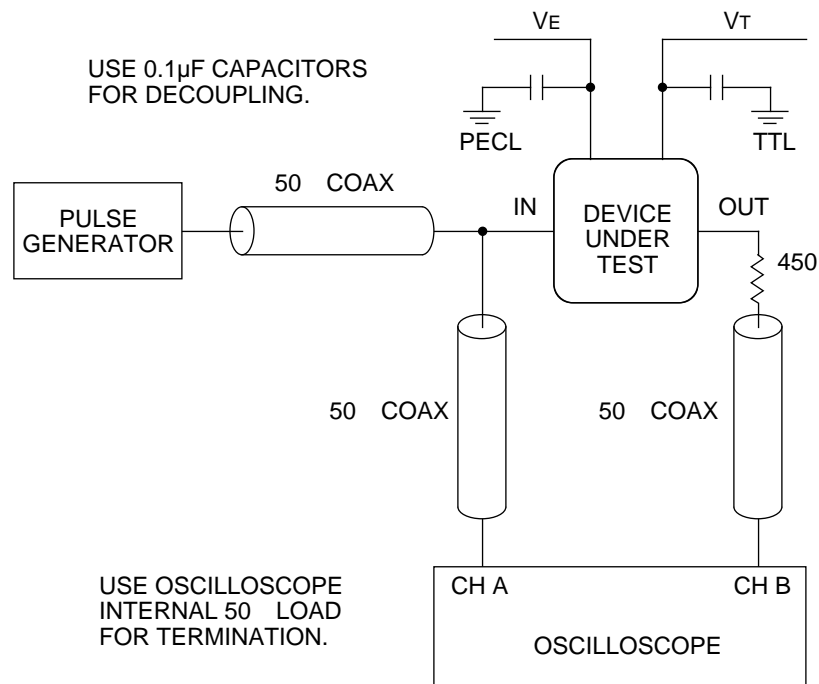
 $V_T = V_E = 5.0V \pm 5\%$ 

Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay D to Output	5.0	6.0	5.0	6.0	5.0	6.0	ns	CL = 50pF
t <sub>skpp</sub>	Part-to-Part Skew <sup>(1,4)</sup>	—	0.5	—	0.5	—	0.5	ns	CL = 50pF
t <sub>skew++</sub>	Within-Device Skew <sup>(2,4)</sup>	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
t <sub>skew--</sub>	Within-Device Skew <sup>(3,4)</sup>	—	0.3	—	0.3	—	0.3	ns	CL = 50pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay LEN to Output	4.9	6.9	4.9	6.9	5.0	7.0	ns	CL = 50pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay EN to Output	5.0	7.0	4.9	6.9	5.0	7.0	ns	CL = 50pF
t <sub>r</sub> t <sub>f</sub>	Output Rise/Fall Time 0.8V to 2.0V	—	1.7	—	1.7	—	1.7	ns	CL = 50pF
f <sub>MAX</sub>	Maximum Input Frequency <sup>(5,6)</sup>	80	—	80	—	80	—	MHz	CL = 50pF
—	Pulse Width	1.5	—	1.5	—	1.5	—	ns	—
—	Recovery Time	1.25	—	1.25	—	1.25	—	ns	—
t <sub>S</sub>	Set-up Time	0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—
t <sub>H</sub>	Hold Time	0.5 (typ.)		0.5 (typ.)		0.5 (typ.)		ns	—

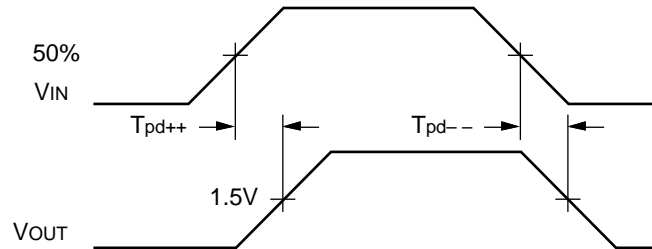
### NOTES:

- Device-to-Device Skew considering HIGH-to-HIGH transitions at common power supply voltage.
- Within-Device Skew considering HIGH-to-HIGH transitions at common power supply voltage.
- Within-Device Skew considering LOW-to-LOW transitions at common power supply voltage.
- All skew parameters are guaranteed but not tested.
- Frequency at which output levels will meet a 0.8V to 2.0V minimum swing.
- The f<sub>MAX</sub> value is specified as the minimum guaranteed maximum frequency. Actual operational maximum frequency may be greater.

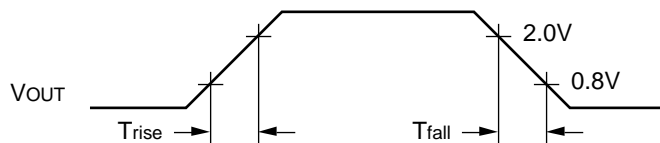
## TTL SWITCHING CIRCUIT



## ECL/TTL PROPAGATION DELAY — SINGLE ENDED



## ECL/TTL WAVEFORMS: RISE AND FALL TIMES



## PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H641AJC	J28-1	Commercial
SY10H641AJCTR	J28-1	Commercial
SY100H641AJC	J28-1	Commercial
SY100H641AJCTR	J28-1	Commercial

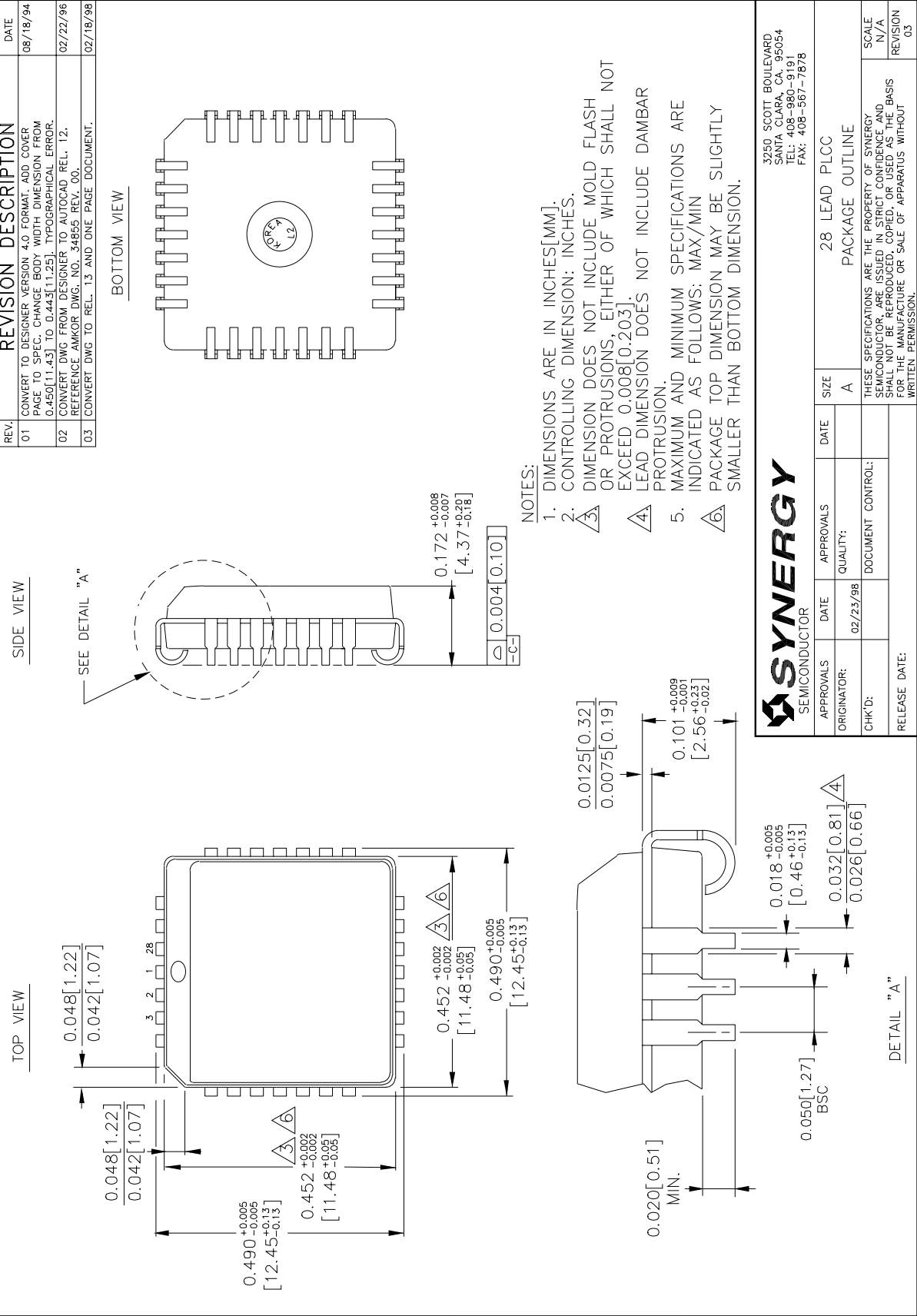
**28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)**

FILE/REV #: PD0008A03

PD/0008/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION 4.0 FORMAT. ADD COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[1.43] TO 0.443[11.25]. TYPOGRAPHICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD. REL. 12. REFERENCE AMKOR.DWG. NO. 34855. REV. 00.	02/22/96
03	CONVERT DWG TO REL. 13 AND ONE PAGE DOCUMENT.	02/18/98



**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

<b>SYNERGY</b> SEMICONDUCTOR		APPROVALS	DATE	SIZE	28 LEAD PLCC	SCALE
ORIGINATOR:	02/23/98	QUALITY:		A	PACKAGE OUTLINE	N/A
CHK'D:		DOCUMENT CONTROL:				REVISION
RELEASE DATE:						03

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