MC10H645

1:9 TTL Clock Driver

Description

The MC10H645 is a single supply, low skew, TTL I/O 1:9 Clock Driver. Devices in the H600 clock driver family utilizes the PLCC−28 for optimal power and signal pin placement.

The device features a 24 mA TTL output stage with AC performance specified into a 50 pF load capacitance. A 2:1 input Mux is provided on chip to allow for distributing both system and diagnostic clock signals or designing clock redundancy into a system. With the SEL input held LOW the DO input will be selected, while the D1 input is selected when the SEL input is forced HIGH.

Features

- Low Skew Typically 0.65 ns Within Device
- Guaranteed Skew Spec 1.25 ns Part−to−Part
- Input Clock Muxing
- Differential ECL Internal Design
- Single Supply
- Extra TTL and ECL Power/Ground Pins
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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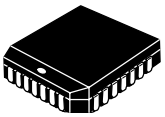
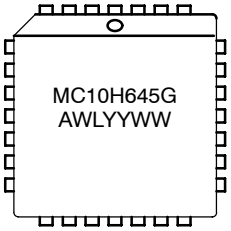


PLCC
FN SUFFIX
CASE 776

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

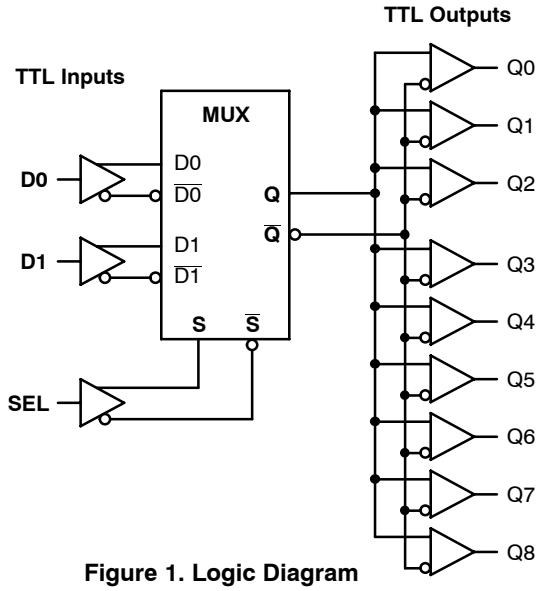


Figure 1. Logic Diagram

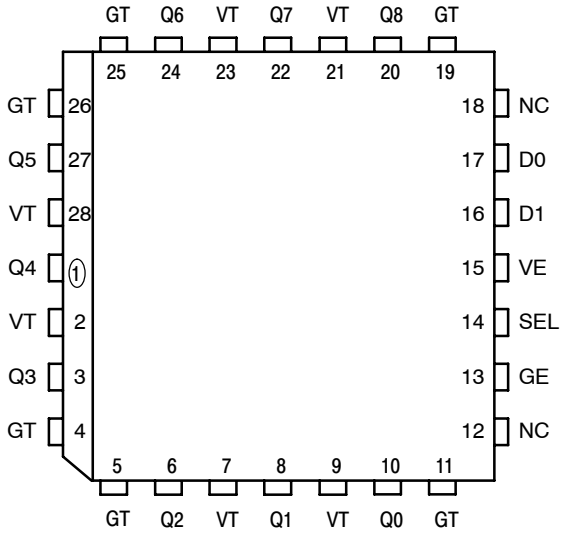


Figure 2. Pinout: 28−Lead PLCC
(Top View)

Table 1. PIN NAMES

PIN	FUNCTION
GT	TTL Ground (0 V)
VT	TTL V_{CC} (+5.0 V)
VE	ECL V_{CC} (+5.0 V)
GE	ECL Ground (0 V)
Dn	TTL Signal Input
Q0 − Q8	TTL Signal Outputs
SEL	TTL Mux Select

Table 2. PIN DESCRIPTIONS

Pin	Symbol	Description	Pin	Symbol	Description
1	Q4	Signal Output (TTL)	15	VE	ECL V_{CC} (+5.0 V)
2	VT	TTL V_{CC} (+5.0 V)	16	D1	Signal Input (TTL)
3	Q3	Signal Output (TTL)	17	D0	Signal Input (TTL)
4	GT	TTL Ground (0 V)	18	NC	No Connection
5	GT	TTL Ground (0 V)	19	GT	TTL Ground (0 V)
6	Q2	Signal Output (TTL)	20	Q8	Signal Output (TTL)
7	VT	TTL V_{CC} (+5.0 V)	21	VT	TTL V_{CC} (+5.0 V)
8	Q1	Signal Output (TTL)	22	Q7	Signal Output (TTL)
9	VT	TTL V_{CC} (+5.0 V)	23	VT	TTL V_{CC} (+5.0 V)
10	Q0	Signal Output (TTL)	24	Q6	Signal Output (TTL)
11	GT	TTL Ground (0 V)	25	GT	TTL Ground (0 V)
12	NC	No Connection	26	GT	TTL Ground (0 V)
13	GE	ECL Ground	27	Q5	Signal Output (TTL)
14	SEL	Select Input (TTL)	28	VT	TTL V_{CC} (+5.0 V)

Table 3. TRUTH TABLE

D0	D1	SEL	Q
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

Table 4. ABSOLUTE RATINGS (Do not exceed)

Symbol	Characteristic	Value	Unit
VE (ECL)	Power Supply Voltage	−0.5 to +7.0	V
VT (TTL)	Power Supply Voltage	−0.5 to +7.0	V
VI (TTL)	Input Voltage	−0.5 to +7.0	V
V_{out}	Disabled 3−State Output	0.0 to V_T	V
T_{stg}	Storage Temperature	−65 to 150	°C
T_{amb}	Operating Temperature	0.0 to +85	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

Table 5. DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C		25°C		85°C		Unit	Condition
			Min	Max	Min	Max	Min	Max		
I_{EE}	Power Supply Current	ECL		30		30		30	mA	VE Pin
I_{CCH}		TTL		30		30		30	mA	Total all VT pins
I_{CCL}				35		35		35	mA	
V_{OH}	Output HIGH Voltage		2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.5		0.5		0.5	V	I_{OL} = 24 mA
I_{OS}	Output Short Circuit Current		−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. TTL DC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic	0°C		25°C		85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	2.0	 0.8	2.0	 0.8	2.0	 0.8	V	
I_{IH}	Input HIGH Current		20 100		20 100		20 100	μA	V_{IN} = 2.7 V V_{IN} = 7.0 V
I_{IL}	Input LOW Current		−0.6		−0.6		−0.6	mA	V_{IN} = 0.5 V
V_{OH}	Output HIGH Voltage	2.5 2.0		2.5 2.0		2.5 2.0		V	I_{OH} = −3.0 mA I_{OH} = −24 mA
V_{OL}	Output LOW Voltage		0.5		0.5		0.5	V	I_{OL} = 24 mA
V_{IK}	Input Clamp Voltage		−1.2		−1.2		−1.2	V	I_{IN} = −18 mA
I_{OS}	Output Short Circuit Current	−100	−225	−100	−225	−100	−225	mA	V_{OUT} = 0 V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. AC CHARACTERISTICS (VT = VE = 5.0 V ±5%)

Symbol	Characteristic		0°C Min	0°C Max	25°C Min	25°C Max	85°C Min	85°C Max	Unit	Condition
t_{PLH}	Propagation Delay D_0 to Output Only	Q0−Q8	4.8	5.8	4.8	5.8	5.2	6.2	ns	CL = 50 pF
t_{PLH}	Propagation Delay D_1 to Output		4.8	5.8	4.8	5.8	5.2	6.2	ns	
t_{PHL}	Propagation Delay D_0 to Output D_1 to Output		 4.8 4.8	 5.8 5.8	 4.8 4.8	 5.8 5.8	 5.2 5.2	 6.2 6.2	ns	
t_{skpp}	Part−to−Part Skew D_0 to Output Only			1.0		1.0		1.0	ns	
t_{skwd}*	Within−Device Skew D_0 to Output Only			0.65		0.65		0.65	ns	
t_{PLH}	Propagation Delay SEL to Q	Q0−Q8	4.5	6.5	5.0	7.0	5.2	7.2	ns	CL = 50 pF
t_r t_f	Output Rise/Fall Time 0.8V to 2.0V	Q0−Q8	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	0.5 0.5	2.5 2.5	ns	CL = 50 pF
t_S	Setup Time SEL to D		 1.0		 1.0		 1.0		ns	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

*Within−Device Skew defined as identical transitions on similar paths through a device.

Table 8. DUTY CYCLE SPECIFICATIONS (0°C ≤ T_A ≤ 85°C; Duty Cycle Measured Relative to 1.5 V)

Symbol	Characteristic		Min	Nom	Max	Unit	Condition
PW	Range of V_{CC} and CL to Meet Min Pulse Width (HIGH or LOW) at f_{out} ≤50MHz	V_{CC} CL PW	4.875 10.0 9.0	5.0	5.125 50.0 11.0	V pF ns	All Outputs

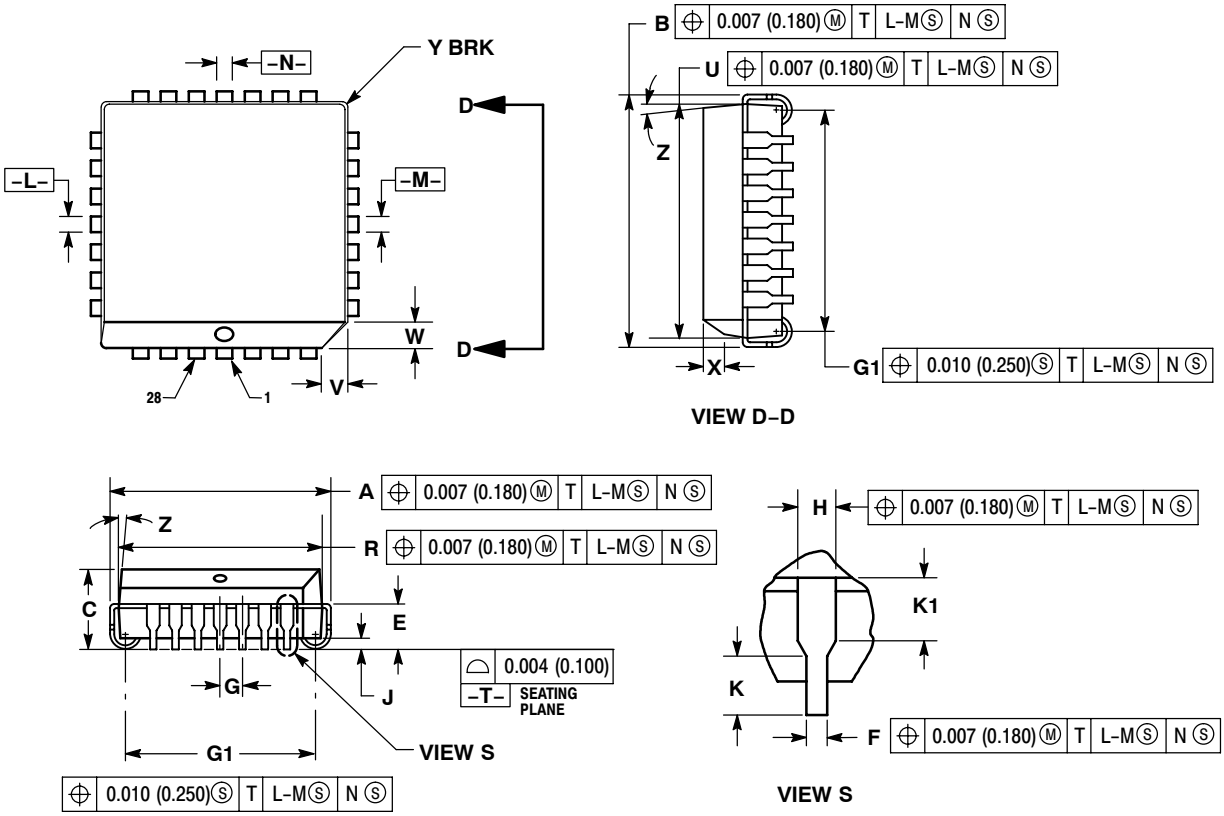
ORDERING INFORMATION

Device	Package	Shipping†
MC10H645FN	PLCC−28	37 Units / Rail
MC10H645FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H645FNR2	PLCC−28	500 / Tape & Reel
MC10H645FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

PLCC–28
FN SUFFIX
CASE 776–02
ISSUE E



NOTES:
1. DATUMS –L–, –M–, AND –N– DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM –T–, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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