

MC100E210

5V ECL Dual 1:4, 1:5 Differential Fanout Buffer

The MC100E210 is a low voltage, low skew dual differential ECL fanout buffer designed with clock distribution in mind. The device features two fanout buffers, a 1:4 and a 1:5 buffer, on a single chip. The device features fully differential clock paths to minimize both device and system skew. The dual buffer allows for the fanout of two signals through a single chip, thus reducing the skew between the two fundamental signals from a part-to-part skew down to an output-to-output skew. This capability reduces the skew by a factor of 4 as compared to using two LVE111's to accomplish the same task.

The lowest TPD delay time results from terminating only one output pair, and the greatest TPD delay time results from terminating all the output pairs. This shift is about 10–20 pS in TPD. The skew between any two output pairs within a device is typically about 25 nS. If other output pairs are not terminated, the lowest TPD delay time results from both output pairs and the skew is typically 25 nS. When all outputs are terminated, the greatest TPD (delay time) occurs and all outputs display about the same 10–20 pS increase in TPD, so the relative skew between any two output pairs remains about 25 nS.

For more information on using PECL, designers should refer to Application Note AN1406/D.

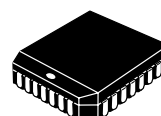
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

- Dual Differential Fanout Buffers
- 200 ps Part-to-Part Skew
- 50 ps Typical Output-to-Output Skew
- Low Voltage ECL/PECL Compatible
- The 100 Series Contains Temperature Compensation
- 28-lead PLCC Packaging
- PECL Mode Operating Range: $V_{CC} = 4.2$ V to 5.7 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC} = 0$ V with $V_{EE} = -4.2$ V to -5.7 V
- Internal Input 75 K Ω Pulldown Resistors
- Q Output will Default LOW with Inputs Open or at V_{EE}
- ESD Protection: Human Body Model; >2 KV, Machine Model; >200 V
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 179 devices

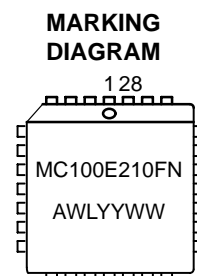


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PLCC-28
FN SUFFIX
CASE 776



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

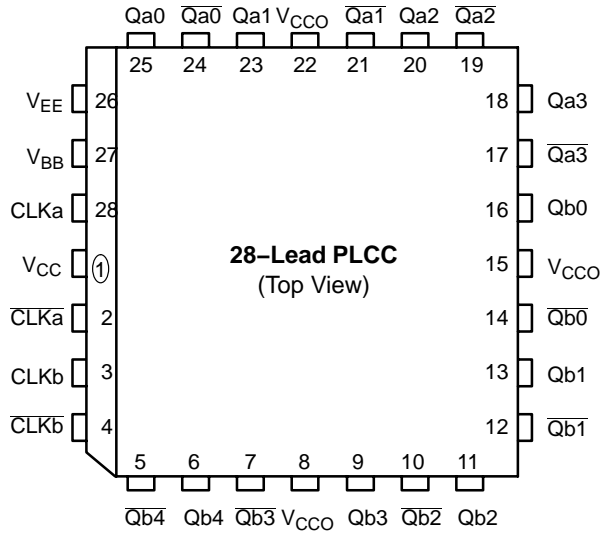
ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|---------|-----------------|
| MC100E210FN | PLCC-28 | 37 Units / Rail |
| MC100E210FNR2 | PLCC-28 | 500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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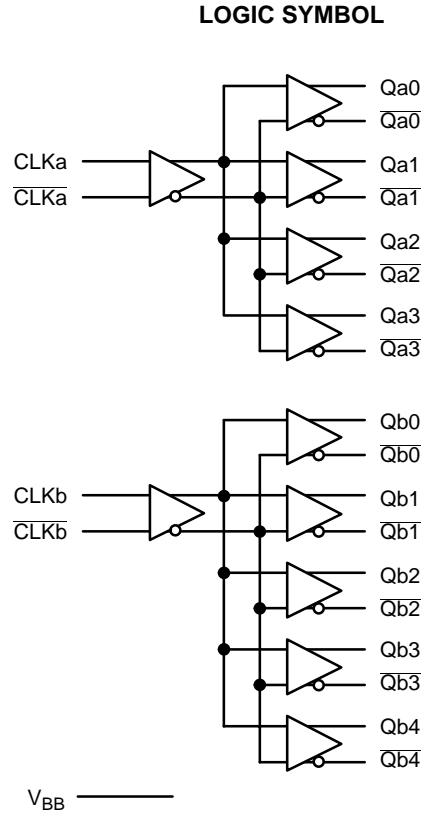
LOGIC DIAGRAM AND PINOUT ASSIGNMENT



Warning: All V_{CC} , V_{CCO} , and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

| PIN | FUNCTION |
|---|------------------------------|
| CLKa, CLKb | ECL Differential Input Pairs |
| \overline{CLKa} , \overline{CLKb} | ECL Differential Input Pairs |
| Qa0:3, Qb0:4 | ECL Differential Outputs |
| $\overline{Qa0:3}$, $\overline{Qb0:4}$ | ECL Differential Outputs |
| V_{BB} | Reference Output Voltage |
| V_{CC} , V_{CCO} | Positive Supply |
| V_{EE} | Negative Supply |



MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------|--|--|--|----------------------------|--|
| V_{CC} | PECL Mode Power Supply | $V_{EE} = 0\text{ V}$ | | 8 | V |
| V_{EE} | NECL Mode Power Supply | $V_{CC} = 0\text{ V}$ | | -8 | V |
| V_I | PECL Mode Input Voltage NECL Mode Input Voltage | $V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$ | $V_I \leq V_{CC}$ $V_I \geq V_{EE}$ | 6 -6 | V V |
| I_{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | 0 to +85 | $^{\circ}\text{C}$ |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | $^{\circ}\text{C}$ |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 LFPM 500 LFPM | 28 PLCC 28 PLCC | 63.5 43.5 | $^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$ |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | 28 PLCC | 22 to 26 | $^{\circ}\text{C}/\text{W}$ |
| V_{EE} | PECL Operating Range NECL Operating Range | | | 4.2 to 5.7 -5.7 to -4.2 | V V |
| T_{sol} | Wave Solder | <2 to 3 sec @ 248 $^{\circ}\text{C}$ | | 265 | $^{\circ}\text{C}$ |

1. Maximum Ratings are those values beyond which device damage may occur.

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PECL DC CHARACTERISTICS $V_{CCx}= 5.0\text{ V}$; $V_{EE}= 0.0\text{ V}$ (Note 2)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | | 55 | | | 55 | | | 65 | mA |
| V_{OH} | Output HIGH Voltage (Note 3) | 3915 | 3995 | 4120 | 3975 | 4050 | 4120 | 3975 | 4050 | 4120 | mV |
| V_{OL} | Output LOW Voltage (Note 3) | 3170 | 3305 | 3445 | 3190 | 3255 | 3380 | 3190 | 3260 | 3380 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | 3835 | 3975 | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | 3190 | 3355 | 3525 | mV |
| V_{BB} | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential) (Note 4) | 2.7 | | 4.6 | 2.7 | | 4.6 | 2.7 | | 4.6 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2$ volts.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

NECL DC CHARACTERISTICS $V_{CCx}= 0.0\text{ V}$; $V_{EE}= -5.0\text{ V}$ (Note 5)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | | 55 | | | 55 | | | 65 | mA |
| V_{OH} | Output HIGH Voltage (Note 6) | -1085 | -1005 | -880 | -1025 | -950 | -880 | -1025 | -950 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 6) | -1830 | -1695 | -1555 | -1810 | -1745 | -1620 | -1810 | -1740 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | -1025 | -880 | -1165 | -1025 | -880 | -1165 | -1025 | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | -1810 | -1645 | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7) | -2.3 | | -0.4 | -2.3 | | -0.4 | -2.3 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| I_{IL} | Input LOW Current | 0.5 | 0.3 | | 0.5 | 0.25 | | 0.5 | 0.2 | | μA |

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with V_{CC} . V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.
- Outputs are terminated through a $50\ \Omega$ resistor to $V_{CC} - 2$ volts.
- V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .

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AC CHARACTERISTICS $V_{CCx}= 5.0\text{ V}; V_{EE}= 0.0\text{ V}$ or $V_{CCx}= 0.0\text{ V}; V_{EE}= -5.0\text{ V}$ (Note 8)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|------------------------|--|------------|----------|-----------------|------------|----------|-----------------|------------|----------|-----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{MAX} | Maximum Toggle Frequency | | 700 | | | 700 | | | 700 | | MHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output IN (differential) (Note 9) IN (single-ended) (Note 10) | 475 400 | | 675 700 | 500 450 | | 700 750 | 500 450 | | 700 750 | ps |
| t_{skew} | Within-Device Skew Qa to Qb Qa to Qa, Qb to Qb Part-to-Part Skew (Differential) (Note 11) | | 50 50 | 75 75 200 | | 50 30 | 75 50 200 | | 50 30 | 75 50 200 | ps |
| t_{JITTER} | Random Clock Jitter (RMS) | | < 1 | | | < 1 | | | < 1 | | ps |
| V_{PP} | Input Voltage Swing (Differential Configuration) (Note 12) | 500 | | | 500 | | | 500 | | | mV |
| t_r / t_f | Output Rise/Fall Time (20%–80%) | 200 | | 600 | 200 | | 600 | 200 | | 600 | ps |

8. V_{EE} can vary $-0.46\text{ V} / +0.8\text{ V}$.

9. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.

10. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.

11. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.

12. $V_{PP}(\text{min})$ is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{PP}(\text{min})$ is AC limited for the E210 as a differential input as low as 50 mV will still produce full ECL levels at the output.

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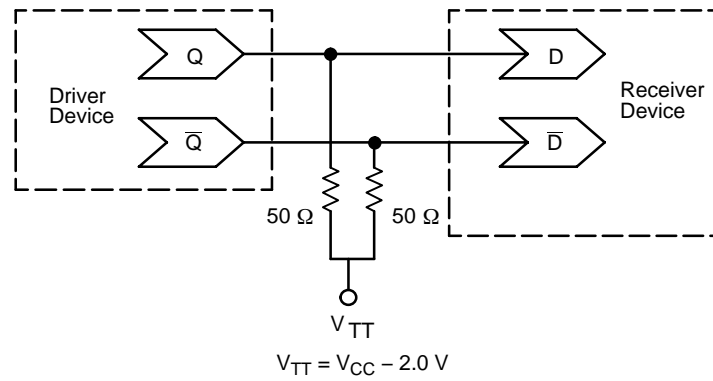


Figure 1. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020 – Termination of ECL Logic Devices.)

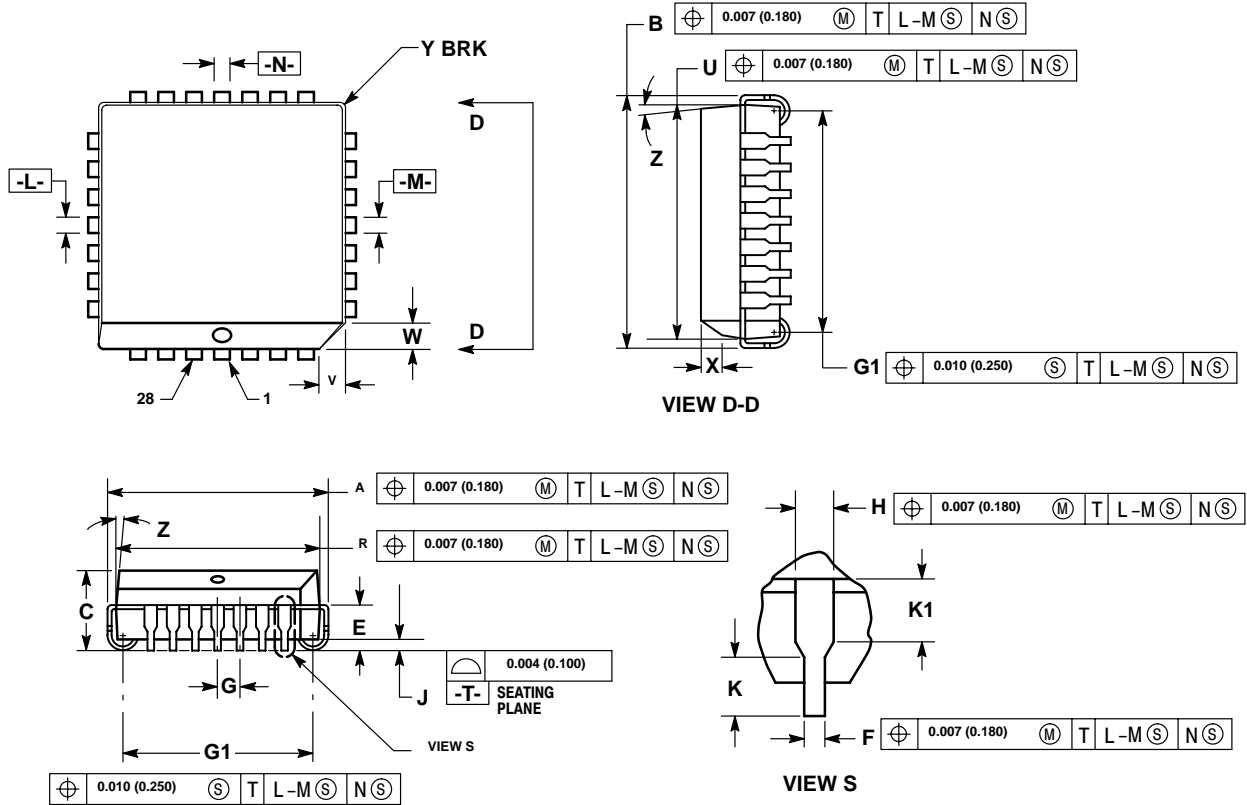
Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

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PACKAGE DIMENSIONS

PLCC-28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776-02
ISSUE E



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.485 | 0.495 | 12.32 | 12.57 |
| B | 0.485 | 0.495 | 12.32 | 12.57 |
| C | 0.165 | 0.180 | 4.20 | 4.57 |
| E | 0.090 | 0.110 | 2.29 | 2.79 |
| F | 0.013 | 0.019 | 0.33 | 0.48 |
| G | 0.050 BSC | | 1.27 BSC | |
| H | 0.026 | 0.032 | 0.66 | 0.81 |
| J | 0.020 | — | 0.51 | — |
| K | 0.025 | — | 0.64 | — |
| R | 0.450 | 0.456 | 11.43 | 11.58 |
| U | 0.450 | 0.456 | 11.43 | 11.58 |
| V | 0.042 | 0.048 | 1.07 | 1.21 |
| W | 0.042 | 0.048 | 1.07 | 1.21 |
| X | 0.042 | 0.056 | 1.07 | 1.42 |
| Y | — | 0.020 | — | 0.50 |
| Z | 2° | 10° | 2° | 10° |
| G1 | 0.410 | 0.430 | 10.42 | 10.92 |
| K1 | 0.040 | — | 1.02 | — |

Notes

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