

# MC100LVEL14

## 3.3V ECL 1:5 Clock Distribution Chip

### Description

The MC100LVEL14 is a low skew 1:5 clock distribution chip designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. The LVEL14 is functionally and pin compatible with the EL14 but is designed to operate in ECL or PECL mode for a voltage supply range of  $-3.0\text{ V}$  to  $-3.8\text{ V}$  ( or  $3.0\text{ V}$  to  $3.8\text{ V}$ ).

The LVEL14 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ( $\overline{\text{EN}}$ ) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The  $V_{\text{BB}}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{\text{BB}}$  as a switching reference voltage.  $V_{\text{BB}}$  may also rebias AC coupled inputs. When used, decouple  $V_{\text{BB}}$  and  $V_{\text{CC}}$  via a  $0.01\text{ }\mu\text{F}$  capacitor and limit current sourcing or sinking to  $0.5\text{ mA}$ . When not used,  $V_{\text{BB}}$  should be left open.

### Features

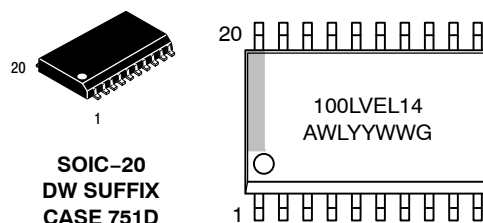
- 50 ps Output-to-Output Skew
  - Synchronous Enable/Disable
  - Multiplexed Clock Input
  - ESD Protection: Human Body Model  $>2\text{ kV}$
  - The 100 Series Contains Temperature Compensation
  - PECL Mode Operating Range:  
 $V_{\text{CC}} = 3.0\text{ V}$  to  $3.8\text{ V}$  with  $V_{\text{EE}} = 0\text{ V}$
  - NECL Mode Operating Range:  
 $V_{\text{CC}} = 0\text{ V}$  with  $V_{\text{EE}} = -3.0\text{ V}$  to  $-3.8\text{ V}$
  - Internal Input Pulldown Resistors on CLK
  - Q Output will Default LOW with Inputs Open or at  $V_{\text{EE}}$
  - Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
  - Moisture Sensitivity Pb = Level 1  
Pb-Free = Level 3
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @  $0.125\text{ in}$ ,  
Oxygen Index: 28 to 34
  - Transistor Count = 303 devices



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### MARKING DIAGRAM



SOIC-20  
DW SUFFIX  
CASE 751D

A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

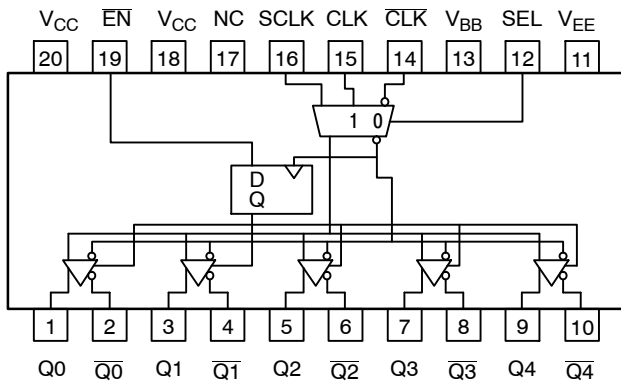
See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

## MC100LVEL14

- Pb-Free Packages are Available\*

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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Warning: All  $V_{CC}$  and  $V_{EE}$  pins must be externally connected to Power Supply to guarantee proper operation.

**Figure 1. Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

PIN	FUNCTION
CLK, $\overline{\text{CLK}}$	ECL Diff Clock Inputs
SCLK	ECL Scan Clock Input
$\overline{\text{EN}}$	ECL Sync Enable
SEL	ECL Clock Select Input
$Q_{0-4}, \overline{Q_{0-4}}$	ECL Diff Clock Outputs
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply
NC	No Connect

**Table 2. FUNCTION TABLE**

CLK	SCLK	SEL	EN	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

\*On next negative transition of CLK or SCLK  
X = Don't Care

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0 \text{ V}$		8 to 0	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0 \text{ V}$		-8 to 0	V
$V_i$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0 \text{ V}$ $V_{CC} = 0 \text{ V}$	$V_i \leq V_{CC}$ $V_i \geq V_{EE}$	6 to 0 -6 to 0	V V
$I_{out}$	Output Current	Continuous Surge		50 100	mA mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
$T_A$	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-20 SOIC-20	90 60	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-20	30 to 35	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder	Pb Pb-Free	<2 to 3 sec @ 248 $^{\circ}\text{C}$ <2 to 3 sec @ 260 $^{\circ}\text{C}$	265 265	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# MC100LEVEL14

**Table 4. LVPECL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 1)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		32	40		32	40		34	42	mA
$V_{OH}$	Output HIGH Voltage (Note 2)	2215	2295	2420	2275	2345	2420	2275	2345	2420	mV
$V_{OL}$	Output LOW Voltage (Note 2)	1470	1605	1745	1490	1595	1680	1490	1595	1680	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2135		2420	2135		2420	2135		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1490		1825	1490		1825	1490		1825	mV
$V_{BB}$	Output Voltage Reference	1.92		2.04	1.92		2.04	1.92		2.04	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	1.3		2.9	1.2		2.9	1.2		2.9	V
		1.5		2.9	1.4		2.9	1.4		2.9	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current Others CLK	0.5			0.5			0.5			$\mu\text{A}$
		-300			-300			-300			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
2. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1.0\text{ V}$ .

**Table 5. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 4)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		32	40		32	40		34	42	mA
$V_{OH}$	Output HIGH Voltage (Note 5)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 5)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{BB}$	Output Voltage Reference	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) $V_{PP} < 500\text{ mV}$ $V_{PP} \geq 500\text{ mV}$	-2.0		-0.4	-2.1		-0.4	-2.1		-0.4	V
		-1.8		-0.4	-1.9		-0.4	-1.9		-0.4	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current Others CLK	0.5			0.5			0.5			$\mu\text{A}$
		-300			-300			-300			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
5. Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2.0\text{ V}$ .
6.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and  $1.0\text{ V}$ .

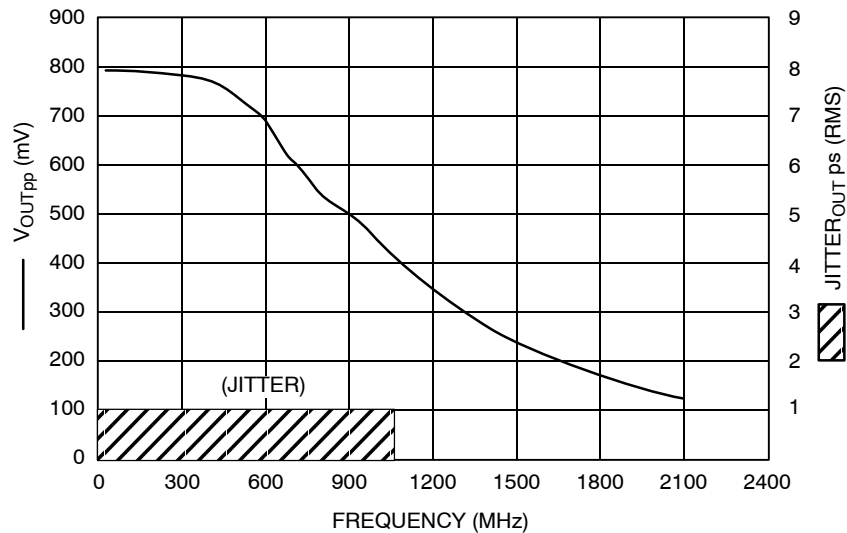
# MC100LVEL14

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  or  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 7)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency (Figure 2)		> 1			> 1			> 1		GHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Prop Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	520 470 470		720 770 770	580 530 530	680 680 680	780 830 830	630 580 580		830 880 880	ps
$t_{\text{SKEW}}$	Part-to-Part Skew Within-Device Skew (Note 8)			200 50			200 50			200 50	ps
$t_{\text{JITTER}}$	Random Clock Jitter (RMS) @ 1 GHz (Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
$t_{\text{S}}$	Setup Time $\overline{\text{EN}}$	0	-95		0	-110		0	-125		ps
$t_{\text{H}}$	Hold Time $\overline{\text{EN}}$	250	150		250	160		250	175		ps
$V_{\text{PP}}$	Input Swing CLK (Note 9)	150		1000	150		1000	150		1000	mV
$t_{\text{r}}$ $t_{\text{f}}$	Output Rise/Fall Times Q (20% - 80%)	230		500	230		500	230		500	ps

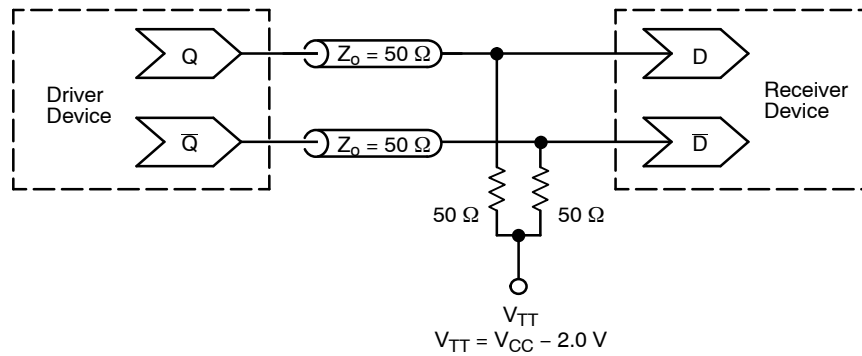
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
8. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
9.  $V_{\text{PP}}(\text{min})$  is minimum input swing for which AC parameters guaranteed.



**Figure 2.  $F_{\max}$ /Jitter**

## MC100LVEL14



**Figure 3. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC100LVEL14DW	SOIC-20	38 Units / Rail
MC100LVEL14DWG	SOIC-20 (Pb-Free)	38 Units / Rail
MC100LVEL14DWR2	SOIC-20	1000 Tape & Reel
MC100LVEL14DWR2G	SOIC-20 (Pb-Free)	1000 Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

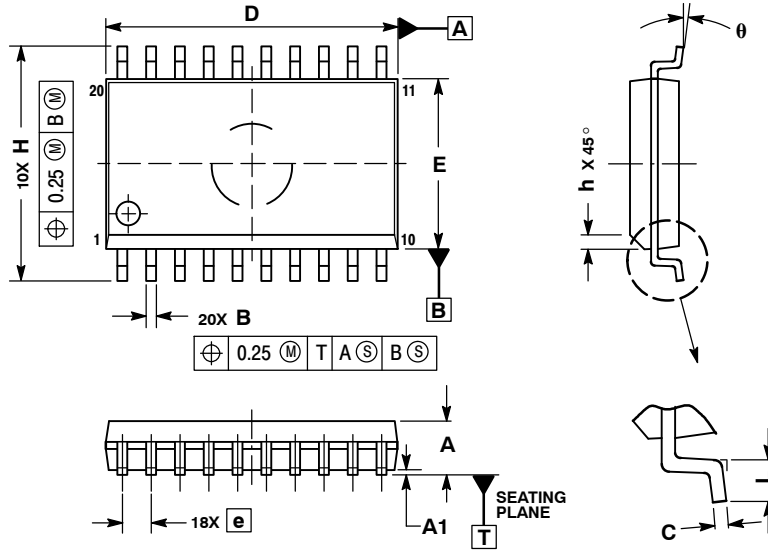
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC100LEVEL14

## PACKAGE DIMENSIONS

SOIC-20  
DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751D-05  
ISSUE G



**NOTES:**

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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