LOW SKEW, 1-TO-12 LVCMOS/LVTTL
FANOUT BUFFER

ICS8312I

General Description

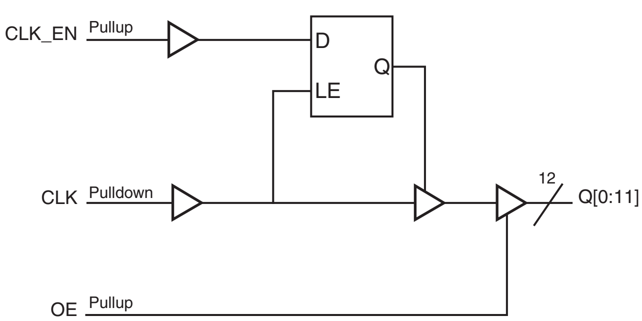
The ICS8312I is a low skew, 1-to-12 LVCMOS/ LVTTL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS8312I single-ended clock input accepts LVCMOS or LVTTL input levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 12 to 24 by utilizing the ability of the outputs to drive two series terminated lines.

The ICS8312I is characterized at full 3.3V, 2.5V, and 1.8V, mixed 3.3V/2.5V, 3.3V/1.8V and 2.5V/1.8V output operating supply modes. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the ICS8312I ideal for high performance, single ended applications that also require a limited output voltage.

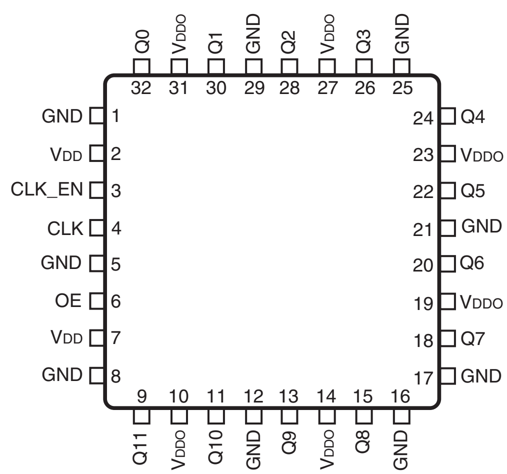
Features

- Twelve LVCMOS/LVTTL outputs
- CLK input supports the following input types: LVCMOS, LVTTL
- Maximum output frequency: 250MHz
- Output skew: 160ps (maximum)
- Supply modes:
  Core/Output
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
  1.8V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8312I

32-Lead LQFP
7mm x 7mm x 1.4mm package body
Y Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 5, 8, 12, 16, 17, 21, 25, 29	GND	Power		Power supply ground.
2, 7	V_{DD}	Power		Positive supply pins.
3	CLK_EN	Input	Pullup	Synchronous control for enabling and disabling clock outputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
6	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q[0:11]. LVCMOS / LVTTL interface levels.
9, 11, 13, 15, 18, 20, 22, 24, 26, 28, 30, 32	Q11, Q10, Q9, Q8, Q7, Q6, Q5, Q4, Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
10, 14, 19, 23, 27, 31	V_{DDO}	Power		Output supply pins.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DDO} = 3.465V			19	pF
		V_{DDO} = 2.625V			18	pF
		V_{DDO} = 2.V			16	pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V ± 5%		7		Ω
		V_{DDO} = 2.5V ± 5%		7		Ω
		V_{DDO} = 1.8V ± 0.2V		10		Ω

Function Tables

Table 3A. Output Enable and Clock Enable Function Table

Inputs		Outputs
OE	**CLK_EN**	**Q [0:11]**
0	X	Hi-Z
1	0	LOW
1	1	Follows CLK input

Table 3B. Output Enable and Clock Enable Function Table

Inputs			Outputs
OE	**CLK_EN**	**CLK**	**Q [0:11]**
1	1	0	LOW
1	1	1	HIGH

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	47.9°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4D. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4E. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4F. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				10	mA
I_{DDO}	Output Supply Current				10	mA

Table 4G. LVCMOS/LVTTL DC Characteristics, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.465V	2		V_{DD} + 0.3	V
			V_{DD} = 2.625V	1.7		V_{DD} + 0.3	V
			V_{DD} = 2.0V	0.65*V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.465V	-0.3		1.3	V
			V_{DD} = 2.625V	-0.3		0.7	V
			V_{DD} = 2.0V	-0.3		0.35*V_{DD}	V
I_{IH}	Input High Current	CLK	V_{DD} = V_{IN} = 3.465V or 2.625V or 2.0V			150	µA
		OE, CLK_EN	V_{DD} = V_{IN} = 3.465V or 2.625V or 2.0V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V or 2.625V or 2.0V, V_{IN} = 0V	-5			µA
		OE, CLK_EN	V_{DD} = 3.465V or 2.625V or 2.0V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%	2.6			V
			V_{DDO} = 2.5V ± 5%;	1.8			V
			V_{DDO} = 2.5V ± 5%; I_{OH} = -1mA	2			V
			V_{DDO} = 1.8V ± 0.2V	V_{DD} – 0.3			V
			V_{DDO} = 1.8V ± 0.2V; I_{OH} = -100µA	V_{DD} – 0.2			V
V_{OL}	Output Low Voltage; NOTE 1		V_{DDO} = 3.3V ± 5%			0.5	V
			V_{DDO} = 2.5V ± 5%;			0.45	V
			V_{DDO} = 2.5V ± 5%; I_{OL} = 1mA			0.4	V
			V_{DDO} = 1.8V ± 0.2V			0.35	V
			V_{DDO} = 1.8V ± 0.2V; I_{OL} = 100µA			0.2	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq 250MHz$	1.2	2.0	2.7	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.037		ps
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				850	ps
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	175		800	ps
odc	Output Duty Cycle	$f \leq 150MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \leq 250MHz$	1.25	2.4	3.5	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.022		ps
*t*sk(o)	Output Skew; NOTE 2, 5				155	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.1	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		800	ps
odc	Output Duty Cycle	$f \leq 150MHz$	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5C. AC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \le$ 200MHz	1.6	3.3	4.9	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.172		ps
*t*sk(o)	Output Skew; NOTE 2, 5				160	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				2.4	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	175		875	ps
odc	Output Duty Cycle	$f \le$ 100MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5D. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	$f \le$ 250MHz	1.5	2.1	2.8	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.045		ps
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		800	ps
odc	Output Duty Cycle	$f \le$ 150MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

Table 5E. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 200MHz	1.5	2.5	3.5	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.136		ps
*t*sk(o)	Output Skew; NOTE 2, 5				150	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.4	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		800	ps
odc	Output Duty Cycle	f ≤ 100MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

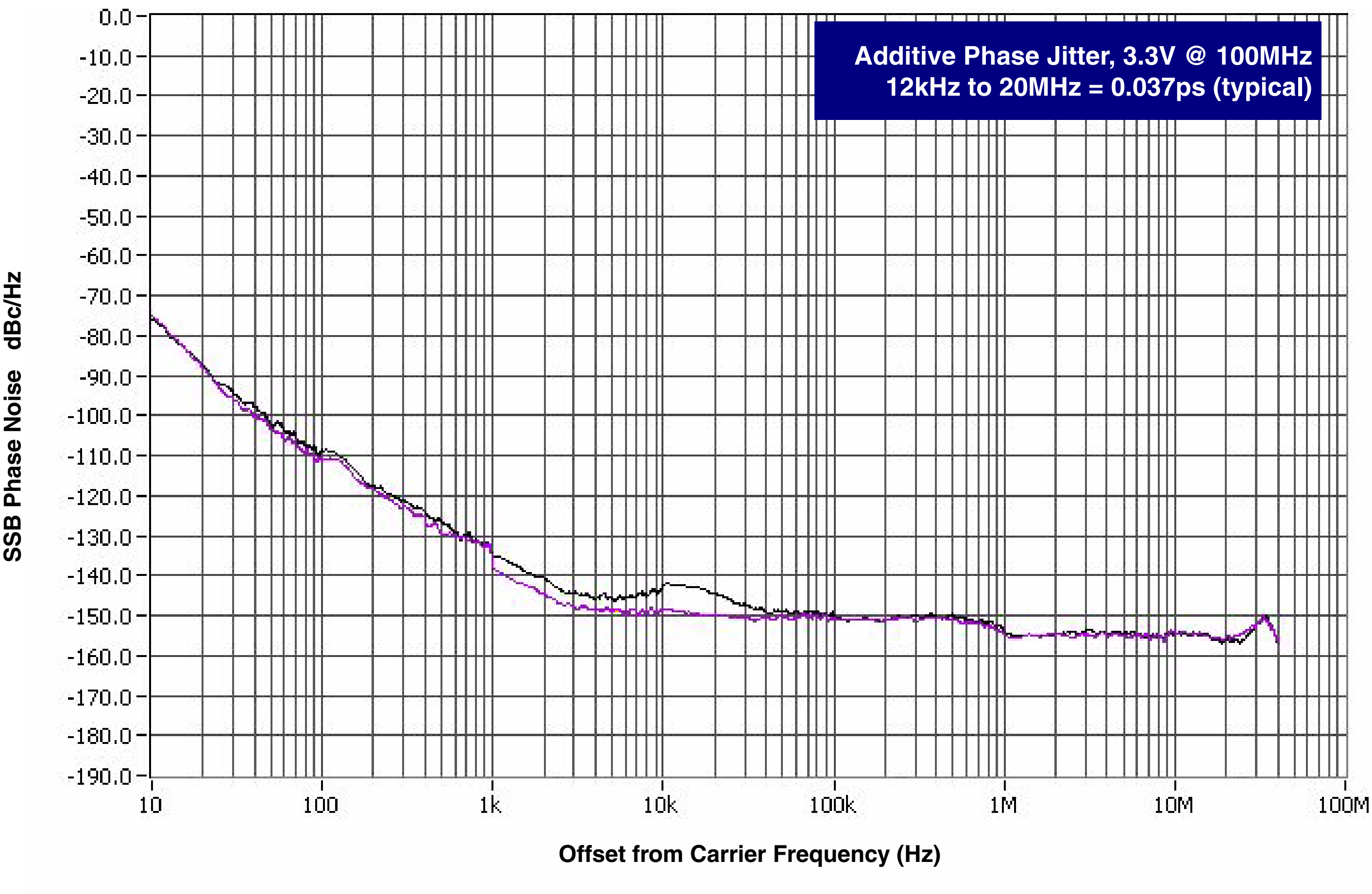
Table 5F. AC Characteristics, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 0.2V, T_A = -40°C to 85°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				200	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1	f ≤ 200MHz	1.4	2.7	3.9	ns
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	100MHz, Integration Range: 12kHz – 20MHz		0.114		ps
*t*sk(o)	Output Skew; NOTE 2, 5				160	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5				1.6	ns
t_R / t_F	Output Rise/Fall Time; NOTE 5	20% to 80%	200		800	ps
odc	Output Duty Cycle	f ≤ 100MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltage and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: These parameters are guaranteed by characterization. Not tested in production.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

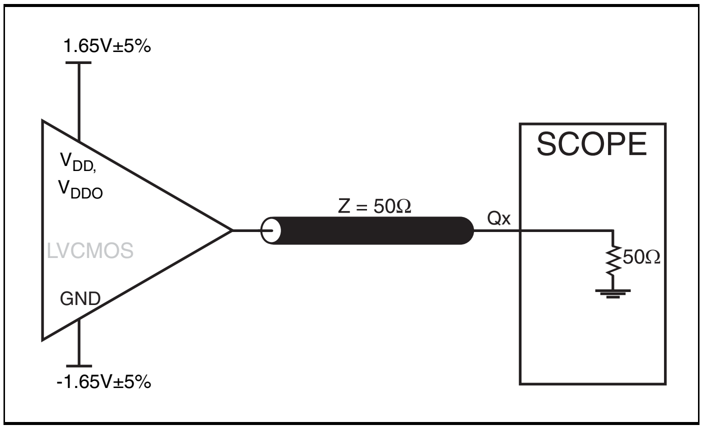
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

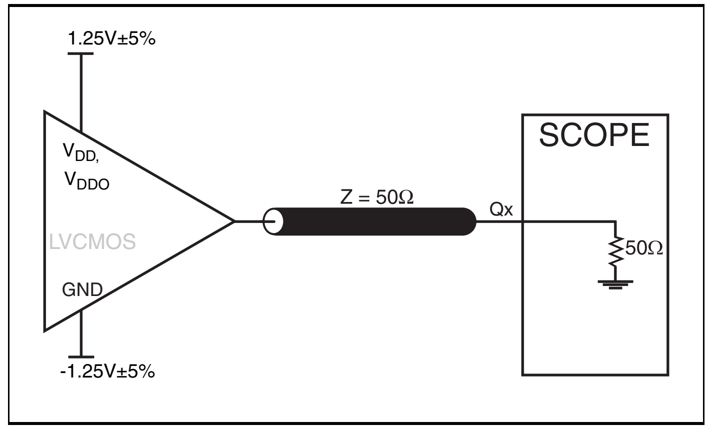


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

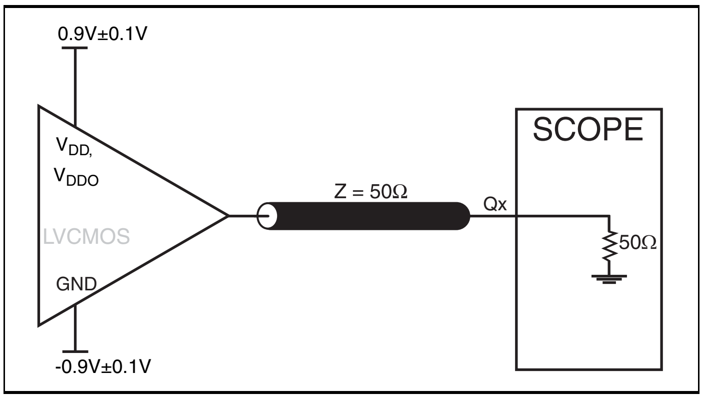
Parameter Measurement Information



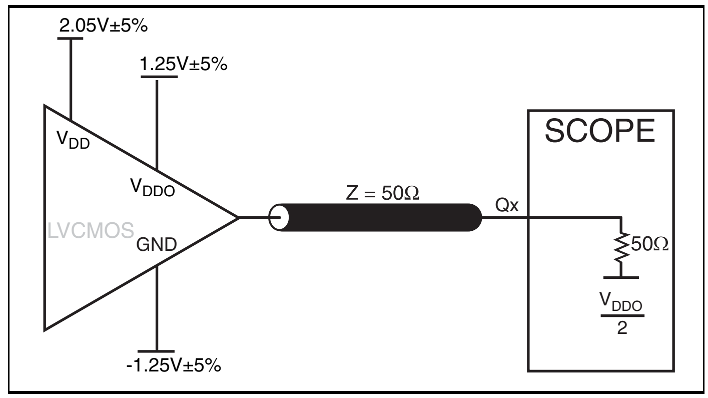
3.3V Core/3.3V LVCMOS Output Load AC Test Circuit



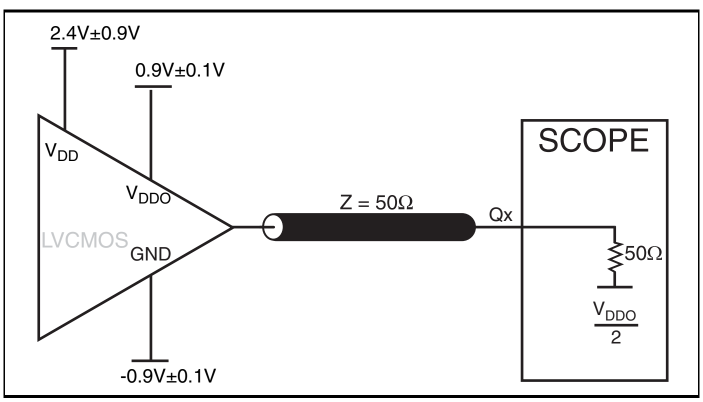
2.5V Core/2.5V LVCMOS Output Load AC Test Circuit



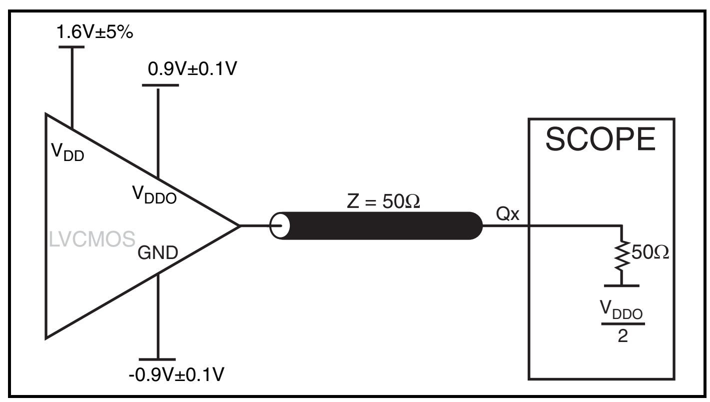
1.8V Core/1.8V LVCMOS Output Load AC Test Circuit



3.3V Core/2.5V LVCMOS Output Load AC Test Circuit

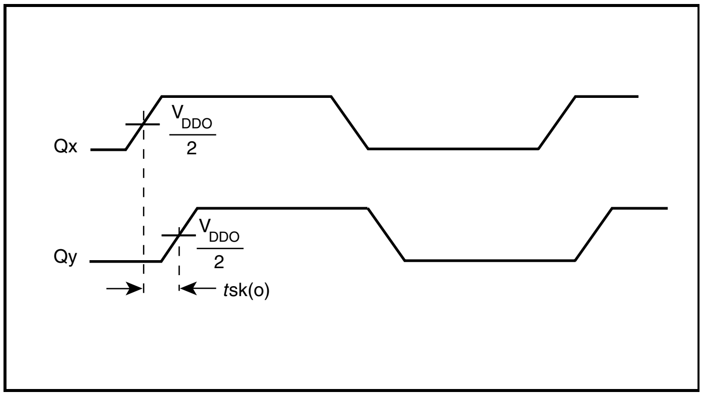


3.3V Core/1.8V LVCMOS Output Load AC Test Circuit

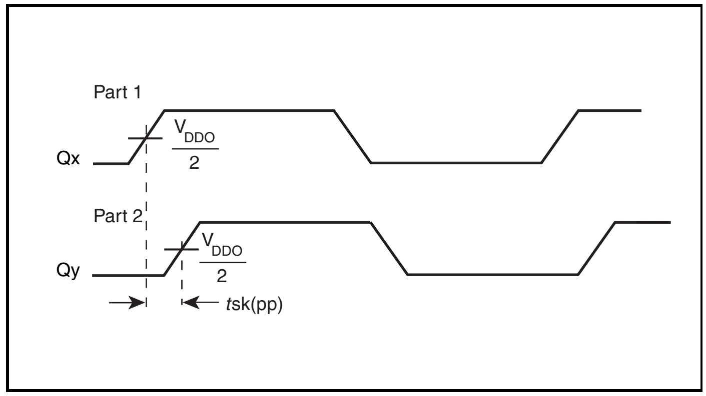


2.5V Core/1.8V LVCMOS Output Load AC Test Circuit

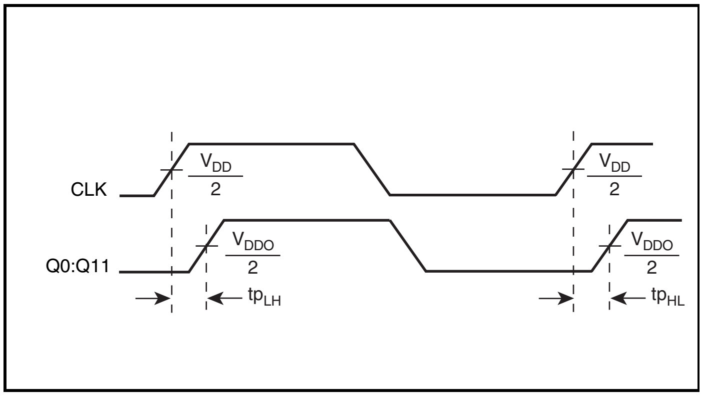
Parameter Measurement Information, continued



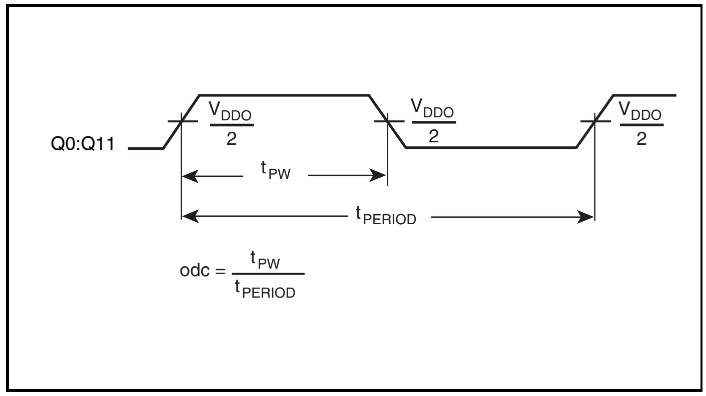
Output Skew



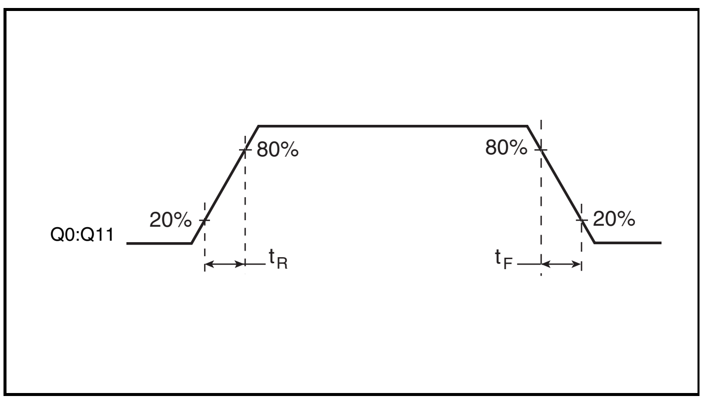
Part-to-Part Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs:

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 32 Lead LQFP

θ_{JA} **vs. Air Flow**			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	67.8°C/W	55.9°C/W	50.1°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	47.9°C/W	42.1°C/W	39.4°C/W

NOTE: Most modern PCB design use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8312I is: 339

Package Outline and Package Dimensions

Package Outline - Y Suffix for 32 Lead LQFP

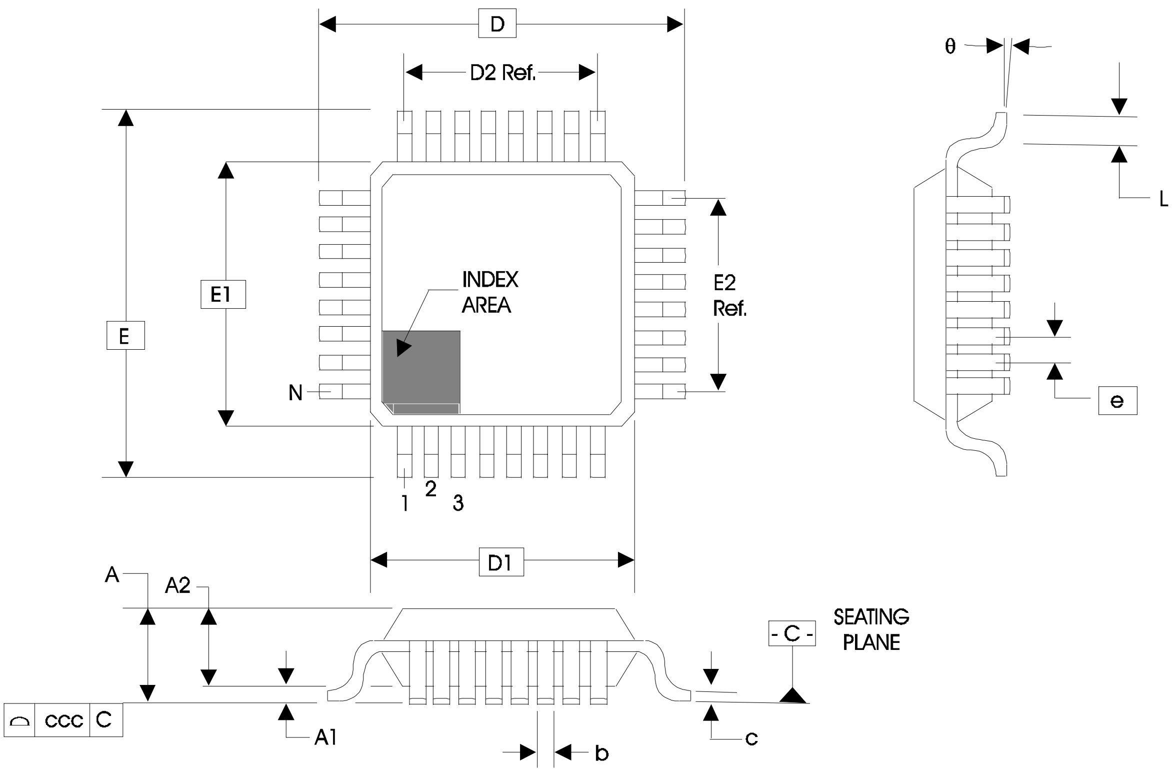


Table 7. Package Dimensions for 32 Lead LQFP

JEDEC Variation: ABC - HD All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A			1.60
A1	0.05	0.10	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D & E		9.00 Basic	
D1 & E1		7.00 Basic	
D2 & E2		5.60 Ref.	
e		0.80 Basic	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.10
N		32	

Reference Document: JEDEC Publication 95, MS-026

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8312AYI	ICS8312AYI	32 Lead LQFP	Tray	-40°C to 85°C
8312AYIT	ICS8312AYI	32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C
8312AYILF	ICS8312AYILF	“Lead-Free” 32 Lead LQFP	Tray	-40°C to 85°C
8312AYILFT	ICS8312AYILF	“Lead-Free” 32 Lead LQFP	1000 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	 T8	1 9 12	Features section - added lead-free bullet. Added *Recommendations for Unused Input & Output Pins* section. Ordering Information Table - added Lead-Free part number, marking and note.	6/28/06
B	T5A - T5F	7 - 9 10	Added Additive Phase Jitter specs to AC Tables. Added Additive Phase Jitter Plot. Updated datasheet to new format.	6/6/08

Contact Information:

www.IDT.com

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)

IDT
www.IDT.com