LOW SKEW, 1-TO-4, CRYSTAL-TO-LVCMOS/LVTTL FANOUT BUFFER

ICS83904I-02

General Description

The ICS83904I-02 is a low skew, high performance 1-to-4 Crystal Oscillator/Crystal-to-LVCMOS Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The ICS83904I-02 has selectable single-ended clock or two crystal-oscillator inputs. There is an output enable to disable the outputs by placing them into a high-impedance state.

Guaranteed output and part-to-part skew characteristics make the ICS83904I-02 ideal for those applications demanding well defined performance and repeatability.

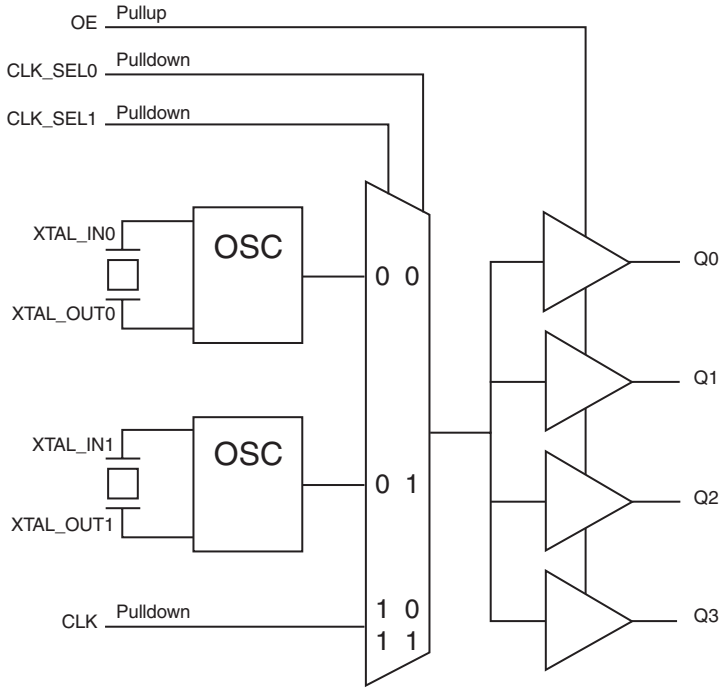
Features

- Four LVCMOS/LVTTL outputs, 19Ω typical output impedance @ $V_{DD} = V_{DDO} = 3.3V$
- Two Crystal oscillator input pairs
  One LVCMOS/LVTTL clock input
- Crystal input frequencry range: 12MHz – 38.88MHz
- Output frequency: 200MHz (maximum)
- Output Skew: 40ps (maximum) @ $V_{DD} = V_{DDO} = 3.3V$
- RMS phase jitter @ 25MHz output, using a 25MHz crystal (100Hz – 1MHz): 0.16ps (typical) @ $V_{DD} = V_{DDO} = 3.3V$
- RMS phase noise at 25MHz:

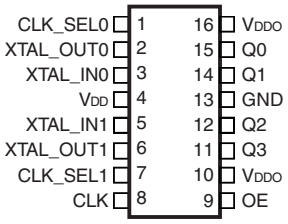
Offset	Noise Power
100Hz	-118.4 dBc/Hz
1kHz	-141.5 dBc/Hz
10kHz	-157.2 dBc/Hz
100kHz	-157.2 dBc/Hz

- Supply Voltage Modes:
  (Core/Output)
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS83904I-02
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7	CLK_SEL0, CLK_SEL1	Input	Pulldown	Clock select inputs. See Table 3, Input Reference Function Table. LVCMOS / LVTTL interface levels.
2, 3	XTAL_OUT0, XTAL_IN0	Input		Crystal oscillator interface. XTAL_IN0 is the input. XTAL_OUT0 is the output.
4	V_{DD}	Power		Core supply pin.
5, 6	XTAL_IN1, XTAL_OUT1	Input		Crystal oscillator interface. XTAL_IN1 is the input. XTAL_OUT1 is the output.
8	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
9	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
10, 16	V_{DDO}	Power		Output supply pins.
11, 12, 14, 15	Q3, Q2, Q1, Q0	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
13	GND	Power		Power supply ground.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V		8		pF
		V_{DDO} = 2.625V		7		pF
		V_{DDO} = 2.0V		7		pF
R_{OUT}	Output Impedance	V_{DDO} = 3.3V		19		Ω
		V_{DDO} = 2.5V		21		Ω
		V_{DDO} = 1.8V		32		Ω

TABLE 3. INPUT REFERENCE FUNCTION TABLE

Control Inputs		Reference
CLK_SEL1	CLK_SEL0	
0	0	XTAL0 (default)
0	1	XTAL1
1	0	CLK
1	1	CLK

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	100.3°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
I_{DDO}	Output Supply Current	No Load & CLK selected			1	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
I_{DDO}	Output Supply Current	No Load & CLK selected			1	mA

Table 4C. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	No Load & XTALx selected @ 12MHz			7	mA
		No Load & CLK selected			1	mA
I_{DDO}	Output Supply Current	No Load & CLK selected			1	mA

Table 4D. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current	No Load & XTALx selected @ 12MHz			3	mA
		No Load & CLK selected			1	mA
I_{DDO}	Output Supply Current	No Load & CLK selected			1	mA

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 2.5V±5%, V_{DDO} = 1.8V±0.2V, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current	No Load & XTALx selected @ 12MHz			3	mA
		No Load & CLK selected			1	mA
I_{DDO}	Output Supply Current	No Load & CLK selected			1	mA

TABLE 4F. DC CHARACTERISTICS, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2.2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.6		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		1.3	V
			V_{DD} = 2.5V ± 5%	-0.3		0.9	V
I_{IH}	Input High Current	CLK, CLK_SEL0:1	V_{DD} = 3.3V or 2.5V ± 5%			150	µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	CLK, CLK_SEL0:1	V_{DD} = 3.3V or 2.5V ± 5%	-5			µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%	-150			µA
V_{OH}	Output HighVoltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1	1.2			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.6	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 1.8V ± 0.2V; NOTE 1			0.4	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12		38.88	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

TABLE 6A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/external XTAL		12		38.88	MHz
		w/external CLK				200	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.4	1.9	2.4	ns
*t*sk(o)	Output Skew; NOTE 2					40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					700	ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz – 1MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL		45		55	%
		w/external CLK	*ƒ* < 150MHz	46		54	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/external XTAL		12		38.88	MHz
		w/external CLK				200	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.5	2.0	2.5	ns
*t*sk(o)	Output Skew; NOTE 2					40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					700	ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL		45		55	%
		w/external CLK	*ƒ* < 150MHz	46		54	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6C. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V±0.2V, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/external XTAL		12		38.88	MHz
		w/external CLK				200	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.7	2.2	2.7	ns
*t*sk(o)	Output Skew; NOTE 2					40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					700	ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	100		1000	ps
odc	Output Duty Cycle	w/external XTAL		45		55	%
		w/external CLK	*f* < 150MHz	46		54	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6D. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 2.5V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/external XTAL		12		38.88	MHz
		w/external CLK				200	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.5	2.2	3.0	ns
*t*sk(o)	Output Skew; NOTE 2					40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					700	ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.20		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	100		800	ps
odc	Output Duty Cycle	w/external XTAL		45		55	%
		w/external CLK	*f* < 150MHz	48		52	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

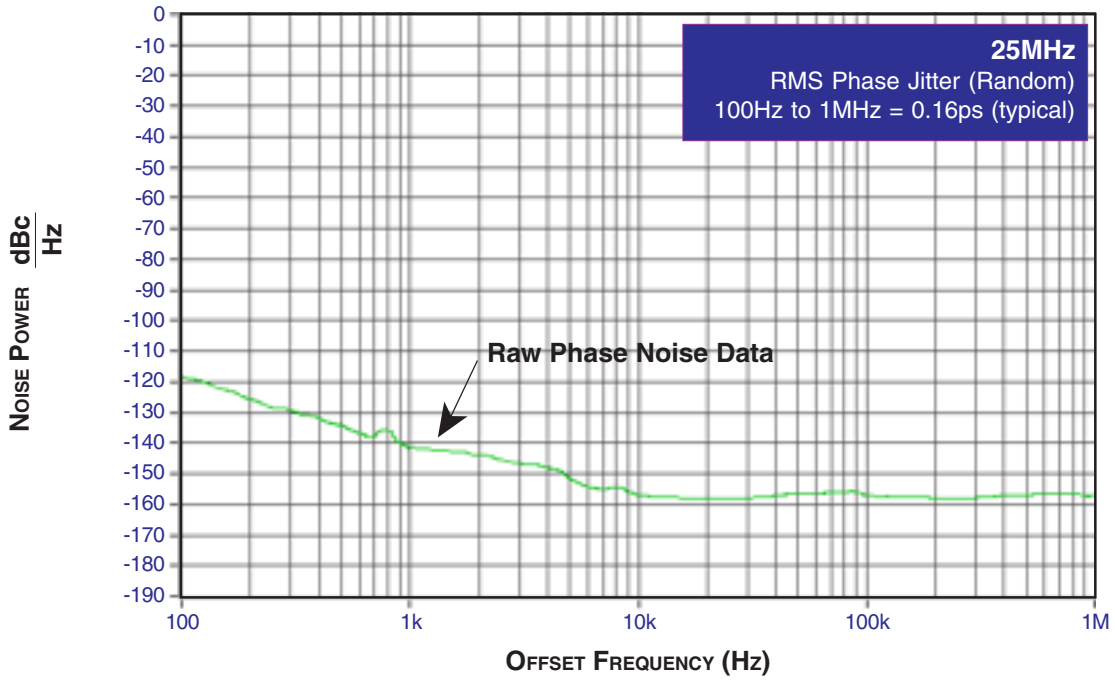
NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

TABLE 6E. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V±0.2V, T_A = -40°C TO 85°C

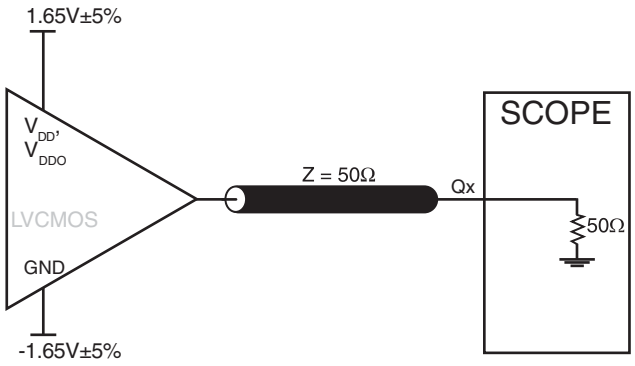
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	w/external XTAL		12		38.88	MHz
		w/external CLK				200	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1			1.7	2.5	3.3	ns
*t*sk(o)	Output Skew; NOTE 2					40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 3					700	ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 2, 4		25MHz, Integration Range: 100Hz - 1MHz		0.19		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	100		1000	ps
odc	Output Duty Cycle	w/external XTAL		45		55	%
		w/external CLK	*ƒ* < 150MHz	46		54	%
t_{EN}	Output Enable Time; NOTE 5					10	ns
t_{DIS}	Output Disable Time; NOTE 5					10	ns

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 4: Phase jitter is dependent on the input source used.
NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

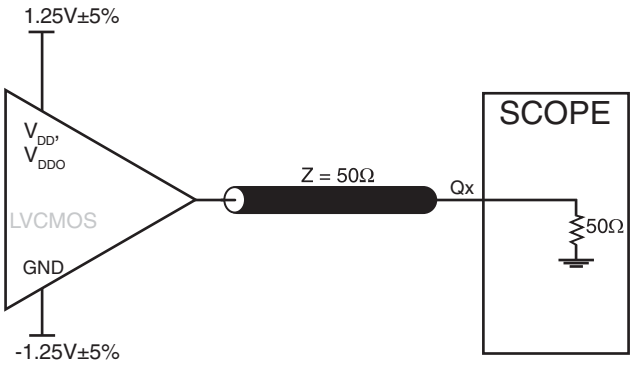
TYPICAL PHASE NOISE AT 25MHZ



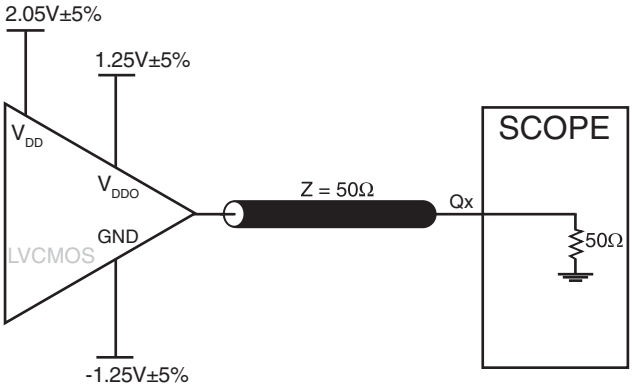
Parameter Measurement Information



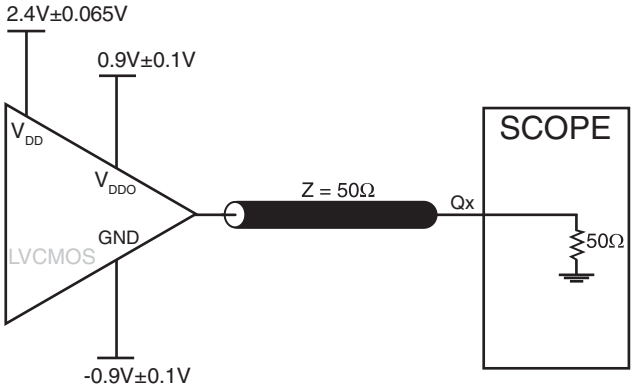
3.3V Core/3.3V Output Load AC Test Circuit



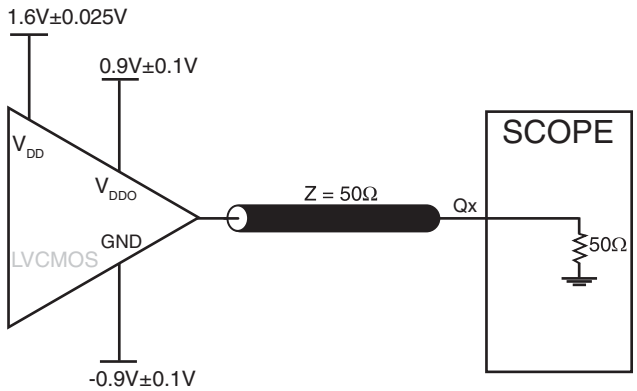
2.5V Core/2.5V Output Load AC Test Circuit



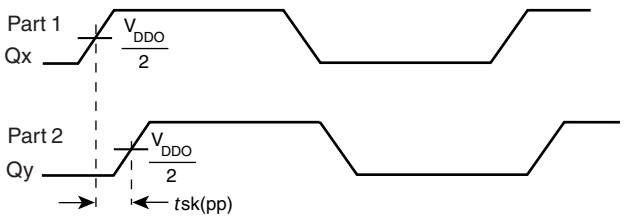
3.3V Core/2.5V Output Load AC Test Circuit



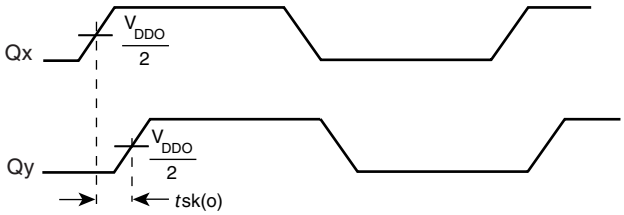
3.3V Core/1.8V Output Load AC Test Circuit



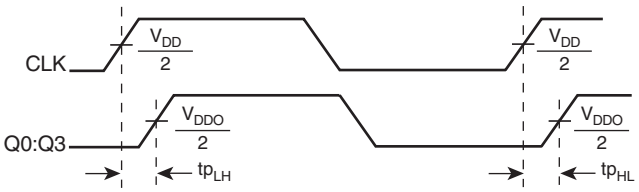
2.5 Core/1.8V Output Load AC Test Circuit



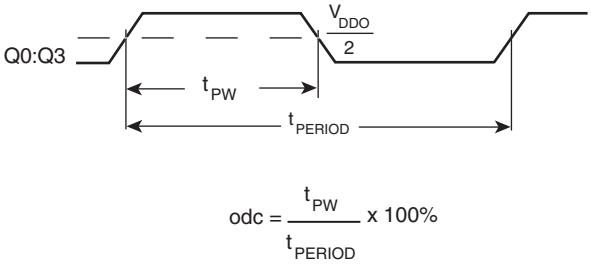
Part-to-Part Skew



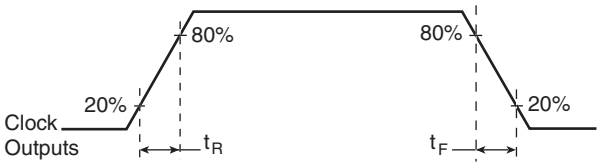
Output Skew



Propagation Delay



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

Figure 1 shows an example of ICS83904I-02 crystal interface with a parallel resonant crystal. The frequency accuracy can be fine tuned by adjusting the C1 and C2 values. For a parallel crystal with loading capacitance CL = 18pF, we suggest C1 = 15pF and C2 = 15pF to start with. These values may be slightly fine tuned further to optimize the frequency accuracy for different board layouts. Slightly increasing the C1 and C2 values will slightly reduce the frequency. Slightly decreasing the C1 and C2 values will slightly increase the frequency. For the oscillator circuit below, R1 can be used, but is not required. For new designs, it is recommended that R1 not be used.

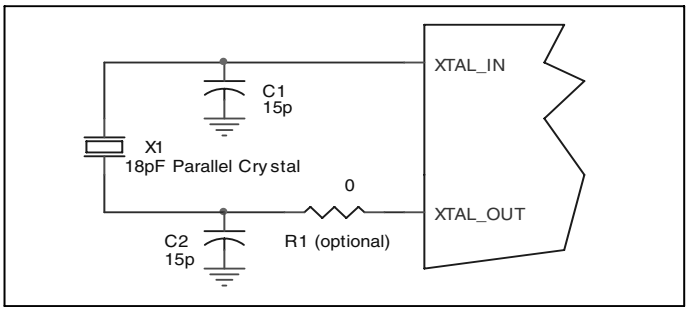


FIGURE 1. CRYSTAL INPUT INTERFACE

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 2.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

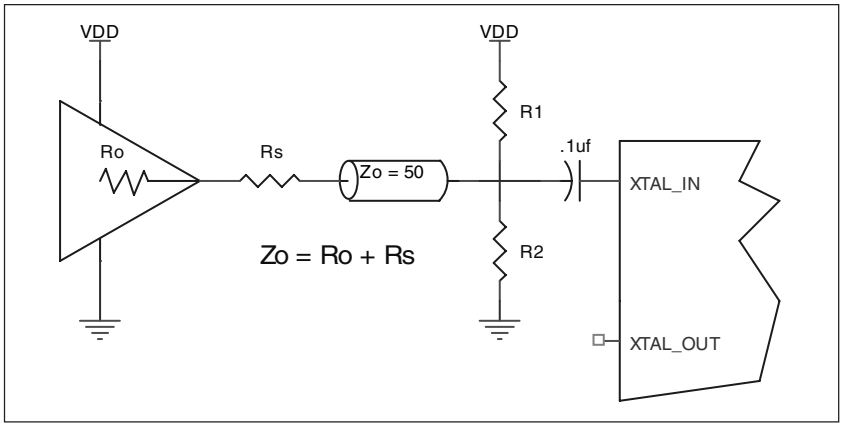


FIGURE 2. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK Input

For applications not requiring the use of the clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

Select Pins

All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for 16 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Transistor Count

The transistor count for ICS83904I-02 is: 205

Package Outline - G Suffix for 16 Lead TSSOP

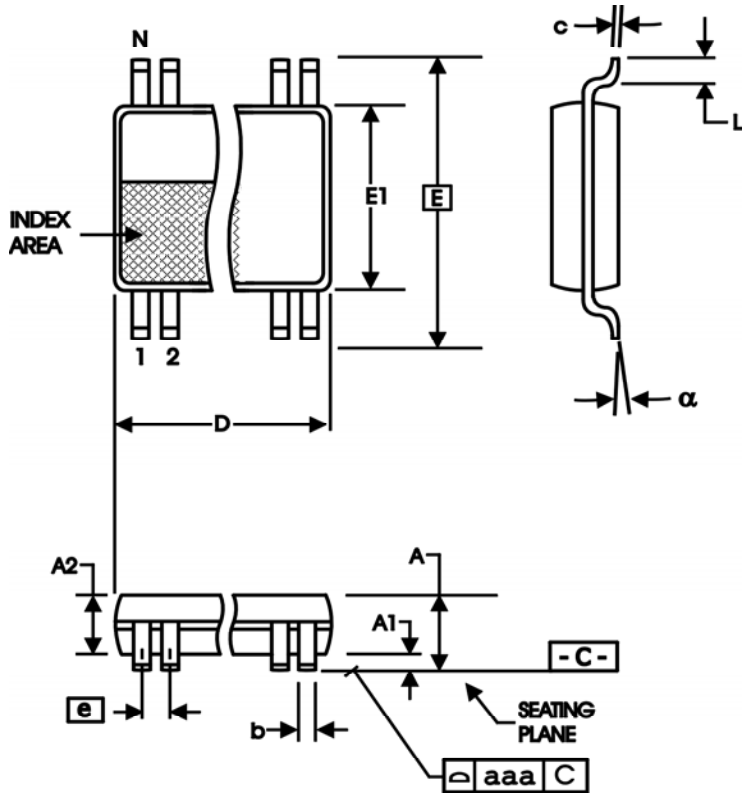


Table 8. Package Dimensions

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS83904AGI-02	3904AI02	16 Lead TSSOP	tube	-40°C to 85°C
ICS83904AGI-02T	3904AI02	16 Lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS83904AGI-02LF	904AI02L	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS83904AGI-02LFT	904AI02L	16 Lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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